中山大学软件学院 **2009** 级计算机应用软件专业 (2011 学年秋季学期)

《SE-315 计算机体系结构》期末试题 (A 卷)

(考试形式：闭 卷 考试时间：2 小时)

警示

《中山大学授予学士学位工作细则》第六条

考试作弊不授予学士学位

方向：_____ 姓名：_____ 学号：_____

I. Fill in the blank (1 pt per blank, 20 pts in total)

1. An ideal computer system should make a balance among operation speed, _____ and _____.
2. The directly-mapped Cache with the size of _____ and the 2-way group connected Cache with the size of _____ have the same missing rate.
3. _____ is a group of internationally-recognized standard testing procedures, using which to run on a target machine, and calculate the running speed indicators of this computer according to the practical runtime. The score of standard runtime is _____.
4. In instruction pipelines, if hardware resources cannot meet the requirements when instructions are overlappingly executed, _____ conflicts will occur, and we call this pipeline has _____ correlation.
5. According to the "85/60 Branches Jumping Rule", about 85% of the _____ branches occur, and about 60% of the _____ branches occur.
6. Static scheduling and dynamic scheduling are commonly-used methods to improve the instruction-level machine parallelism. Static scheduling is usually implemented by _____, and dynamic scheduling is usually implemented by _____.
7. MTTR means _____. MTTF means _____.
8. In order to improve the versatility of machines, a vector processor should have the function of processing both _____ and _____.
9. A processor which can transmit more than two instructions parallelly in a clock cycle is called _____ processor; a processor which can transmit multiple instructions separately in a clock circle is called _____ processor.
10. Two basic structures of a multi-processor system are _____ and _____.

II. Single-choice questions (1 pt per question, 10 pts)

1. In the structural design of computer systems, improving the proportion of software function implementation will ( )

A. increase problem-solving speed

B. reduce the required memory capacity

C. improve the flexibility of the system

D. improve the capability/price ratio of the system

2． ( ) uses time overlap concept to implement parallel processing.
A. Flow computer
B. Multi-processor
C. Array machine
D. cluster system

3. Instruction pipeline belongs to ( ) pipeline
A. operative
B. component-level
C. processor-level
D. system-level

4. Static pipeline is ()
A． A pipeline that function cannot be changed
B. A multi-functional pipeline that only one function can be finished in one time
C. A pipeline that multiple functions can be performed simultaneously
D. A pipeline that the connections between each segment are fixed.

5. ( ) is related to maximum throughput rate of linear pipelines.
A. The execution time of each sub-process
B. The execution time of the largest sub-process
C. The execution time of the slowest sub-process
D. the execution time of the last sub-process

6. For an I/O system composed of multiple channels, the maximum flow of I/O channel is ( ).
A. The maximum value of the maximum flow for each channel
B. The sum of the maximum flow of each channel
C. The maximum value of the actual flow of each channel
D. The sum of the actual flows of each channel

7. When the local Cache data blocks are modified, the Bus Snooping Protocol will pass the modified data blocks to all the Cache of the data blocks through bus. This is the ( ) of the monitoring protocol.
A. writing passing strategy
B. writing back strategy
C. writing invalidate strategy
D. writing updating strategy

8. A computer system which can achieve indication, program and task-level parallelism is ( )
A. SISD
B. SIMD
C. MISD
D. MIMD

9. The parallelism that multiprocessors implement is mainly ()
A. instruction-level
B. thread-level
C. task-level or process-level
D. job or program level

10. The implementation goal of the load balancing scheduling of a heterogeneous multiprocessor system is ( ).
A. The number of tasks assigned to each processor is equal
B. The computation loads assigned to each processor are equalized
C. The time of multi-processing jobs is shortest
D. The particle size of the tasks assigned to each processor is identical

III. T or F questions (the right to play "√"; the wrong fight "×", 1 pt per question, 10 pts in total)

1. Through careful quantitative analysis, architecture designers can always find a technical "optimal point" by balancing price, performance and complexity. ( )
2. Parallel processor and array processor are both instruction-level parallel processors ( )
3. Superscalar processors use resource repetition method to increase spatial parallelism and thus to improve the average execution speed of instructions based on a single pipeline processor. ( )
4. In tightly-coupled multiprocessors, if the read-after-write data are relevant between the program passages each processor runs, parallelism is not allowed. ( )
5. Single-transmission processor refers to a processor that executes one instruction every time. ( )
6. User A's applications run very well, so the computer system's performance is also very good. ( )
7. One program's Cache Performance can be inferred from another program's Cache Performance. ( )
8. In computer architecture design one should focus on supporting the acceleration of controlling indications. ( )
9. The dynamic scheduling of instructions is at the cost of the significantly increased hardware complexity. ( )
10. The parallel computer performance of parallel processors with distributed memory structure is closely related to the distribution of data in each memory. （ ）

IV. Calculation or to answer the following questions (12 points per question, 60 points in total)

1. (1) What is the definition of the classic "computer architecture"? Describe briefly the quantification principles of modern computer architecture.
   (2) What factors does speedup depend on?
   (3) What periods does a computer architecture experience from generated to die-out?

2. Assume that there are multiple adders, and there is no resource conflict of the adders. The codes formed by three consecutive instructions are as follows:

I_1 ADD R1, R2, R4 ; $R_1 \leftarrow (R_2)+(R_4)$

I_2 ADD R2, R1, 1 ; $R_2 \leftarrow (R_1)+1$

I_3 SUB R1, R4, R5 ; $R_1 \leftarrow (R_4)-(R_5)$

(1) Analyze the data correlation in the codes;

(2) Which hardware technology can be adopted to address these data correlations? Please describe it.

3. (1) According to the average accessing and saving time equation, from which aspects can the performance of Cache be improved?

(2) Explain the Cache's coherence problem of multiprocessors and explain the reason this problem appears.

4. (1) Why are the architectures of memory often designed as hierarchical structures?

(2) If a level of the memory hierarchy has a hit rate of 75 percent, memory requests take12ns to complete if they hit in the level, and memory requests that miss in the level take 100ns to complete, what is the average access time of the level?

5. (1) Which three factors is the flow-out capability of indication multiple flow-out processors influenced by?

(2) Compare the main differences between using CPI and IPC to evaluate computer performance.