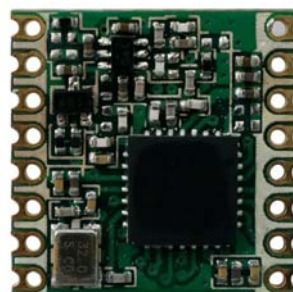


RFM95/96/97/98(W) - Low Power Long Range Transceiver Module V1.0

GENERAL DESCRIPTION

LORENZ

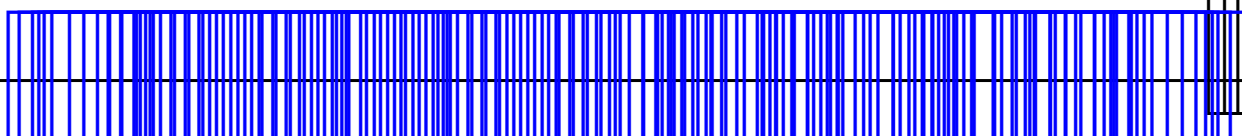
**RFM95/96/97/98(W)**

KEY PRODUCT FEATURES

-

APPLICATIONS

-



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21	22	23	24	25	26	27	28	29	30
31	32	33	34	35	36	37	38	39	40
41	42	43	44	45	46	47	48	49	50
51	52	53	54	55	56	57	58	59	60
61	62	63	64	65	66	67	68	69	70
71	72	73	74	75	76	77	78	79	80
81	82	83	84	85	86	87	88	89	90
91	92	93	94	95	96	97	98	99	100



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Section

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1. General Description

1.1. Simplified Block Diagram

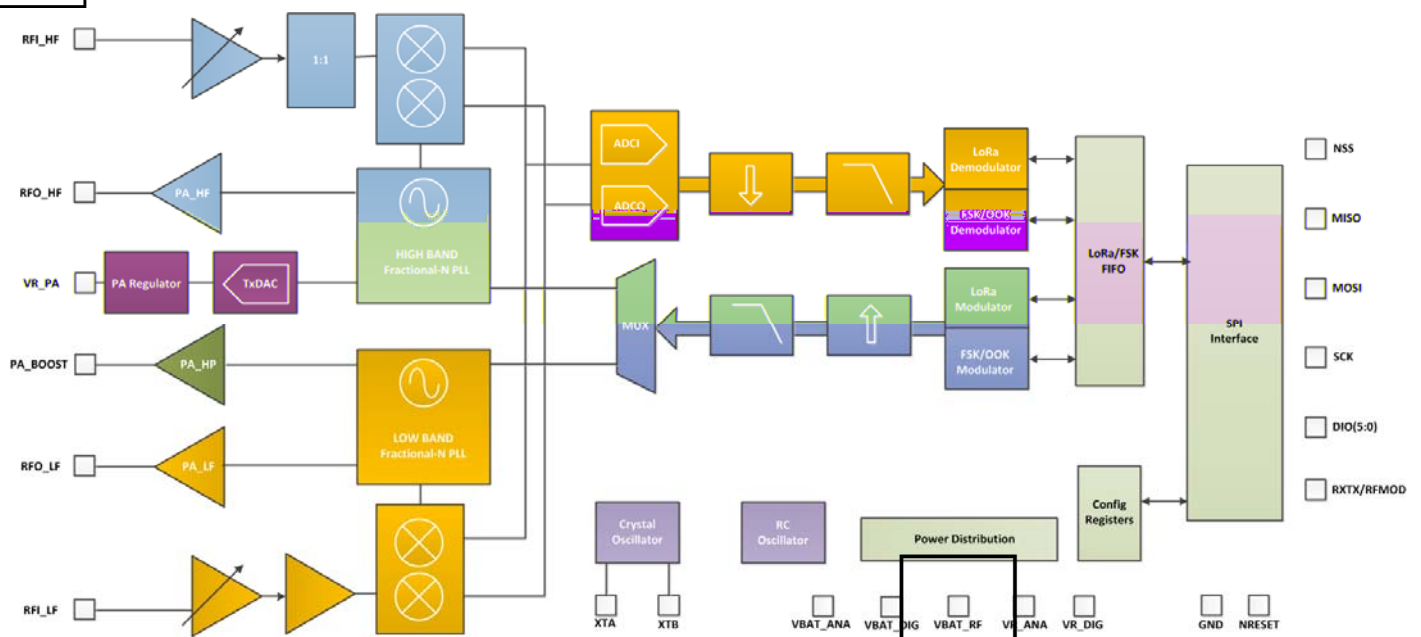


Figure 1. Block Diagram

1.2. Product Versions

Table 48. RFM95/96/97/98(W) Device Variants and Key Parameters

Part Number	Frequency Range	Spreading Factor	Bandwidth	Effective Bitrate	Est. Sensitivity

1.3. ~~IMP Diagram~~

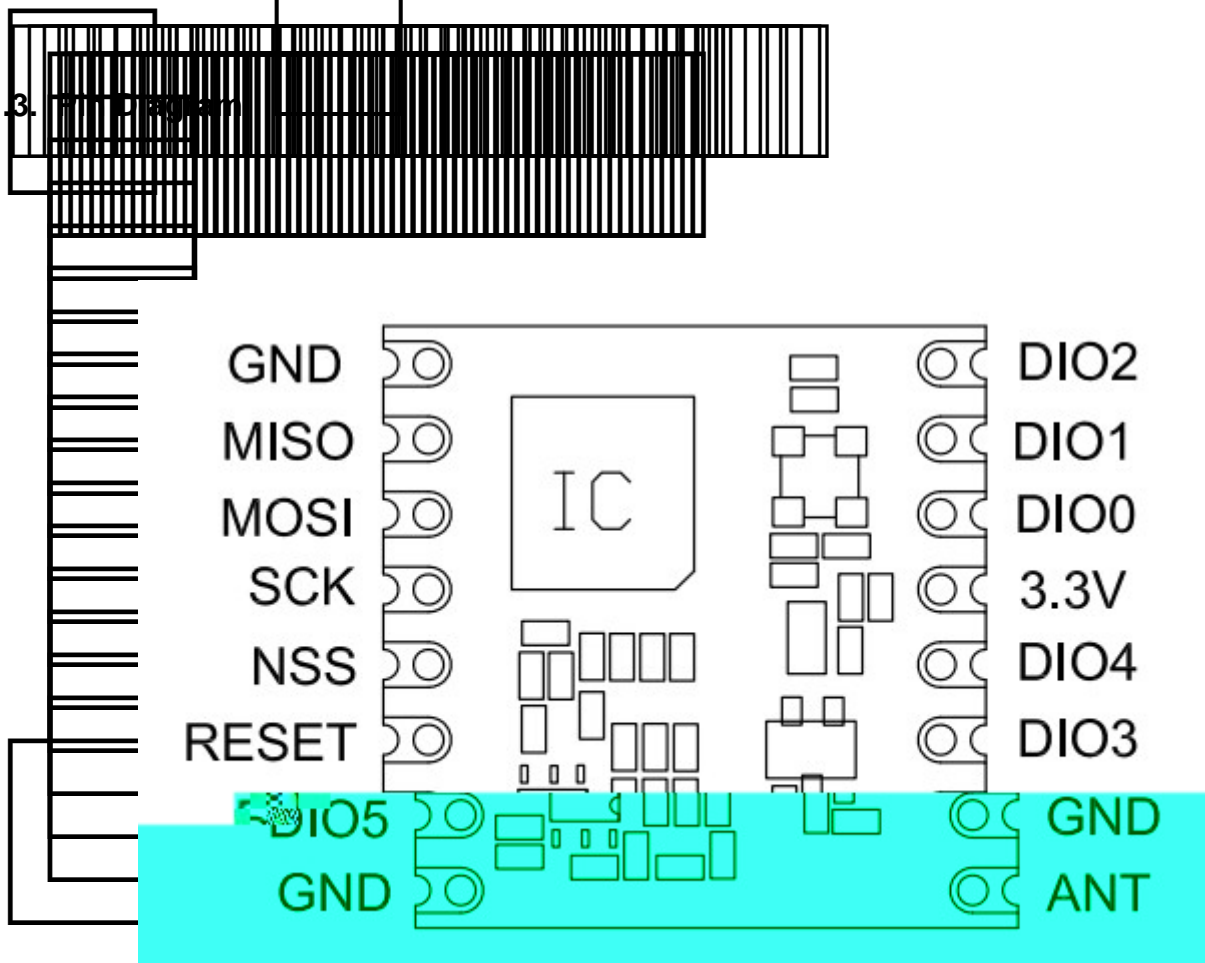


Figure 2. Pin Diagrams

1.4. Pin Description

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2. Electrical Characteristics

2.1. ESD Notice



2.2. Absolute Maximum Ratings

Table 49 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit

Note Specific ratings apply to +20 dBm operation (see Section 5.4.3).

2.3. Operating Range

Table 50 Operating Range

Symbol	Description	Min	Max	Unit

Note A specific supply voltage range applies to +20 dBm operation (see Section 5.4.3).



2.4. CHINA'S CURRENT POLICY

2|4.1. Power Consumption

Table 51 Power Consumption Specification

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2.4.3. FSKVO-KIT-De-Roos

Appendix 1

Table 53 FSK/OOK Receiver Specification

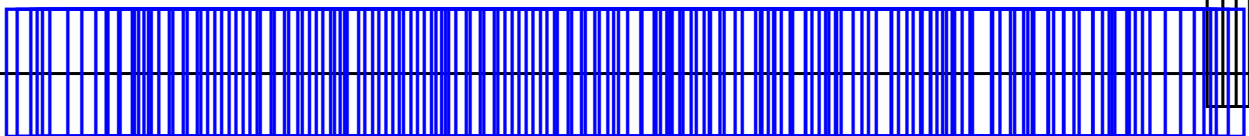
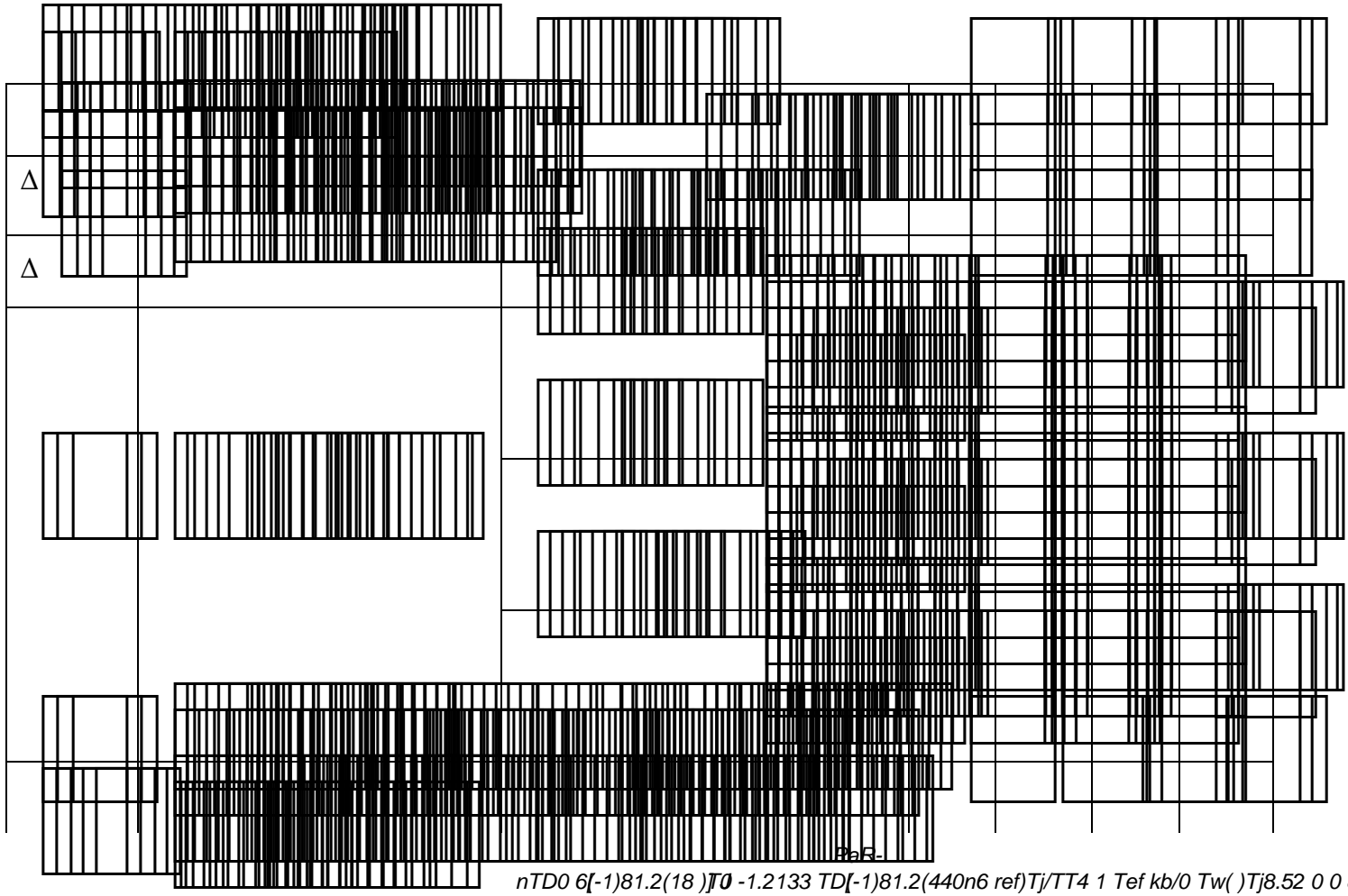
[illegible]

* $RxBw = 83 \text{ kHz}$ (Single Side Bandwidth)
 ** $RxBw = 50 \text{ kHz}$ (Single Side Bandwidth)
 * * $RxBw = 250 \text{ kHz}$ (Single Side Bandwidth)

24.4. FSK/OOK Mode Transmitter

Table 54 Transmitter Specification

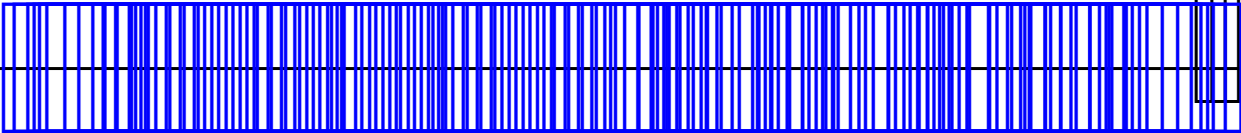
Symbol	Definition	Conditions	Min	Typ	Max	Unit
Δ	Frequency Error					



[illegible]

Table 56. Electrical specifications: Lora™ mode





2.4.6 Digital Specification

Table 57 Digital Specification

[illegible]

3. RFM95/96/97/98(W) Features

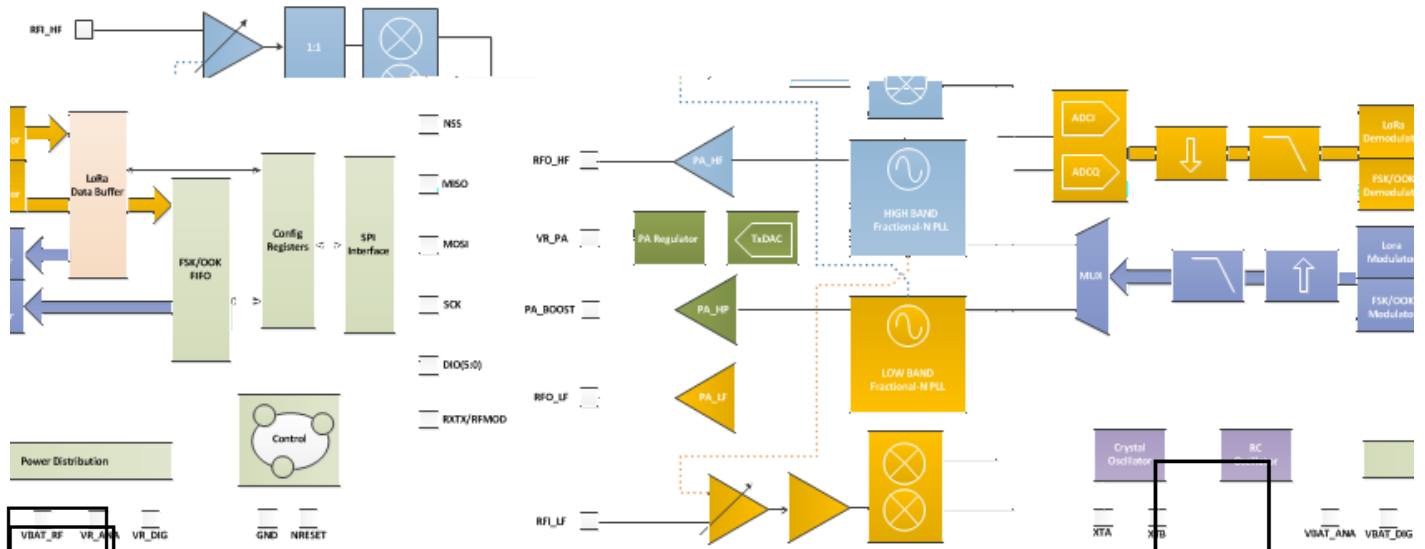


Figure 1. RFM95/96/97/98(W) Block Diagram

3.1.1.1 Lorentz-Magneton

3.2. TSK/DOH/9001

HPB™

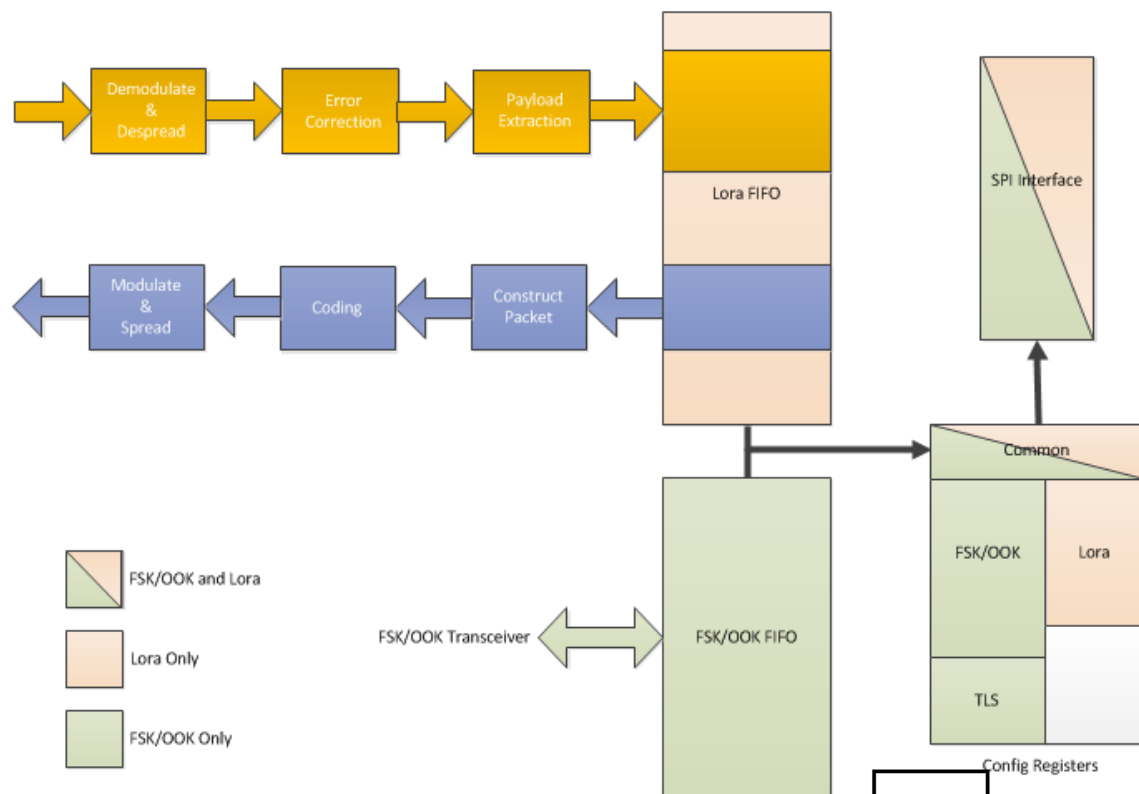
ORP™

4. RFM95/96/97/98(W) Digital Electronics



4.1.1. Link Design Using the LoRa™ Modem

4.1.1.1. Overview



4.1.1.2. LoRa™ Modem Generating

LDX-TV



4.11.2 Spreading Factor

LoRa™

Table 59 Range of Spreading Factors

Spreading Factor (RegModulationCfg)	Spreading Factor (Chips / symbol)	LoRa Demodulator SNR
7	128	-17.0
8	256	-17.6
9	512	-18.1
10	1024	-18.6
11	2048	-19.1
12	4096	-19.6
13	8192	-20.1
14	16384	-20.6
15	32768	-21.1
16	65536	-21.6
17	131072	-22.1
18	262144	-22.6
19	524288	-23.1
20	1048576	-23.6
21	2097152	-24.1
22	4194304	-24.6
23	8388608	-25.1
24	16777216	-25.6
25	33554432	-26.1
26	67108864	-26.6
27	134217728	-27.1
28	268435456	-27.6
29	536870912	-28.1
30	1073741824	-28.6
31	2147483648	-29.1
32	4294967296	-29.6
33	8589934592	-30.1
34	17179869184	-30.6
35	34359738368	-31.1
36	68719476736	-31.6
37	137438953472	-32.1
38	274877906944	-32.6
39	549755813888	-33.1
40	1099511627776	-33.6
41	2199023255552	-34.1
42	4398046511104	-34.6
43	8796093022208	-35.1
44	17592186044416	-35.6
45	35184372088832	-36.1
46	70368744177664	-36.6
47	140737488355328	-37.1
48	281474976710656	-37.6
49	562949953421312	-38.1
50	1125899906842624	-38.6
51	2251799813685248	-39.1
52	4503599627370496	-39.6
53	9007199254740992	-40.1
54	18014398509481984	-40.6
55	36028797018963968	-41.1
56	72057594037927936	-41.6
57	144115188075855872	-42.1
58	288230376151711744	-42.6
59	576460752303423488	-43.1
60	1152921504606846976	-43.6
61	2305843009213693952	-44.1
62	4611686018427387904	-44.6
63	9223372036854775808	-45.1
64	18446744073709551616	-45.6
65	36893488147419103232	-46.1
66	73786976294838206464	-46.6
67	147573952589676412928	-47.1
68	295147905179352825856	-47.6
69	590295810358705651712	-48.1
70	1180591620717411303424	-48.6
71	2361183241434822606848	-49.1
72	4722366482869645213696	-49.6
73	9444732965739290427392	-50.1
74	18889465931478580854784	-50.6
75	37778931862957161709568	-51.1
76	75557863725914323419136	-51.6
77	151115727451828646838272	-52.1
78	302231454903657293676544	-52.6
79	604462909807314587353088	-53.1
80	1208925819614629174706176	-53.6
81	2417851639229258349412352	-54.1
82	4835703278458516698824704	-54.6
83	9671406556917033397649408	-55.1
84	19342813113834066795298816	-55.6
85	38685626227668133590597632	-56.1
86	77371252455336267181195264	-56.6
87	154742504910672534362390528	-57.1
88	309485009821345068724781056	-57.6
89	618970019642690137449562112	-58.1
90	1237940039285380274899124224	-58.6
91	2475880078570760549798248448	-59.1
92	4951760157141521099596496896	-59.6
93	9903520314283042199192993792	-60.1
94	19807040628566084398385987584	-60.6
95	39614081257132168796771975168	-61.1
96	79228162514264337593543950336	-61.6
97	158456325028528675187087900672	-62.1
98	316912650057057350374175801344	-62.6
99	633825300114114700748351602688	-63.1
100	1267650600228229401496703205376	-63.6
101	2535301200456458802993406410752	-64.1
102	5070602400912917605986812821504	-64.6
103	10141204801825835211973625643008	-65.1
104	20282409603651670423947251286016	-65.6
105	40564819207303340847894502572032	-66.1
106	81129638414606681695789005144064	-66.6
107	162259276829213363391578010288128	-67.1
108	324518553658426726783156020576256	-67.6
109	649037107316853453566312041152512	-68.1
110	1298074214633706907132624082305024	-68.6
111	2596148429267413814265248164610048	-69.1
112	5192296858534827628530496329220096	-69.6
113	10384593717069655257060992658440192	-70.1
114	20769187434139310514121985316880384	-70.6
115	41538374868278621028243970633760768	-71.1
116	83076749736557242056487941267521536	-71.6
117	166153499473114484112975882535043072	-72.1
118	332306998946228968225951765070086144	-72.6
119	664613997892457936451903530140172288	-73.1
120	1329227995784915872903807060280344576	-73.6
121	2658455991569831745807614120560689152	-74.1
122	5316911983139663491615228241121378304	-74.6
123	10633823966279326983230456482242756608	-75.1
124	21267647932558653966460912964485513216	-75.6
125	42535295865117307932921825928971026432	-76.1
126	85070591730234615865843651857942052864	-76.6
127	170141183460469231731687303715884105728	-77.1
128	340282366920938463463374607431768211456	-77.6
129	680564733841876926926749214863536422912	-78.1
130	1361129467683753853853498429727072845824	-78.6
131	2722258935367507707706996859454145691648	-79.1
132	5444517870735015415413993718908291383296	-79.6
133	10889035741470030830827987437816582766592	-80.1
134	21778071482940061661655974875633165533184	-80.6
135	43556142965880123323311949751266331066368	-81.1
136	87112285931760246646623899502532662132736	-81.6
137	174224571863520493293247799005065324265472	-82.1
138	348449143727040986586495598010130648530944	-82.6
139	696898287454081973172991196020261297061888	-83.1
140	1393796574908163946345982392040522594123776	-83.6
141	2787593149816327892691964784081045188247552	-84.1
142	5575186299632655785383929568162090376495104	-84.6
143	11150372599265311570767859136324180752990208	-85.1
144	22300745198530623141535718272648361505980416	-85.6
145	44601490397061246283071436545296723011960832	-86.1
146	89202980794122492566142873090593446023921664	-86.6
147	178405961588244985132285746181186892047843328	-87.1
148	356811923176489970264571492362373784095686656	-87.6
149	713623846352979940529142984724747568191373312	-88.1
150	1427247692705959881058285969449495136382746624	-88.6
151	2854495385411919762116571938898990272765493248	-89.1
152	5708990770823839524233143877797980545530986496	-89.6
153	11417981541647679048466287755595961091061972992	-90.1
154	22835963083295358096932575511191922182123945984	-90.6
155	45671926166590716193865151022383844364247891968	-91.1
156	91343852333181432387730302044767688728495783936	-91.6
157	182687704666362864775460604089535377456991567872	-92.1
158	365375409332725729550921208179070754913983135744	-92.6
159	730750818665451459101842416358141509827966271488	-93.1
160	1461501637330902918203684832716283019655932542976	-93.6
161	2923003274661805836407369665432566039311865085952	-94.1
162	5846006549323611672814739330865132078623730171904	-94.6
163	11692013098647223345629478661730264157247460343808	-95.1
164	23384026197294446691258957323460528314494920687616	-95.6
165	46768052394588893382517914646921056628989841375232	-96.1
166	93536104789177786765035829293842113257979682750464	-96.6
167	187072209578355573530071658587684226515959365500928	-97.1
168	374144419156711147060143317175368453031918731001856	-97.6
169	748288838313422294120286634350736906063837462003712	-98.1
170	1496577676626844588240573268701473812127674924007424	-98.6
171	2993155353253689176481146537402947624255349848014848	-99.1
172	5986310706507378352962293074805895248510699696029696	-99.6
173	11972621413014756705924586149611790497021399392059392	-100.1
174	23945242826029513411849172299223580994042798784118784	-100.6
175	47890485652059026823698344598447161988085597568237568	-101.1
176	95780971304118053647396689196894323976171195136475136	-101.6
177	191561942608236107294793378393788647952342390272950272	-102.1
178	383123885216472214589586756787577295904684780545900544	-102.6
179	766247770432944429179173513575154591809369561091801088	-103.1
180	1532495540865888858358347027150309183618739122183602176	-103.6
181	3064991081731777716716694054300618367237478244367204352	-104.1
182	6129982163463555433433388108601236734474956488734408704	-104.6
183	12259964326927110866866776217202473468949912977468817408	-105.1
184	24519928653854221733733552434404946937899825954937634816	-105.6
185	49039857307708443467467104868809893875799651909875269632	-106.1
186	98079714615416886934934209737619787751599303819750539264	-106.6
187	196159429230833773869868419475239575503198607639501078528	-107.1
188	392318858461667547739736838950479151006397215279002157056	-107.6
189	784637716923335095479473677900958302012794430558004314112	-108.1
190	1569275433846670190958947355801916604025588861116008628224	-108.6
191	3138550867693340381917894711603833208051177722232017256448	-109.1
192	6277101735386680763835789423207666416102355444464034512896	-109.6
193	12554203470773361527671578846415332832204710888928069025792	-110.1
194	25108406941546723055343157692830665664409421777856138051584	-110.6
195	50216813883093446110686315385661331328818843555712276103168	-111.1
196	100433627766186892221372630771322662657637687111424552206336	-111.6
197	200867255532373784442745261542645325315275374222849104412672	-112.1
198	401734511064747568885490523085290650630550748445698208825344	-112.6
199	803469022129495137770981046170581301261101496891396417650688	-113.1
200	1606938044258990275541962092341162602522202993782792835301376	-113.6
201	3213876088517980551083924184682325205044405987565585670602752	-114.1
202	6427752177035961102167848369364650410088811975131171341205504	-114.6
203	12855504354071922204335696738729300820177623950262342682411008	-115.1
204	25711008708143844408671393477458601640355247900524685364822016	-115.6
205	51422017416287688817342786954917203280710495801049370729644032	-116.1
206	102844034832575377634685573909834406561420991602098741459288064	-116.6
207	205688069665150755269371147819668813122841983204197482918576128	-117.1
208	411376139330301510538742295639337626245683966408394965837152256	-117.6
209	8227522786606030210774	

4.1.1.4. Signal 3: Motion

Note In the lower band (169 MHz), the 250 kHz and 500 kHz bandwidths are not supported.

4.1.1.1.6

4.1.1.1.6.1

4.1.1.1.6.1.1

4.1.1.1.6.1.1.1

4.1.1.1.6.1.1.1.1

4.1.1.1.6.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

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4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

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4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

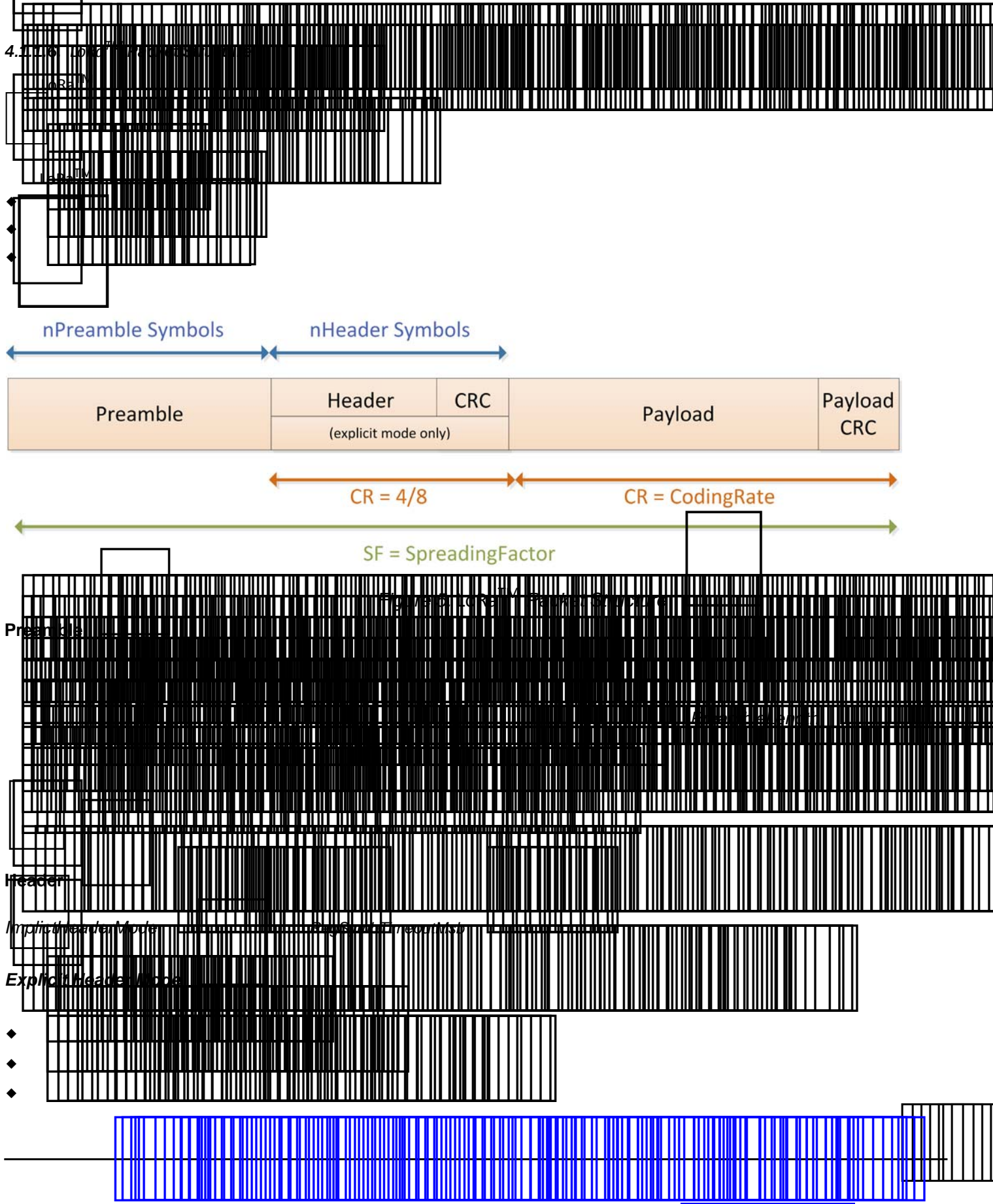
4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1

4.1.1.1.6.1



modem header mode

Note With SF = 6 selected, implicit header mode is the only mode of operation possible

Payload

4.1.1.1 Preamble

$$R_s = \frac{1}{T_s}$$

$$T_{preamble} = l_{preamble} \cdot T_{sym} + 428 \cdot T_{sym}$$

Preamble length

$$T_{payload} = \begin{cases} T_{sym} \left[8 + \text{ceil} \left(\frac{8l_{payload} - 4SF + 24}{4SF} \right) \right] (CR + 4) & \text{where: } l_{payload} > 0, \text{ implicit header} \\ T_{sym} \left[8 + \text{ceil} \left(\frac{8l_{payload} - 4SF + 44}{4SF} \right) \right] (CR + 4) & \text{where: } l > 0, \text{ explicit header} \end{cases}$$

$$T_{packet} = T_{preamble} + T_{payload}$$

4.1.1.3 Frequency Offset Compensation

LdBal™

FlssMode

RegTxCfg1



Principle of Frequency Hopping

Hopping Period

$$HoppingPeriod = H \times F_{Hopping} \times N_{Channels}$$

FhssChangeChannel

FhssPresentChannel

FhssChangeChannel

Timing of Channel Updates

FhssChangeChannel

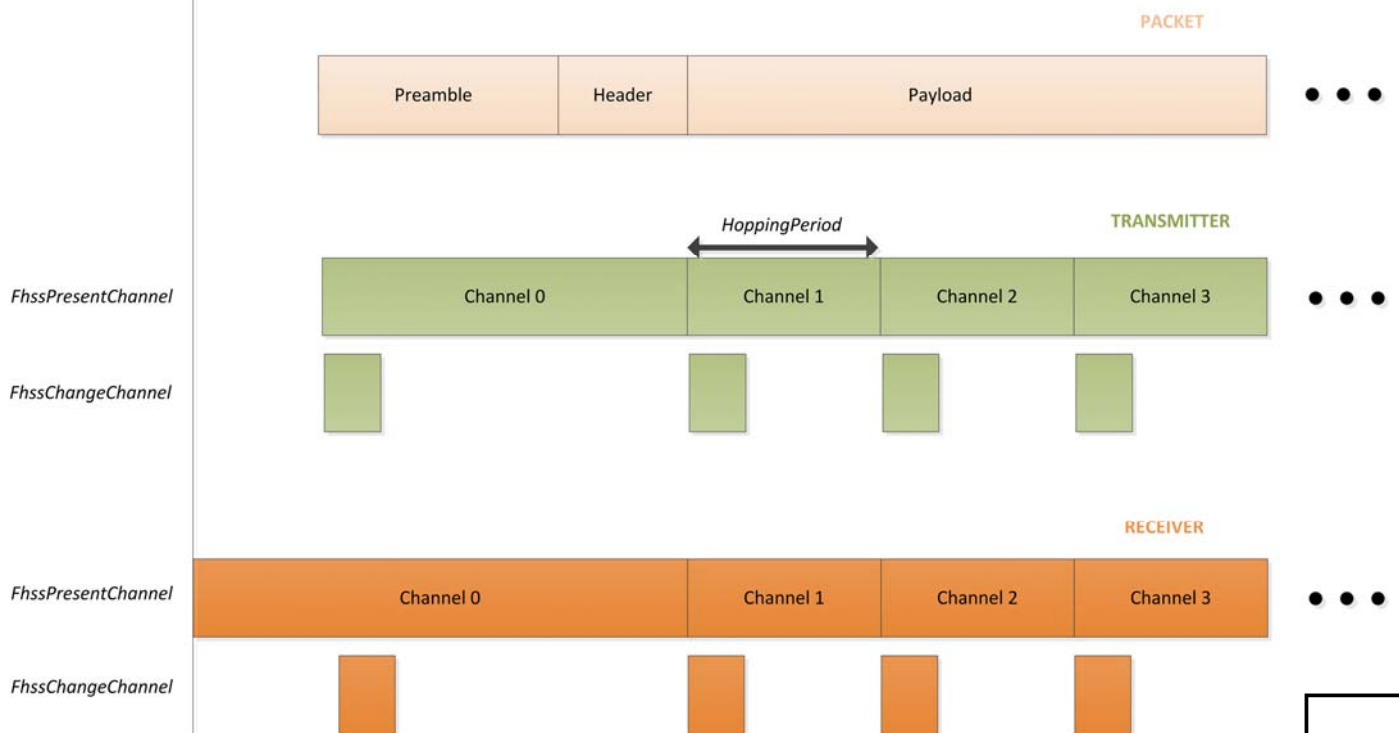


Figure 6. Interrupts generated in the case of successful frequency hopping communication.

4.1.2. LoRa™ Modem Registers

(45h)

4.1.2.1. LoRa™ Configuration Registers

Registers 0x00 to 0x0F are only in Sleep and Standby modes. Registers 0x10 to 0x1F are in the automatic top byte sequence (TUS modes) are not available in LoRa™ mode. LoRa™ Modem register mapping changes as shown in Table 4-1.

4.1.2.2. Status Registers

4.1.2.3. LoRa™ TUS Mode Fundamentals

OVERVIEW

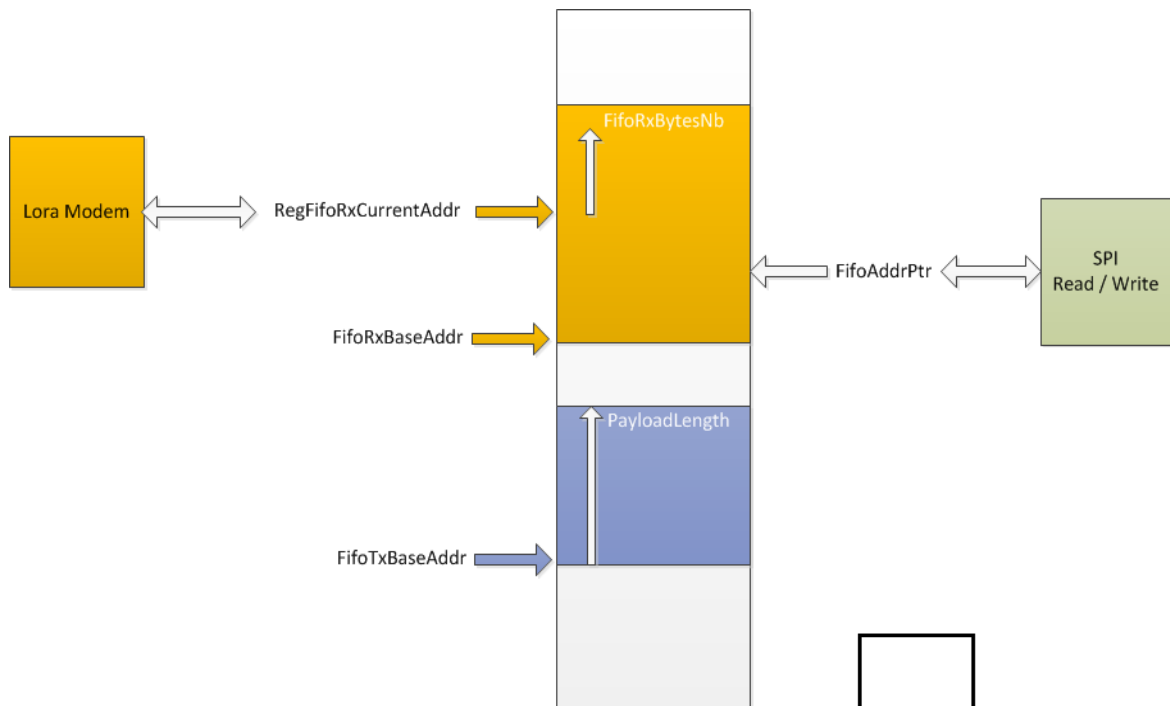


Figure 7. LoRa™ data buffer

Principle of operation

1. Basic principle

2. Basic principle

3. Basic principle

4. Basic principle

5. Basic principle

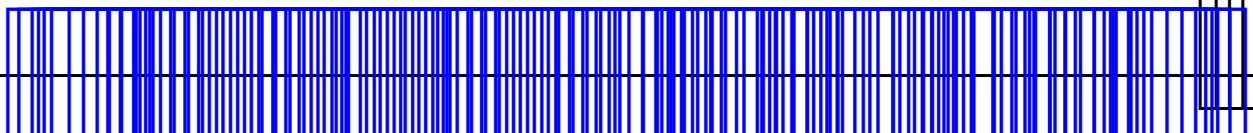
6. Basic principle

7. Basic principle

8. Basic principle

9. Basic principle

10. Basic principle



4.1.3. Operation of the LoRa™ Modem

4.1.3.1. Operating Mode Control

The LoRa™ Modem can be configured to operate in one of the following modes. The operating mode is controlled by the **RegOpMode** register.

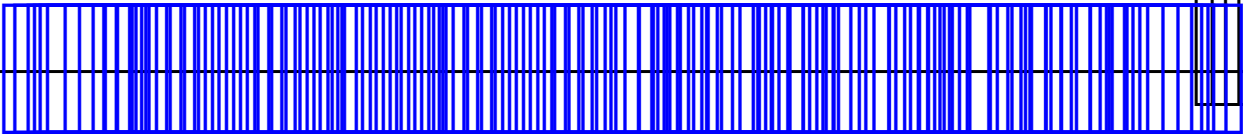
Table 61 LoRa™ Operating Mode Functionality

Operating Mode	Functionality
SLEEP	The LoRa™ Modem enters a low-power sleep mode. The internal clock is stopped, and the modem is not able to receive or transmit data. The modem wakes up when the RegOpMode register is updated.
STAND-BY	The LoRa™ Modem enters a low-power stand-by mode. The internal clock is stopped, and the modem is not able to receive or transmit data. The modem wakes up when the RegOpMode register is updated.
FSTX	The LoRa™ Modem enters a fast transmit mode. The modem transmits data at a high rate. The modem returns to the STAND-BY mode when the transmission is complete.
FSRX	The LoRa™ Modem enters a fast receive mode. The modem receives data at a high rate. The modem returns to the STAND-BY mode when the reception is complete.
TX	The LoRa™ Modem enters a transmit mode. The modem transmits data at a normal rate. The modem returns to the STAND-BY mode when the transmission is complete.
RXCONTINUOUS	The LoRa™ Modem enters a continuous receive mode. The modem continuously receives data. The modem returns to the STAND-BY mode when the reception is complete.
RXSINGLE	The LoRa™ Modem enters a single receive mode. The modem receives data at a normal rate. The modem returns to the STAND-BY mode when the reception is complete.
CAD	The LoRa™ Modem enters a channel access detection mode. The modem continuously monitors the channel for activity. The modem returns to the STAND-BY mode when the channel is clear.

4.1.4. Frequency Settings

$$F_{STEP} = \frac{E_{RSS}}{1000}$$

$$F_{RF} = F_{STEP} \times F_{rf}(23,0)$$



4.1.5. LoRa™ Modem State Machine Sequences

Data Transmission Sequence

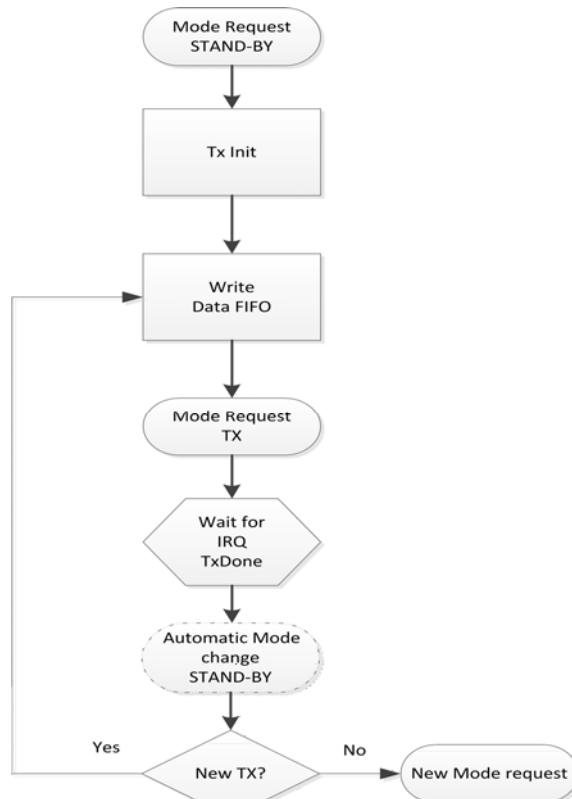


Figure 4.1.5. LoRa™ modulation transmission sequence.

- ◆
- ◆
- ◆
- ◆
- ◆

Long™ Transfer Data RF B Pinning

Pin: PinAddr

Pin: TxPinBase

Pin: PinAddr

Data Reception Sequence

LoRa™

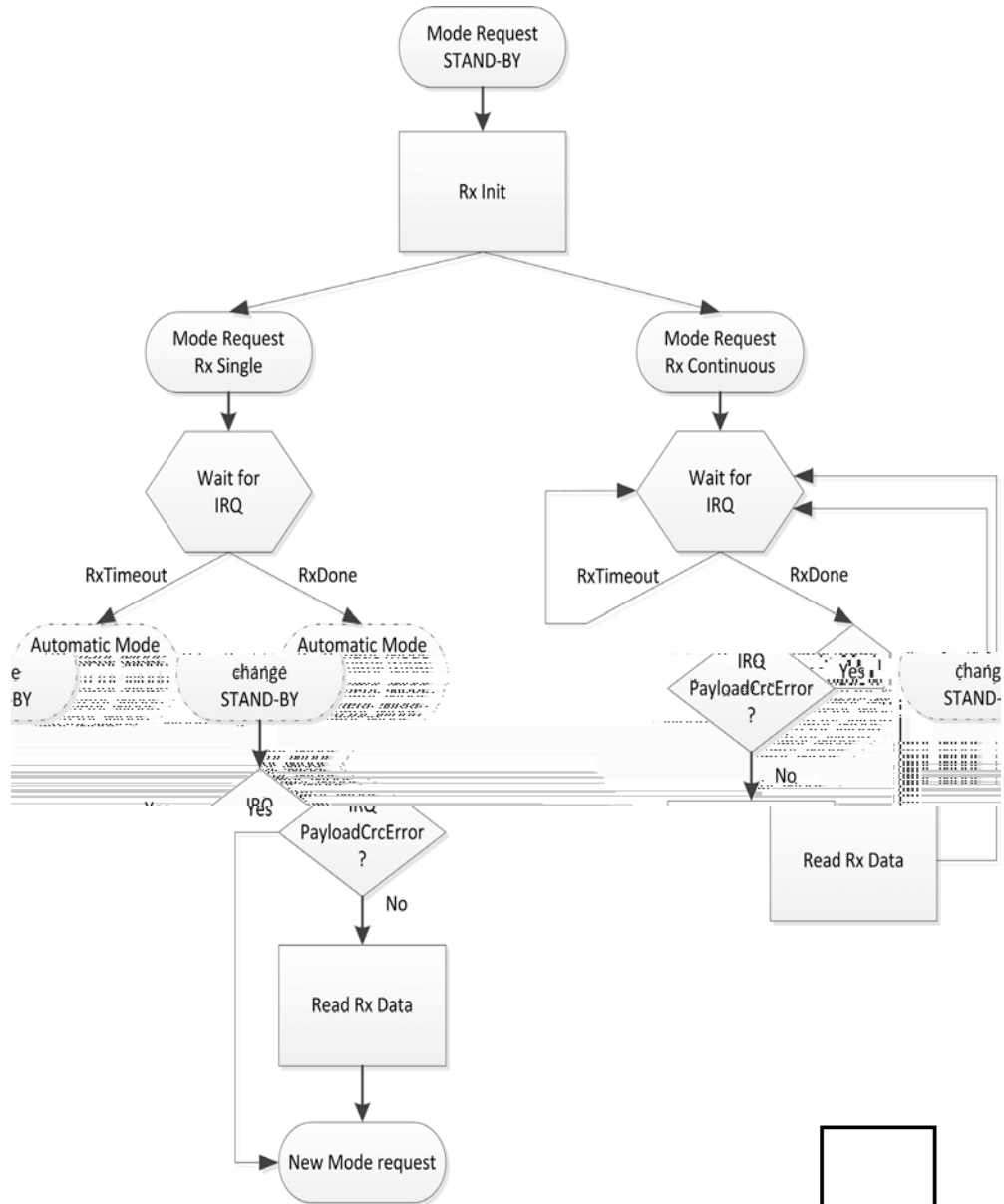
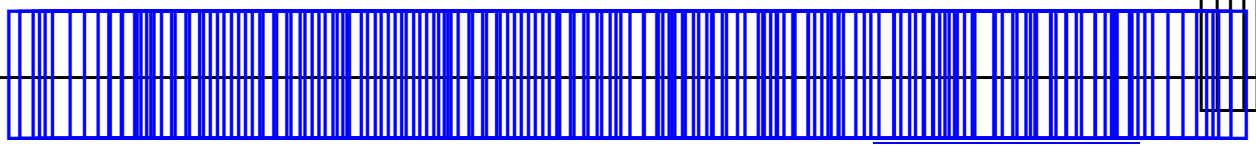


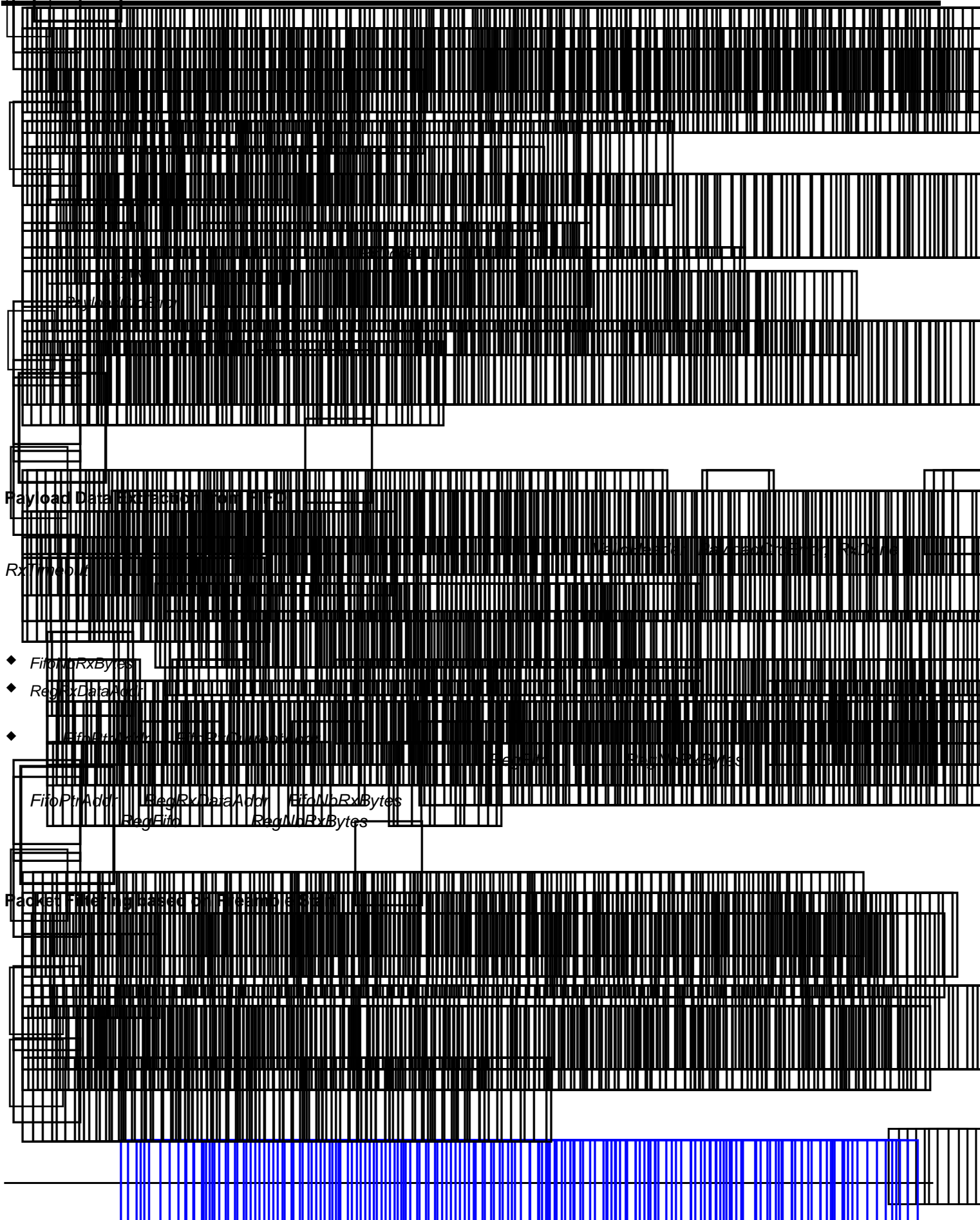
Figure 9. LoRa™ receive sequence.

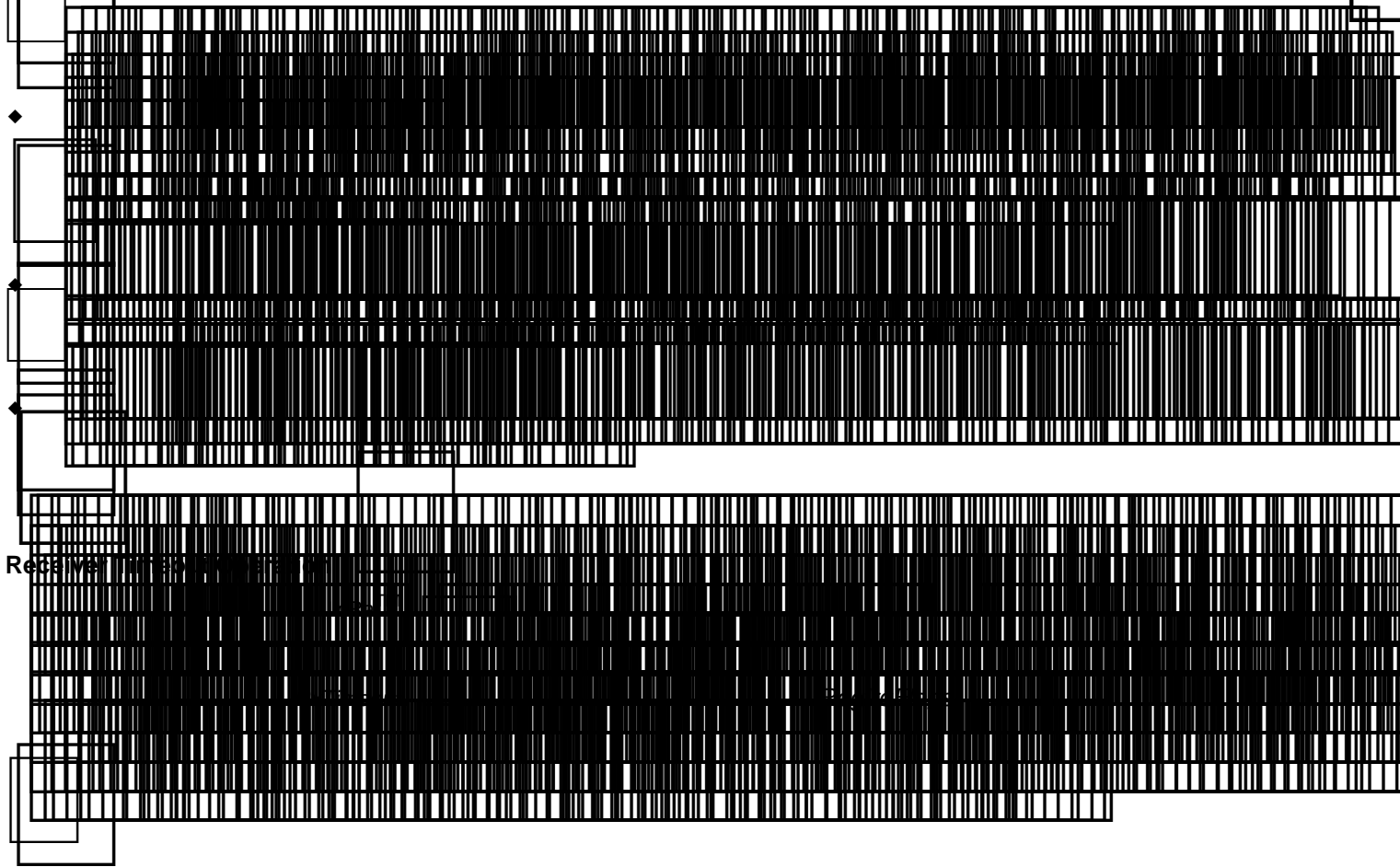
Single Reception Disturbing Wave

Reception Disturbing Wave

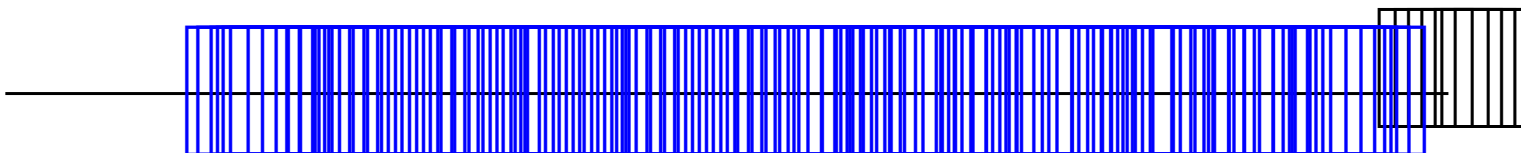
Continuous Reception Disturbing Wave







$$TimeOut = LoraRxTimeout \cdot Ts$$



Channel Access Mode

LoRa™



Figure 10. LoRa™ CAD flow

Principle of Operation

- ◆
- ◆
- ◆
- ◆
- ◆

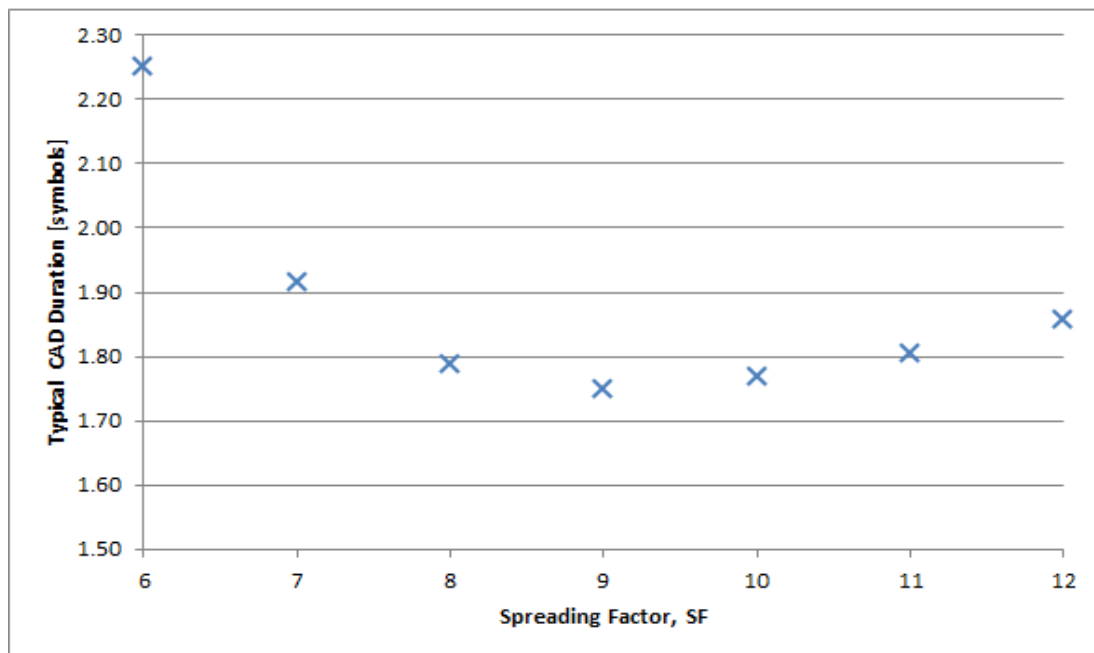


Figure 11. Channel activity detection (CAD) time as a function of spreading factor

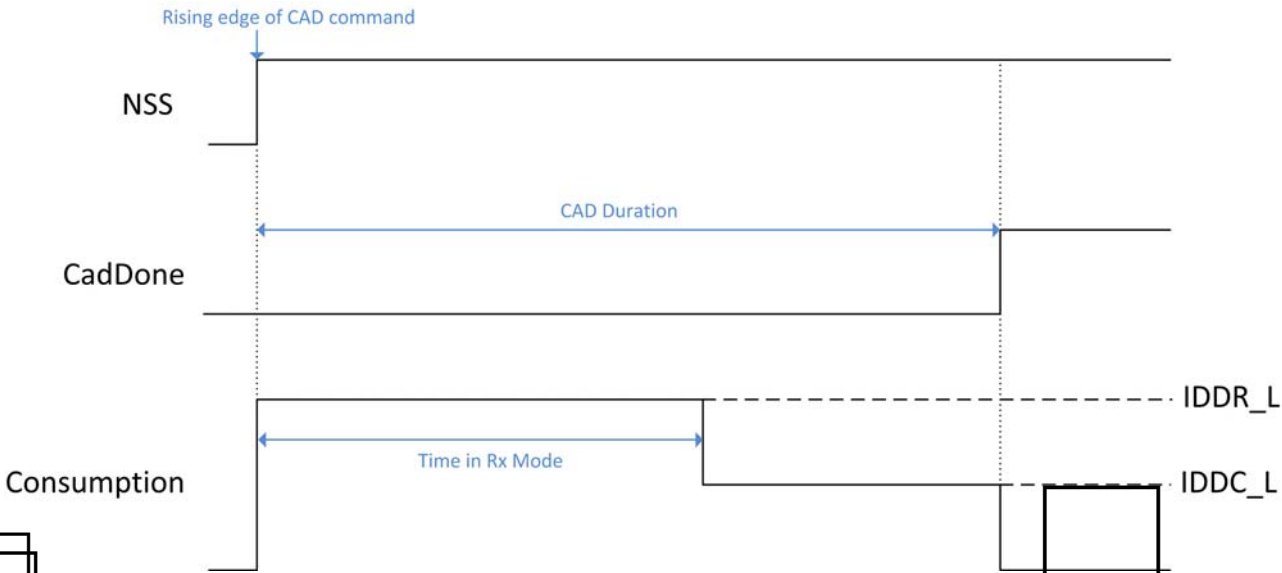


Figure 12: Consumption Power Profile for LoRa CAD Process

Table 62: LoRa CAD Consumption Figures

Bandwidth (kHz)	Full Rx, IDDR_L (mA)	Processing, IDDC_L (mA)
125	10.5	10.5
250	10.5	10.5
500	10.5	10.5
1000	10.5	10.5
125	10.5	10.5
250	10.5	10.5
500	10.5	10.5
1000	10.5	10.5

4.1.5.1: Digital I/O Pin Mapping

LoRa™
RegDioMapping1 RegDioMapping2.

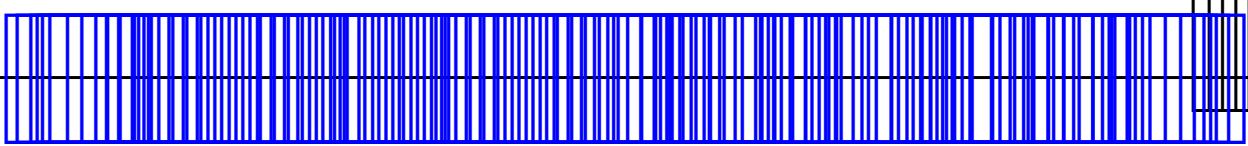


Table 63 DIO Mapping LoRa™ Mode

Operating Mode	DIO Mapping	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0
FSK/OOK Modem							
LoRa™ Modem							

4.2 FSK/OOK Modem

4.2.1 BitRate

RegBitrateMsb and RegBitrateLsb	Bitrate

$$BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{itrateFrac}{16}}$$

Note: BitRate and itrateFrac have no effect when the device is configured to operate in LoRa™ mode.

Bitrate (Hz)



Table 64 Bit Rate Examples

Type	BitRate (15.0)	BitRate (7.0)	(G)FSK (G)MSK	OOK	Actual BR (bits)

4.2.2 FSK/OOK Transmission

4.2.2.1 FSK(13,0) Transmission

$$F_{DEV} = F_{STEP} \times F_{dev}(13,0)$$

$$F_{DEV} + \frac{R}{2} \leq (250)kHz$$



Note No constraint applies to the modulation index of the transmitter, but the frequency deviation must be set between 600 Hz and 200 kHz.

4.2.2.2. OOK Modulation

4.2.2.3. Modulation Shaping

The Modulation Shaping setting is used to select the modulation shaping method.

Note The transmitter must be restarted if the ModulationShaping setting is changed, in order to recalibrate the built-in filter.

4.2.3. FSK/OOK Reception

4.2.3.1. FSK Carrier Frequency

$$0 \leq \Delta f \leq \frac{2 \times K_F}{2 \times B_A} \leq 0$$

4.2.3.2. OOK Detection Threshold

Modulation Type RegDokPeak



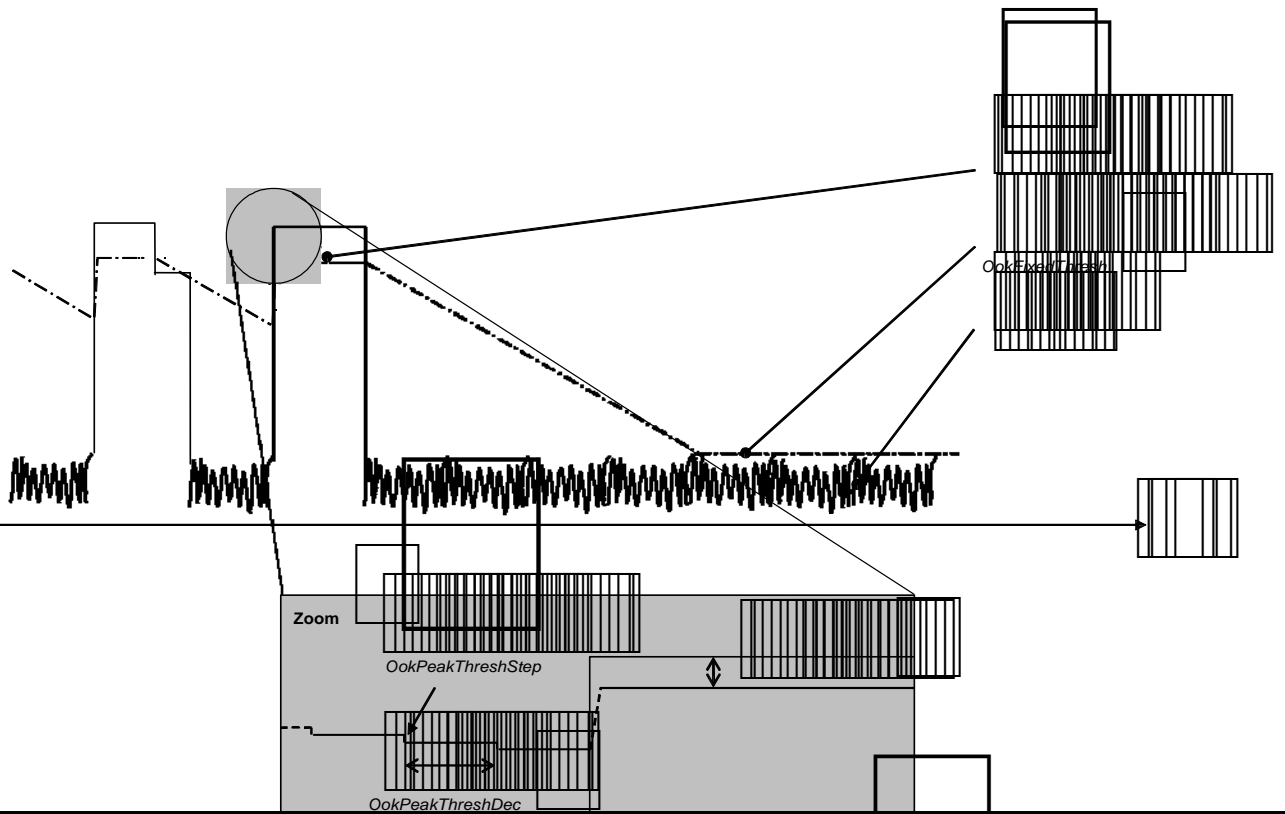


FIGURE 3. OOK Peak Detection Description

Optimizing Peak Detection

OokPeakThreshStep

OokPeakThreshDec

OokPeakThreshStep

OokPeakThreshDec

OokPeakThreshStep

OokPeakThreshDec

OokPeakThreshStep

OokPeakThreshDec

OokPeakThreshStep

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OokPeakThreshDec

OokPeakThreshStep

OokPeakThreshDec

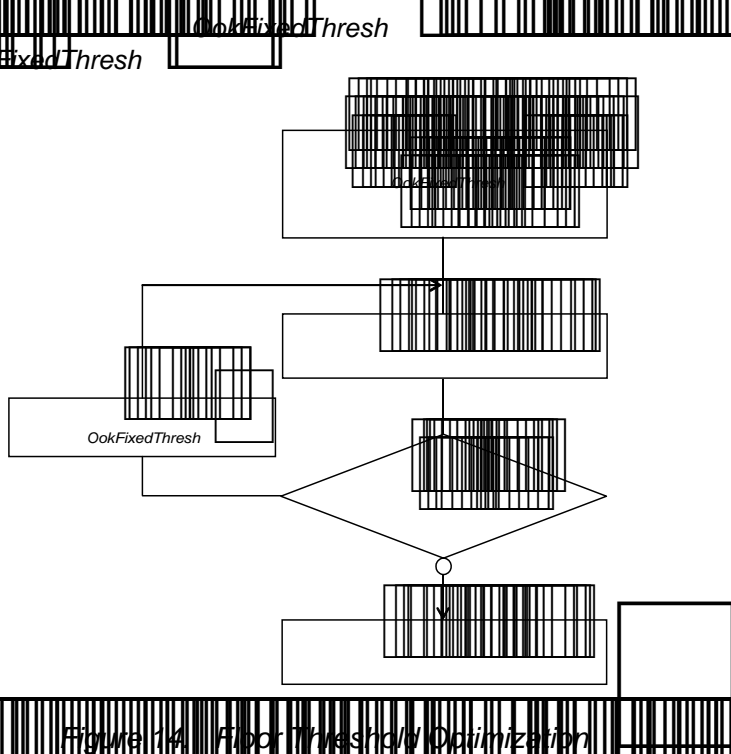


Figure 14. Floor Threshold Optimization

Optimizing On Demand Thresholding Schemes

OokPeakThreshStep OokPeakThreshDec
RegOokPeak

Alternative OOK Demodulator Threshold Modes

◆ $\text{RegModemThresh} = \text{ModemThresh}$

4.2.3.3 Bit Synchronizer

RegBitrate.

BitRateLsb

BitRateLsb

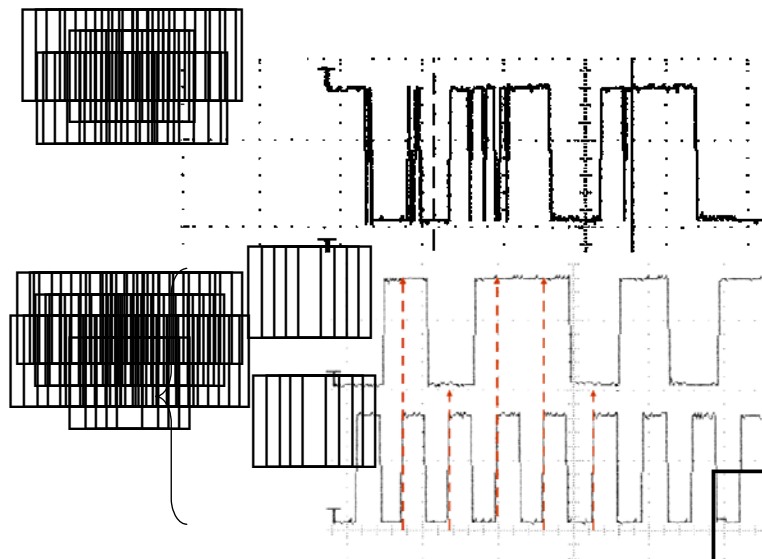


Figure 4.5 Bit Synchronizer Description

◆

◆

◆



4.2.3.4.1. Feedback Frequency

The feedback frequency is calculated as follows:

The feedback frequency is calculated as follows:

The feedback frequency is calculated as follows:

$$BW_{2dB} = 2 \times k \left(F_{DEV} + \frac{1}{2} \right)$$

$$FEI = F_{STEP} \times FeiValue$$

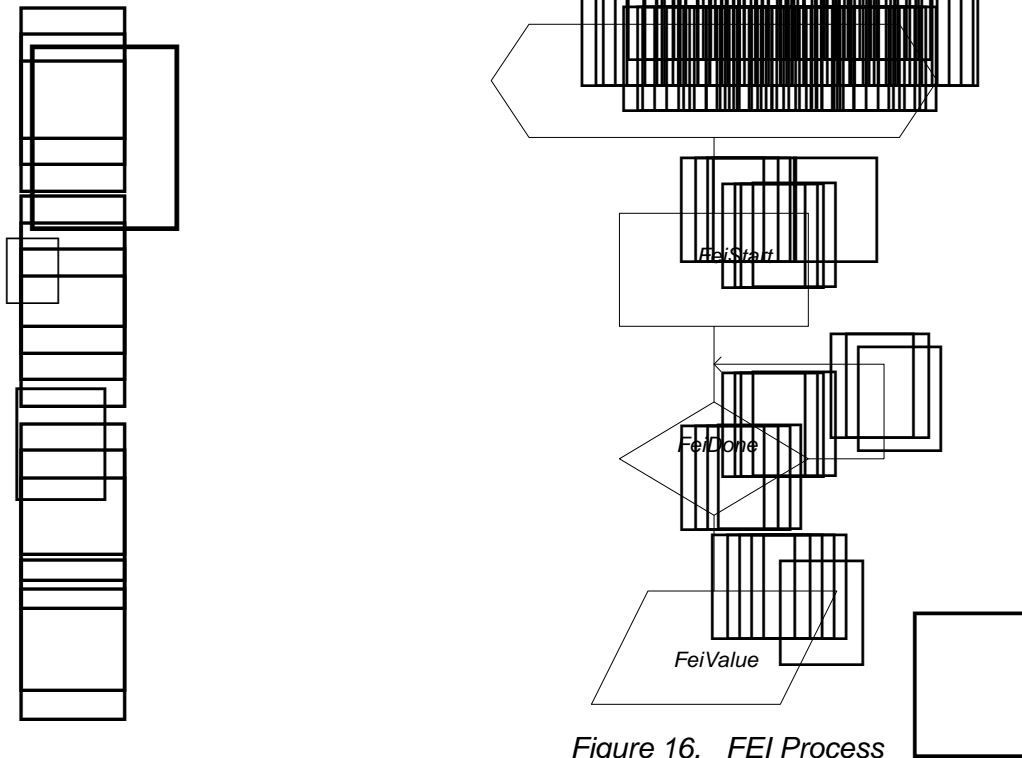


Figure 16. FEI Process

Afca Auto On

◆ **Barcode**

Page 4

THE UNIVERSITY OF CHICAGO

Prevalence/Detect

San Diego On Preamble

RegRxConfig

4.2.3.6. *Predefined Data*

PreambleDetectorSize

RegPreambleDetect

Table 65 Preamble Detector Settings

[illegible]

Национальный парк «Байкал» 1

Barcode Detector On

4.2.3.7 Image Reject Filter

4.2.3.8 Image and RSSI Detector

- ◆
- ◆
- ◆

AutoImageCalOn

4.2.3.9 Timeout Functions

- ◆ Timeout $\text{TimeOut} = \text{RxRssi} \times 16 \times \text{Tbit}$ Rssi
- ◆ Timeout $\text{TimeOut} = \text{Preamble} \times 16 \times \text{Tbit}$ PreambleDetect
- ◆ Timeout $\text{TimeOut} = \text{SyncAddress} \times 16 \times \text{Tbit}$ SyncAddress

RegRxConfig:

Table 66 RxTrigger Settings to Enable Timeout Interrupts

Receiver Triggering Event	RxTrigger (2.0)	Timeout on Rssi	Timeout on Preamble	Timeout on SyncAddress
Rssi				
PreambleDetect				
Rssi				
PreambleDetect				

4.2.4. Operating Modes of FSK/DOK Mode

See On Mode

Table 67 Basic Transceiver Modes

Mode	Selected mode	Symbol	Enabled blocks
Standby	Standby	⏻	RF, TX, RX, PA, LNA, PLL, FSK, DOK, FSK, DOK, FSK, DOK
Transmit	Transmit	➡	RF, TX, PA, LNA, PLL, FSK, DOK, FSK, DOK, FSK, DOK
Receive	Receive	⬅	RF, RX, LNA, PLL, FSK, DOK, FSK, DOK, FSK, DOK
Transmit and Receive	Transmit and Receive	↔	RF, TX, RX, PA, LNA, PLL, FSK, DOK, FSK, DOK, FSK, DOK

4.2.5. Startup Times

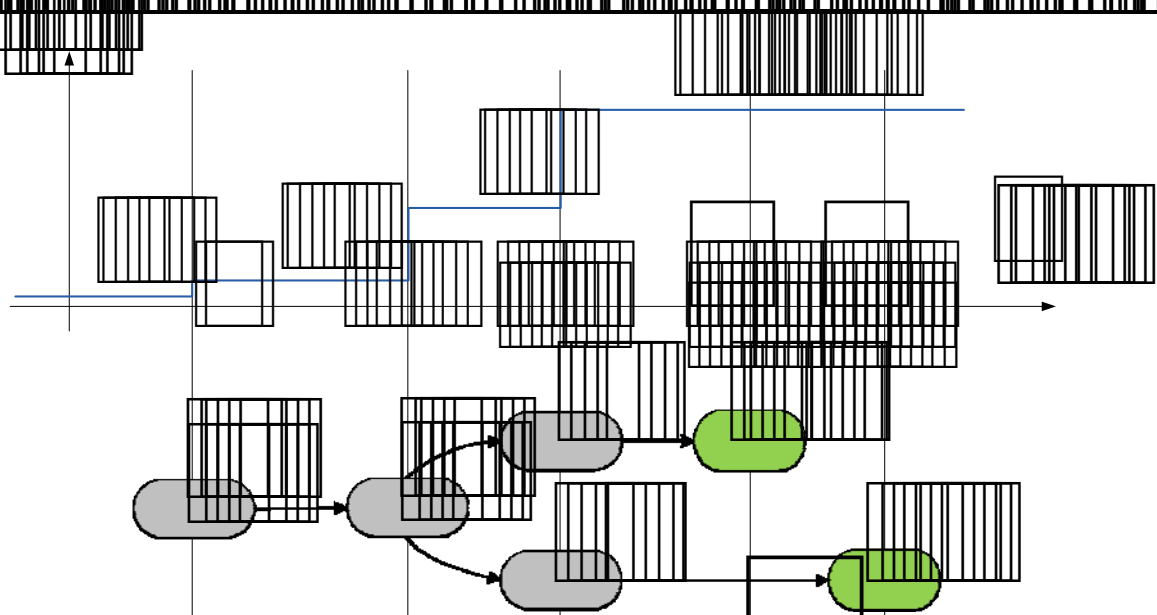


Figure 47 Startup process

$$TS_{-TR} = 5 \times s + 1.25 \times PaRamp + \frac{1}{2} \times Wit$$

~~Reinforced Concrete~~

Whit

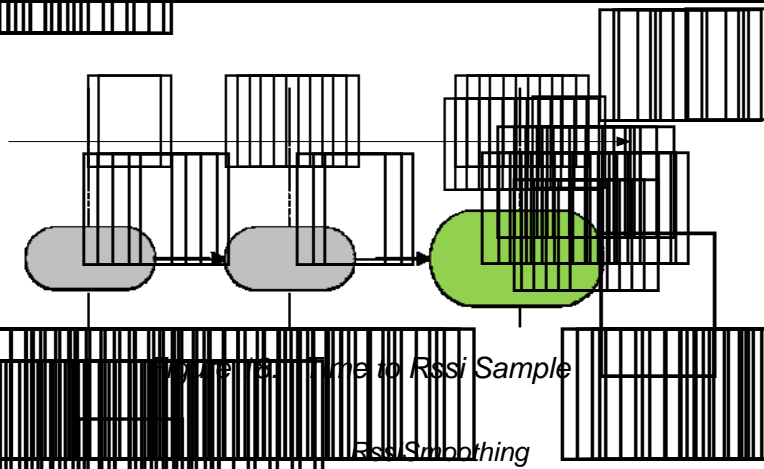
$$TS_{TR} = 5\mu s + \frac{1}{2} \times T_{bit}$$

 Δf_{CBW}
$$A_{\mu} \times B_{\mu}$$

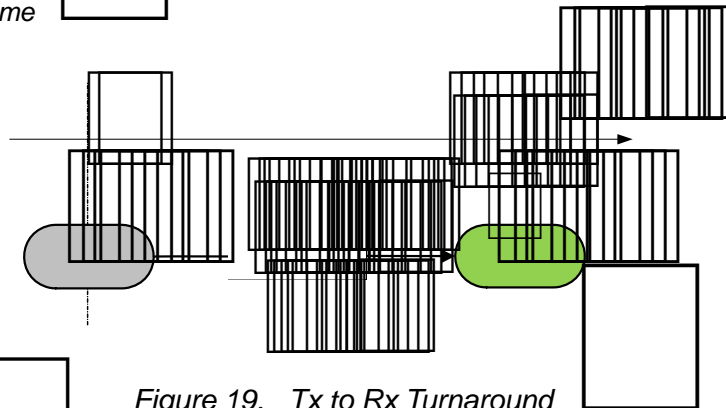
Table 68 Receiver Startup Time Summary

[illegible]

4.2.5.3 Time to Rssi Evaluation

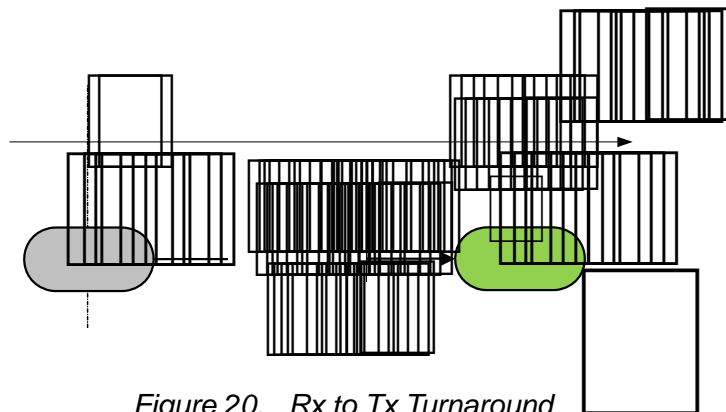


4.2.5.4 Tx to Rx Turnaround Time



Note The SPI instruction times are omitted, as they can generally be very small as compared to other timings (up to 10MHz SPI clock).

4.2.5.5 Rx to Tx



4.2.5.6 Receiver Hopping Rx to Rx

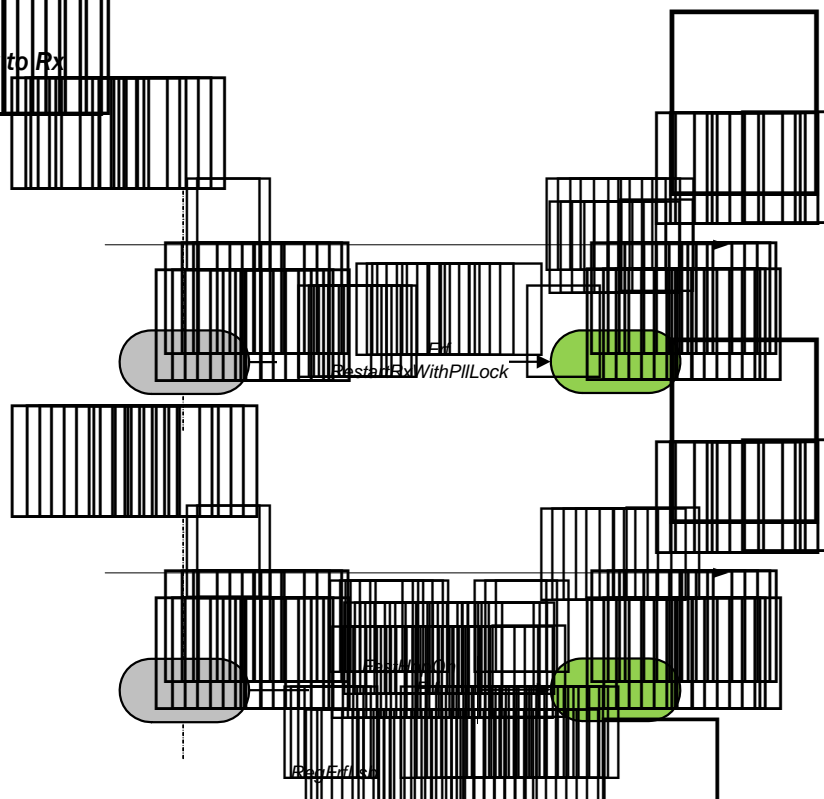


Figure 21. Receiver Hopping

4.2.5.7 Tx to Tx

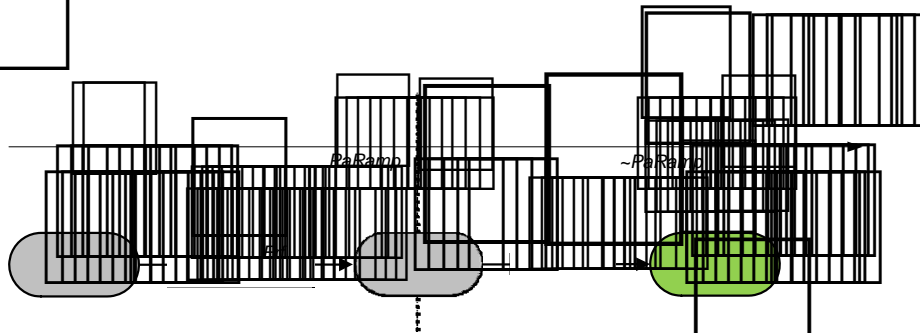


Figure 22. Transmitter Hopping

4.2.6 Receiver Start-Up Options

- ◆ RestartRxWithPLL Lock When Rx is in Sleep Mode
- ◆ RestartRxWithPLL Lock When Rx is in Standby Mode
- ◆ RestartRxWithPLL Lock When Rx is in Shutdown Mode

Table 69 Receiver Startup Options

Triggering Event	Realized Function	AgcAutoOn	AfcAutoOn	RxTrigger (2:0)
Rssi				
PreambleDetect				
Rssi				
PreambleDetect				
AgcAutoOn		naGain	Reg na	

4.2.7. Receiver Restart Methods

4.2.7.1. Restarting the Receiver

- ◆ The receiver can be restarted by sending a RestartRx command to the module. The command is sent via the SPI interface. The command is sent to the module via the SPI interface. The command is sent to the module via the SPI interface.
- ◆ The receiver can be restarted by sending a RestartRx command to the module. The command is sent via the SPI interface. The command is sent to the module via the SPI interface.
- ◆ The receiver can be restarted by sending a RestartRx command to the module. The command is sent via the SPI interface. The command is sent to the module via the SPI interface.

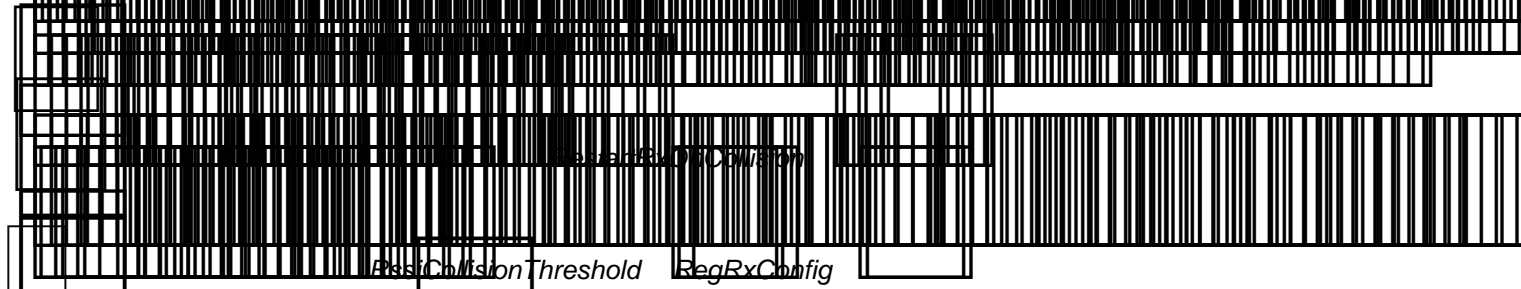
Note: ModeReady must be at logic level 1 for a new RestartRx command to be taken into account.

4.2.7.2. Automatic Restart after a Packet Reception Error

4.2.7.2.1. Automatic Restart after a Packet Reception Error

- ◆ The receiver can be restarted by sending a RestartRx command to the module. The command is sent via the SPI interface. The command is sent to the module via the SPI interface.
- ◆ The receiver can be restarted by sending a RestartRx command to the module. The command is sent via the SPI interface. The command is sent to the module via the SPI interface.
- ◆ The receiver can be restarted by sending a RestartRx command to the module. The command is sent via the SPI interface. The command is sent to the module via the SPI interface.
- ◆ The receiver can be restarted by sending a RestartRx command to the module. The command is sent via the SPI interface. The command is sent to the module via the SPI interface.

4.2.7.3. RFM95/96/97/98(W) Register 0x7F: Rx Collision



4.2.8. Top Level Sequencer



NOTE THAT THIS FUNCTIONALITY IS ONLY AVAILABLE IN FSK/OOK MODE.

Note: SequencerSel and Stop are never both set at the same time.

4.2.9. Sequencer States

Table 70 Sequencer States

Sequencer State	Description
SequencerOff State	SequencerSel = 0, RxCollision = 0, RxCollisionThreshold = 0, RxCollision = 0
Idle State	SequencerSel = 1, RxCollision = 0, RxCollisionThreshold = 0, RxCollision = 0
Transmit State	SequencerSel = 1, RxCollision = 0, RxCollisionThreshold = 0, RxCollision = 0
Receive State	SequencerSel = 1, RxCollision = 0, RxCollisionThreshold = 0, RxCollision = 0
PacketReceived	SequencerSel = 1, RxCollision = 0, RxCollisionThreshold = 0, RxCollision = 0
LowPowerSelection	SequencerSel = 1, RxCollision = 0, RxCollisionThreshold = 0, RxCollision = 0
RxTimeout	SequencerSel = 1, RxCollision = 0, RxCollisionThreshold = 0, RxCollision = 0

Table 71 Sequencer Transition Options

[illegible]

4.2.6.2 Timers

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100

SequencerStart

32 interrupt

77 interrupt

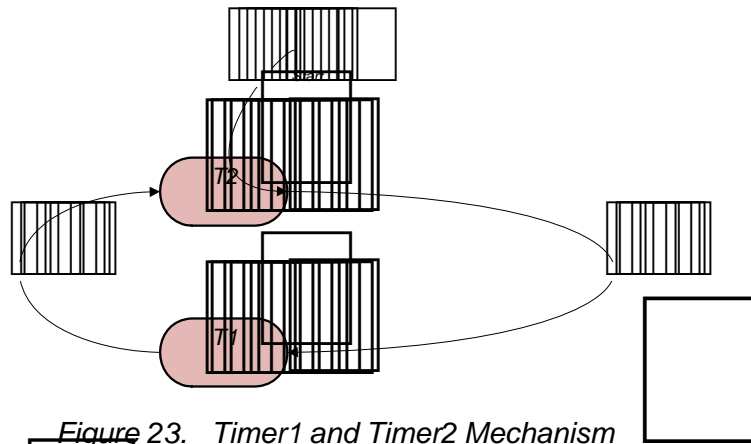


Figure 23. Timer1 and Timer2 Mechanism

Note The timer sequence is completed independently of the actual Sequencer state. Thus, both timers need to be on to achieve periodic cycling.



4.2.3.4. Sequential Search Method

Stop RegSeqConfig1

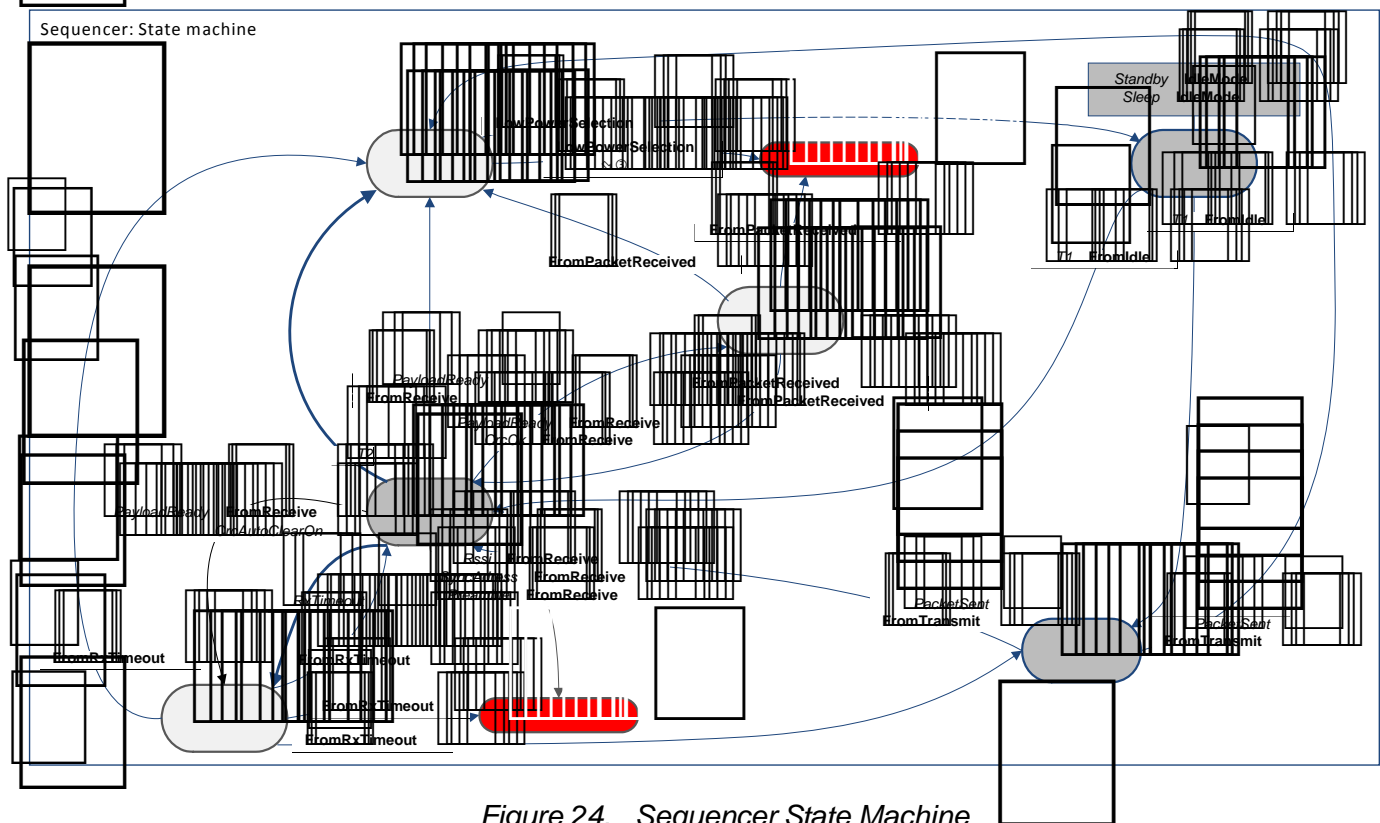
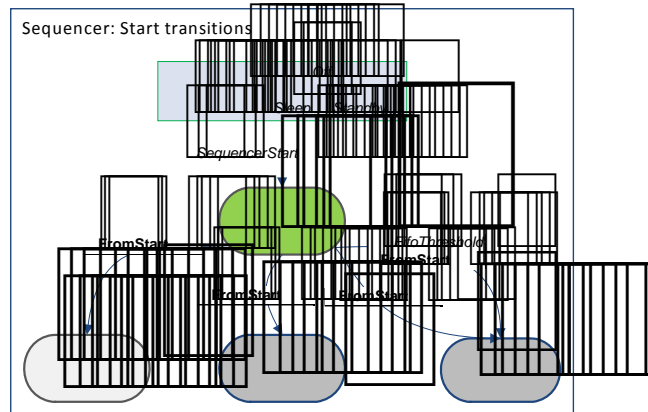


Figure 24. Sequencer State Machine

4.2.9. Data Processing in FSK/OOK Mode

~~4.2.9.1: Block Diagram~~

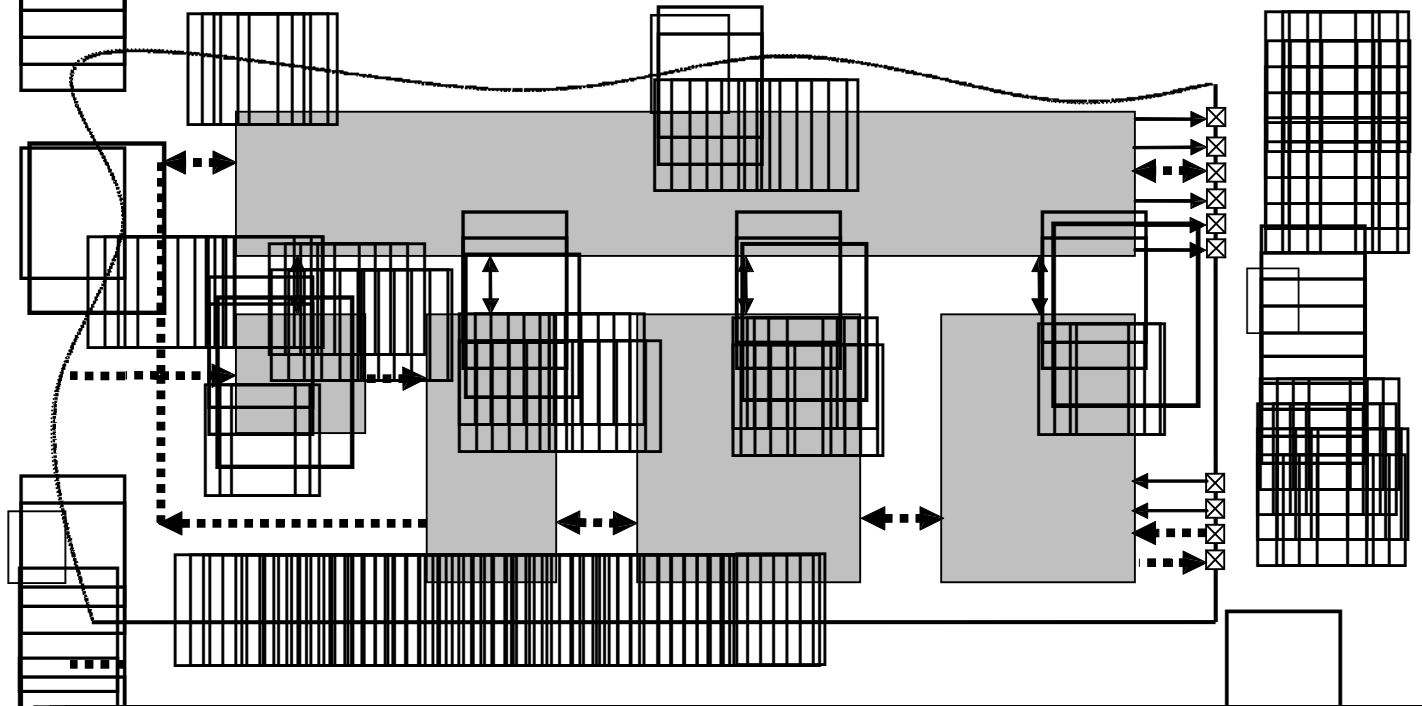


Figure 20. R² vs D/90/97/98/11/12/14/15/16/17/18/19/20/21/22/23/24/25/26/27/28/29/30/31/32/33/34/35/36/37/38/39/40/41/42/43/44/45/46/47/48/49/50/51/52/53/54/55/56/57/58/59/60/61/62/63/64/65/66/67/68/69/70/71/72/73/74/75/76/77/78/79/80/81/82/83/84/85/86/87/88/89/90/91/92/93/94/95/96/97/98/99/100/101/102/103/104/105/106/107/108/109/110/111/112/113/114/115/116/117/118/119/120/121/122/123/124/125/126/127/128/129/130/131/132/133/134/135/136/137/138/139/140/141/142/143/144/145/146/147/148/149/150/151/152/153/154/155/156/157/158/159/160/161/162/163/164/165/166/167/168/169/170/171/172/173/174/175/176/177/178/179/180/181/182/183/184/185/186/187/188/189/190/191/192/193/194/195/196/197/198/199/200/201/202/203/204/205/206/207/208/209/210/211/212/213/214/215/216/217/218/219/220/221/222/223/224/225/226/227/228/229/230/231/232/233/234/235/236/237/238/239/240/241/242/243/244/245/246/247/248/249/250/251/252/253/254/255/256/257/258/259/260/261/262/263/264/265/266/267/268/269/270/271/272/273/274/275/276/277/278/279/280/281/282/283/284/285/286/287/288/289/290/291/292/293/294/295/296/297/298/299/300/301/302/303/304/305/306/307/308/309/310/311/312/313/314/315/316/317/318/319/320/321/322/323/324/325/326/327/328/329/330/331/332/333/334/335/336/337/338/339/340/341/342/343/344/345/346/347/348/349/350/351/352/353/354/355/356/357/358/359/360/361/362/363/364/365/366/367/368/369/370/371/372/373/374/375/376/377/378/379/380/381/382/383/384/385/386/387/388/389/390/391/392/393/394/395/396/397/398/399/400/401/402/403/404/405/406/407/408/409/410/411/412/413/414/415/416/417/418/419/420/421/422/423/424/425/426/427/428/429/430/431/432/433/434/435/436/437/438/439/440/441/442/443/444/445/446/447/448/449/450/451/452/453/454/455/456/457/458/459/460/461/462/463/464/465/466/467/468/469/470/471/472/473/474/475/476/477/478/479/480/481/482/483/484/485/486/487/488/489/490/491/492/493/494/495/496/497/498/499/500/501/502/503/504/505/506/507/508/509/510/511/512/513/514/515/516/517/518/519/520/521/522/523/524/525/526/527/528/529/530/531/532/533/534/535/536/537/538/539/540/541/542/543/544/545/546/547/548/549/550/551/552/553/554/555/556/557/558/559/560/561/562/563/564/565/566/567/568/569/570/571/572/573/574/575/576/577/578/579/580/581/582/583/584/585/586/587/588/589/590/591/592/593/594/595/596/597/598/599/600/601/602/603/604/605/606/607/608/609/610/611/612/613/614/615/616/617/618/619/620/621/622/623/624/625/626/627/628/629/630/631/632/633/634/635/636/637/638/639/640/641/642/643/644/645/646/647/648/649/650/651/652/653/654/655/656/657/658/659/660/661/662/663/664/665/666/667/668/669/670/671/672/673/674/675/676/677/678/679/680/681/682/683/684/685/686/687/688/689/690/691/692/693/694/695/696/697/698/699/700/701/702/703/704/705/706/707/708/709/710/711/712/713/714/715/716/717/718/719/720/721/722/723/724/725/726/727/728/729/730/731/732/733/734/735/736/737/738/739/740/741/742/743/744/745/746/747/748/749/750/751/752/753/754/755/756/757/758/759/760/761/762/763/764/765/766/767/768/769/770/771/772/773/774/775/776/777/778/779/780/781/782/783/784/785/786/787/788/789/790/791/792/793/794/795/796/797/798/799/800/801/802/803/804/805/806/807/808/809/810/811/812/813/814/815/816/817/818/819/820/821/822/823/824/825/826/827/828/829/830/831/832/833/834/835/836/837/838/839/840/841/842/843/844/845/846/847/848/849/850/851/852/853/854/855/856/857/858/859/860/861/862/863/864/865/866/867/868/869/870/871/872/873/874/875/876/877/878/879/880/881/882/883/884/885/886/887/888/889/890/891/892/893/894/895/896/897/898/899/900/901/902/903/904/905/906/907/908/909/910/911/912/913/914/915/916/917/918/919/920/921/922/923/924/925/926/927/928/929/930/931/932/933/934/935/936/937/938/939/940/941/942/943/944/945/946/947/948/949/950/951/952/953/954/955/956/957/958/959/960/961/962/963/964/965/966/967/968/969/970/971/972/973/974/975/976/977/978/979/980/981/982/983/984/985/986/987/988/989/990/991/992/993/994/995/996/997/998/999/1000/1001/1002/1003/1004/1005/1006/1007/1008/1009/1010/1011/1012/1013/1014/1015/1016/1017/1018/1019/1020/1021/1022/1023/1024/1025/1026/1027/1028/1029/1030/1031/1032/1033/1034/1035/1036/1037/1038/1039/1040/

4.2.9.2. Data Summary

-

4.2.10 FIFO and SR

Overview and Shift Register (SR)

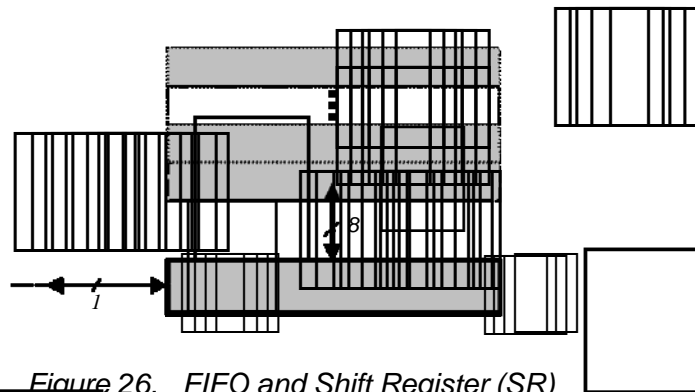
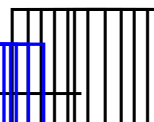
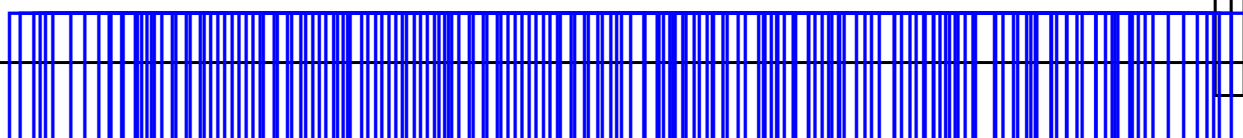


Figure 26. FIFO and Shift Register (SR)

Note When switching to Sleep mode, the FIFO can only be used once the ModeReady flag is set (quasi immediate from all modes except from Tx).

Interrupt Sources and Flags

- ◆ *FifoEmpty* *FifoEmptyFlag*
- ◆ *FifoFull* *FifoFullFlag*
- ◆ *FifoOverflow* *FifoOverflowFlag*
- ◆ *PacketSent* *PacketSentFlag*
- ◆ *FifoLevel* *FifoThreshold* *RegFifoThresh*



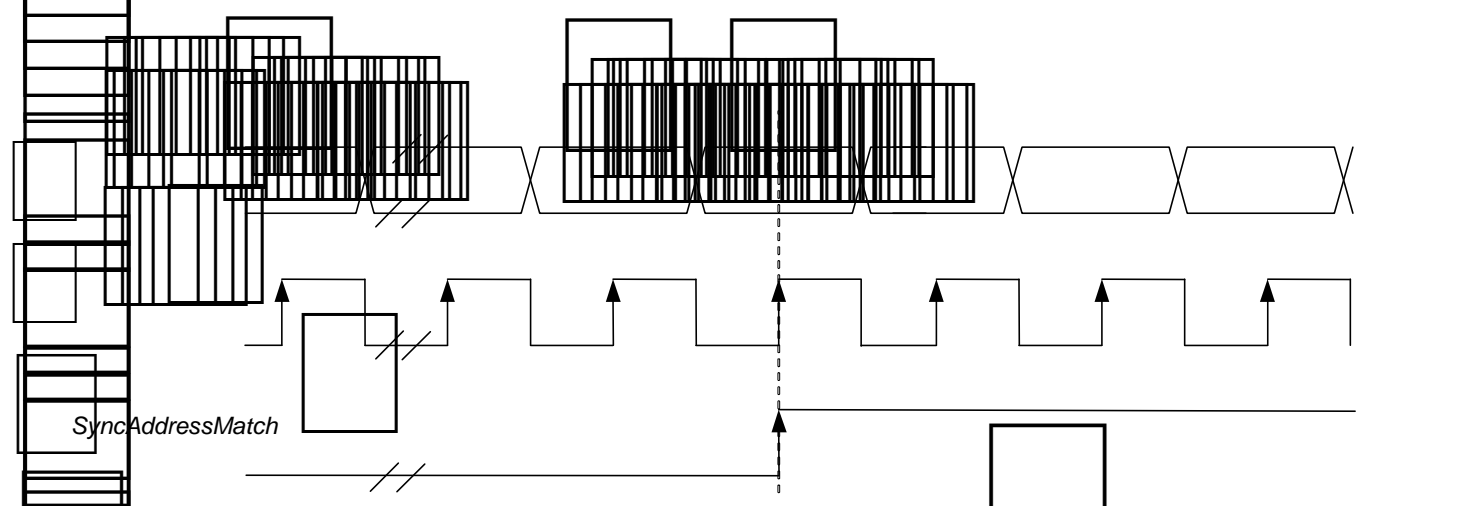
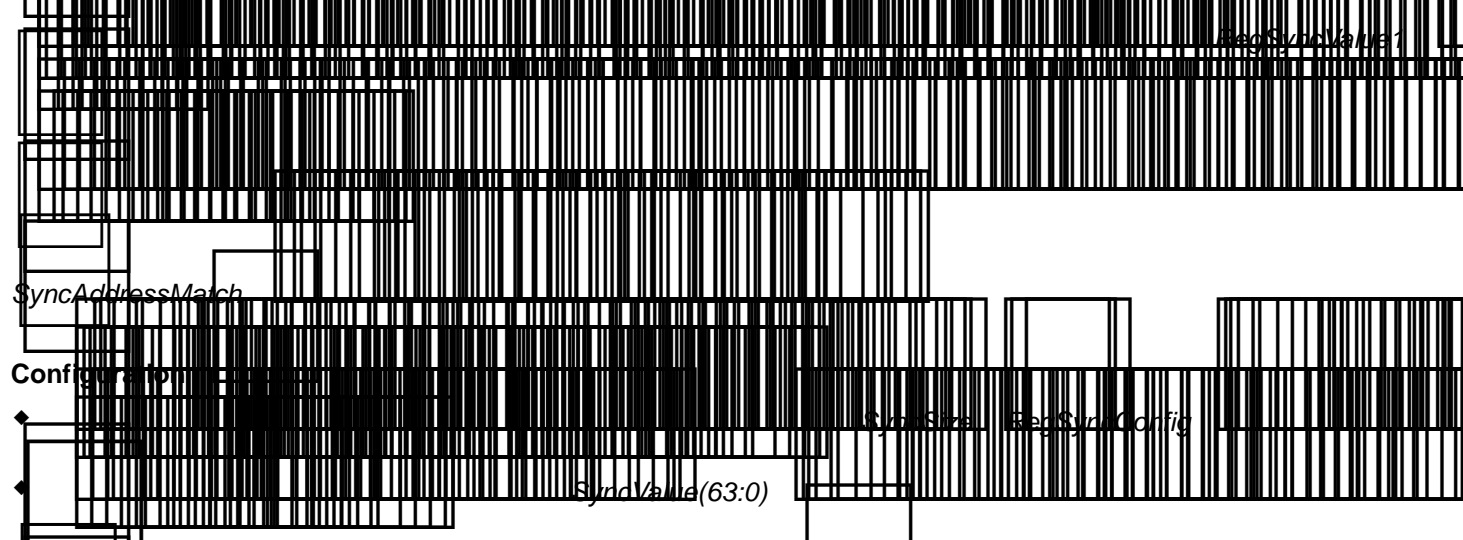


Figure 2-1: Sync Word Recognition



Note: SyncValue choices containing 0x00 bytes are not allowed.



4.2.4.1. Figure DIO Pins Mapping

RegDioMapping1

RegDioMapping2.

Table 74 DIO Mapping, Continuous Mode

	DIOx Mapping	Sleep	Standby	FSRx/Tx	Rx	Tx
DIO0						
DIO1						
DIO2						
DIO3						
DIO4						
DIO5						

Table 75 DIO Mapping, Packet Mode

	DIOx Mapping	Sleep	Standby	FSRx/Tx	Rx	Tx
DIO0						
DIO1						
DIO2						
DIO3						
DIO4						
DIO5						

4.2.12 Continuous Mode

4.2.12.1 General Description

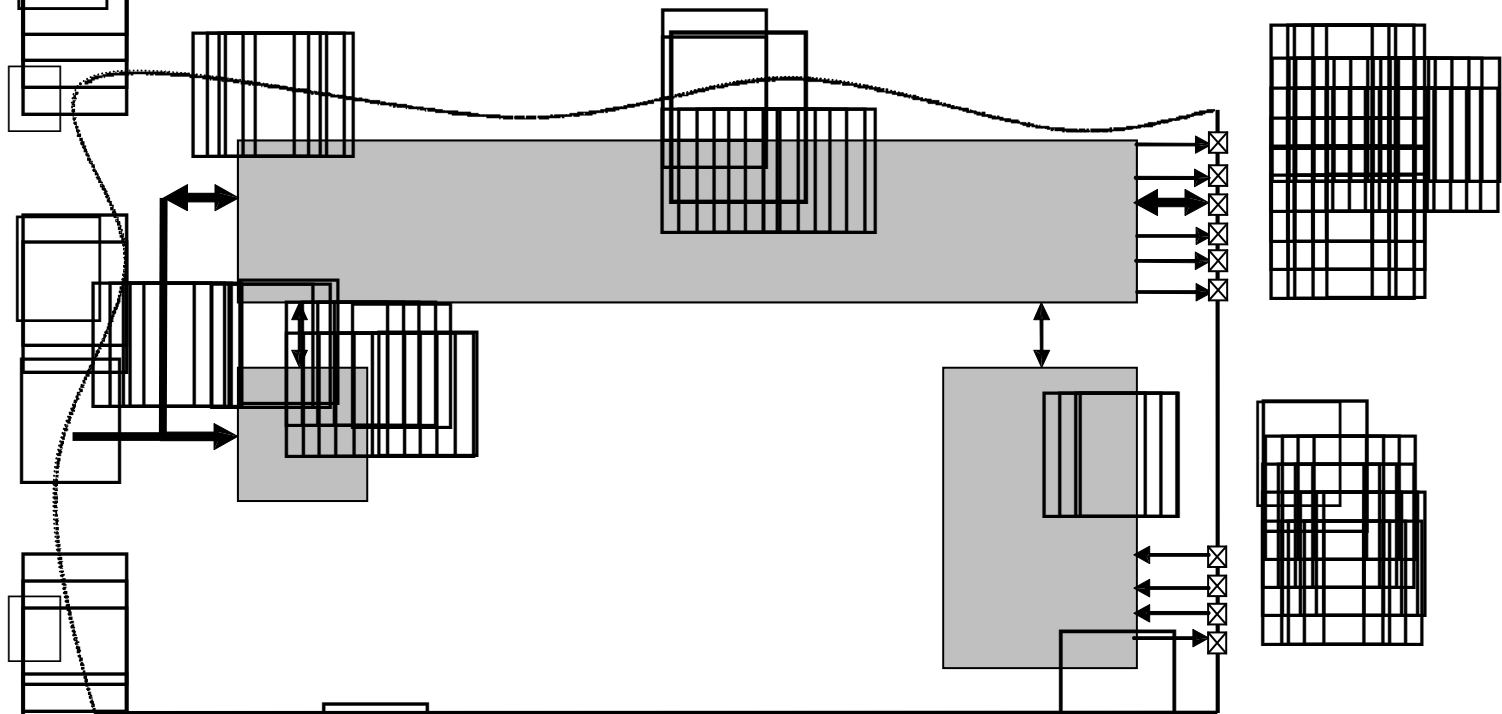


Figure 29. Continuous Mode Conceptual View

4.2.12.2 Timing Diagram

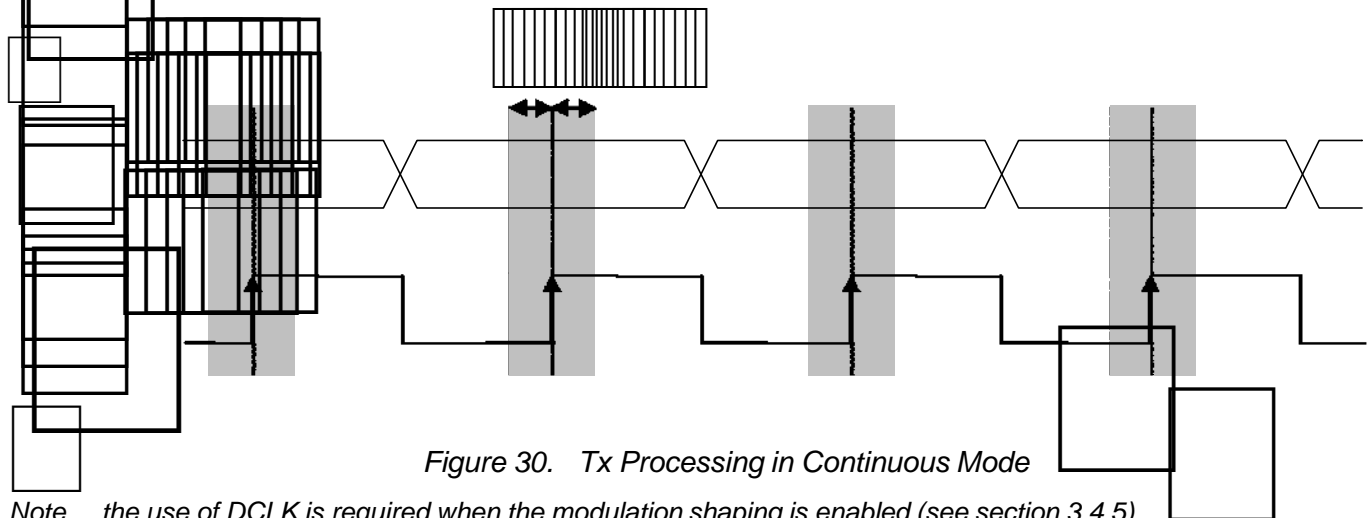


Figure 30. Tx Processing in Continuous Mode

Note the use of DCLK is required when the modulation shaping is enabled (see section 3.4.5).



4.2.12 Rx Processing

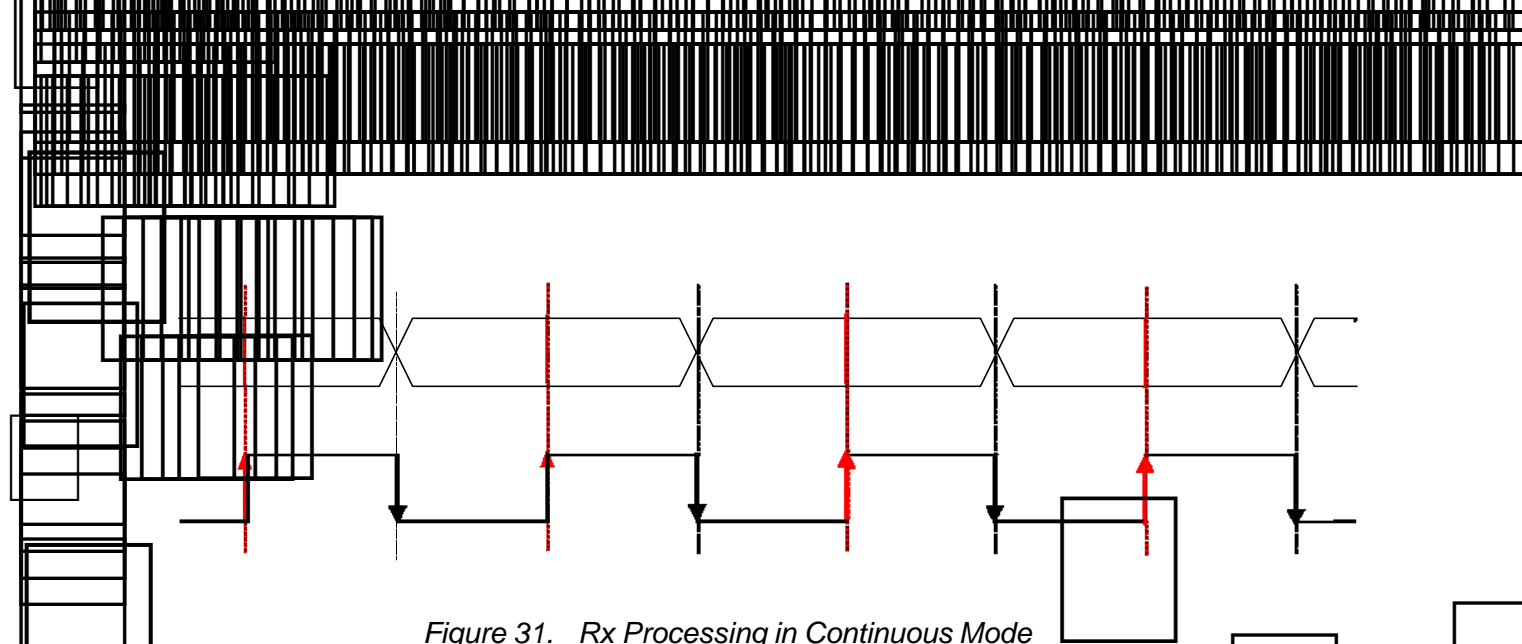
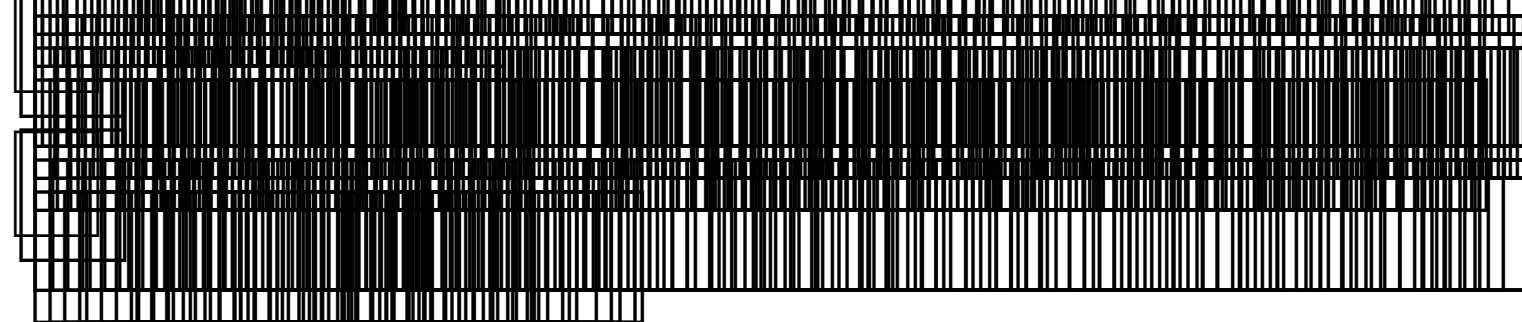


Figure 31. Rx Processing in Continuous Mode

Note In Continuous mode it is always recommended to enable the bit synchronizer to clean the DATA signal even if the DCLK signal is not used by the uC (bit synchronizer is automatically enabled in Packet mode).

4.2.13 Packet Mode

4.2.13.1 General Description



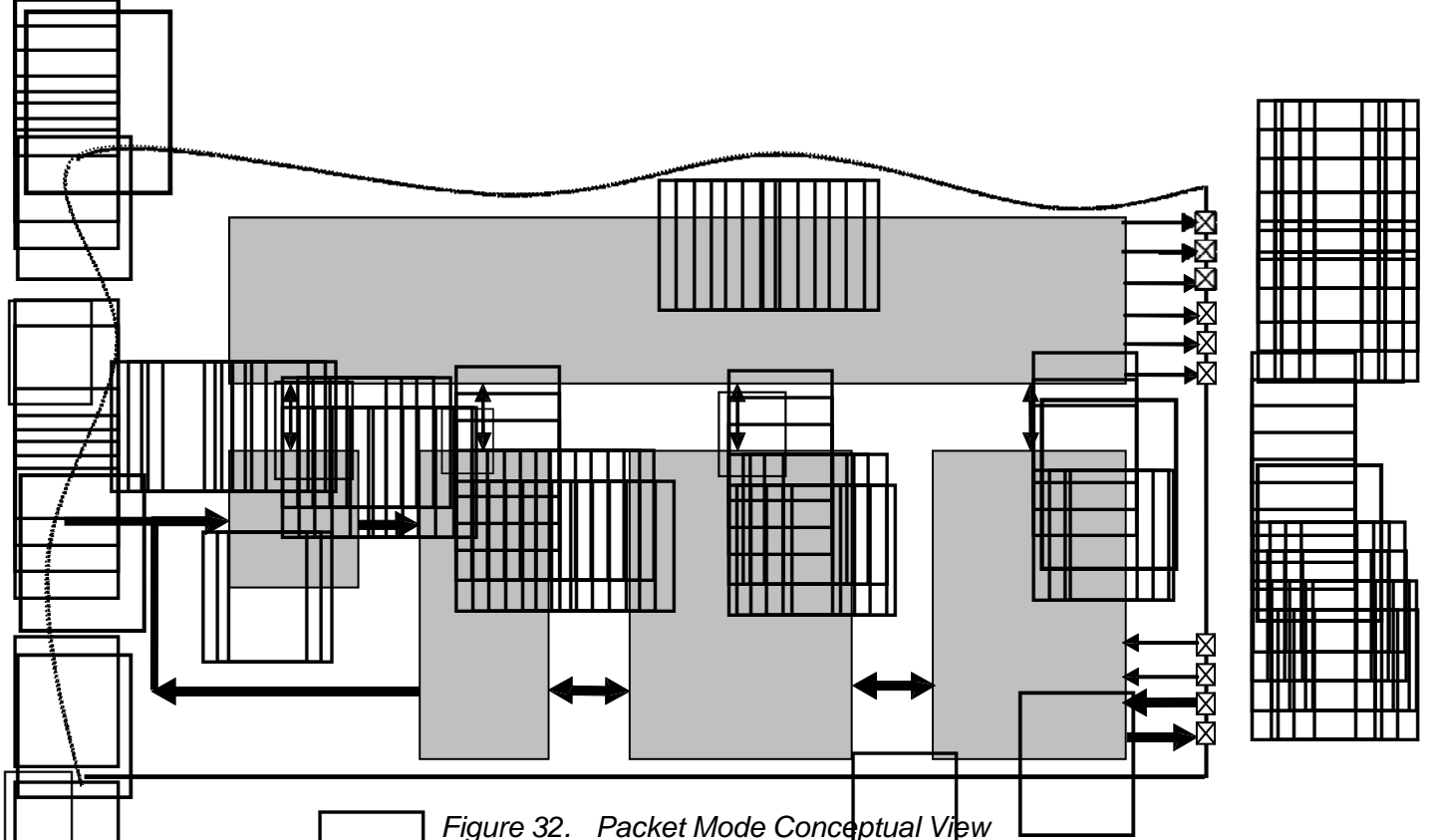
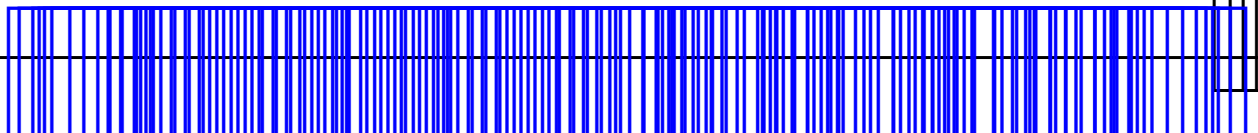
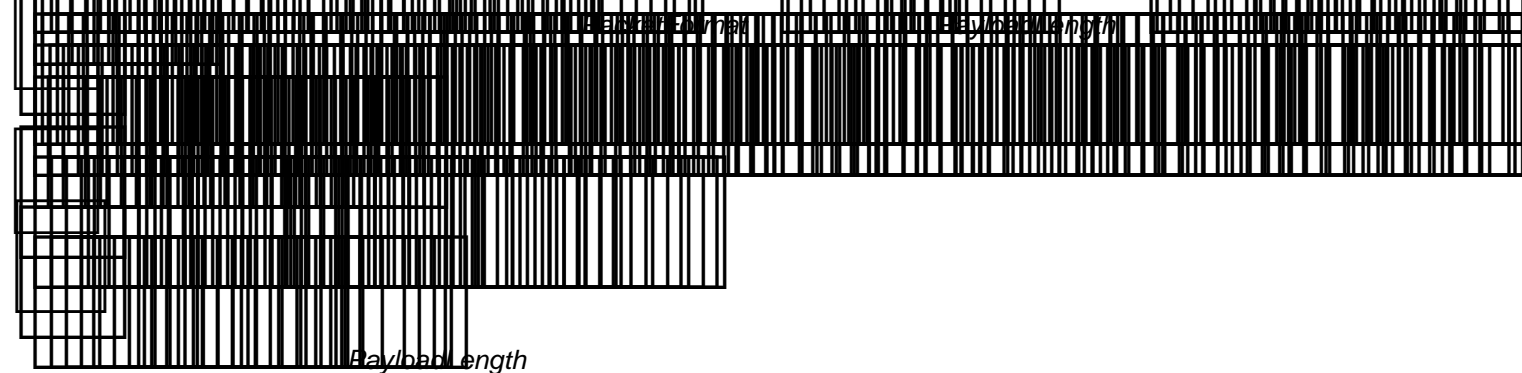


Figure 32. Packet Mode Conceptual View

Note The Bit Synchronizer is automatically enabled in Packet mode.

4.2.1.3.2 Packet Format

Fixed-length Packet Format



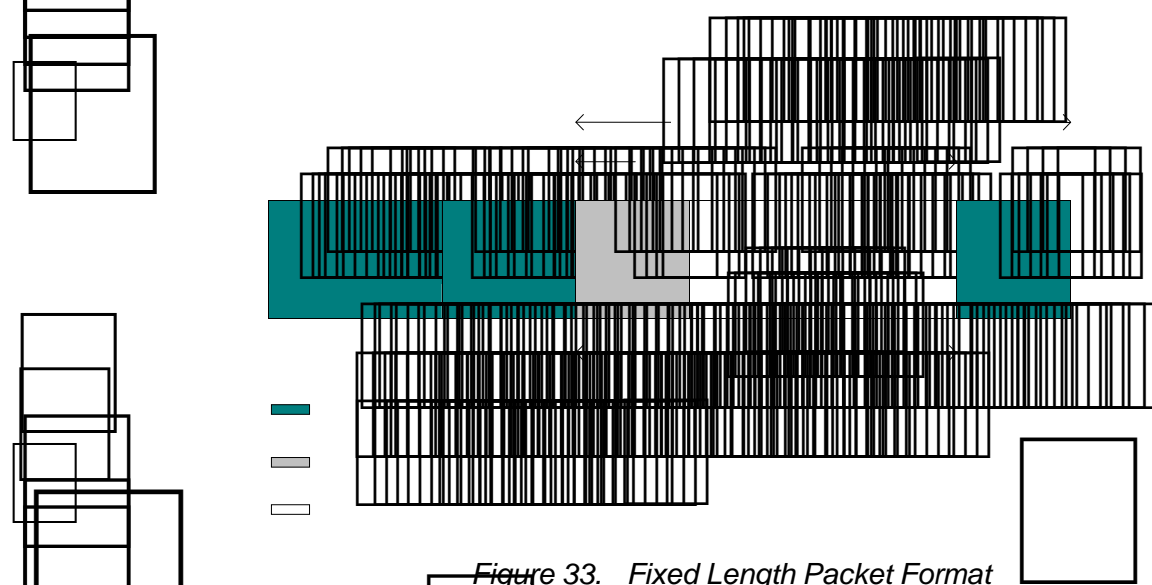
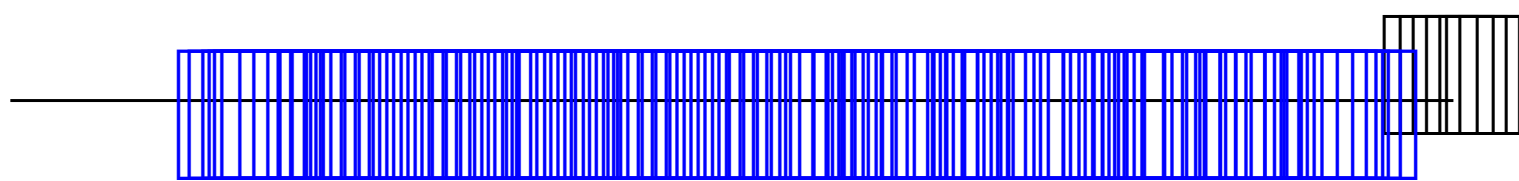
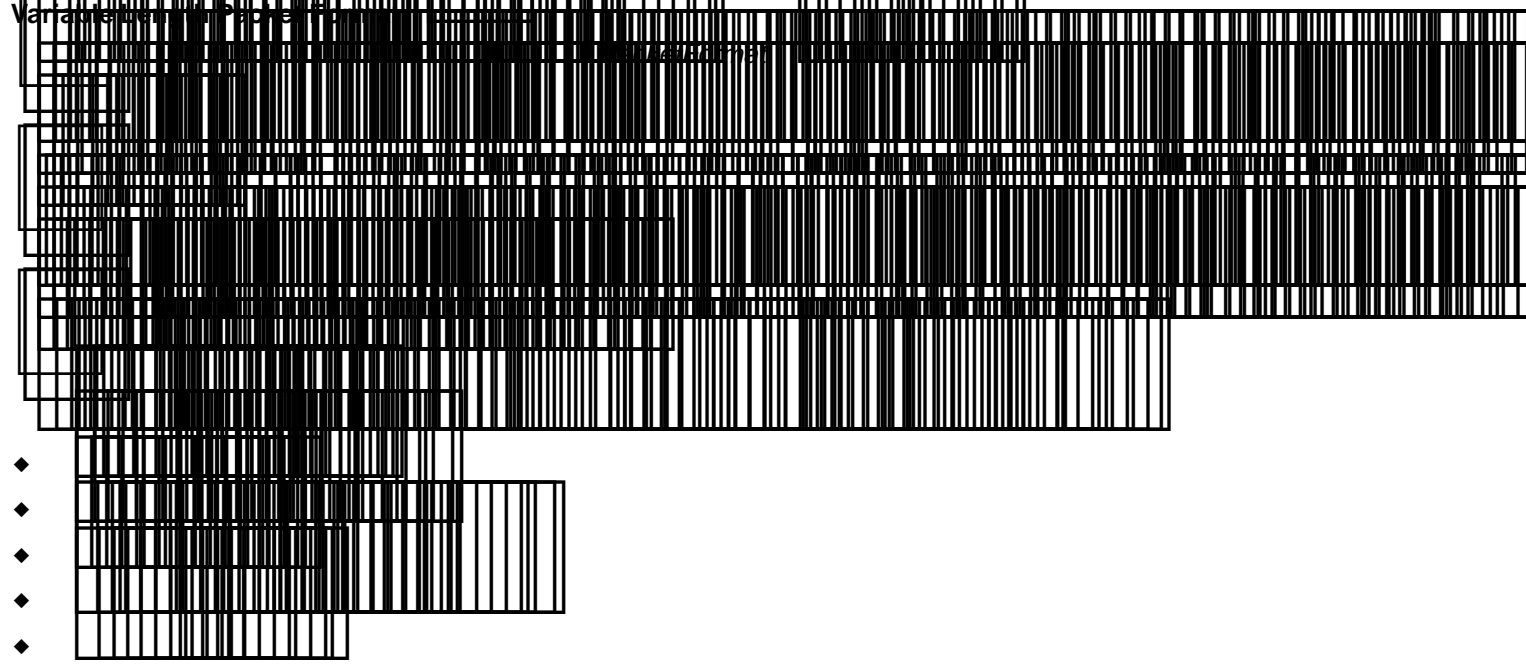


Figure 33. Fixed Length Packet Format

Variable Length Packet Format



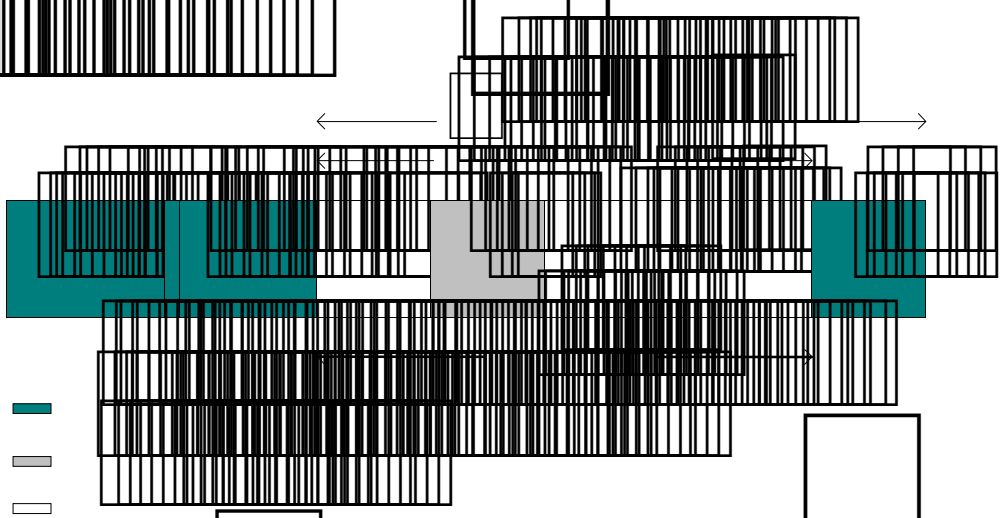


Figure 34. Variable Length Packet Format

Unlimited Length Packet Format

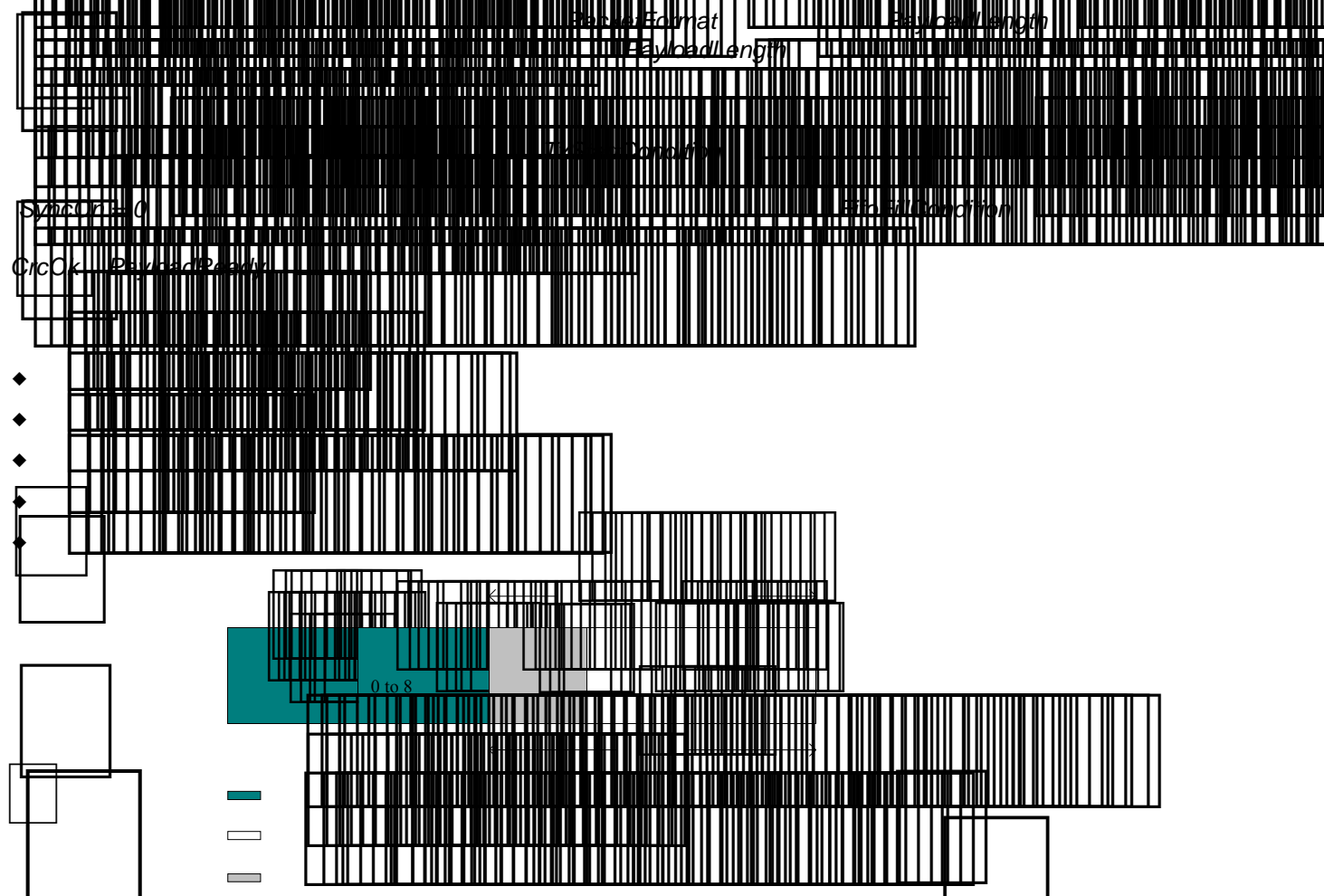


Figure 35. Unlimited Length Packet Format



4.2.133 *FSK Modulation*

- ◆
- ◆
- ◆
- ◆

4.2.134 *FSK Demodulation*

◆ *FSK Standard 10101*

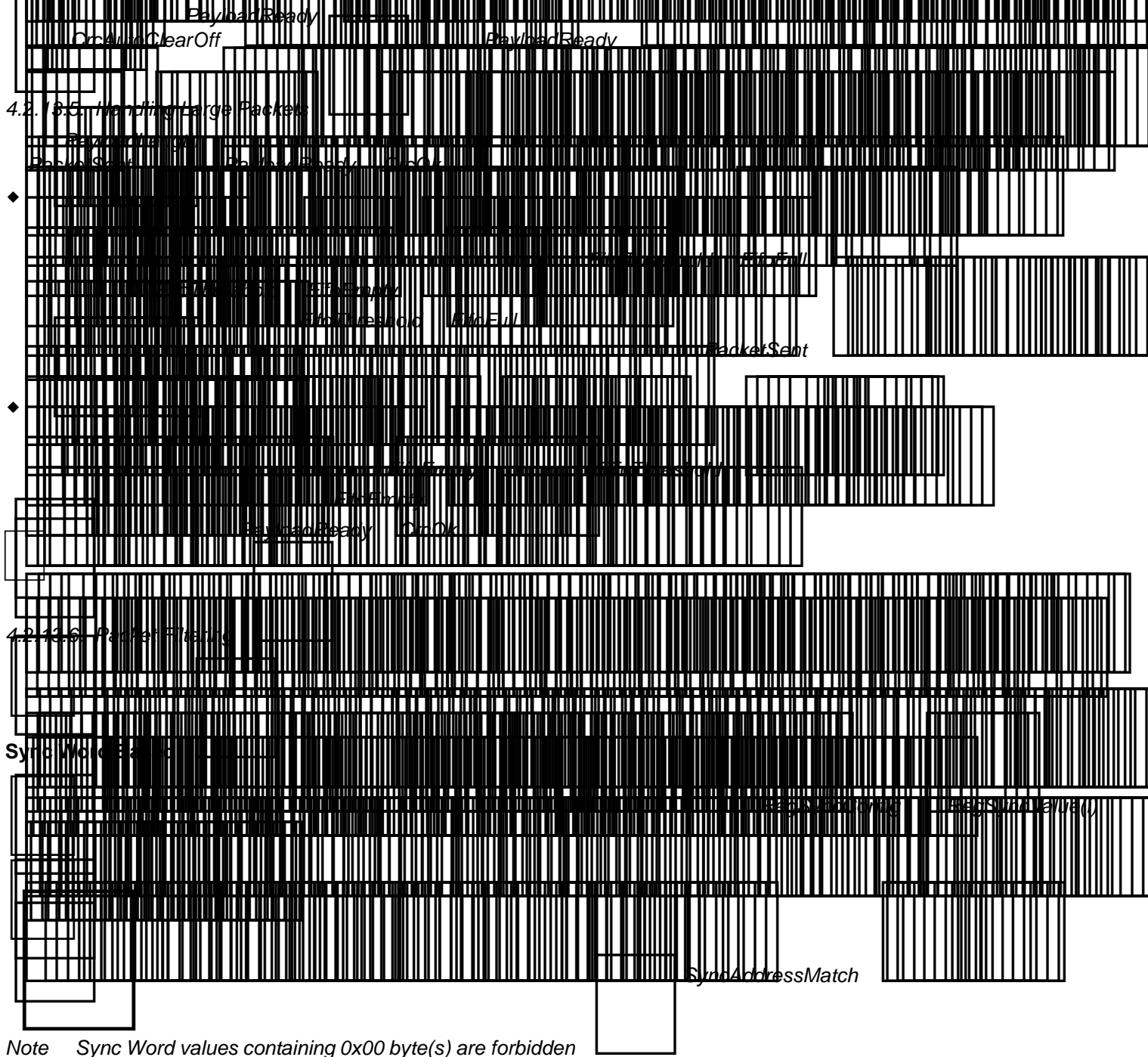
- ◆
- ◆

4.2.134 *FSK Processing*

- ◆
- ◆
- ◆
- ◆

◆ *FSK Modulation*

Not Address



Address Based

Address Filtering

◆ Address Filtering: The receiver will only accept packets whose address is in the address list.

◆ Address Filtering: The receiver will only accept packets whose address is in the address list.

◆ Address Filtering: The receiver will only accept packets whose address is in the address list.

◆ Address Filtering: The receiver will only accept packets whose address is in the address list.

Length Based

◆ Length Based: The receiver will only accept packets whose length is in the length list.

CRC Based

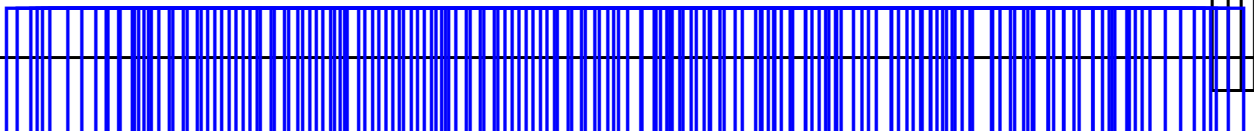
◆ CRC Based: The receiver will only accept packets whose CRC is in the CRC list.

◆ CRC Based: The receiver will only accept packets whose CRC is in the CRC list.

CrcWhiteningType

Table 76 CRC Description

Crc Type	CrcWhiteningType	PolyMod	Seed Value	Complemented
CCITT				
IBM				



4.2.1.3.1 Manchester Encoding Methods

Note Only one of the two methods can be enabled at a time.

Manchester Encoding Method 1

See Figure 4-11

Figure 4-11 Manchester Encoding Method 1

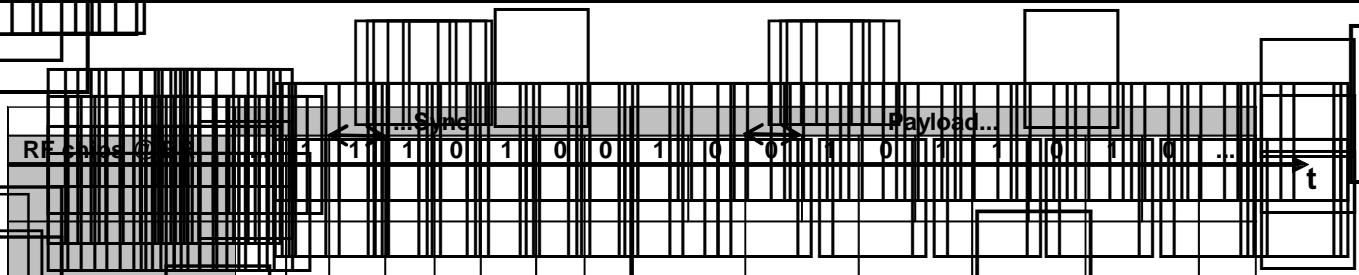
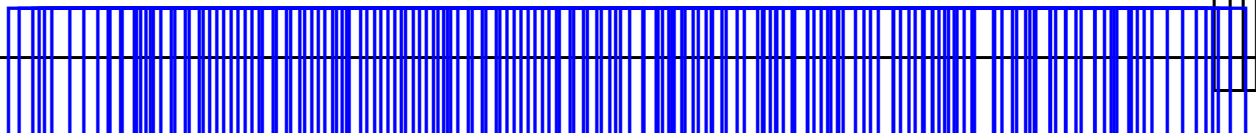


Figure 4-11 Manchester Encoding Method 1

Data Wrapping

See Figure 4-12



LFSR Polynomial = $X^9 + X^5 + 1$

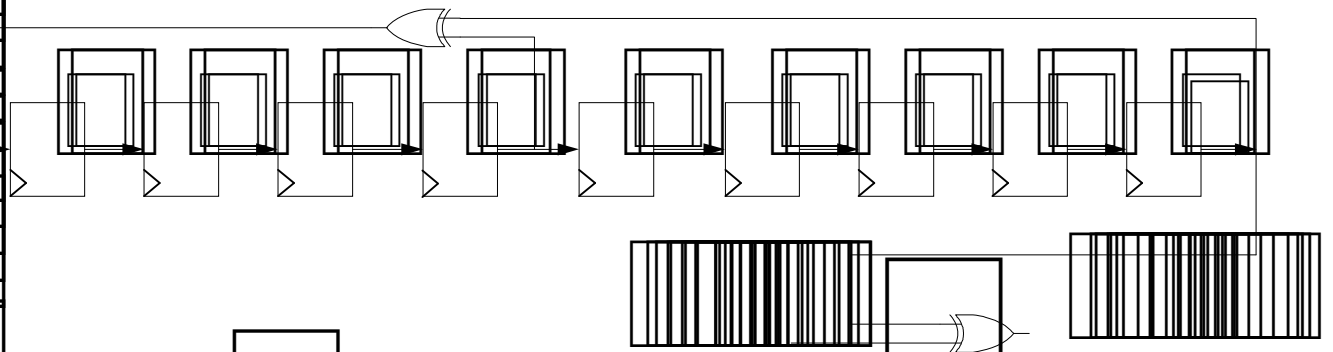
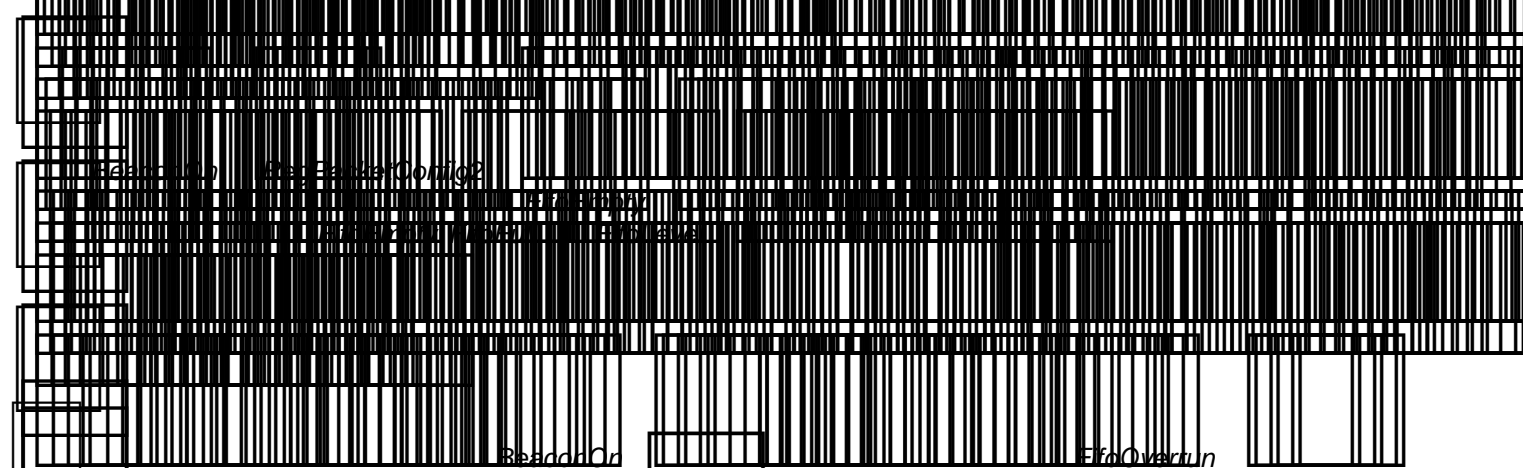
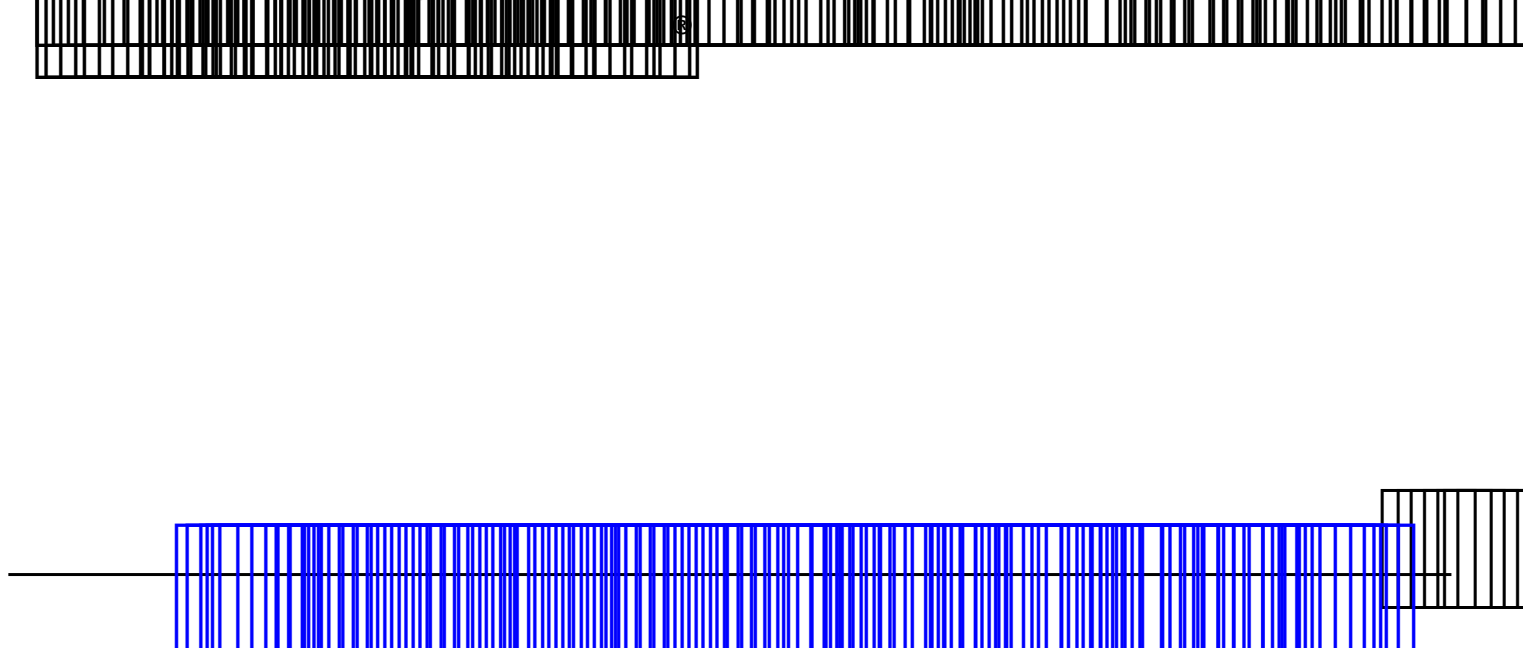


Figure 37 Data Writing Polynomial

4.2.13. Reader Config



4.2.14. Reader Config Concatenation Mode



4.3. SPIN-1/2

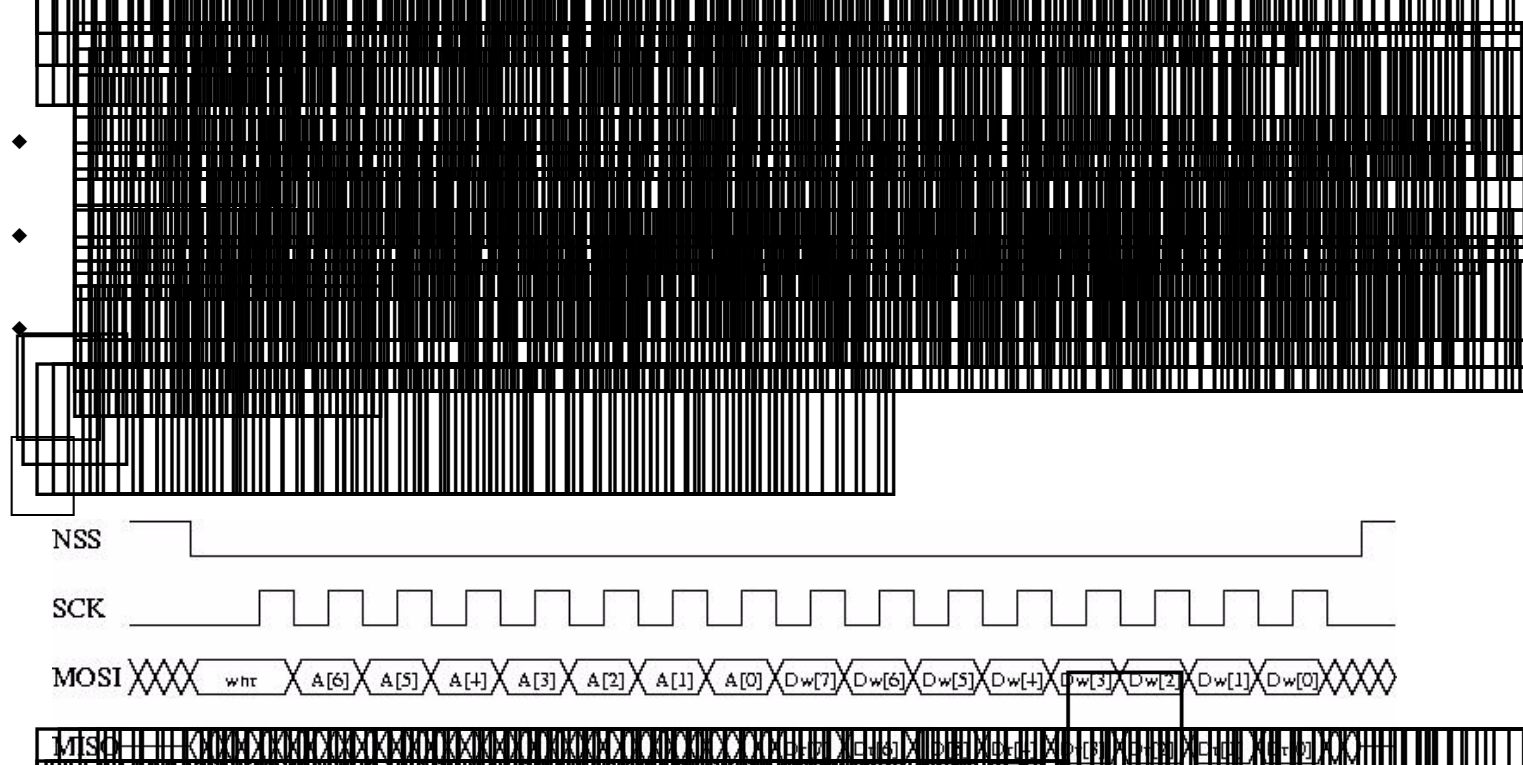


Figure 38: SP Timing Diagram (single access)

5. RFM95/96/97/98(W) Analog & RF Frontend Electronics

5.1. Power Supply Strategy

5.2. Low Battery Detection

RegDio Mapping

RegLowBat

5.3. Frequency Synthesis

5.3.1. Crystal Oscillator

5.3.2.6 PLL Frequency Step Size (FSTEP) (23,0) (RegFSTEP[11:0])

Note To minimize the current consumption of the RFM95/96/97/98(W), please ensure that the CLKOUT signal is disabled when not required.

5.3.3. PLL

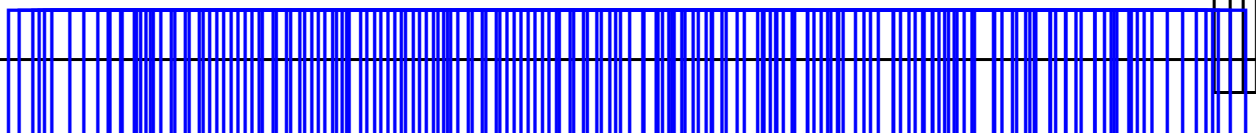
$$F_{STEP} = \frac{F_{RF}}{2^{23}}$$

RegFrf

$$F_{RF} = F_{STEP} \times Frf(23,0)$$

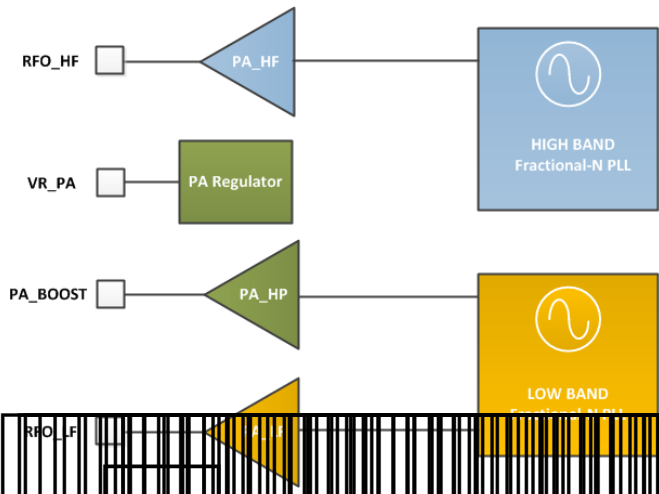
Note The Frf setting is split across 3 bytes. A change in the center frequency will only be taken into account when the least significant byte FrfLsb in RegFrfLsb is written. This allows the potential for user generation of m-ary FSK at very low bit rates. This is possible where frequency modulation is achieved by direct programming of the programmed RF centre frequency. To enable this functionality set the FastHopOn bit of register RegPllHop.

5.3.4. RFOscillator



5.4. Transceiver Description

5.4.1. Architecture Description



5.4.2. RF LOW BAND

Table 77 Power Amplifier Mode Selection Truth Table

PaSelect	Mode	Power Range	Power Formula
0	PA_HF	0 to +20 dBm	$P_{out} = P_{in} - 1$
1	PA_HP	0 to +20 dBm	$P_{out} = P_{in} - 1$
2	PA_BOOST	0 to +20 dBm	$P_{out} = P_{in} - 1$
3	PA_BOOST	0 to +20 dBm	$P_{out} = P_{in} - 1$

- Notes
- For +20 dBm restrictions on operation please consult the following section.
 - To ensure correct operation at the highest power levels ensure that the current limiter OcpTrim is adjusted to permit delivery of the requisite supply current.
 - If the PA_BOOST pin is not used it may be left floating.

5.4.3 High Power +20dBm Operation

Table 78 High Power Settings

Register	Address	Value for High Power	Default value PA_HF/LF or +17dBm	Description
RegPaDac				

Notes - High Power settings must be turned off when using PA_LF or PA_HF

PA_HF and PA_LF Power limits should be adapted to the actual power level in RegCcd

Table 79 Operating Range, +20dBm Operation

Symbol	Description	Min	Max	Unit

Table 80 Operating Range, +20dBm Operation

Symbol	Description	Min	Max	Unit

5.4.4. Overview of the OCP

OcpTrim

RegOcp

Table 81 Trimming of the OCP Current

OcpTrim	I _{max}	I _{max} Formula
		OcpTrim
		OcpTrim
		240 mA

Note: I_{max} sets a limit on the current drain of the Power Amplifier only, hence the maximum current drain of the is equal to I_{max} + I_{FS}

5.5. Receiver Description

5.5.1. Overview

5.5.2. Receiver block diagram of the RFM95/96/97/98

5.5.3. Automatic Gain Control in FS/OOK Mode



Table 82 LNA Gain Control and Performances

RX input level (Pin)	Gain Setting	LnaGain	Relative LNA Gain [dB]	NF Lower/Higher band [dB]	IIP3 Lower/Higher band [dBm]
Pin <= AgcThresh1					
AgcThresh1 < Pin <= AgcThresh2					
AgcThresh2 < Pin <= AgcThresh3					
AgcThresh3 < Pin <= AgcThresh4					
AgcThresh4 < Pin <= AgcThresh5					
AgcThresh5 < Pin					

5.54. RSSI (RSSI0~RSSI4)

RSSI Value

$RssiValue = 2 \times RssiValue + Round(10 \times RssiValue)$

RssiOffset

$$RSSI[dBm] = \frac{RssiValue}{2}$$

RssiSmoothing

RssiSmoothing

Table 83 *RssiSmoothingOptions*

<i>RssiSmoothing</i>	Number of Samples	Estimated Accuracy	Response Time
			$\frac{2^{(RssiSmoothing+1)}}{4 \cdot RxBw[kHz]} [ms]$

5.5.5. RS\$ in LoRa™ Mode

~~PGSI ID 1 107 PGSI~~

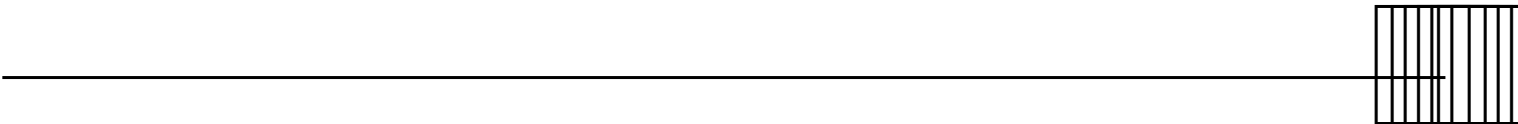
5.3.6.0

Note: To respect sampling criterion in the decimation chain of the receiver, the communication bit rate cannot be set at a higher than twice the single side receiver bandwidth (Bit Rate < 2x R_{RF} Bw).

$$R_{\text{cBw}} = \frac{FXCSG}{R_{\text{cB}} \times \text{Mann} \times 10^4 \times \text{Exp} + 2}$$

Table 84 Available RxBw Settings

[illegible]

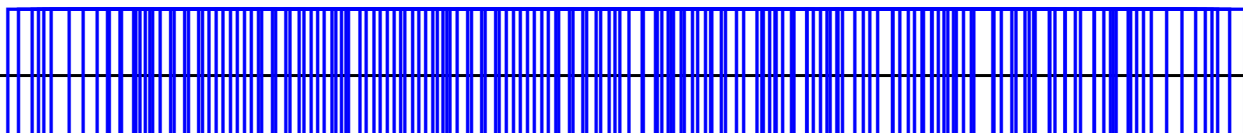


6. Description of the Registers

6.1. Register Table Summary

Table 85 Registers Summary

Address	Register Name		Reset (POR)	Default (FSK)	Description	
	FSK/OOK Mode	LoRa™ Mode			FSK Mode	LoRa™ Mode
0x00	0x00	0x00	0x00	0x00	0x00	0x00
0x01	0x01	0x01	0x01	0x01	0x01	0x01
0x02	0x02	0x02	0x02	0x02	0x02	0x02
0x03	0x03	0x03	0x03	0x03	0x03	0x03
0x04	0x04	0x04	0x04	0x04	0x04	0x04
0x05	0x05	0x05	0x05	0x05	0x05	0x05
0x06	0x06	0x06	0x06	0x06	0x06	0x06
0x07	0x07	0x07	0x07	0x07	0x07	0x07
0x08	0x08	0x08	0x08	0x08	0x08	0x08
0x09	0x09	0x09	0x09	0x09	0x09	0x09
0x0A	0x0A	0x0A	0x0A	0x0A	0x0A	0x0A
0x0B	0x0B	0x0B	0x0B	0x0B	0x0B	0x0B
0x0C	0x0C	0x0C	0x0C	0x0C	0x0C	0x0C
0x0D	0x0D	0x0D	0x0D	0x0D	0x0D	0x0D
0x0E	0x0E	0x0E	0x0E	0x0E	0x0E	0x0E
0x0F	0x0F	0x0F	0x0F	0x0F	0x0F	0x0F
0x10	0x10	0x10	0x10	0x10	0x10	0x10
0x11	0x11	0x11	0x11	0x11	0x11	0x11
0x12	0x12	0x12	0x12	0x12	0x12	0x12
0x13	0x13	0x13	0x13	0x13	0x13	0x13
0x14	0x14	0x14	0x14	0x14	0x14	0x14
0x15	0x15	0x15	0x15	0x15	0x15	0x15
0x16	0x16	0x16	0x16	0x16	0x16	0x16
0x17	0x17	0x17	0x17	0x17	0x17	0x17
0x18	0x18	0x18	0x18	0x18	0x18	0x18
0x19	0x19	0x19	0x19	0x19	0x19	0x19
0x1A	0x1A	0x1A	0x1A	0x1A	0x1A	0x1A
0x1B	0x1B	0x1B	0x1B	0x1B	0x1B	0x1B
0x1C	0x1C	0x1C	0x1C	0x1C	0x1C	0x1C
0x1D	0x1D	0x1D	0x1D	0x1D	0x1D	0x1D
0x1E	0x1E	0x1E	0x1E	0x1E	0x1E	0x1E
0x1F	0x1F	0x1F	0x1F	0x1F	0x1F	0x1F
0x20	0x20	0x20	0x20	0x20	0x20	0x20
0x21	0x21	0x21	0x21	0x21	0x21	0x21
0x22	0x22	0x22	0x22	0x22	0x22	0x22
0x23	0x23	0x23	0x23	0x23	0x23	0x23
0x24	0x24	0x24	0x24	0x24	0x24	0x24
0x25	0x25	0x25	0x25	0x25	0x25	0x25
0x26	0x26	0x26	0x26	0x26	0x26	0x26
0x27	0x27	0x27	0x27	0x27	0x27	0x27
0x28	0x28	0x28	0x28	0x28	0x28	0x28
0x29	0x29	0x29	0x29	0x29	0x29	0x29
0x2A	0x2A	0x2A	0x2A	0x2A	0x2A	0x2A
0x2B	0x2B	0x2B	0x2B	0x2B	0x2B	0x2B
0x2C	0x2C	0x2C	0x2C	0x2C	0x2C	0x2C
0x2D	0x2D	0x2D	0x2D	0x2D	0x2D	0x2D
0x2E	0x2E	0x2E	0x2E	0x2E	0x2E	0x2E
0x2F	0x2F	0x2F	0x2F	0x2F	0x2F	0x2F
0x30	0x30	0x30	0x30	0x30	0x30	0x30
0x31	0x31	0x31	0x31	0x31	0x31	0x31
0x32	0x32	0x32	0x32	0x32	0x32	0x32
0x33	0x33	0x33	0x33	0x33	0x33	0x33
0x34	0x34	0x34	0x34	0x34	0x34	0x34
0x35	0x35	0x35	0x35	0x35	0x35	0x35
0x36	0x36	0x36	0x36	0x36	0x36	0x36
0x37	0x37	0x37	0x37	0x37	0x37	0x37
0x38	0x38	0x38	0x38	0x38	0x38	0x38
0x39	0x39	0x39	0x39	0x39	0x39	0x39
0x3A	0x3A	0x3A	0x3A	0x3A	0x3A	0x3A
0x3B	0x3B	0x3B	0x3B	0x3B	0x3B	0x3B
0x3C	0x3C	0x3C	0x3C	0x3C	0x3C	0x3C
0x3D	0x3D	0x3D	0x3D	0x3D	0x3D	0x3D
0x3E	0x3E	0x3E	0x3E	0x3E	0x3E	0x3E
0x3F	0x3F	0x3F	0x3F	0x3F	0x3F	0x3F
0x40	0x40	0x40	0x40	0x40	0x40	0x40
0x41	0x41	0x41	0x41	0x41	0x41	0x41
0x42	0x42	0x42	0x42	0x42	0x42	0x42
0x43	0x43	0x43	0x43	0x43	0x43	0x43
0x44	0x44	0x44	0x44	0x44	0x44	0x44
0x45	0x45	0x45	0x45	0x45	0x45	0x45
0x46	0x46	0x46	0x46	0x46	0x46	0x46
0x47	0x47	0x47	0x47	0x47	0x47	0x47
0x48	0x48	0x48	0x48	0x48	0x48	0x48
0x49	0x49	0x49	0x49	0x49	0x49	0x49
0x4A	0x4A	0x4A	0x4A	0x4A	0x4A	0x4A
0x4B	0x4B	0x4B	0x4B	0x4B	0x4B	0x4B
0x4C	0x4C	0x4C	0x4C	0x4C	0x4C	0x4C
0x4D	0x4D	0x4D	0x4D	0x4D	0x4D	0x4D
0x4E	0x4E	0x4E	0x4E	0x4E	0x4E	0x4E
0x4F	0x4F	0x4F	0x4F	0x4F	0x4F	0x4F
0x50	0x50	0x50	0x50	0x50	0x50	0x50
0x51	0x51	0x51	0x51	0x51	0x51	0x51
0x52	0x52	0x52	0x52	0x52	0x52	0x52
0x53	0x53	0x53	0x53	0x53	0x53	0x53
0x54	0x54	0x54	0x54	0x54	0x54	0x54
0x55	0x55	0x55	0x55	0x55	0x55	0x55
0x56	0x56	0x56	0x56	0x56	0x56	0x56
0x57	0x57	0x57	0x57	0x57	0x57	0x57
0x58	0x58	0x58	0x58	0x58	0x58	0x58
0x59	0x59	0x59	0x59	0x59	0x59	0x59
0x5A	0x5A	0x5A	0x5A	0x5A	0x5A	0x5A
0x5B	0x5B	0x5B	0x5B	0x5B	0x5B	0x5B
0x5C	0x5C	0x5C	0x5C	0x5C	0x5C	0x5C
0x5D	0x5D	0x5D	0x5D	0x5D	0x5D	0x5D
0x5E	0x5E	0x5E	0x5E	0x5E	0x5E	0x5E
0x5F	0x5F	0x5F	0x5F	0x5F	0x5F	0x5F
0x60	0x60	0x60	0x60	0x60	0x60	0x60
0x61	0x61	0x61	0x61	0x61	0x61	0x61
0x62	0x62	0x62	0x62	0x62	0x62	0x62
0x63	0x63	0x63	0x63	0x63	0x63	0x63
0x64	0x64	0x64	0x64	0x64	0x64	0x64
0x65	0x65	0x65	0x65	0x65	0x65	0x65
0x66	0x66	0x66	0x66	0x66	0x66	0x66
0x67	0x67	0x67	0x67	0x67	0x67	0x67
0x68	0x68	0x68	0x68	0x68	0x68	0x68
0x69	0x69	0x69	0x69	0x69	0x69	0x69
0x6A	0x6A	0x6A	0x6A	0x6A	0x6A	0x6A
0x6B	0x6B	0x6B	0x6B	0x6B	0x6B	0x6B
0x6C	0x6C	0x6C	0x6C	0x6C	0x6C	0x6C
0x6D	0x6D	0x6D	0x6D	0x6D	0x6D	0x6D
0x6E	0x6E	0x6E	0x6E	0x6E	0x6E	0x6E
0x6F	0x6F	0x6F	0x6F	0x6F	0x6F	0x6F
0x70	0x70	0x70	0x70	0x70	0x70	0x70
0x71	0x71	0x71	0x71	0x71	0x71	0x71
0x72	0x72	0x72	0x72	0x72	0x72	0x72
0x73	0x73	0x73	0x73	0x73	0x73	0x73
0x74	0x74	0x74	0x74	0x74	0x74	0x74
0x75	0x75	0x75	0x75	0x75	0x75	0x75
0x76	0x76	0x76	0x76	0x76	0x76	0x76
0x77	0x77	0x77	0x77	0x77	0x77	0x77
0x78	0x78	0x78	0x78	0x78	0x78	0x78
0x79	0x79	0x79	0x79	0x79	0x79	0x79
0x7A	0x7A	0x7A	0x7A	0x7A	0x7A	0x7A
0x7B	0x7B	0x7B	0x7B	0x7B	0x7B	0x7B
0x7C	0x7C	0x7C	0x7C	0x7C	0x7C	0x7C
0x7D	0x7D	0x7D	0x7D	0x7D	0x7D	0x7D
0x7E	0x7E	0x7E	0x7E	0x7E	0x7E	0x7E
0x7F	0x7F	0x7F	0x7F	0x7F	0x7F	0x7F
0x80	0x80	0x80	0x80	0x80	0x80	0x80
0x81	0x81	0x81	0x81	0x81	0x81	0x81
0x82	0x82	0x82	0x82	0x82	0x82	0x82
0x83	0x83	0x83	0x83	0x83	0x83	0x83
0x84	0x84	0x84	0x84	0x84	0x84	0x84
0x85	0x85	0x85	0x85	0x85	0x85	0x85
0x86	0x86	0x86	0x86	0x86	0x86	0x86
0x87	0x87	0x87	0x87	0x87	0x87	0x87
0x88	0x88	0x88	0x88	0x88	0x88	0x88
0x89	0x89	0x89	0x89	0x89	0x89	0x89
0x8A	0x8A	0x8A	0x8A	0x8A	0x8A	0x8A
0x8B	0x8B	0x8B	0x8B	0x8B	0x8B	0x8B
0x8C	0x8C	0x8C	0x8C	0x8C	0x8C	0x8C
0x8D	0x8D	0x8D	0x8D	0x8D	0x8D	0x8D
0x8E	0x8E	0x8E	0x8E	0x8E	0x8E	0x8E
0x8F	0x8F	0x8F	0x8F	0x8F	0x8F	0x8F
0x90	0x90	0x90	0x90	0x90	0x90	0x90
0x91	0x91	0x91	0x91	0x91	0x91	0x91
0x92	0x92	0x92	0x92	0x92	0x92	0x92
0x93	0x93	0x93	0x93	0x93	0x93	0x93
0x94	0x94	0x94	0x94	0x94	0x94	0x94
0x95	0x95	0x95	0x95	0x95	0x95	0x95
0x96	0x96	0x96	0x96	0x96	0x96	0x96
0x97	0x97	0x97	0x97	0x97	0x97	0x97
0x98	0x98	0x98	0x98	0x98	0x98	0x98
0x99	0x99	0x99	0x99	0x99	0x99	0x99
0x9A	0x9A	0x9A	0x9A	0x9A	0x9A	0x9A
0x9B	0x9B	0x9B	0x9B	0x9B	0x9B	0x9B
0x9C	0x9C	0x9C	0x9C	0x9C	0x9C	0x9C
0x9D	0x9D	0x9D	0x9D	0x9D	0x9D	0x9D
0x9E	0x9E	0x9E	0x9E	0x9E	0x9E	0x9E
0x9F	0x9F	0x9F	0x9F	0x9F	0x9F	0x9F
0xA0	0xA0	0xA0	0xA0	0xA0	0xA0	0xA0
0xA1	0xA1	0xA1	0xA1	0xA1	0xA1	0xA1
0xA2	0xA2	0xA2	0xA2	0xA2	0xA2	0xA2
0xA3	0xA3	0xA3	0xA3	0xA3	0xA3	0xA3
0xA4	0xA4	0xA4	0xA4	0xA4	0xA4	0xA4
0xA5	0xA5	0xA5	0xA5	0xA5	0xA5	0xA5
0xA6	0xA6	0xA6	0xA6	0xA6	0xA6	0xA6
0xA7	0xA7	0xA7	0xA7	0xA7	0xA7	0xA7
0xA8	0xA8	0xA8	0xA8	0xA8	0xA8	0xA8
0xA9	0xA9	0xA9	0xA9	0xA9	0xA9	0xA9
0xAA	0xAA	0xAA	0xAA	0xAA	0xAA	0xAA
0xAB	0xAB	0xAB	0xAB	0xAB	0xAB	0xAB
0xAC	0xAC	0xAC	0xAC	0xAC	0xAC	0xAC
0xAD	0xAD	0xAD	0xAD	0xAD	0xAD	0xAD
0xAE	0xAE	0xAE	0xAE	0xAE	0xAE	0xAE
0xAF	0xAF	0xAF	0xAF	0xAF	0xAF	0xAF
0xB0	0xB0	0xB0	0xB0	0xB0	0xB0	0xB0
0xB1	0xB1	0xB1	0xB1	0xB1	0xB1	0xB1
0xB2	0xB2	0xB2	0xB2	0xB2	0xB2	0xB2
0xB3	0xB3	0xB3	0xB3	0xB3	0xB3	0xB3
0xB4	0xB4	0xB4	0xB4	0xB4	0xB4	0xB4
0xB5	0xB5	0xB5	0xB5	0xB5	0xB5	0xB5
0xB6	0xB6	0xB6	0xB6	0xB6	0xB6	0xB6
0xB7	0xB7	0xB7	0xB7	0xB7	0xB7	0xB7
0xB8	0xB8	0xB8	0xB8	0xB8	0xB8	0xB8
0xB9	0xB9	0xB9	0xB9	0xB9	0xB9	0xB9
0xBA	0xBA	0xBA	0xBA	0xBA	0xBA	0xBA</



[illegible]

Note - Reset values are automatically refreshed in the chip at Power On Reset

- Default values are the Hope RF recommended register values, optimizing the device operation

- Registers for which the Default value differs from the Reset value are denoted by a * in the tables of section 6.2

6.2. FSK/PSK Mode Register Map

Table 86 Register Map

[illegible]

[illegible]

[illegible]

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp+2}}$$

Age Group	Percentage
18-24	15%
25-34	20%
35-44	25%
45-54	20%
55-64	15%
65-74	10%
75-84	5%
85+	5%

[illegible]

[illegible]

[illegible]

[illegible]

[illegible]

Name (Address)	Bits	Variable Name	Mode	Default value	FSK/DCK Description
					Mode
2					
					FIR filter coefficients
					Initial value of FIR filter coefficients



[illegible]

6.3. **RESEARCH DESIGN**

Table 87 Low Frequency Additional Registers

[illegible]

[illegible]

6.4 LoRa Mode Register Map

[illegible]



[illegible]

$$SNR[dB] = \frac{Packet\ Snr[two\ complement]}{4}$$

[illegible]

[illegible]

7. Application Information

~~7.1 Crystal Resonator Specification~~

Table 89 Crystal Specification

[illegible]

- Notes** – the initial frequency tolerance, temperature stability and ageing performance should be chosen in accordance with the target operating temperature range and the receiver bandwidth selected.
- the loading capacitance should be applied externally, and adapted to the actual Cloud specification of the XTAL.

7.2. Reset of the Chip

7.2.1.1 FON

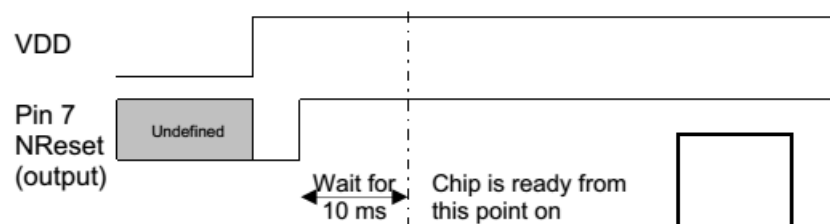


Figure 42. POR Timing Diagram

7.2.2. Manual Reset

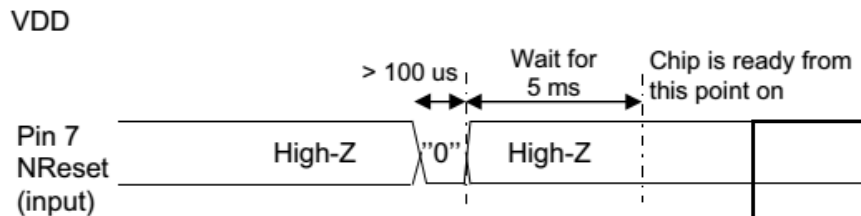
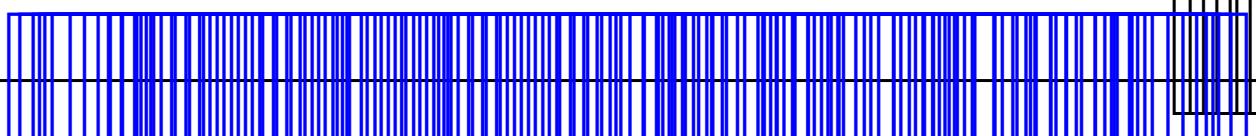
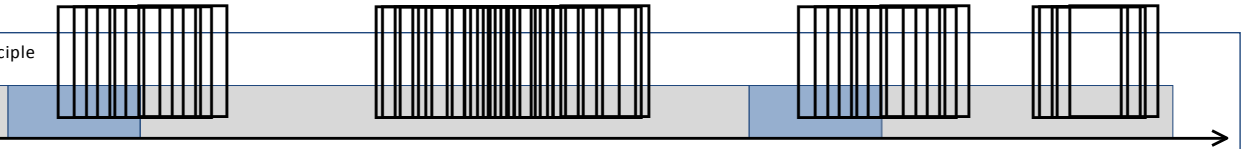


Figure 43. Manual Reset Timing Diagram

Note whilst pin 7 is driven low, an over current consumption of up to one milliampere can be seen on VDD.

7.3. Top Level Block Diagrams : Example

Listen mode : principle



7.3.1.1 Listen Mode

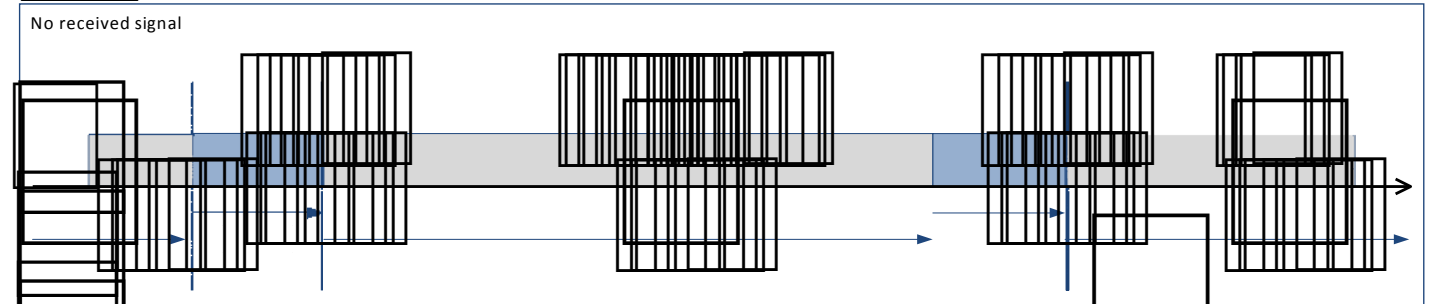


Figure 45. Listen Mode with no Preamble Received

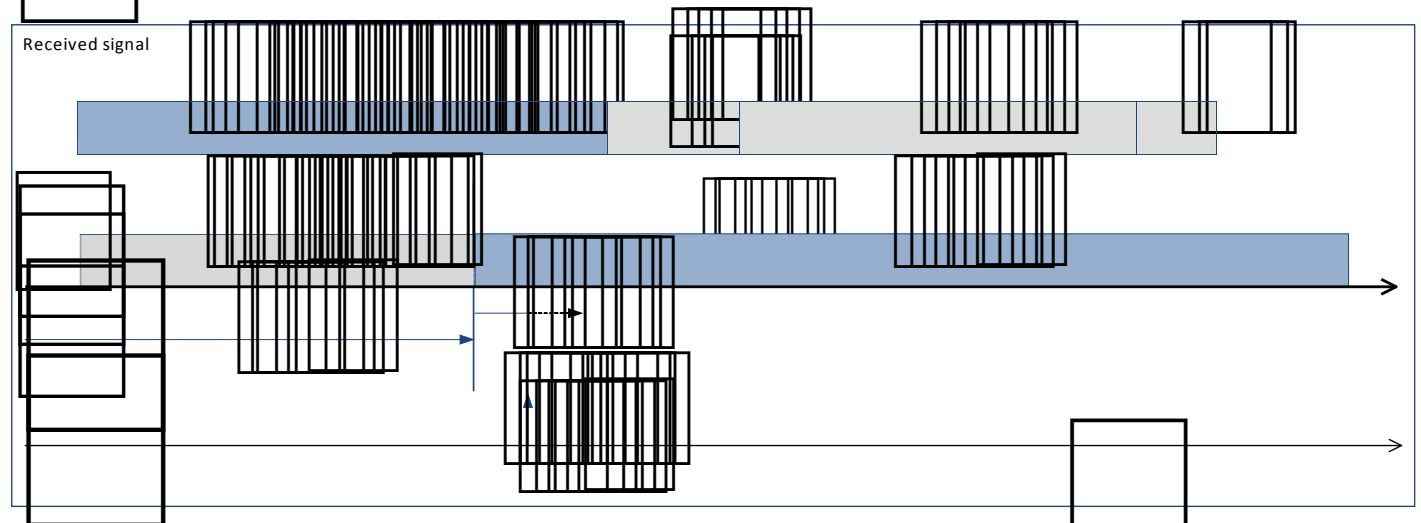
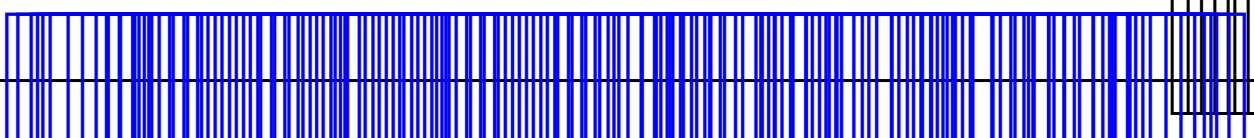
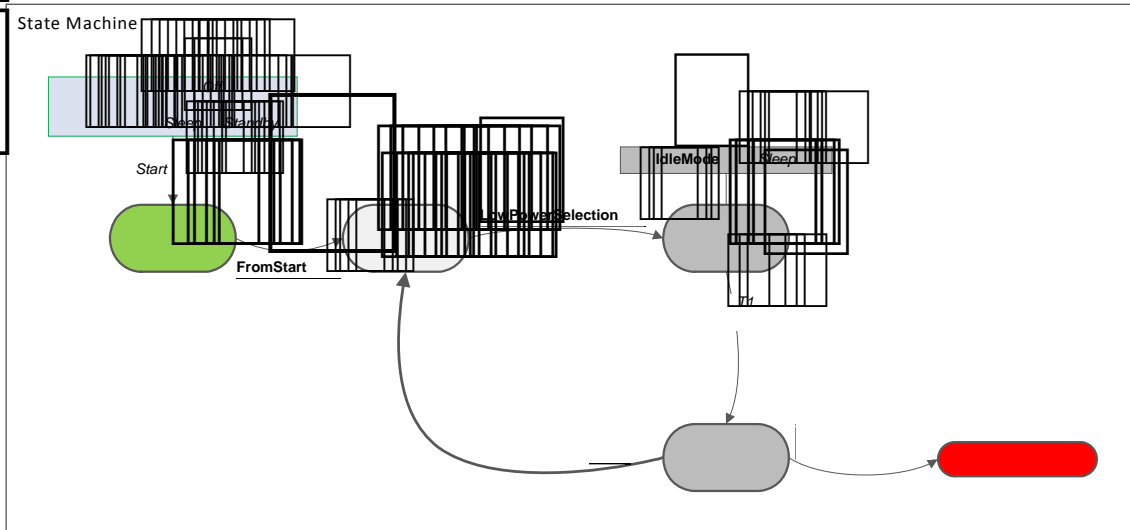


Figure 46. Listen Mode with Preamble Received



7.3.1.2 Sequence Configuration

Preamble Detect



7.3.2.2 Wake up SyncAddress received and no SyncAddress

7.3.2.3 Timing Diagram

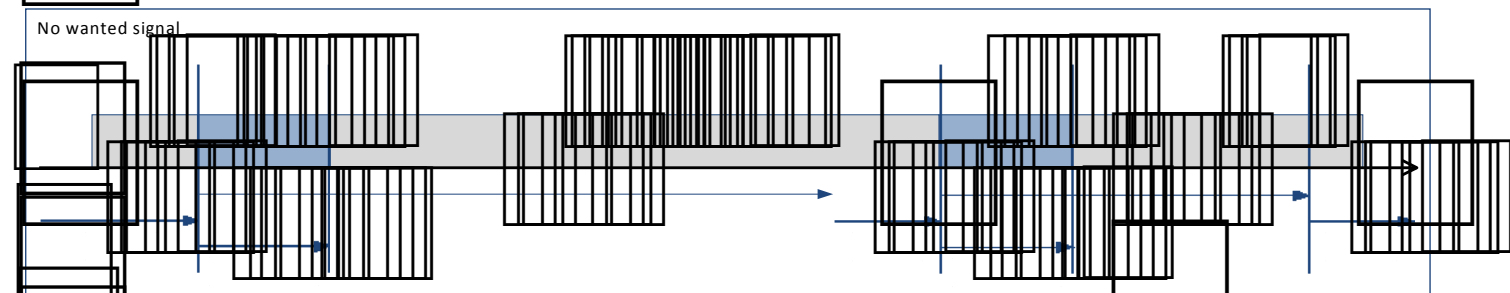


Figure 46: Listen Mode with SyncAddress Detected

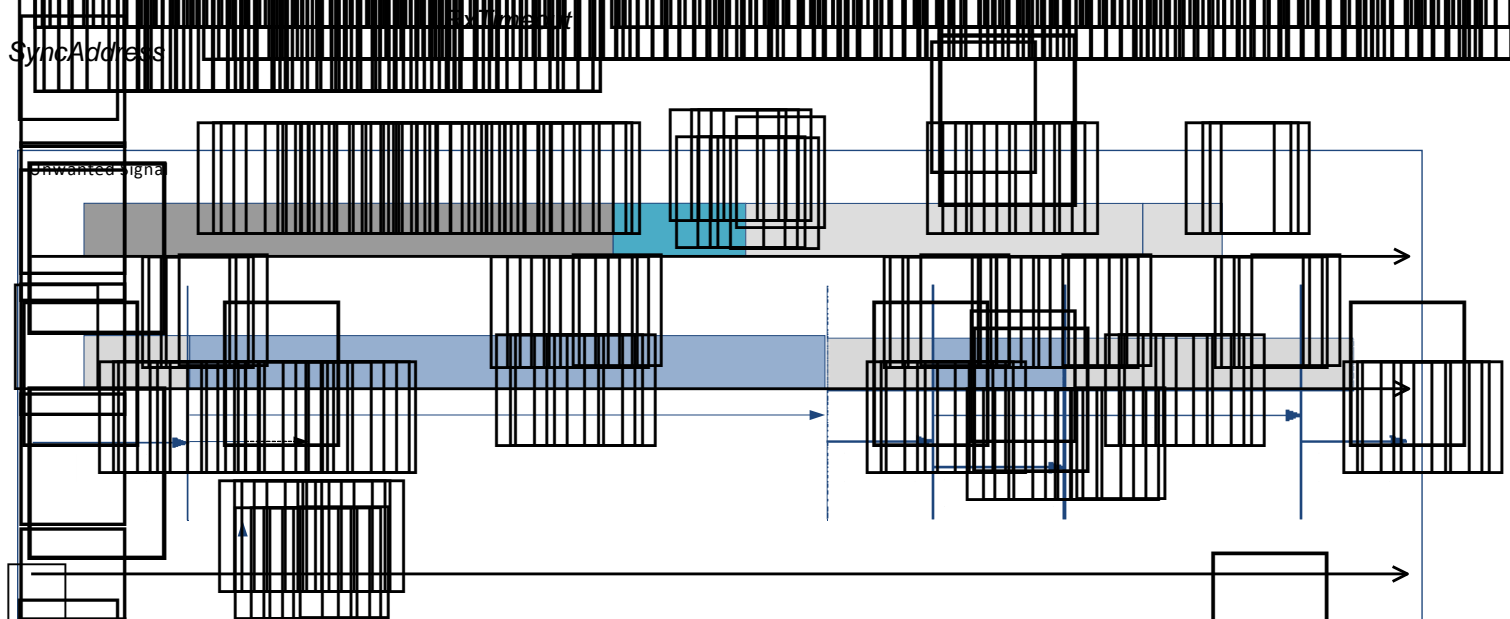
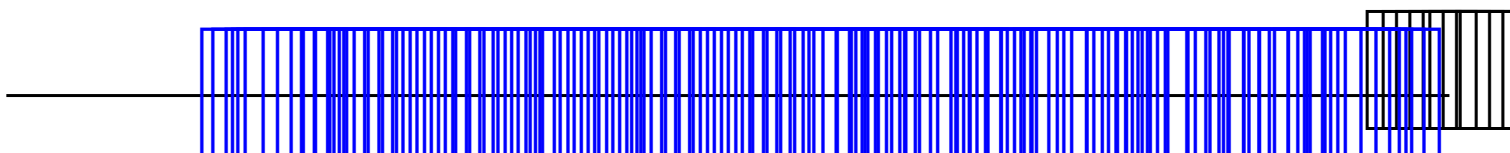


Figure 49: Listen Mode with Preamble Received and no SyncAddress



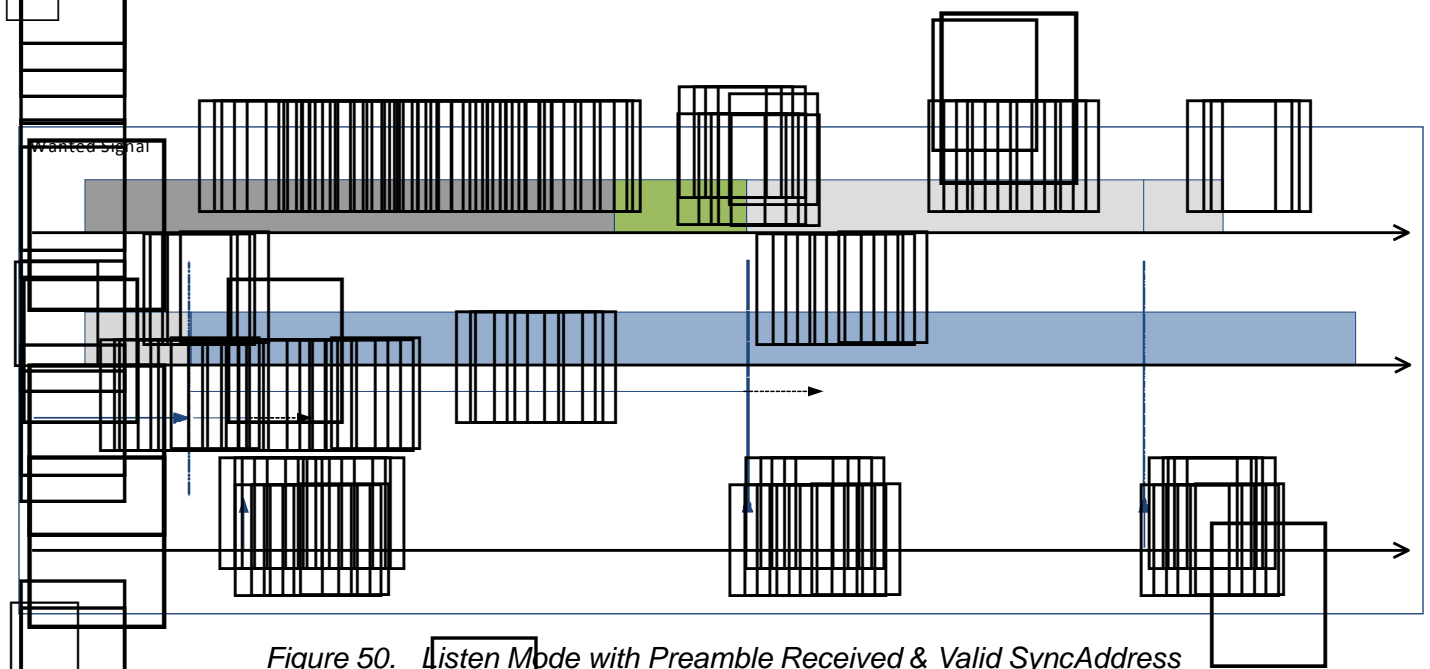


Figure 50. Listen Mode with Preamble Received & Valid SyncAddress

7.3.2.2. Sequence Configuration



Figure 51. Wake On SyncAddress State Machine

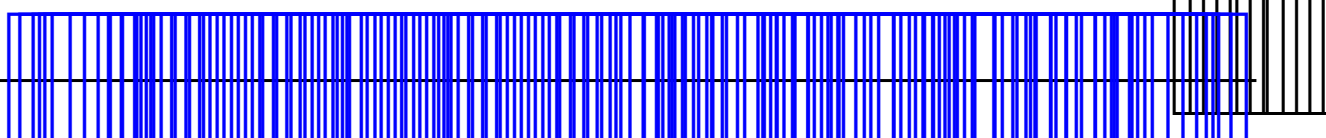
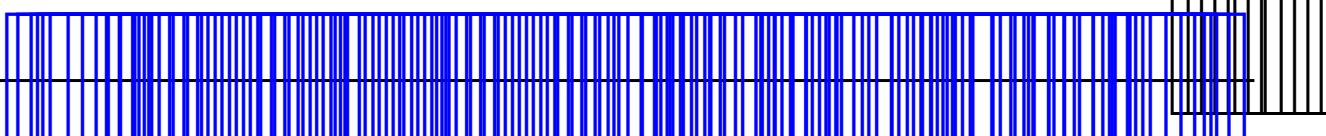


Table 92 Listen Mode with SyncAddress Condition Settings

[illegible]

Table 93 Listen Mode with Preamble Detect Condition Recommended DIO Mapping

[illegible]

7.4 Top Sequencer Packet Format

Payload Length Beacon On RegPacketConfig2

7.4.1 Beacon Packet Format

Beacon Sent

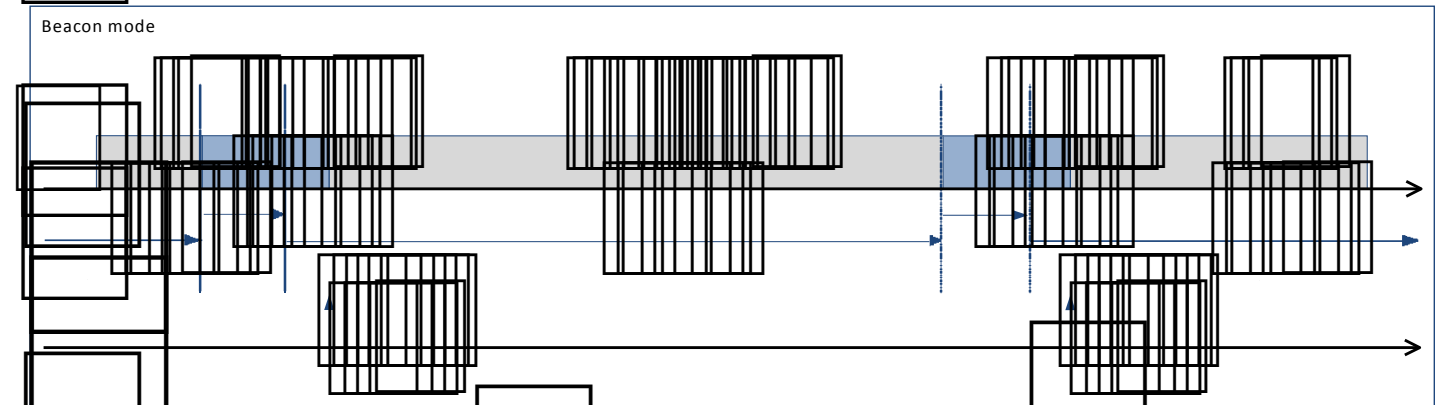


Figure 52. Beacon Mode Timing Diagram

7.4.2 Sequence Configuration

SequenceStop RegSeqConfig1

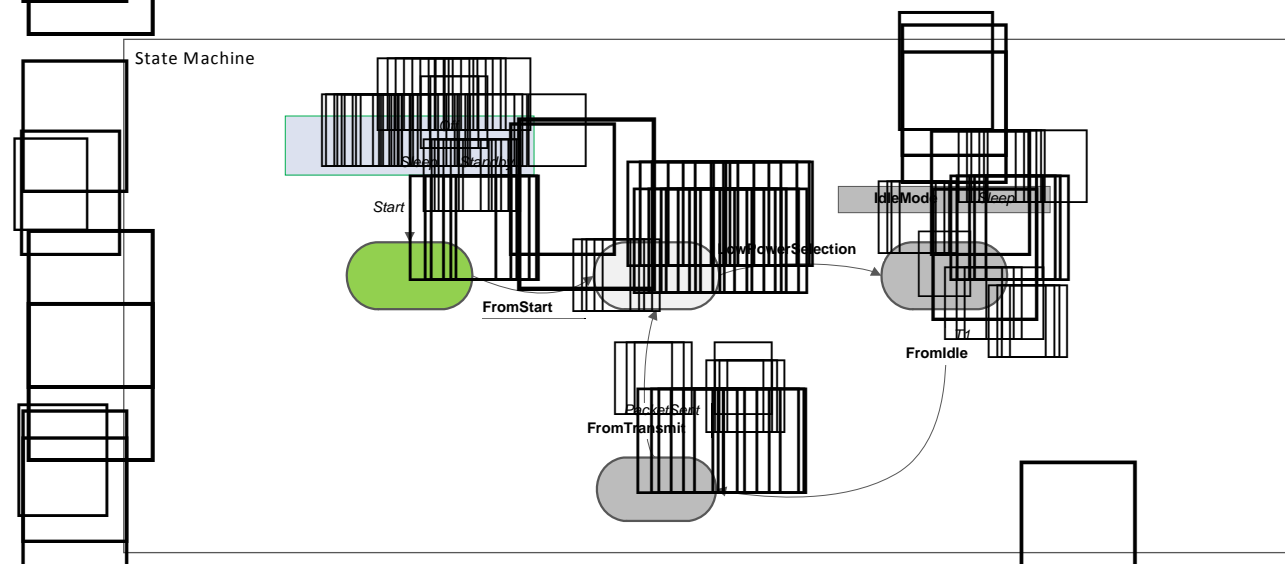


Figure 53. Beacon Mode State Machine

Table 94 Beacon Mode Settings

Variable	Default	Effect
BeaconPowerSelection	0	Low Power Selection
BeaconRateSelection	0	Low Rate Selection
PacketSent	0	Packet Sent



7.5. Example CRC Calculation

```

1 // CRC types
2 #define CRC_TYPE_CCITT 0
3 #define CRC_TYPE_IBM 1
4
5 // Polynomial = X^16 + X^12 + X^5 + 1
6 #define POLYNOMIAL_CCITT 0x1021
7 // Polynomial = X^16 + X^15 + X^2 + 1
8 #define POLYNOMIAL_IBM 0x8005
9
10 // Seeds
11 #define CRC_IBM_SEED 0xFFFF
12 #define CRC_CCITT_SEED 0x1D0F
13
14 /*
15  * CRC algorithm implementation
16  *
17  * \param[IN] crc Previous CRC value
18  * \param[IN] data New data to be added to the CRC
19  * \param[IN] polynomial CRC polynomial selection [CRC_TYPE_CCITT, CRC_TYPE_IBM]
20  *
21  * \retval crc New computed CRC
22  */
23 U16 ComputeCrc( U16 crc, U8 data, U16 polynomial )
24 {
25     U8 i;
26     for( i = 0; i < 8; i++ )
27     {
28         if( ( ( crc & 0x8000 ) >> 8 ) ^ ( data & 0x80 ) ) != 0 )
29         {
30             crc <<= 1; // shift left once
31             crc ^= polynomial; // XOR with polynomial
32         }
33         else
34         {
35             crc <<= 1; // shift left once
36         }
37         data <<= 1; // Next data bit
38     }
39     return crc;
40 }
41
42 /*
43  * CRC algorithm implementation
44  *
45  * \param[IN] buffer Array containing the data
46  * \param[IN] bufferLength Buffer length
47  * \param[IN] crcType Selects the CRC polynomial [CRC_TYPE_CCITT, CRC_TYPE_IBM]
48  *
49  * \retval crc Buffer computed CRC
50  */
51 U16 RadioPacketComputeCrc( U8 *buffer, U8 bufferLength, U8 crcType )
52 {
53     U8 i;
54     U16 crc;
55     U16 polynomial;
56
57     polynomial = ( crcType == CRC_TYPE_IBM ) ? POLYNOMIAL_IBM : POLYNOMIAL_CCITT;
58     crc = ( crcType == CRC_TYPE_IBM ) ? CRC_IBM_SEED : CRC_CCITT_SEED;
59
60     for( i = 0; i < bufferLength; i++ )
61     {
62         crc = ComputeCrc( crc, buffer[i], polynomial );
63     }
64
65     if( crcType == CRC_TYPE_IBM )
66     {
67         return crc;
68     }
69     else
70     {
71         return ( U16 ) ( ~crc );
72     }
73 }

```

Figure 54. Example CRC Code

7.6. Example Temperature Reading

```

1
2  /*!
3  * Reads the raw temperature
4  * \retval temperature New raw temperature reading in 2's complement format
5  */
6  S8 RadioGetRawTemp( void )
7  {
8      S8 temp = 0;
9      U8 regValue = 0;
10
11      regValue = RadioRead( 0x3C );
12
13      // 2's complements conversion
14      temp = regValue & 0x7F;
15      if( ( regValue & 0x80 ) == 0x80 )
16      {
17          temp *= -1;
18      }
19      return temp;
20  }
21
22  /*!
23  * Computes the temperature compensation factor
24  * \param [IN] actualTemp Actual temperature measured by an external device
25  * \retval compensationFactor Computed compensation factor
26  */
27  S8 RadioCalibrateTemp( S8 actualTemp )
28  {
29      return actualTemp - RadioGetRawTemp( );
30  }
31
32  /*!
33  * Gets the actual compensated temperature
34  * \param [IN] compensationFactor Return value of the calibration function
35  * \retval New compensated temperature value
36  */
37  S8 RadioGetTemp( S8 compensationFactor )
38  {
39      return RadioGetRawTemp( ) + compensationFactor;
40  }
41
42  /*!
43  * Usage example
44  */
45  void main( void )
46  {
47      S8 temp;
48      S8 actualTemp = 0;
49      S8 compensationFactor = 0;
50
51      // Ask user for the temperature during calibration
52      actualTemp = AskUserTemperature( );
53      compensationFactor = RadioCalibrateTemp( actualTemp );
54
55      while( True )
56      {
57          temp = RadioGetTemp( compensationFactor );
58      }
59  }

```

Figure 55. Example Temperature Reading

7.7. Reference Design

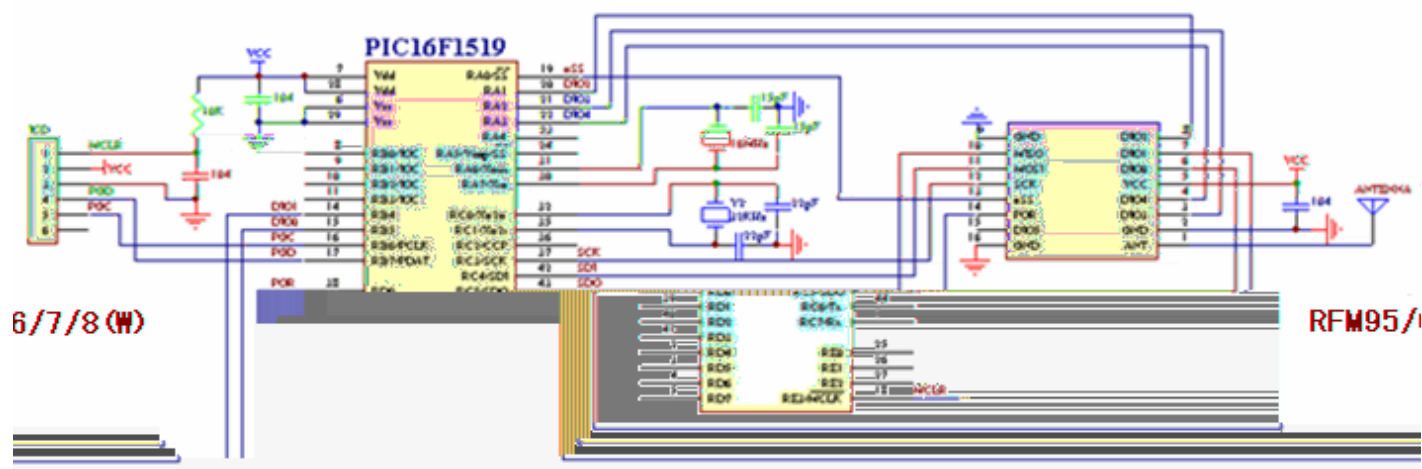
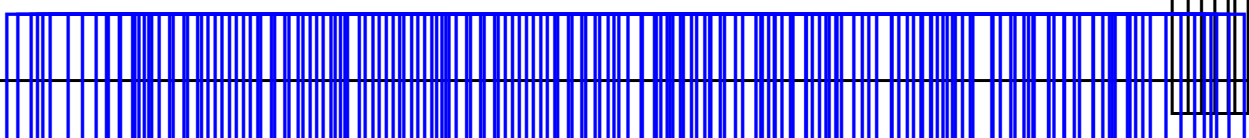
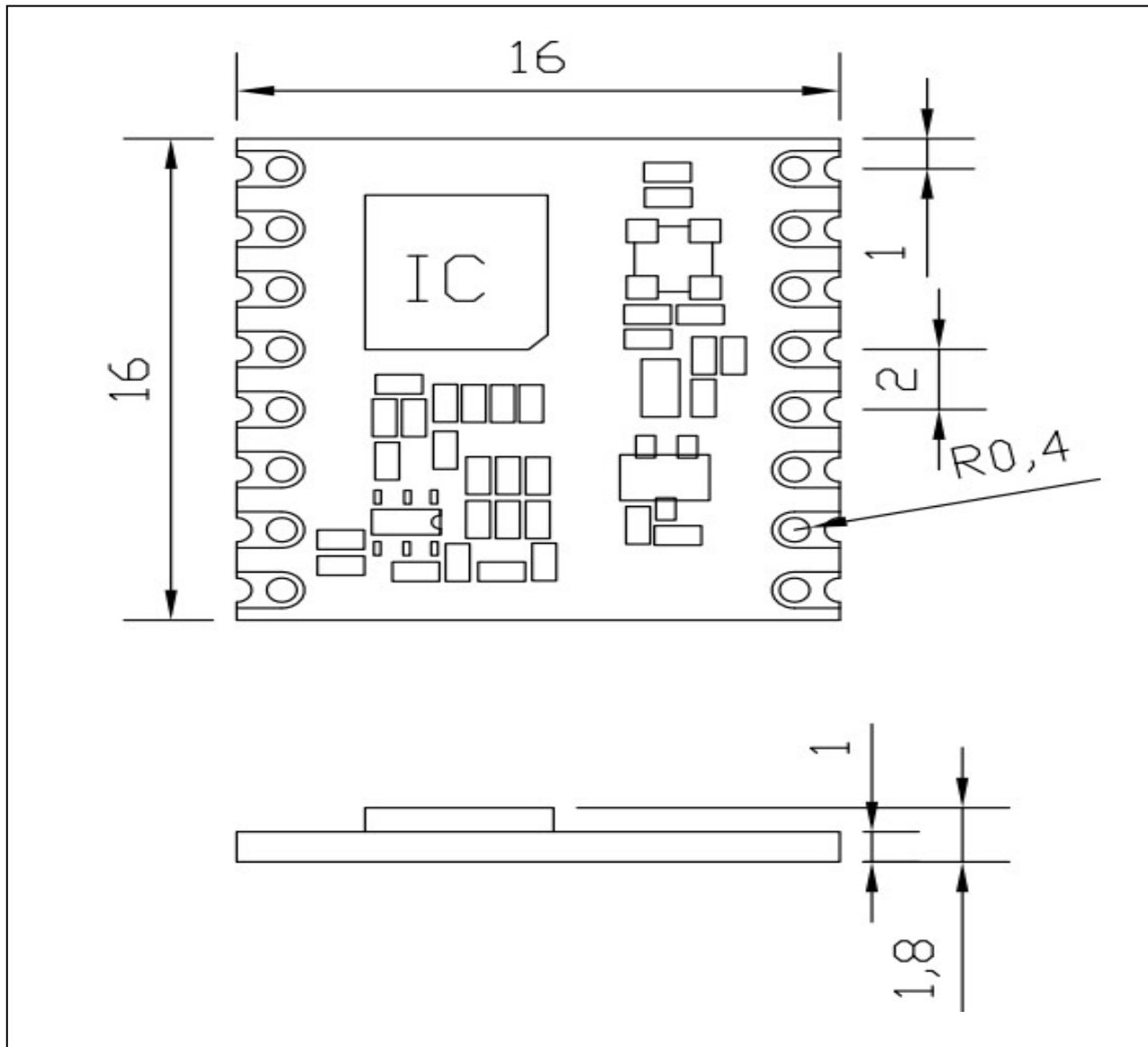


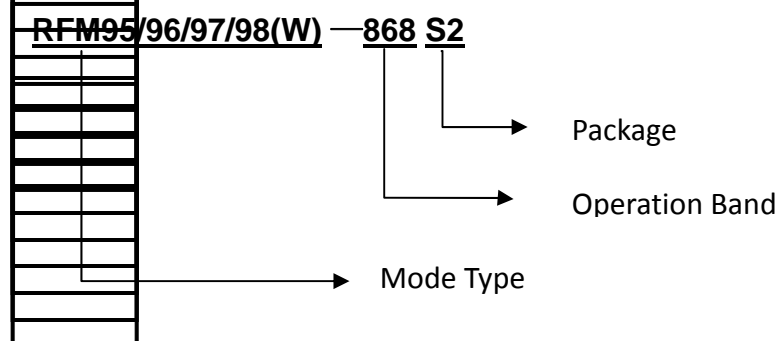
Figure 56:+20dBm Schematic

8. Packaging Information

8.1. Package Outline Drawing



15.2. Ordering Information



P/N: RFM95W-868S2

RFM95W module at 868MHz band, SMD Package

P/N: RFM95W-915S2

RFM95W module at 915MHz band, SMD Package

P/N: RFM96W-315S2

RFM96W module at 315MHz band, SMD Package

P/N: RFM96W-433S2

RFM96W module at 433MHz band, SMD Package

P/N: RFM97W-868S2

RFM97W module at 868MHz band, SMD Package

P/N: RFM97W-915S2

RFM97W module at 915MHz band, SMD Package

P/N: RFM98W-315S2

RFM98W module at 315MHz band, SMD Package

P/N: RFM98W-433S2

RFM98W module at 433MHz band, SMD Package

