RFM95/96/97/98(W) - Low Power Long Range Transceiver Module V1.0

GENERAL DESCRIPTION

LoRa™

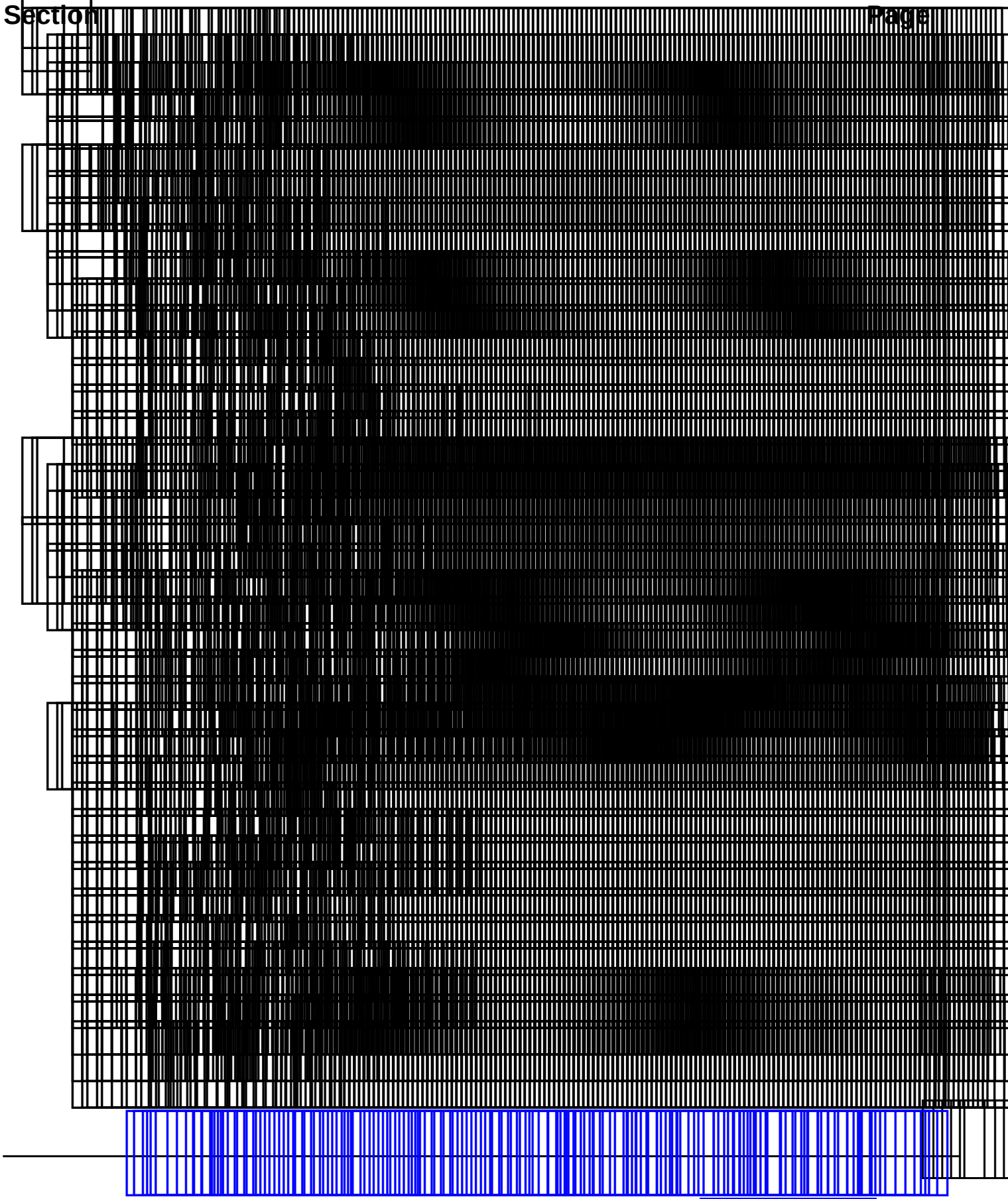
RFM95/96/97/98(W)

APPLICATIONS

KEY PRODUCT FEATURES

- LoRa™
- LoRa™

Section Page



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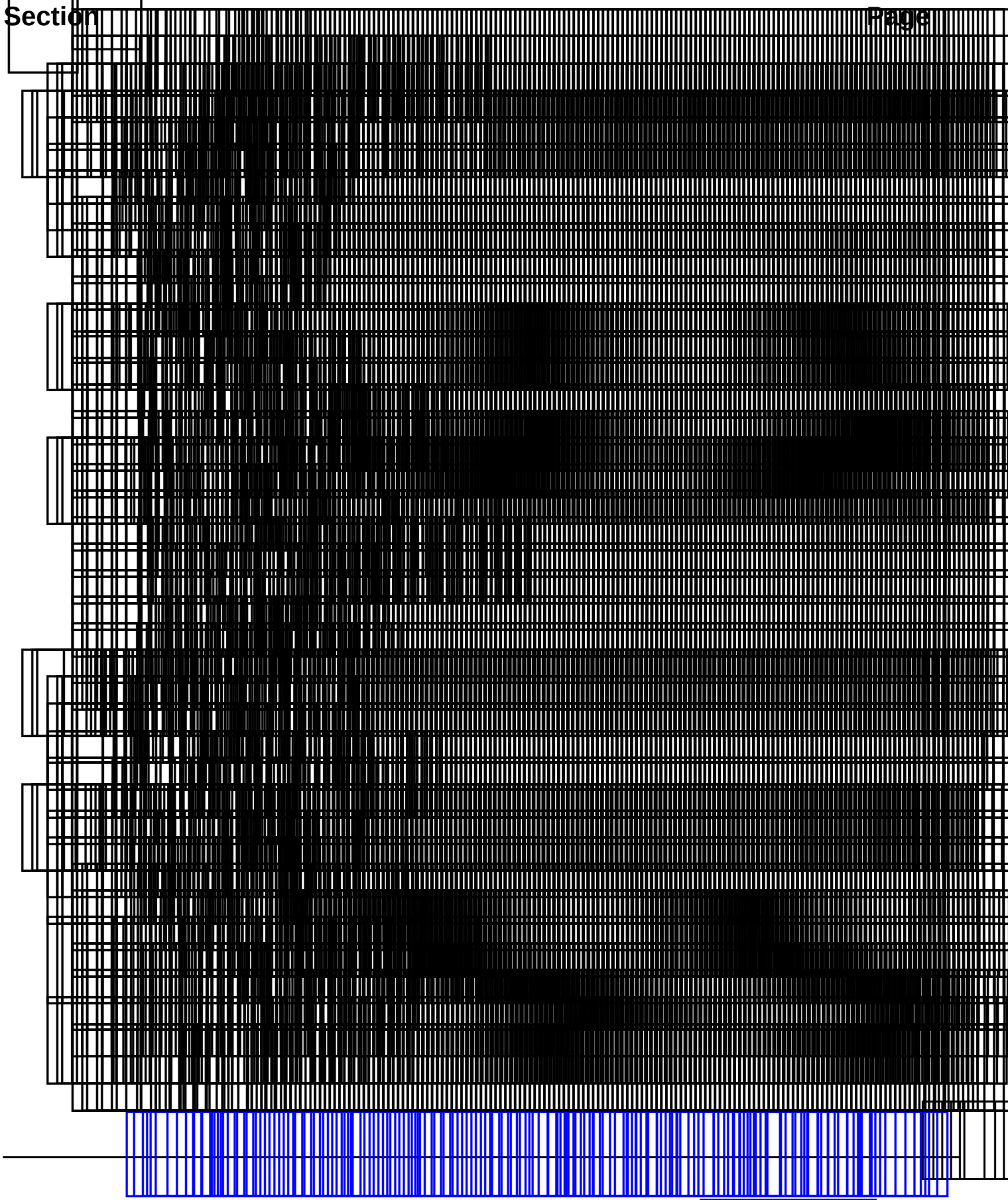

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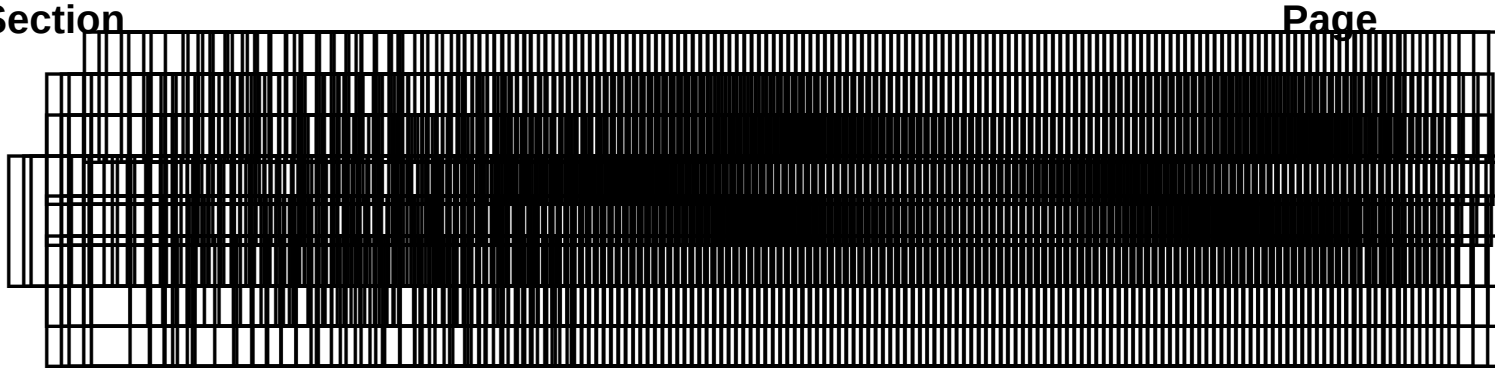

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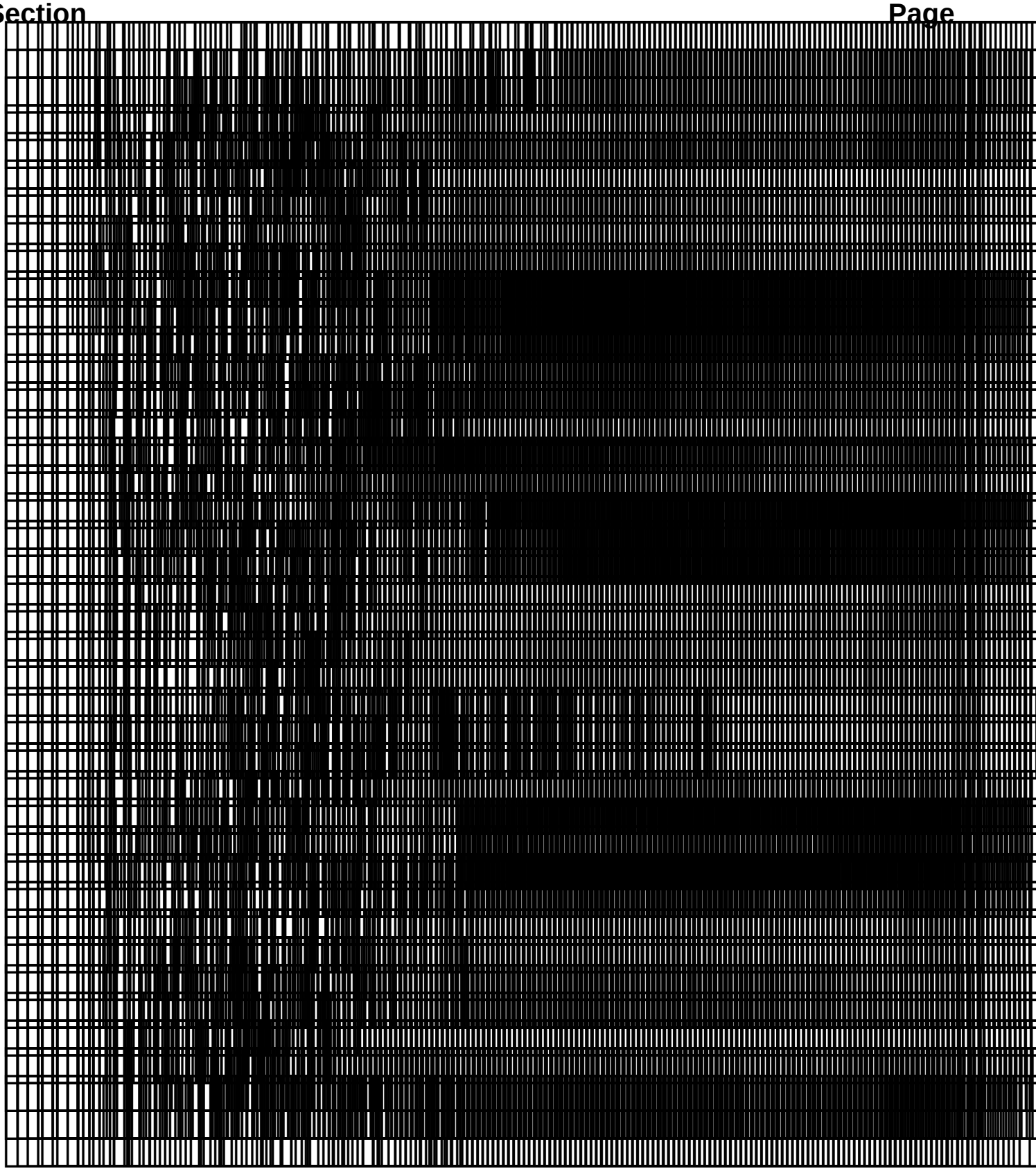

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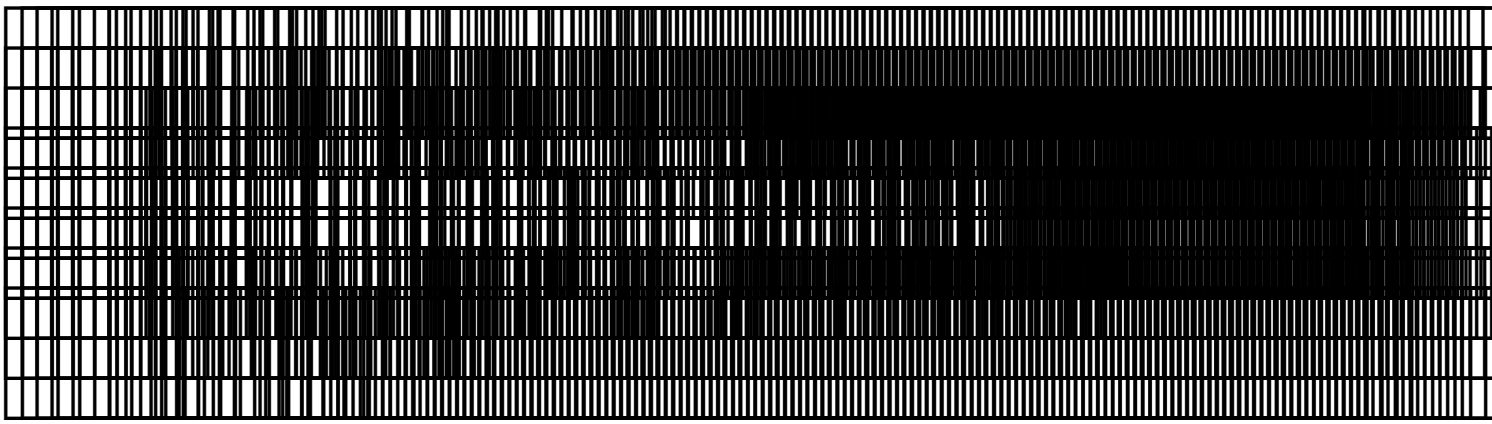

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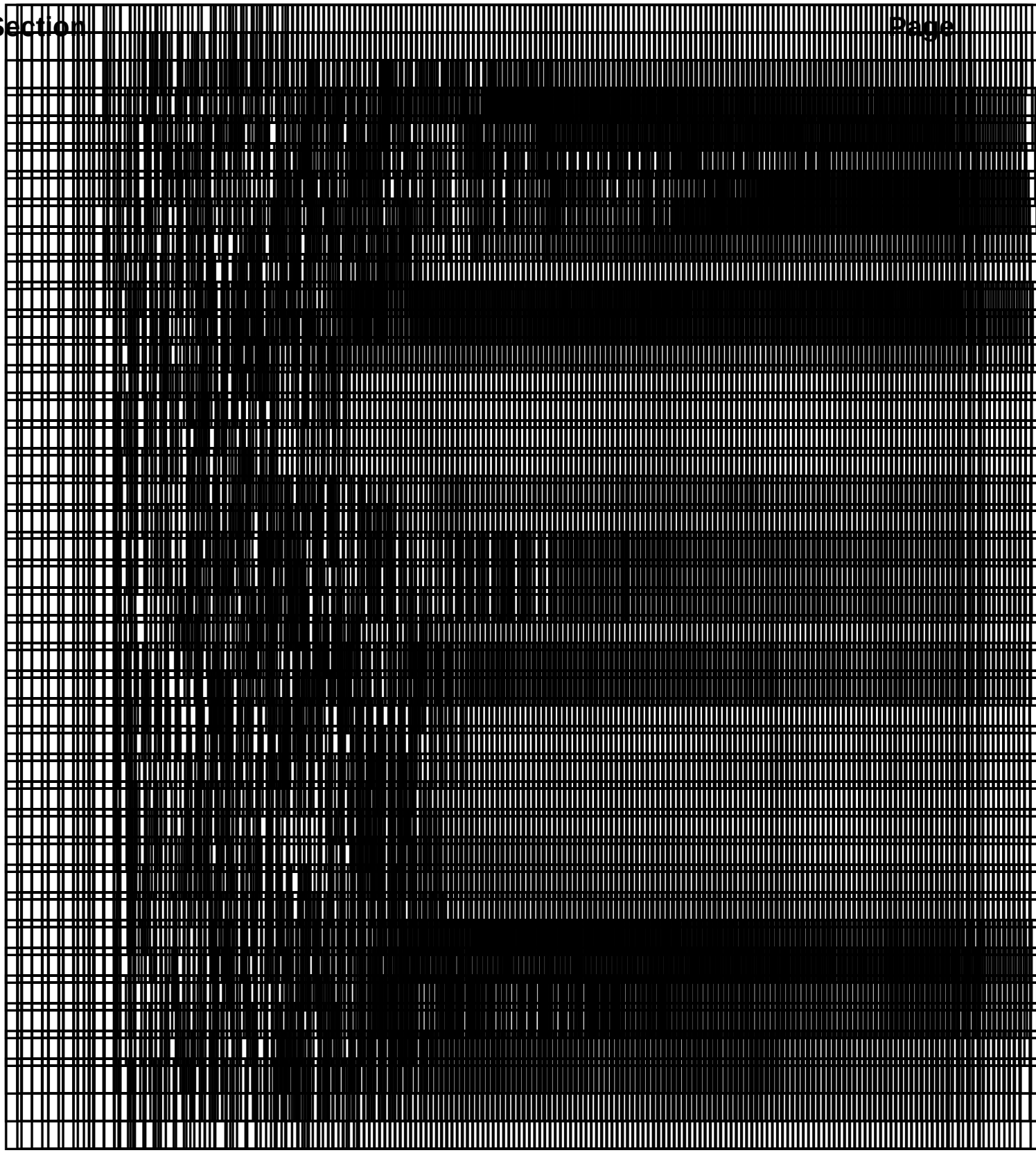

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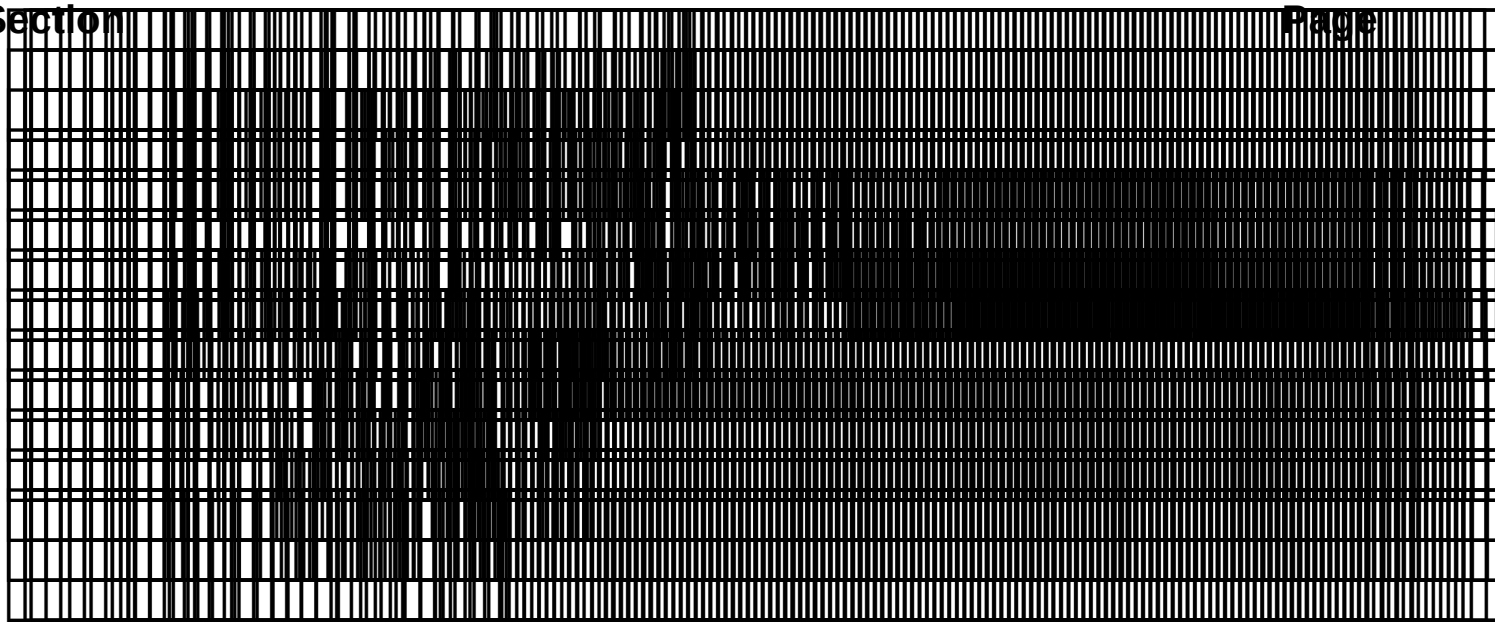


1. General Description

1.1. Simplified Block Diagram

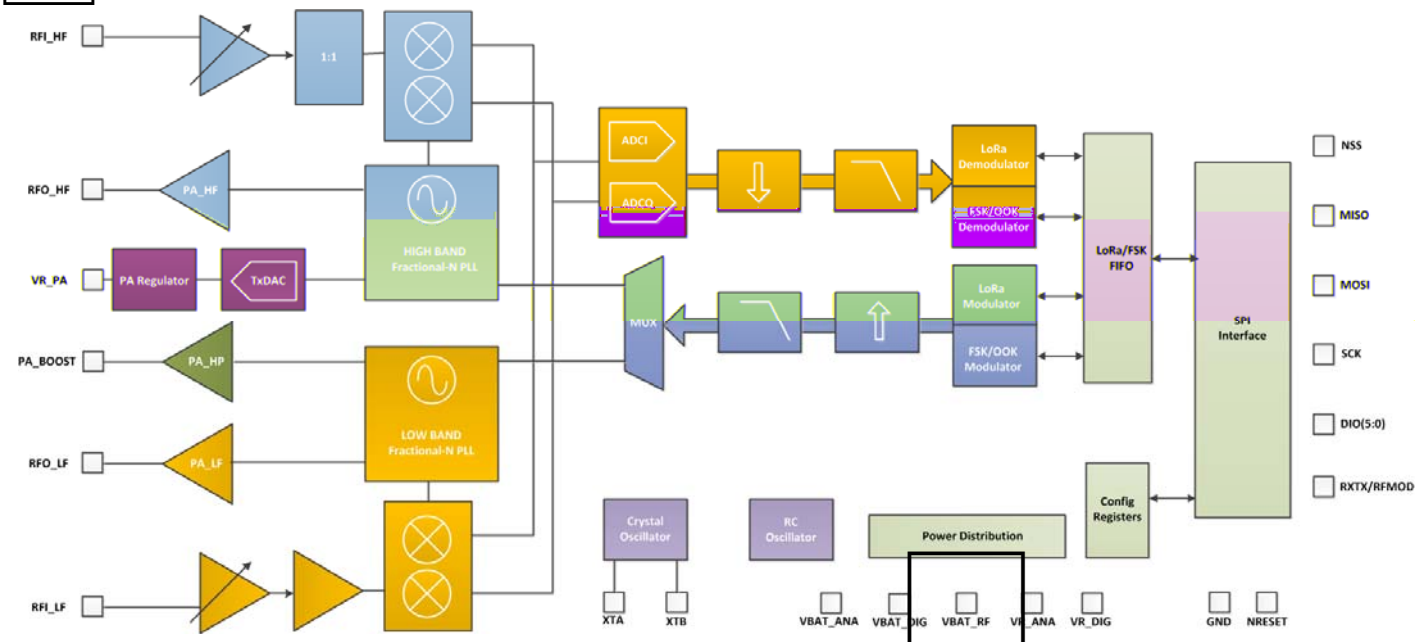


Figure 1. Block Diagram

1.2. Product Versions

Table 48 RFM95/96/97/98(W) Device Variants and Key Parameters

Part Number	Frequency Range	Spreading Factor	Bandwidth	Effective Bitrate	Est. Sensitivity

1.3. Pin Diagram

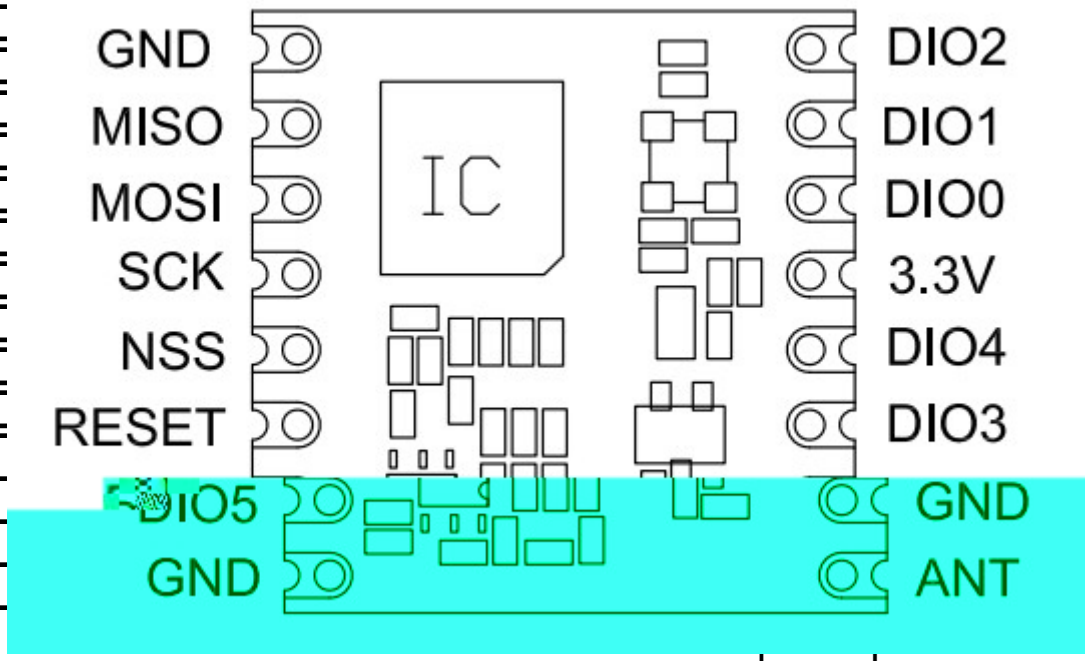


Figure 2. Pin Diagrams

1.4. Pin Description

Number	Name	Type	Description Description Stand Alone Mode

2. Electrical Characteristics

2.1. ESD Notice

2.2. Absolute Maximum Ratings

Table 49 Absolute Maximum Ratings

Symbol	Description	Min	Max	Unit

Note Specific ratings apply to +20 dBm operation (see Section 5.4.3).

2.3. Operating Range

Table 50 Operating Range

Symbol	Description	Min	Max	Unit

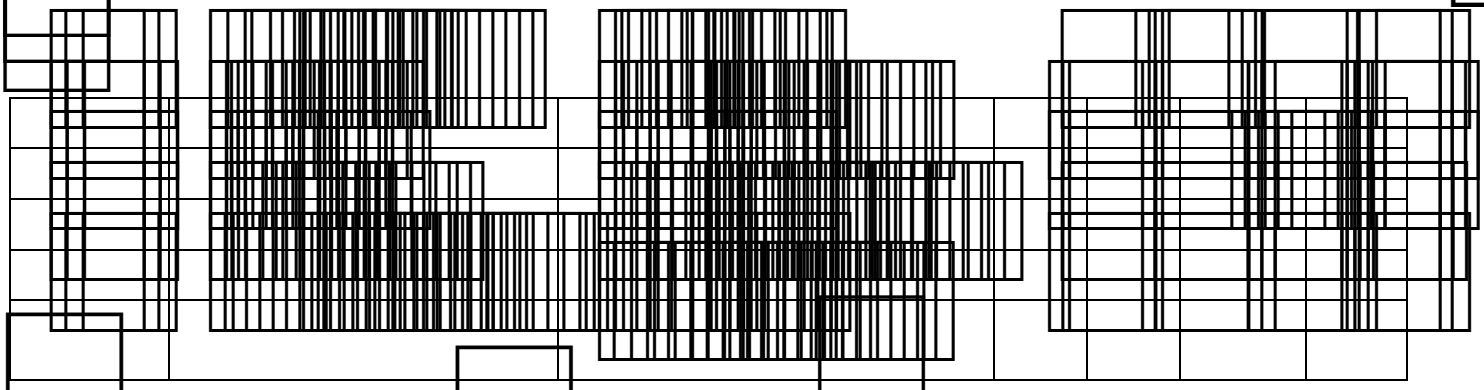
Note A specific supply voltage range applies to +20 dBm operation (see Section 5.4.3).

2.4. [illegible]

2.4.1. Power Consumption

Table 51 Power Consumption Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit



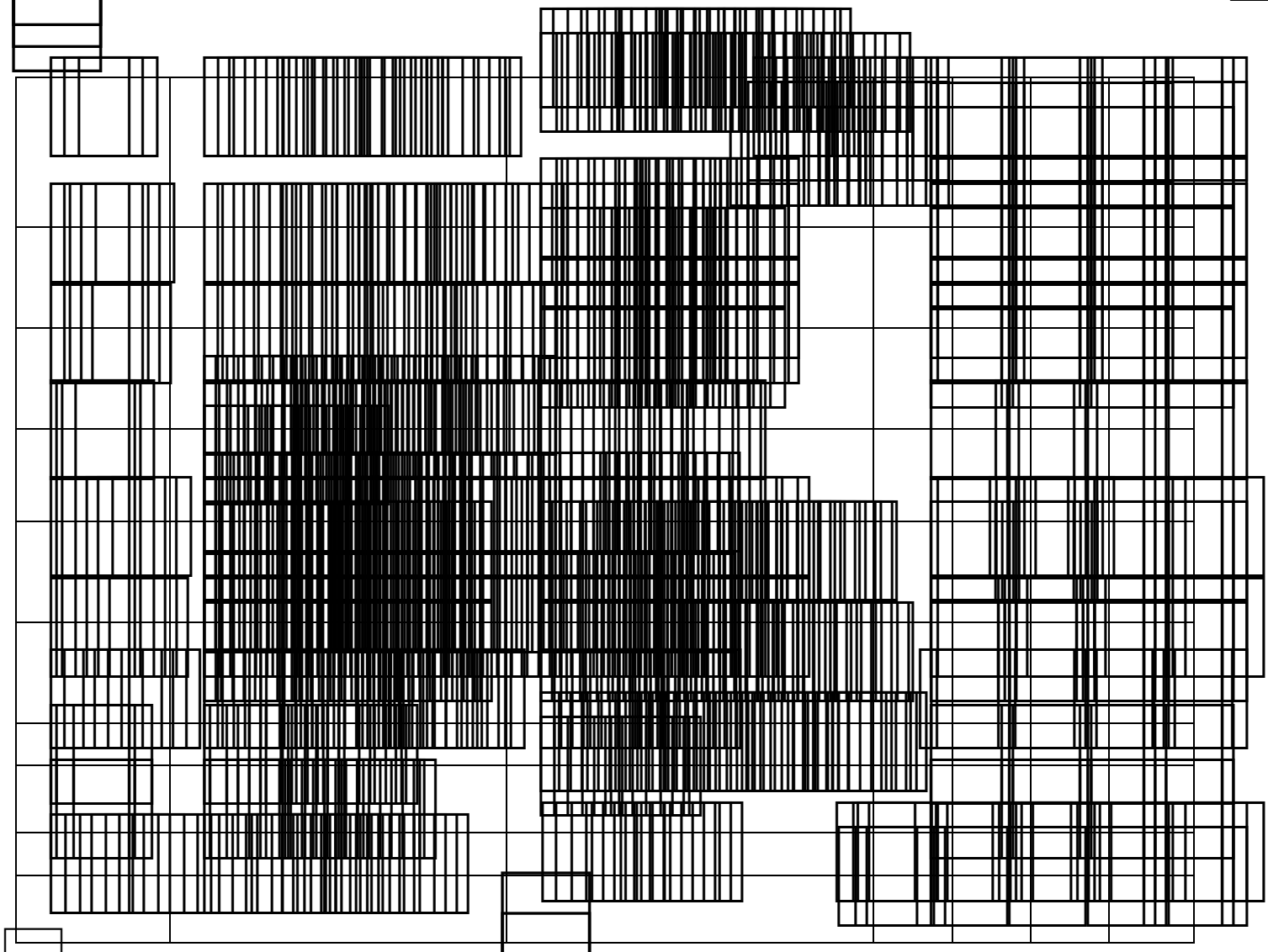
Note: For Maximum Bit rate, the maximum modulation index is 0.5.

2.4.3. FSK/OOK [illegible]

Typ: Fc=434MHz

Table 53 FSK/OOK Receiver Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit



* *RxBw = 83 kHz (Single Side Bandwidth)*

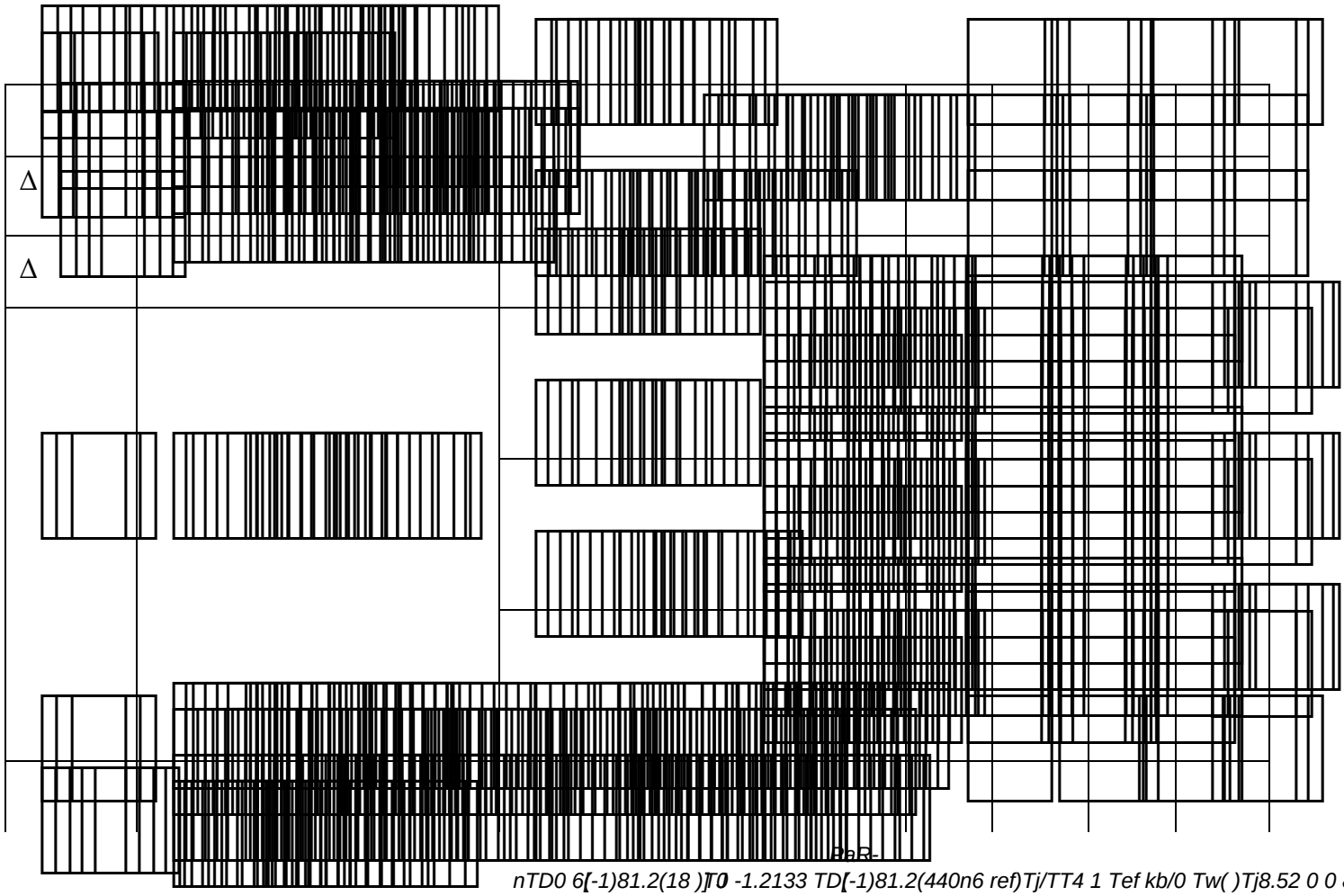
** *RxBw = 50 kHz (Single Side Bandwidth)*

*** *RxBw = 250 kHz (Single Side Bandwidth)*

2.4.4. FSK/OOK Mode Transmitter

Table 54 Transmitter Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit
Δ						



nTD0 6[-1)81.2(18)]T0 -1.2133 TD[-1)81.2(440n6 ref)Tj/TT4 1 Tef kb/0 Tw( )Tj8.52 0 0 8

Table 55 LoRa Receiver Specification.

Symbol	Description	Conditions	Min	Typ	Max	Unit
LoRaTM						

Table 56. Electrical specifications: Lora™ *mode*

2.4.6. Digital Specification

Table 57 Digital Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit

3. RFM95/96/97/98(W) Features

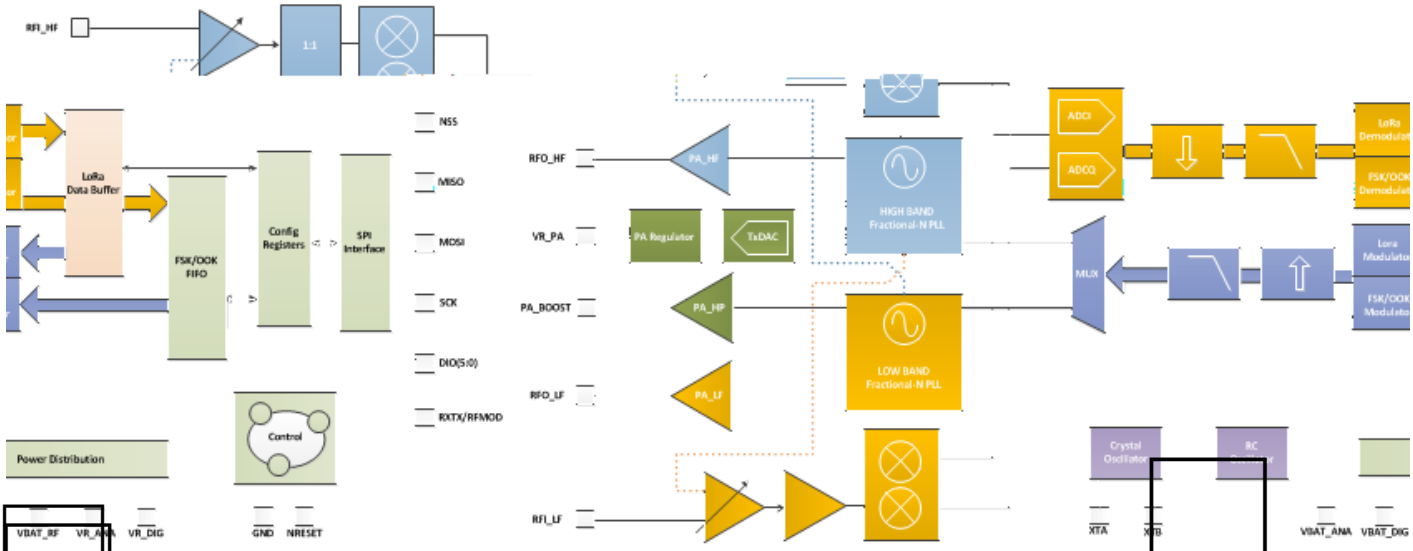


Figure 1 RFM95/96/97/98(W) Block Diagram

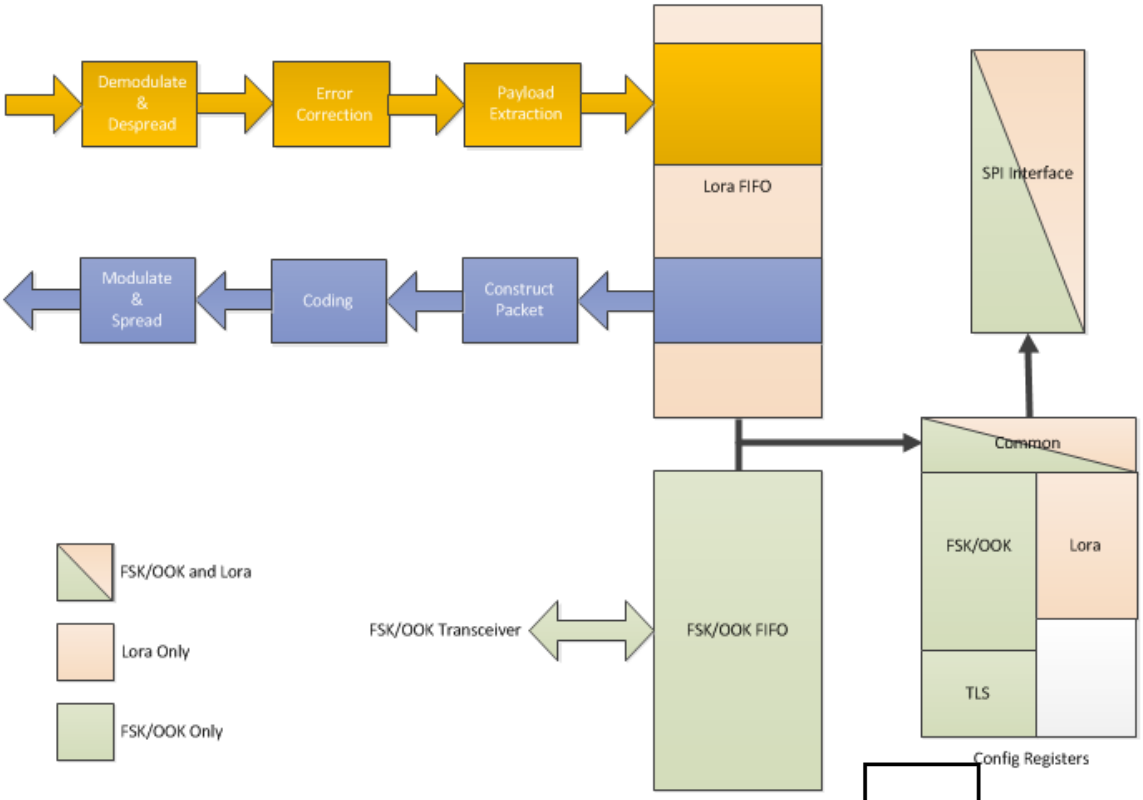
LoRa™
FSK

3.1. LoRa™ Mode

3.2. FSK/GFSK Mode

4. RFM95/96/97/98(W) Digital Electronics

4.1.1. Link Design Using the LoRa™ Modem



4.1.1.2. Spreading Factor

LoRa™

Table 59 Range of Spreading Factors

SpreadingFactor (RegModulationCfg)	Spreading Factor (Chips / symbol)	LoRa Demodulator SNR

Spreading Factor

- Spreading Factor
- Spreading Factor
- Spreading Factor
- Spreading Factor

4.1.1.3. Coding Rate

LoRa™

Table 60 Cyclic Coding Overhead

CodingRate (RegTxCfg1)	Cyclic Coding Rate	Overhead Ratio

LoRa™

4.1.1.4. Sto

LoRa™

LoRa™

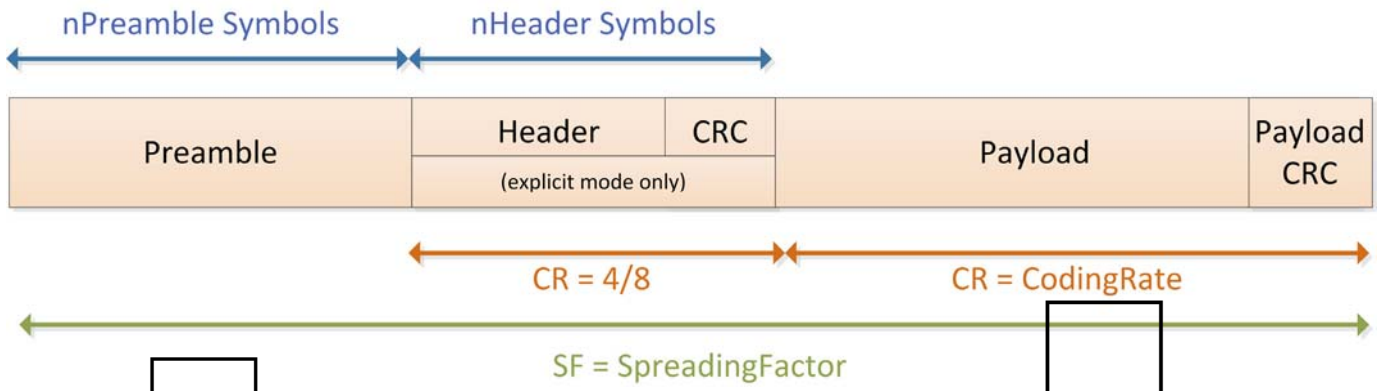
Bandwidth (kHz)	Spreading Factor	Coding rate	Nominal Rb (bps)

Note: In the lower band (169 MHz), the 250 kHz and 500 kHz bandwidths are not supported.

4.1.1.5. LoRa™ Transmission Parameter Relationship

LoRa™

Rs =


nPreamble Symbols
nHeader Symbols
Preamble
Header
CRC
(explicit mode only)
Payload
Payload CRC
CR = 4/8
CR = CodingRate
SF = SpreadingFactor

[redacted]

Note: With SF = 6 selected, implicit header mode is the only mode of operation possible.

[redacted]

$$T_s = \frac{1}{R_s}$$

$$T_{preamble} = (n_{preamble} + 4.25)T_s$$

$$T_{payload} = \begin{cases} T_{sym}\left[8 + ceil\left(\frac{8l_{payload} - 4SF + 24}{4SF}\right)\right](CR+4) & \text{where: } l_{payload} > 0, \text{ implicit header} \\ T_{sym}\left[8 + ceil\left(\frac{8l_{payload} - 4SF + 44}{4SF}\right)\right](CR+4) & \text{where: } l > 0, \text{ explicit header} \end{cases}$$

$$T_{packet} = T_{preamble} + T_{payload}$$

[redacted]

Principle of operation

HoppingPeriod

HoppingPeriod = Tx/RxFreqHoppingPeriod

FhssChangeChannel

FhssPresentChannel

Timing of Channel Updates

FhssChannelChange

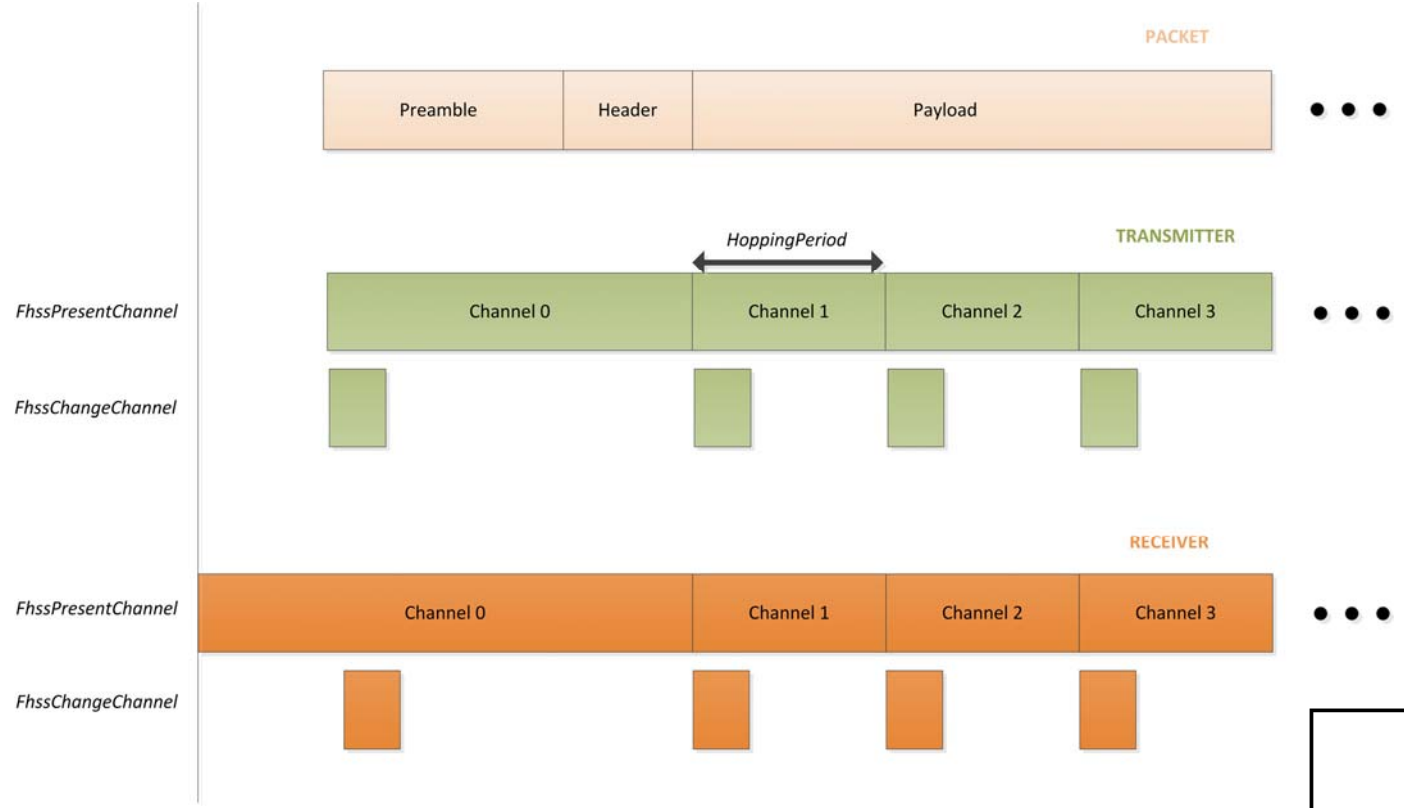


Figure16. Interrupts generated in the case of successful frequency hopping communication.

4.1.2. LoRa™ Mode Register Map

LoRa™

4.1.2.1. LoRa™ Configuration Registers

Write only in Sleep and Stand-by modes (except RegFifoAddrPtr and RegFifoTxBaseAddr which are accessible in all modes). The configuration register mapping in LoRa™ mode is shown in Table

LoRa™

4.1.2.2. Status Registers

4.1.2.3. LoRa™ Modem FIFO Data Buffer

Overview

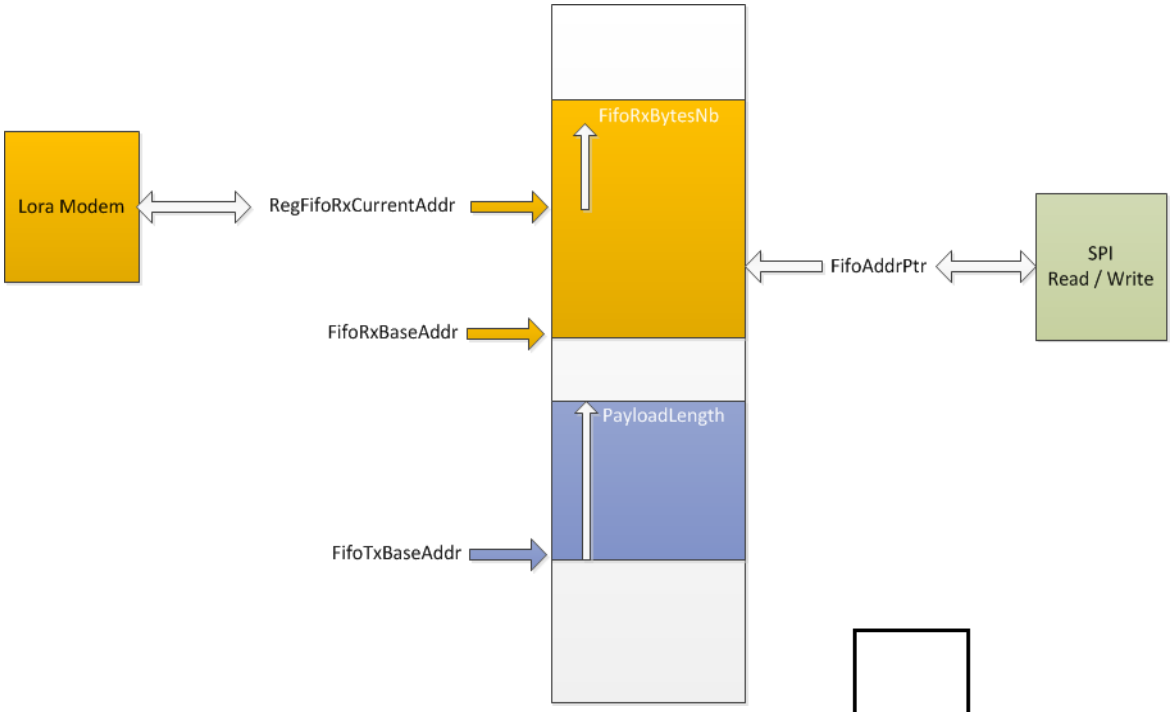
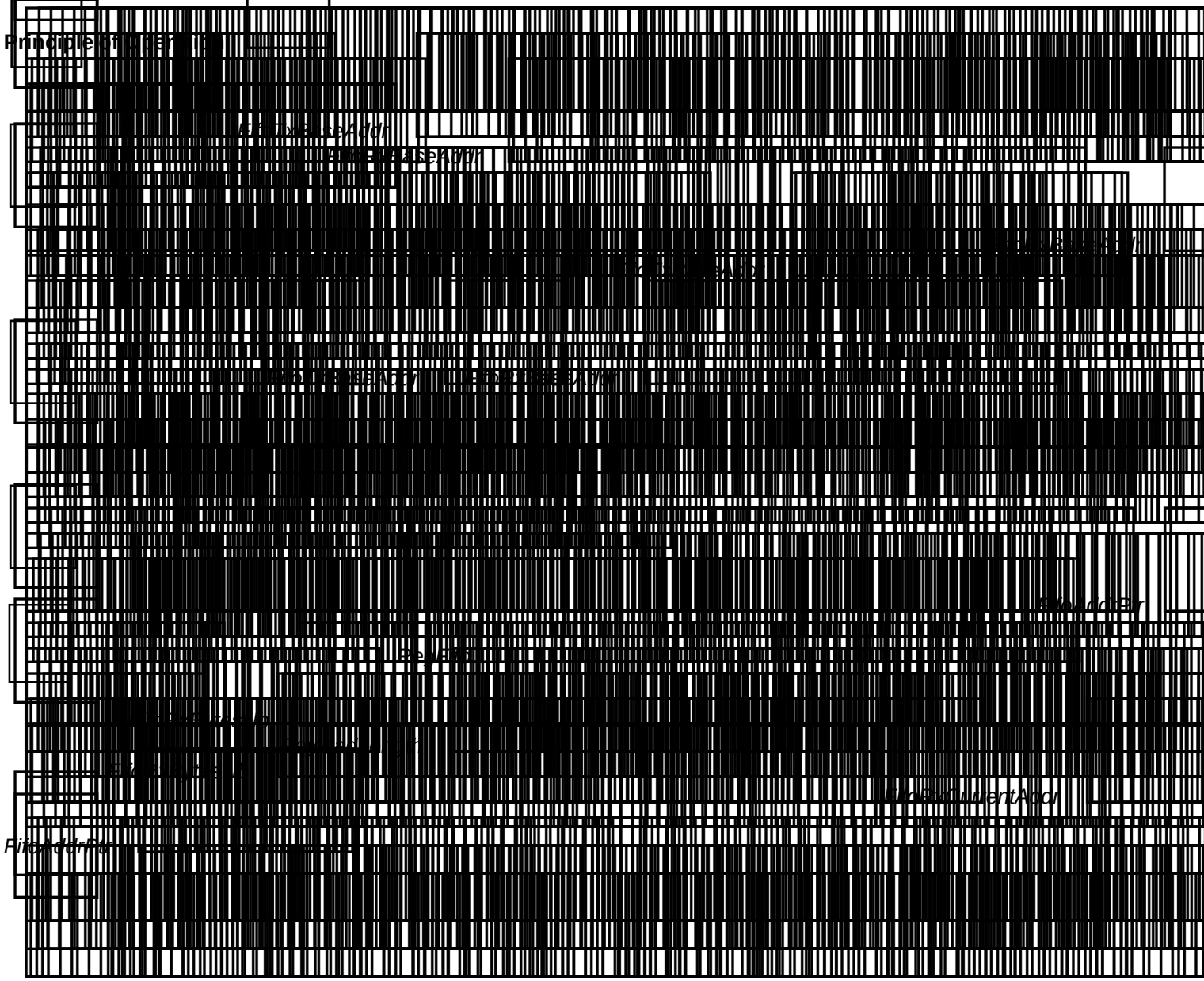


Figure 7. LoRa™ data buffer

Principle of Operation



4.1.3. Operation of the LoRa™ Modem

4.1.3.1. Operating Mode Control

RegOpMode

Table 61 LoRa™ Operating Mode Functionality

Operating Mode	
SLEEP	
STAND-BY	
FSTX	
FSRX	
TX	
RXCONTINUOUS	
RXSINGLE	
CAD	

RegOpMode

4.1.4. Frequency Settings

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

$$F_{RF} = F_{STEP} \times Frf(23,0)$$

4.1.5. LoRa™ Modem State Machine Sequences

LoRa™

Data Transmission Sequence

LoRa™

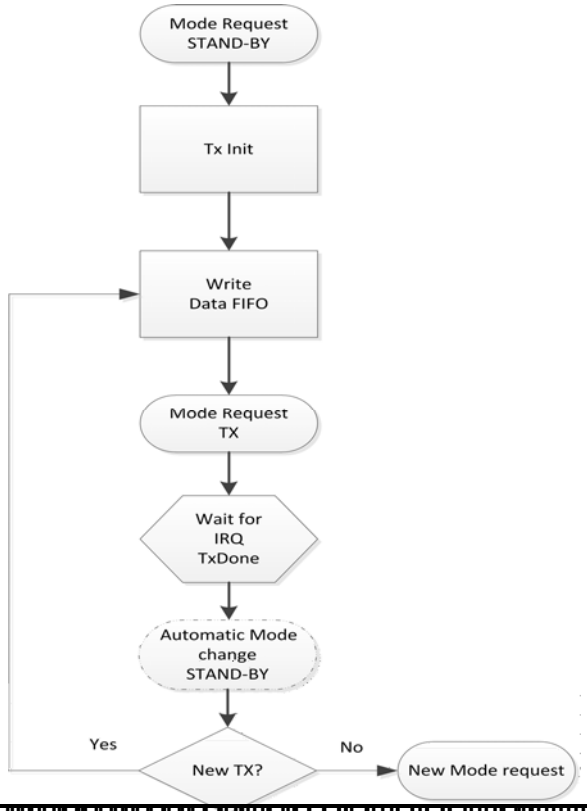


Figure 5. LoRa™ modulation transmission sequence.

- LoRa™
- Frequency hopping
- Packet engine
- FSK/OOK

Data Reception Sequence

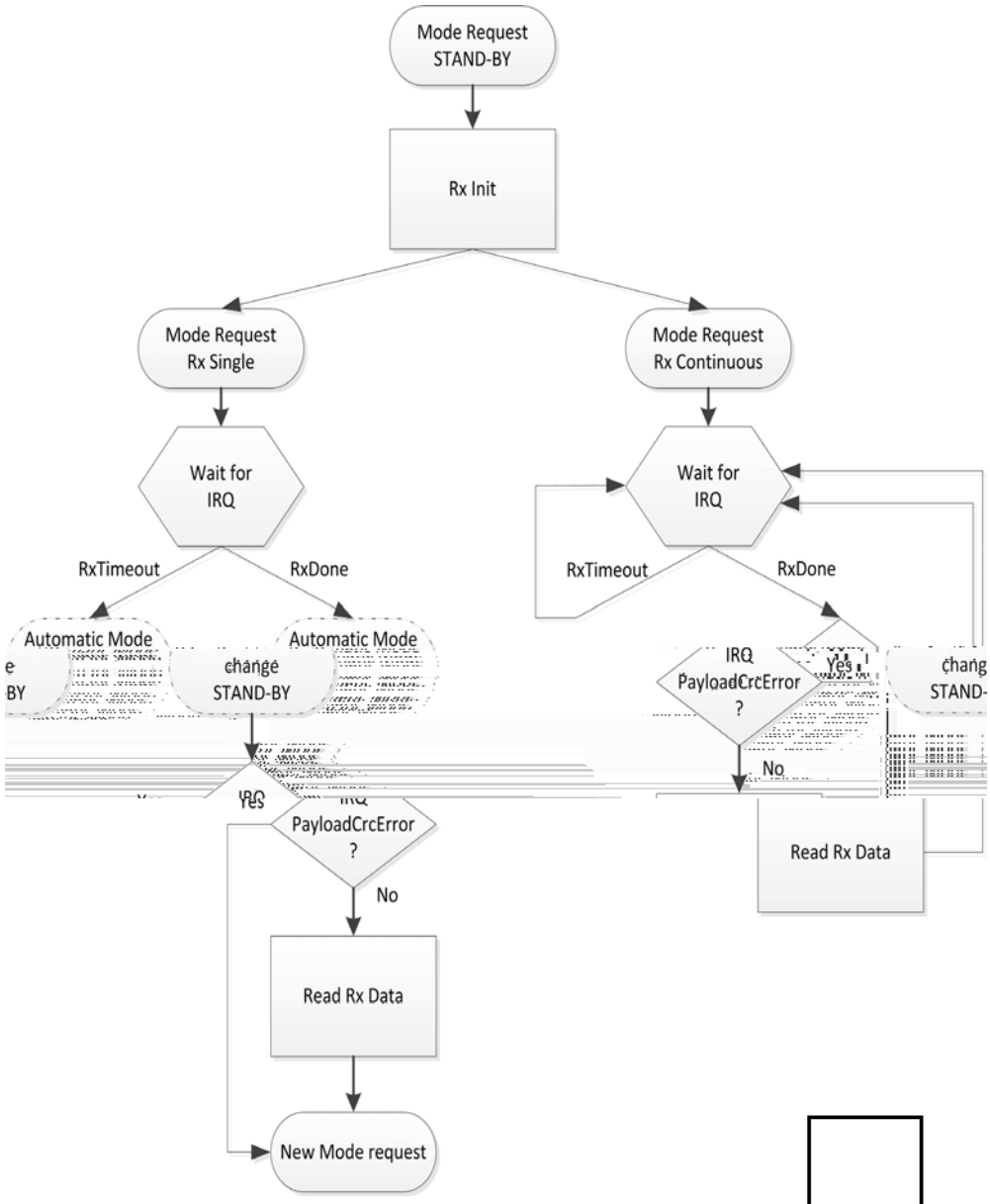
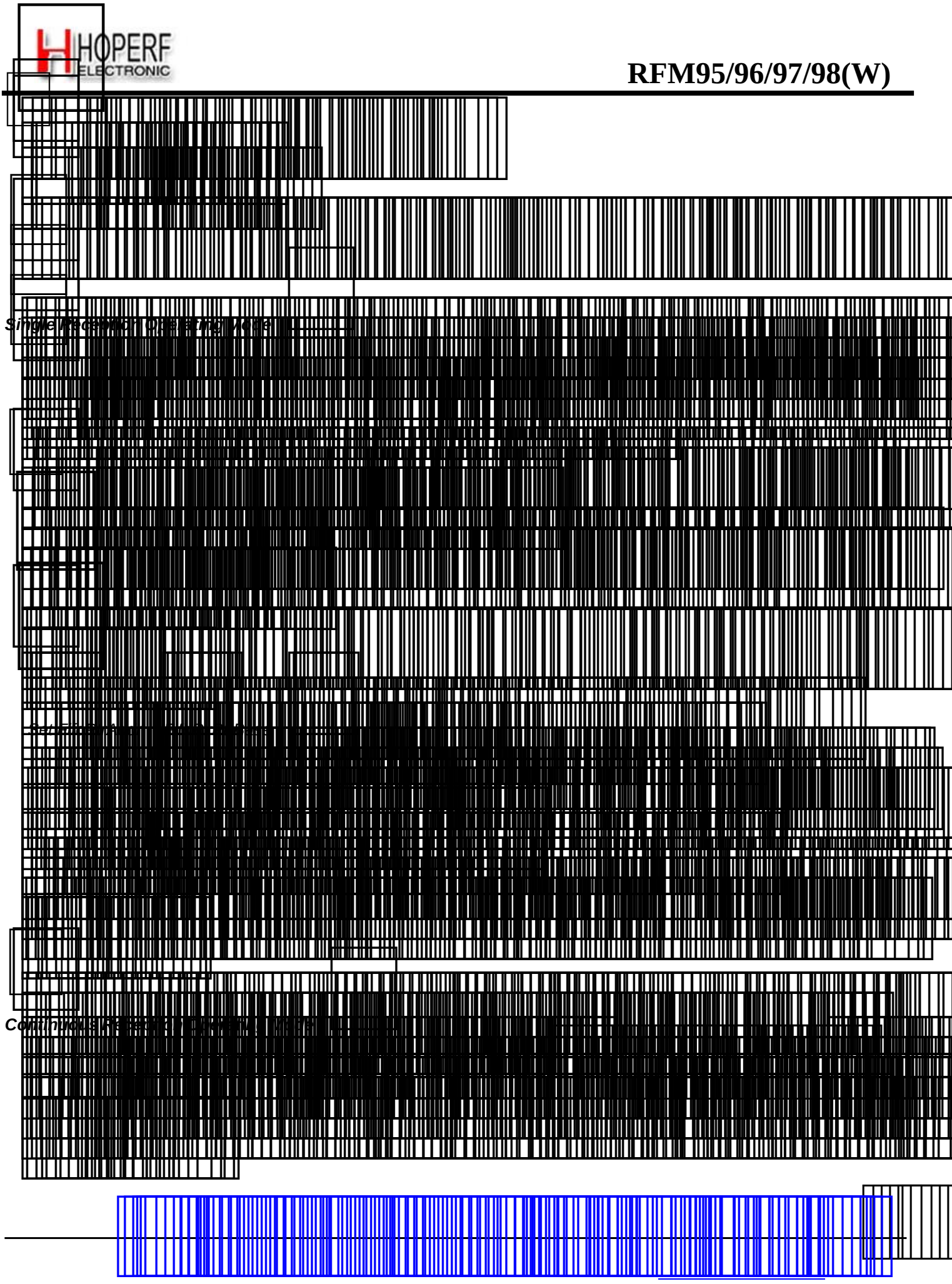
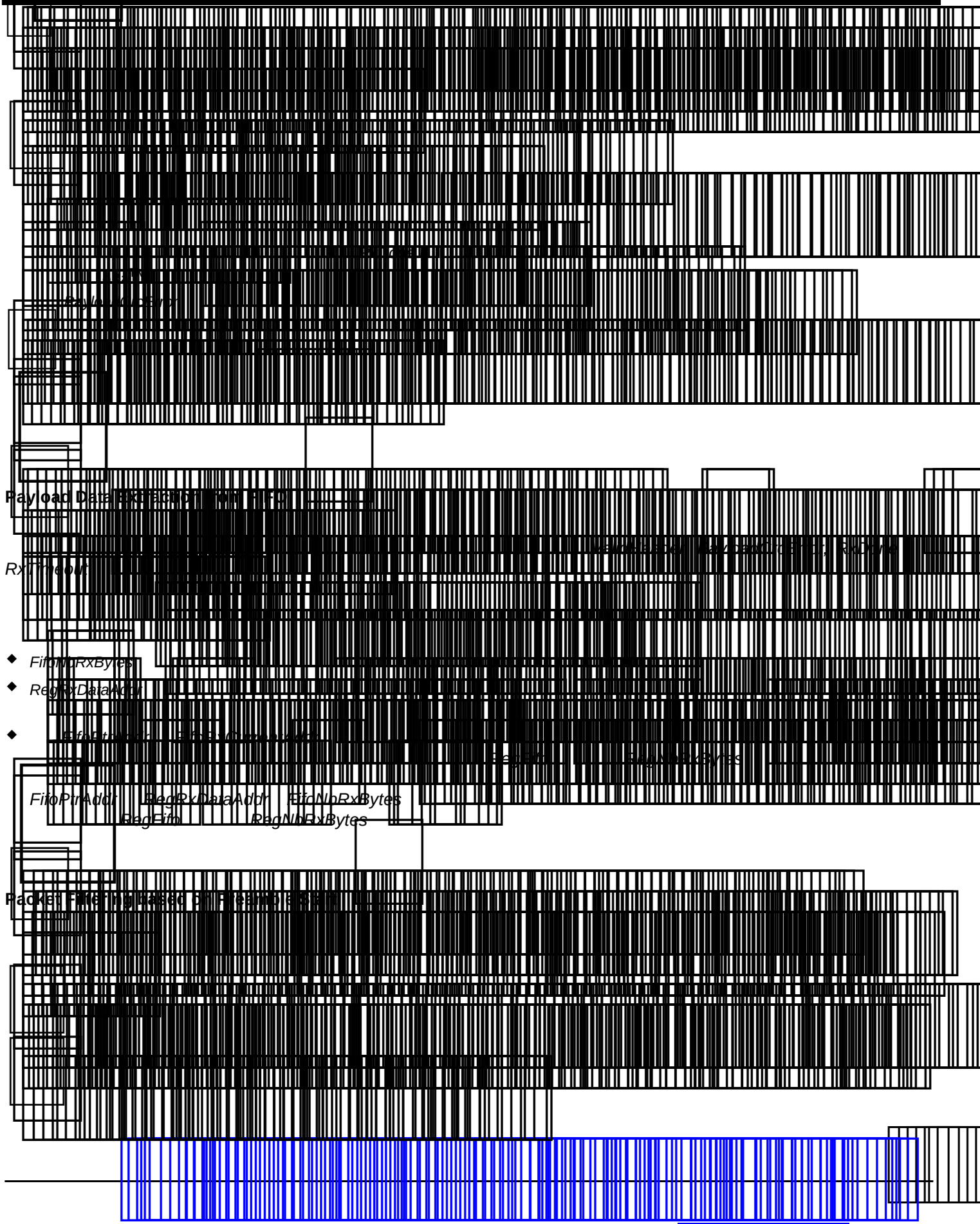


Figure 9. LoRa™ receive sequence.


Single Mechanical Operation Valve
Continuous Rotation Type



Payload Data FIFO

Packet Filtering based on Preamble Start

- [redacted]
- [redacted]
- [redacted]

Receiver [redacted]

[redacted]

$$TimeOut = LoraRxTimeout \cdot Ts$$

[redacted]

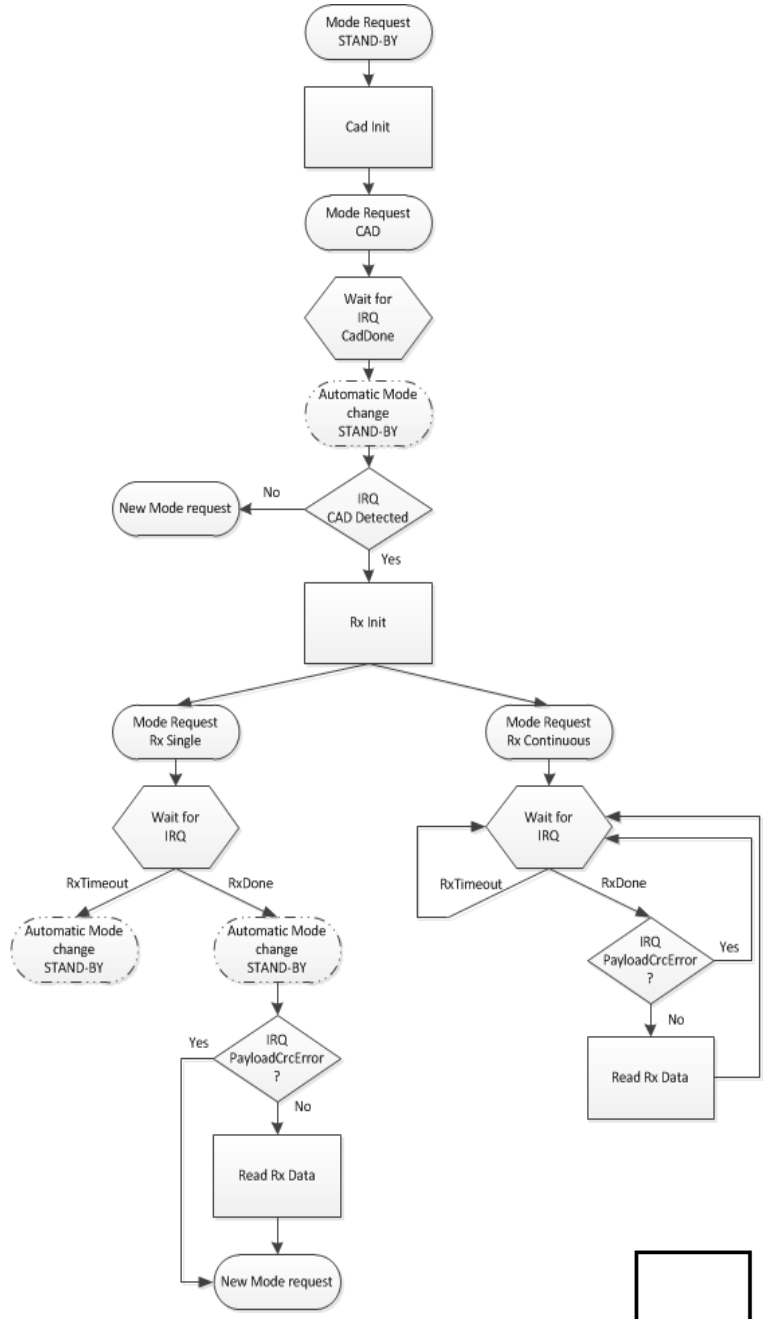


Figure 10. LoRa™ *CAD flow*

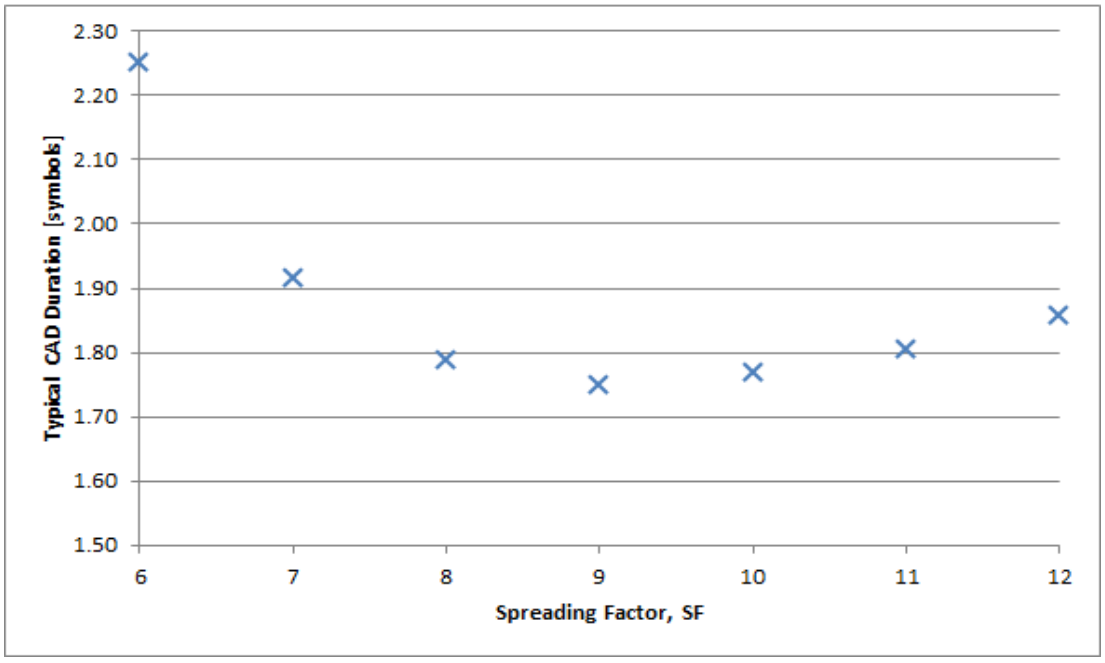


Figure 11. Channel activity detection (CAD) time as a function of spreading factor

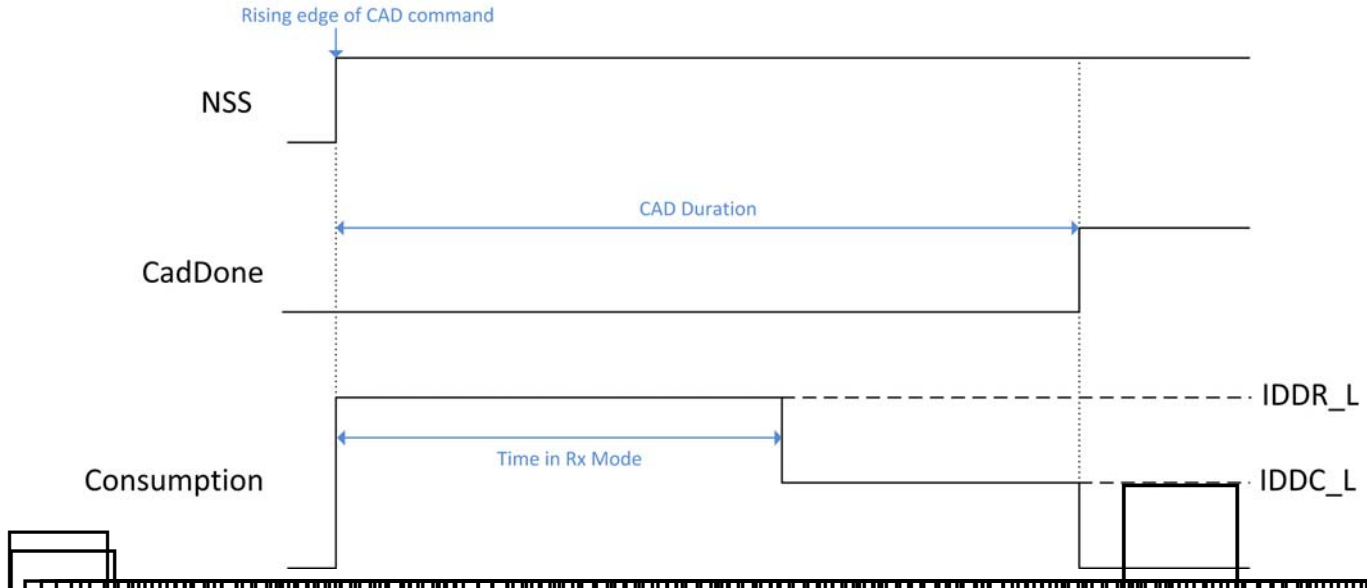


Figure 12 CAD Typical Sequence Diagram

Table 62 LoRa CAD Consumption Figures

Bandwidth (kHz)	Full Rx, IDDR_L (mA)	Processing, IDDC_L (mA)

4.1.6.1. Digital IO Pin Mapping

LoRa™ *RegDioMapping1* *RegDioMapping2.*

Table 63 DIO Mapping LoRa™ Mode

Operating Mode	DIOx Mapping	DIO5	DIO4	DIO3	DIO2	DIO1	DIO0

4.2. FSK/OOK Modem

4.2.1. Bit Rate

Bitrate RegBitrateMsb and RegBitrateLsb

$$BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{itrateFrac}{16}}$$

Note: Bitrate values have to be set such that the resulting register value is greater than or equal to 1 in FSK mode.

Bitrate

Table 64 Bit Rate Examples

Type	BitRate (15:8)	BitRate (7:0)	(G)FSK (G)MSK	OOK	Actual BR (b/s)

4.2.2. FSK/OOK Transmission

4.2.2.1. FSK/GFSK/MSK/GMSK

$$F_{DEV} = F_{STEP} \times Fdev(13,0)$$

$$F_{DEV} + \frac{R}{2} \le (250)kHz$$

Note: No constraint applies to the modulation index of the transmitter, but the frequency deviation must be set between 600 Hz and 200 kHz.

4.2.2.2. OOK Modulation

4.2.2.3. Modulation Shaping

-
-

Note: The transmitter must be restarted if the ModulationShaping setting is changed, in order to recalibrate the built-in filter.

4.2.3. FSK/OOK Reception

4.2.3.1. FSK Demodulator

$$0.5 \le \beta = \frac{2 \times F_{DEV}}{BR} \le 10$$

4.2.3.2. OOK Demodulator

OokThresholdType PeakOokThresh

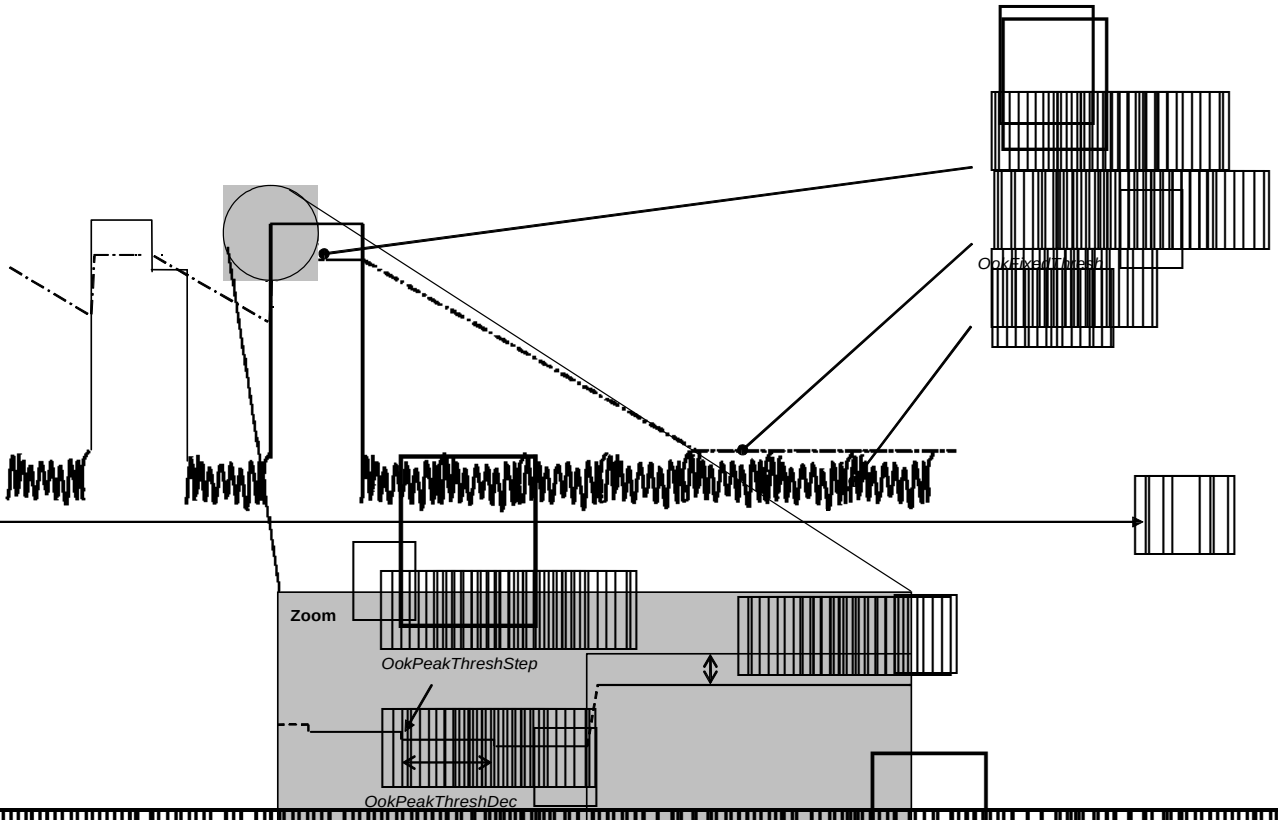


Figure 16 OokPeak Threshold Parameters

Optimizing the OokPeak Threshold

OokPeakThreshStep

-
-
-
-

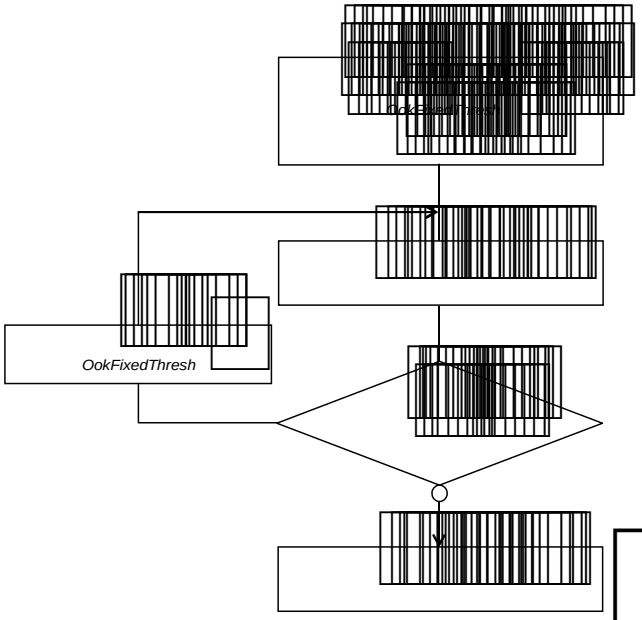


Figure 14. Floor Threshold Optimization

Optimizing Peak Detection and Fast Fading Signals

Alternative OOK Demodulator Threshold Modes

- *Peak*
- *Average*

4.2.3.3. Bit Synchronizer

BitRateMsb BitRateLsb

RegBitrate.

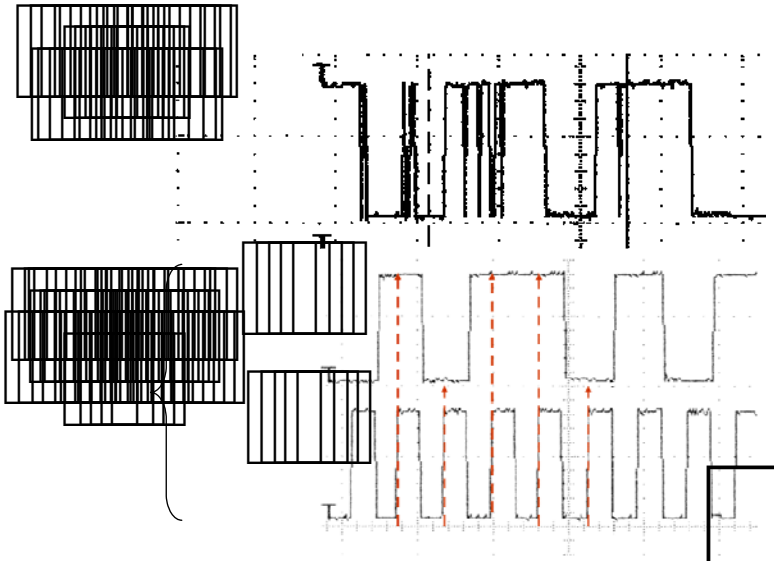


Figure 15. Bit Synchronizer Description

-
-
-

4.2.3.4. Frequency Error Indicator

FeiValue[19:0]

$$BW_{3dB} = 2 \times \left(F_{Dev} + \frac{F_{Xo}}{2}\right)$$

$$FEI = F_{STEP} \times FeiValue$$

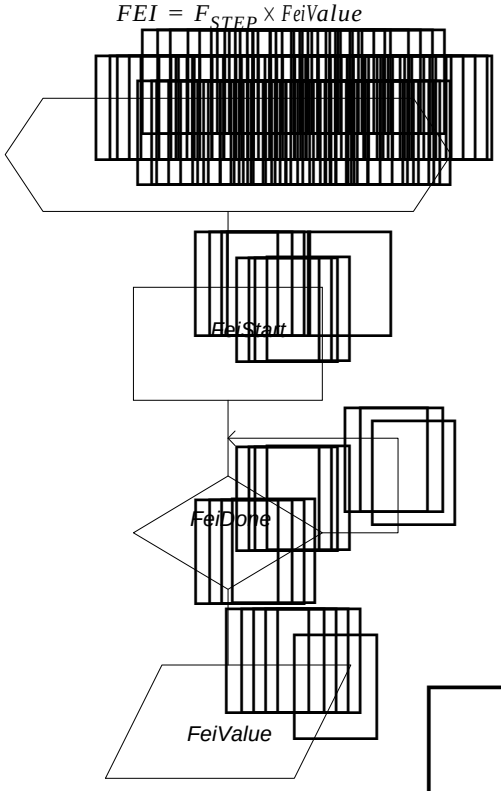


Figure 16. FEI Process

4.2.13.6. AFC

AfcAutoOn

-
-

AfcAutoClear

4.2.13.7. Preamble Detector

PreambleDetectorSize RegPreambleDetect

Table 65 Preamble Detector Settings

PreambleDetectorSize	# of Bytes

PreambleDetectorOn

RxTimeout1

RxTimeout2

RxTimeout3

RssiValue

PreambleDetect

StartRxOnPreamble

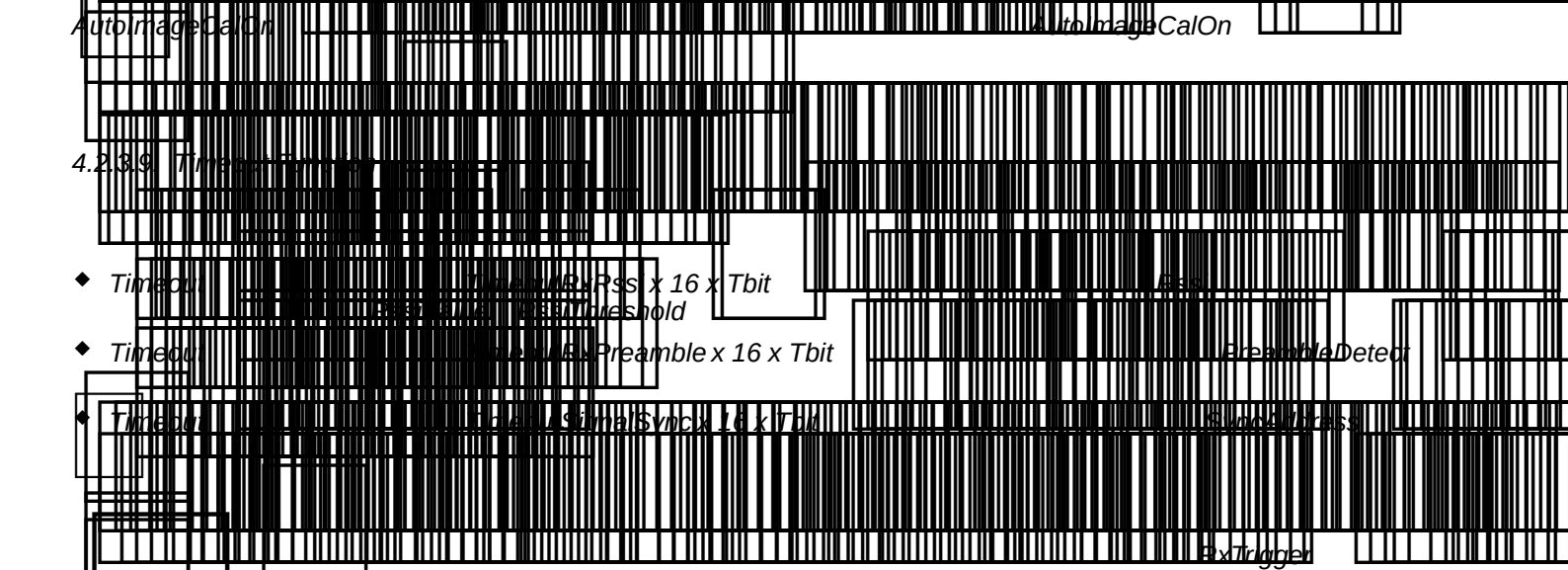
RegRxConfig

4.2.3.7. ImageReject Mixer

4.2.3.8. Timeout

-
-
-

AutoImageCalOn



AutoImageCalOn

4.2.3.9. Timeout Interrupts

- Timeout
- Timeout
- Timeout

RxTrigger

RegRxConfig:

Table 66 RxTrigger Settings to Enable Timeout Interrupts

Receiver Triggering Event	RxTrigger (2:0)	Timeout on Rssi	Timeout on PreambleDetect	Timeout on SyncAddress
Rssi				
PreambleDetect				
SyncAddress				

4.2.4. Operating Modes in FSK/OOK Mode

RegOpMode

Table 67 Basic Transceiver Modes

Mode	Selected mode	Symbol	Enabled blocks

4.2.5. Startup Times

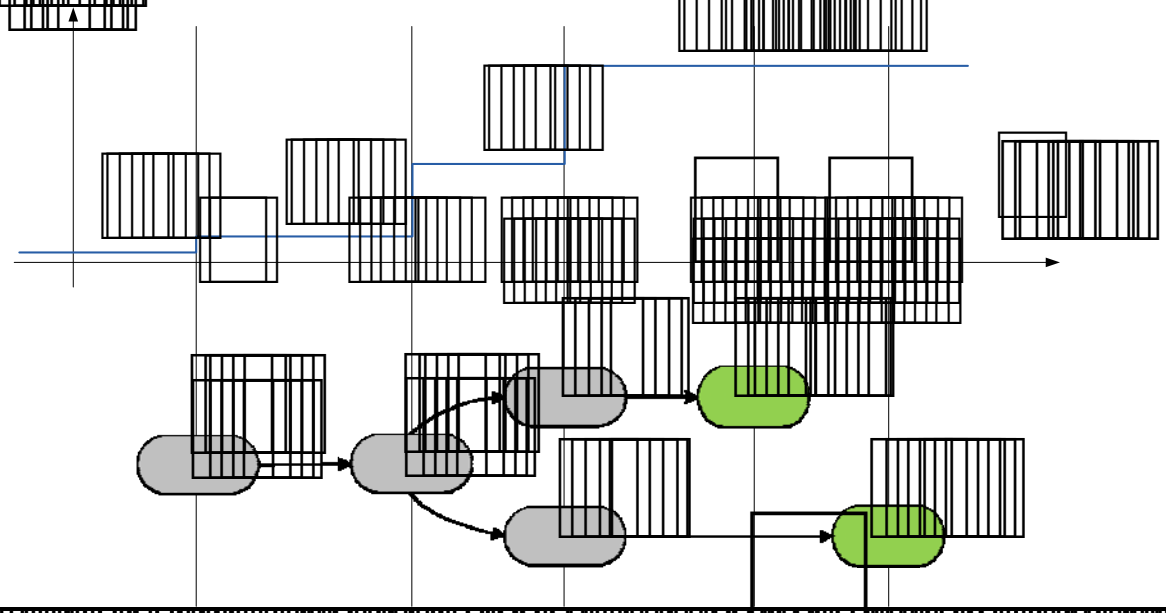


Figure 17. Startup Process

4.2.5.1. Transmitter Startup Time

$$TS\_TR = 5\mu s + 1.25 \times PaRamp + \frac{1}{2} \times Tbit$$

PaRamp *RegPaRamp* *Tbit*

4.2.5.2. Receiver Startup Time

$$TS\_TR = 5\mu s + \frac{1}{2} \times Tbit$$

AfcAutoOn *AfcBw* *RxBw*

Table 68 Receiver Startup Time Summary

RxBw if ***AfcAutoOn=0*** **RxBwAfc** if ***AfcAutoOn=1***	**TS_RE (+/-5%)**

4.2.5.3. Time to RSSI Evaluation

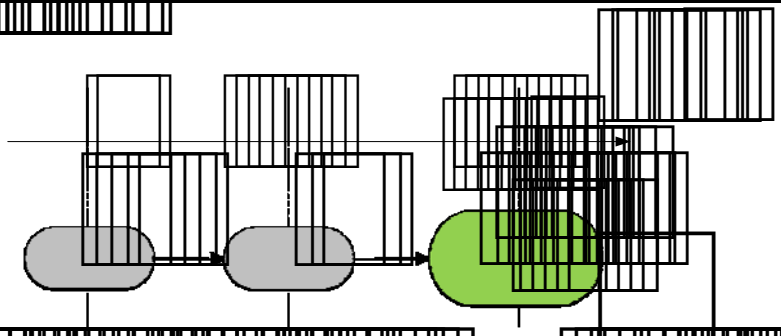


Figure 18. Time to Rssi Sample

RssiSmoothing

4.2.5.4. Tx to Rx Turnaround Time

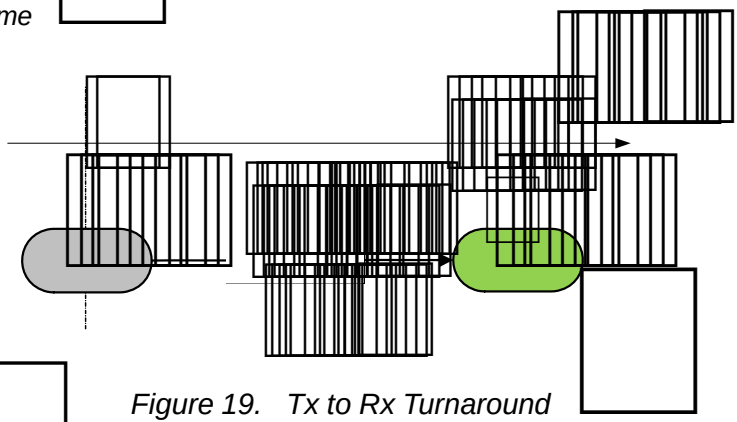


Figure 19. Tx to Rx Turnaround

Note The SPI instruction times are omitted, as they can generally be very small as compared to other timings (up to 10MHz SPI clock).

4.2.5.5. Rx to Tx

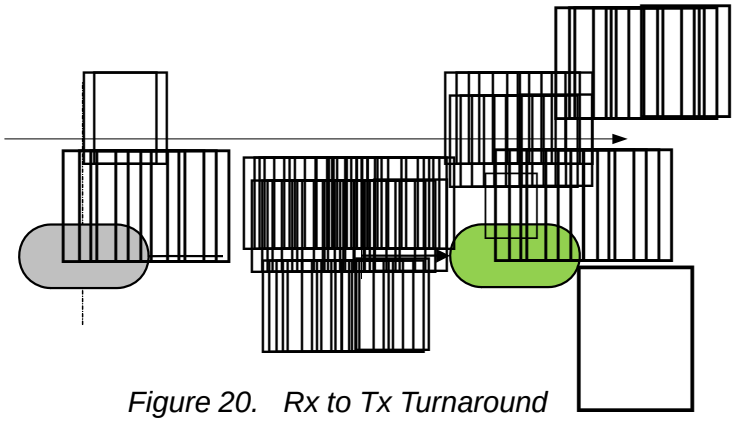


Figure 20. Rx to Tx Turnaround

4.2.5.6. Receiver Hopping Rx to Rx

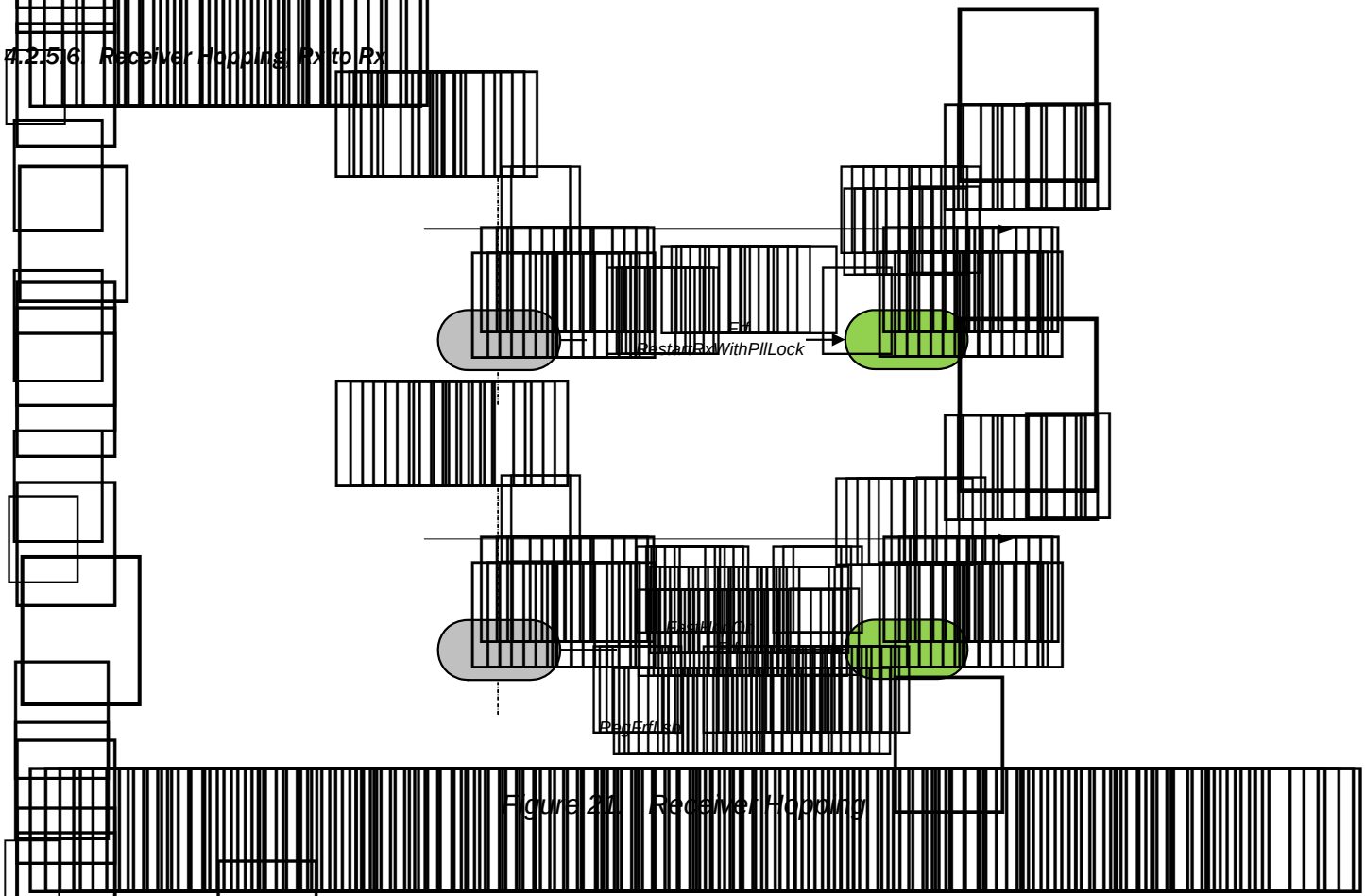


Figure 21. Receiver Hopping

4.2.5.7. Tx to Tx

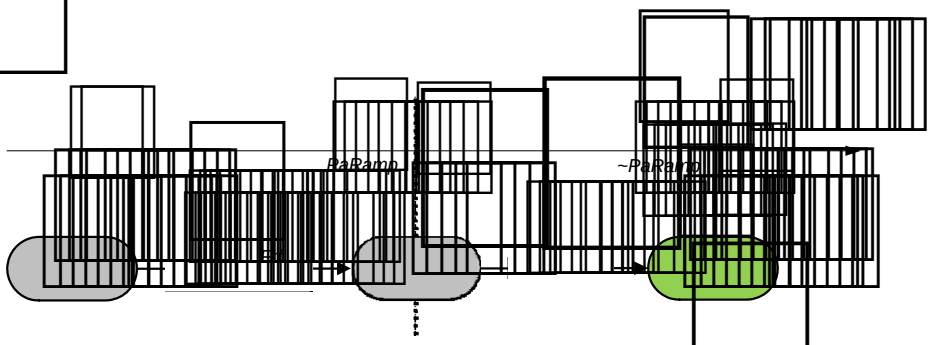


Figure 22. Transmitter Hopping

4.2.6. Receiver Start-up Options

-
- RestartRxWithoutPllLock
- RestartRxWithPllLock
- RestartRxWithPllLock

Table 69 Receiver Startup Options

Triggering Event	Realized Function	AgcAutoOn	AfcAutoOn	RxTrigger (2:0)
Rssi				
PreambleDetect				
Rssi				
PreambleDetect				

AgcAutoOn LnaGain RegLna

4.2.7. Receiver Restart Methods

4.2.7.1. Restart With PLL Lock

- Restart RxWithoutPllLock RegRxConfig
- AfcAutoOn Eff
- RestartRxWithPllLock RegRxConfig

Note: ModeReady must be at logic level 1 for a new RestartRx command to be taken into account.

4.2.7.2. Automatic Restart after manual gain selection

- AutoRestartRxOn
- AutoRestartRxMode
- AutoRestartRxOff

4.2.1.3. Automatic Restart in Rx Mode (Without Waiting for PLL Re-lock)

RestartRxWithoutPllLock

BasicCollisionThreshold *RegRxConfig*

4.2.2. Top Level Sequencer

NOTE THAT THIS FUNCTIONALITY IS ONLY AVAILABLE IN FSK/OOK MODE.

SequencerStart *RegSeqConfig1*

SequencerStop *RegSeqConfig1*

Note : SequencerStart and SequencerStop bits must never be set at the same time.

4.2.2.1. Sequencer States

Table 70 Sequencer States

Sequencer State	Description
SequencerOff State	*SequencerStart* *IdleMode*
Idle State	*Standby* *Sleep* *IdleMode* *RegSeqConfig1*
Transmit State	
Receive State	
PacketReceived	
LowPowerSelection	*LowPowerSelection*
RxTimeout	*TimeoutRxRssi* *TimeoutRxPreamble* *TimeoutSignalSync*

4.2.8.2. Sequencer Transitions

Table 71 Sequencer Transition Options

Variable	Transition
IdleMode	Idle Standby Sleep
FromStart	SequencerStart Sleep Standby LowPowerSelection Receive Transmit
LowPowerSelection	Idle Sleep
FromIdle	Idle T1 Transmit Receive
FromTransmit	Transmit LowPowerSelection Receive
FromReceive	Receive PacketReceived LowPowerSelection SequencerOff T2
FromRxTimeout	Receive RxTimeout PayloadReady FromReceive Transmit LowPowerSelection SequencerOff TimeoutRxRssi TimeoutRxPreamble TimeoutSignalSync
FromPacketReceived	PacketReceived SequencerOff Transmit FifoEmpty LowPowerSelection Receive FS

4.2.9.3. Timer1

T1 T2 SequencerStart

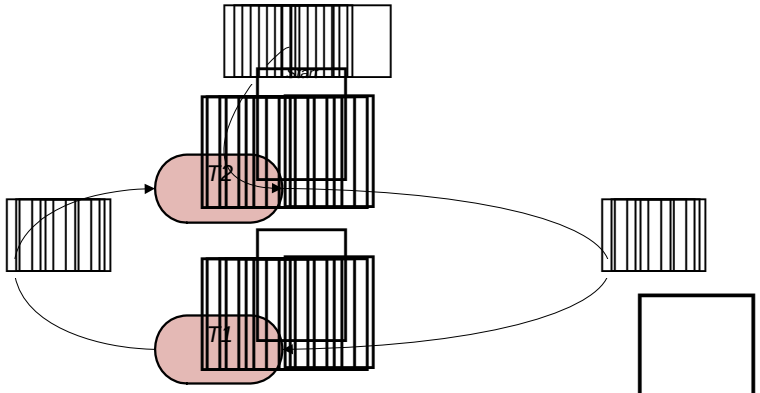


Figure 23. Timer1 and Timer2 Mechanism

Note The timer sequence is completed independently of the actual Sequencer state. Thus, both timers need to be on to achieve periodic cycling.

Table 72 Sequencer Timer Settings

Variable	Description

4.2.8.4. Sequencer State Machine

Stop RegSeqConfig1

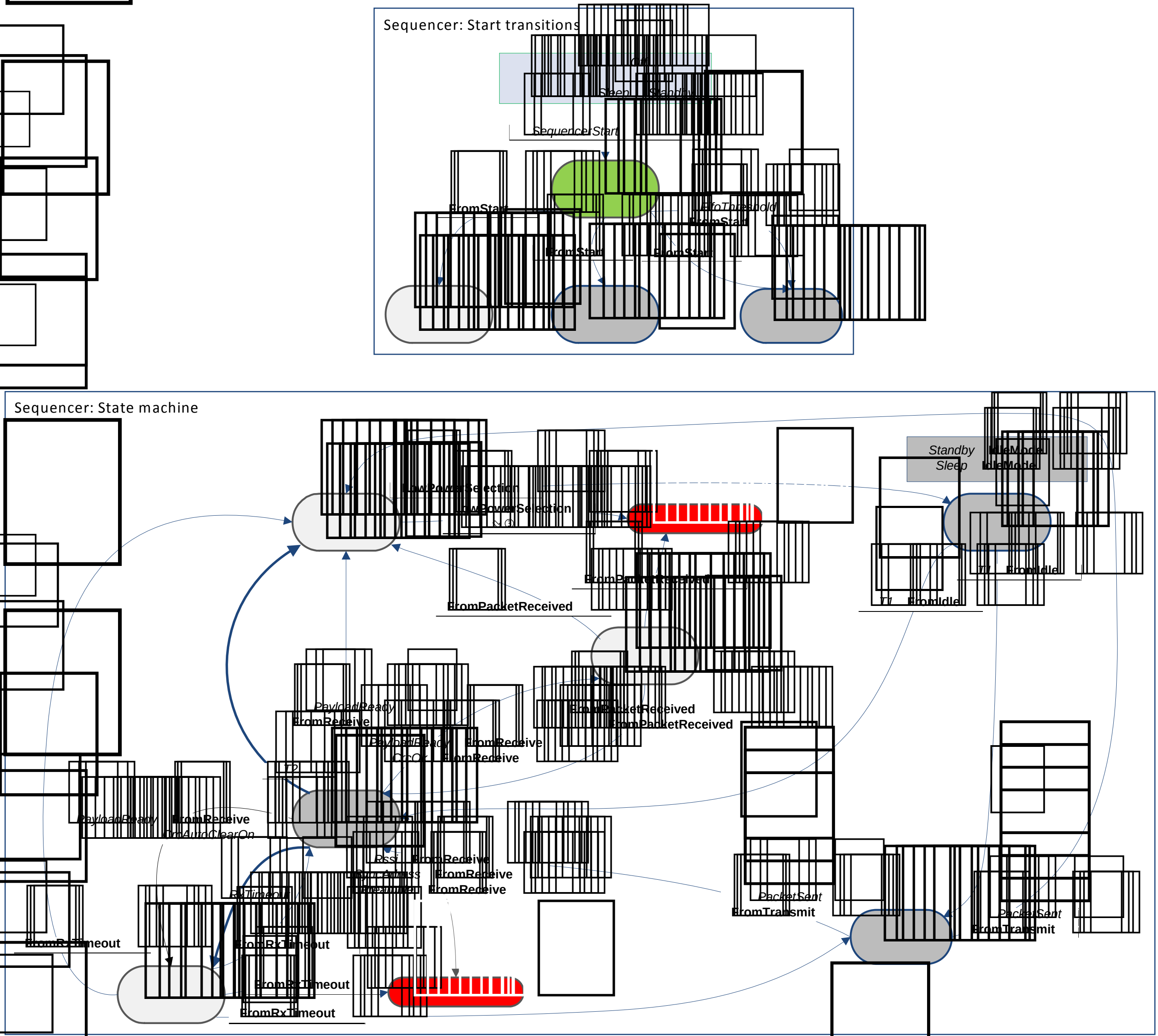


Figure 24. Sequencer State Machine

4.2.9. Data Processing in FSK/OOK Mode

4.2.9.1. Block Diagram

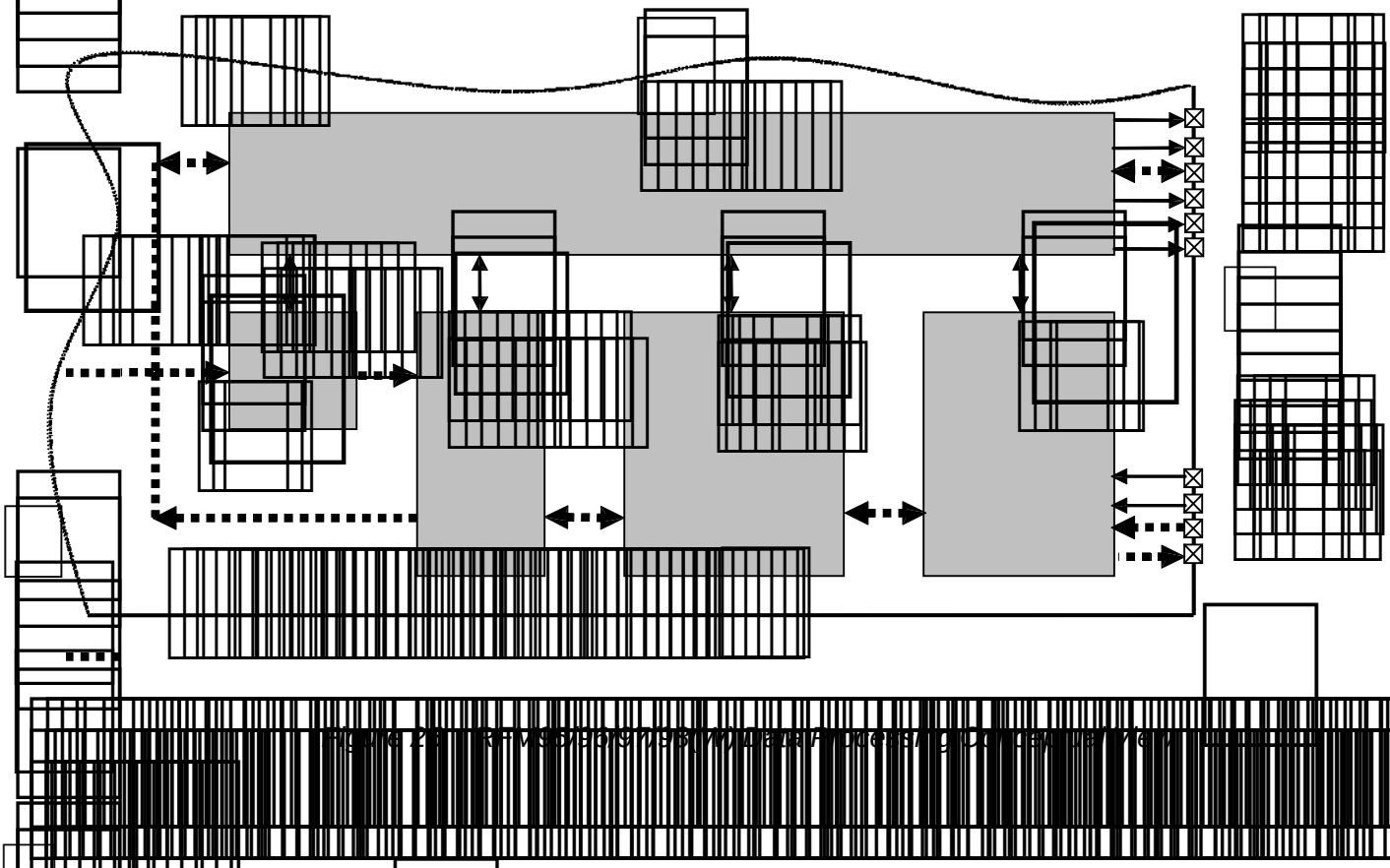


Figure 26 RFM95/96/97/98(W) Data Processing in FSK Mode (Packet Mode)

4.2.9.2. Packet Format

-
-

4.2.10. FIFO

Overview and Shift Register (SR)

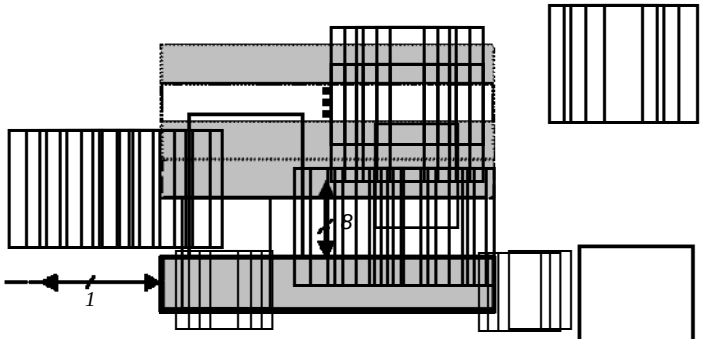
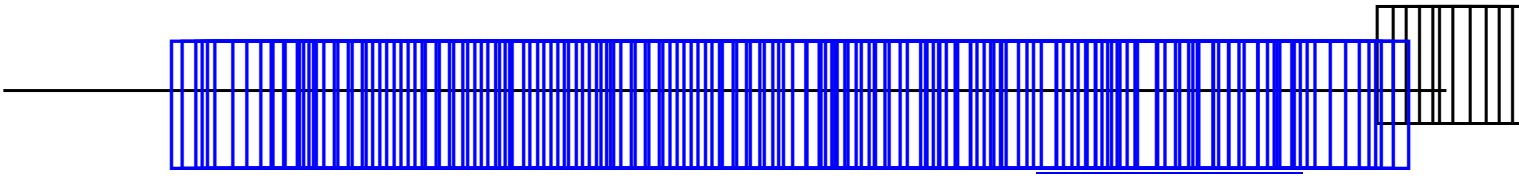


Figure 26. FIFO and Shift Register (SR)

Note – When switching to Sleep mode, the FIFO can only be used once the ModeReady flag is set (quasi immediate from all modes except from Tx).

Interrupt Sources

- *FifoEmpty*
- *FifoFull*
- *FifoOverrun*
- *PacketSent*
- *FifoLevel* *FifoThreshold* *RegFifoThresh*



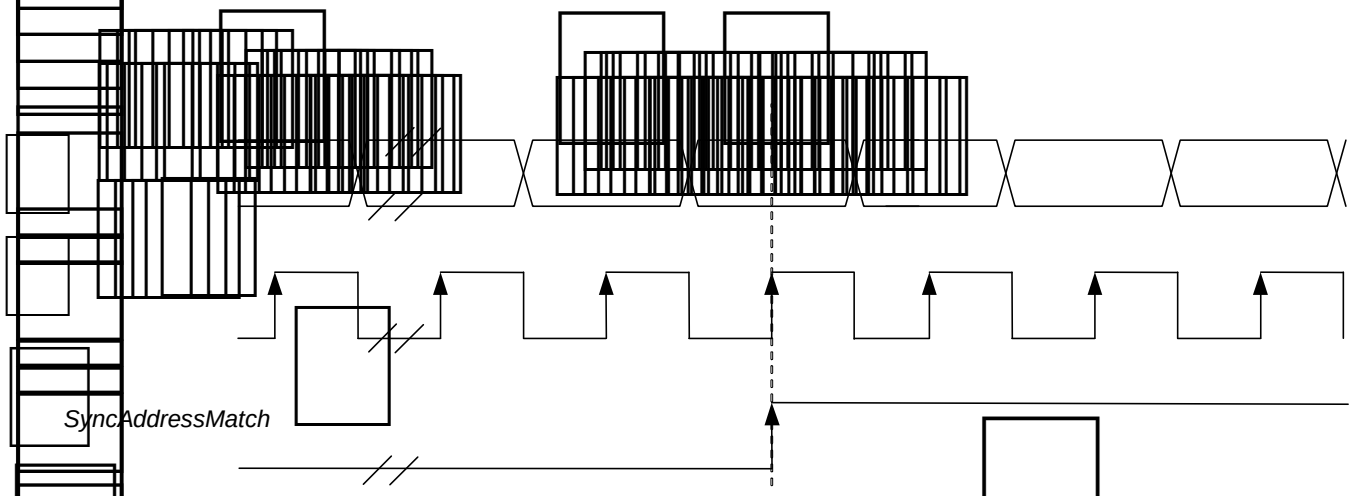


Figure 28 Synchronization Word Detection

RegSyncValue1

SyncAddressMatch

Configuration

- RegSyncConfig
- SyncValue(63:0)

Note: SyncValue choices containing 0x00 bytes are not allowed

Packet Handler

Control

4.2.11. Digital IO Pins Mapping

RegDioMapping1 RegDioMapping2.

Table 74 DIO Mapping, Continuous Mode

DIOx Mapping	Sleep	Standby	FSRx/Tx	Rx	Tx
DIO0					
DIO1					
DIO2					
DIO3					
DIO4					
DIO5					

Table 75 DIO Mapping, Packet Mode

DIOx Mapping	Sleep	Standby	FSRx/Tx	Rx	Tx
DIO0					
DIO1					
DIO2					
DIO3					
DIO4					
DIO5					

4.2.12. Continuous Mode

4.2.12.1. General Description

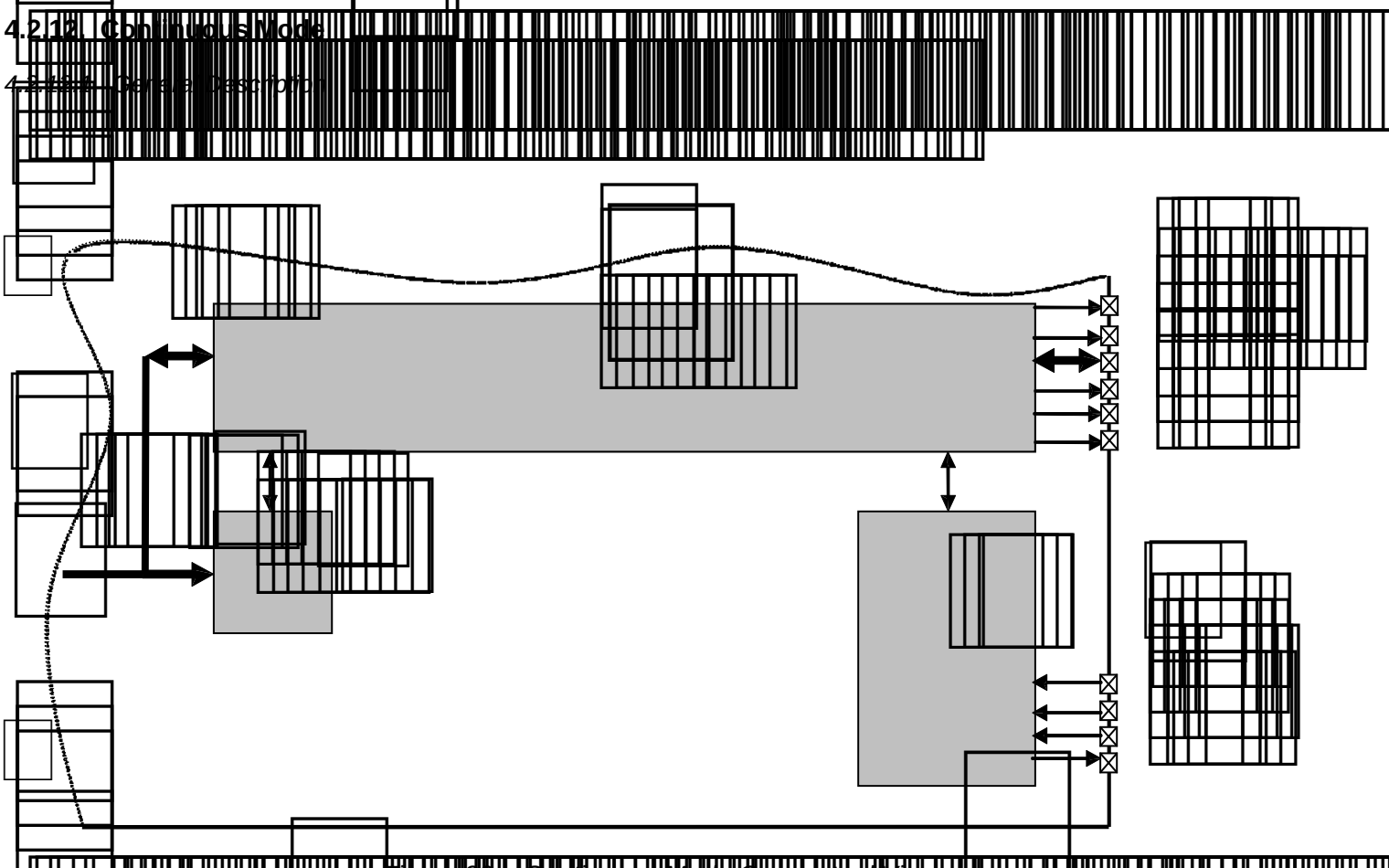


Figure 29. Continuous Mode Conceptual View

4.2.12.2. Tx Processing in Continuous Mode

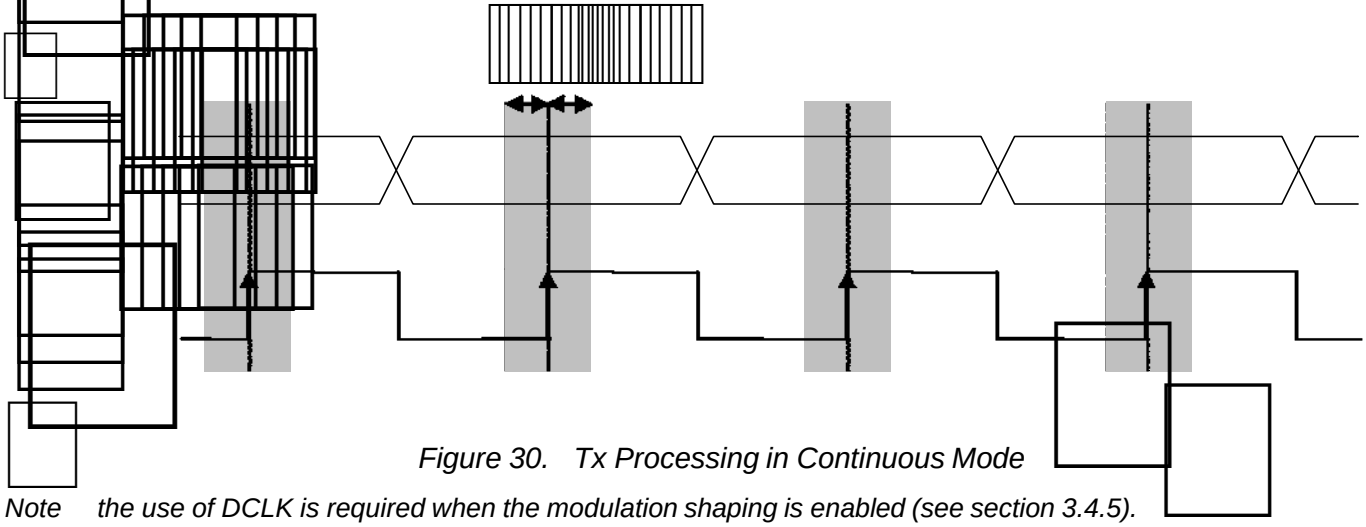


Figure 30. Tx Processing in Continuous Mode

Note the use of DCLK is required when the modulation shaping is enabled (see section 3.4.5).

4.2.12.4. Rx Processing

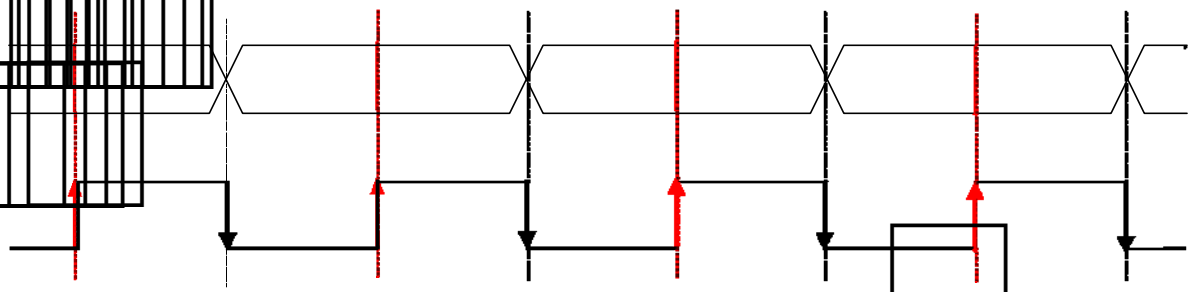


Figure 31. Rx Processing in Continuous Mode

Note In Continuous mode it is always recommended to enable the bit synchronizer to clean the DATA signal even if the DCLK signal is not used by the uC (bit synchronizer is automatically enabled in Packet mode).

4.2.13. Packet Mode

4.2.13.1. General Description

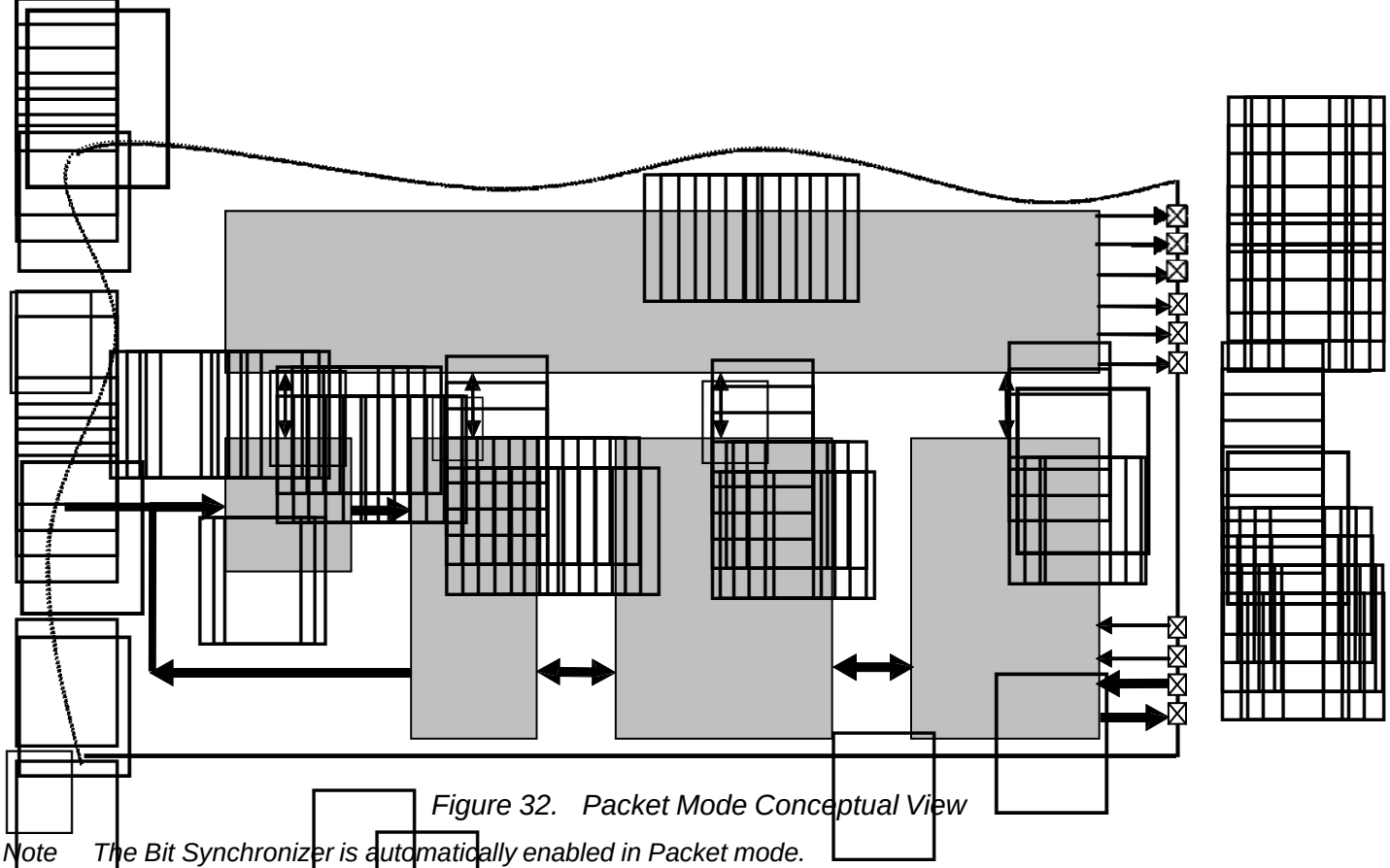


Figure 32. Packet Mode Conceptual View

Note The Bit Synchronizer is automatically enabled in Packet mode.

4.2.1.3.(2) Packet Format

Fixed-length Packet Format

Payload length

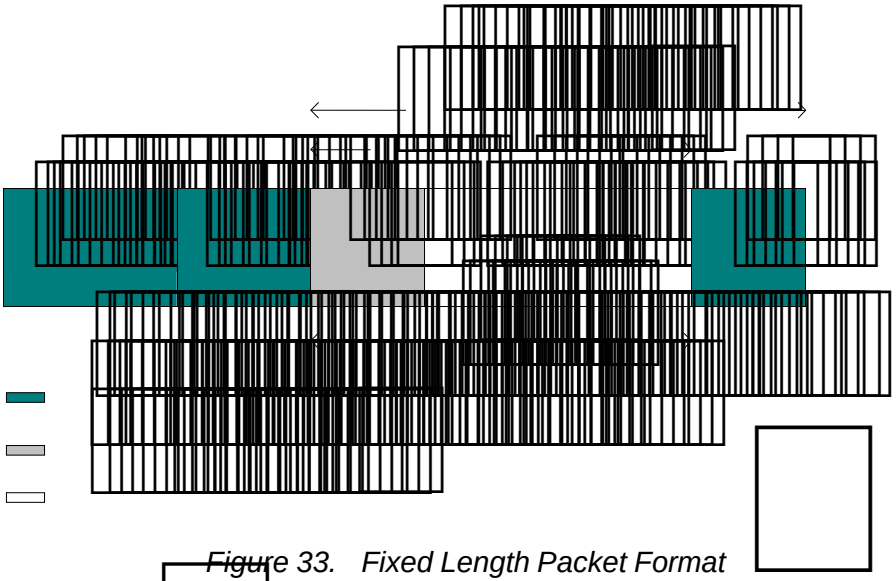


Figure 33. Fixed Length Packet Format

Variable-length Packet Format (Packet Format bit = 1)

-
-
-
-
-

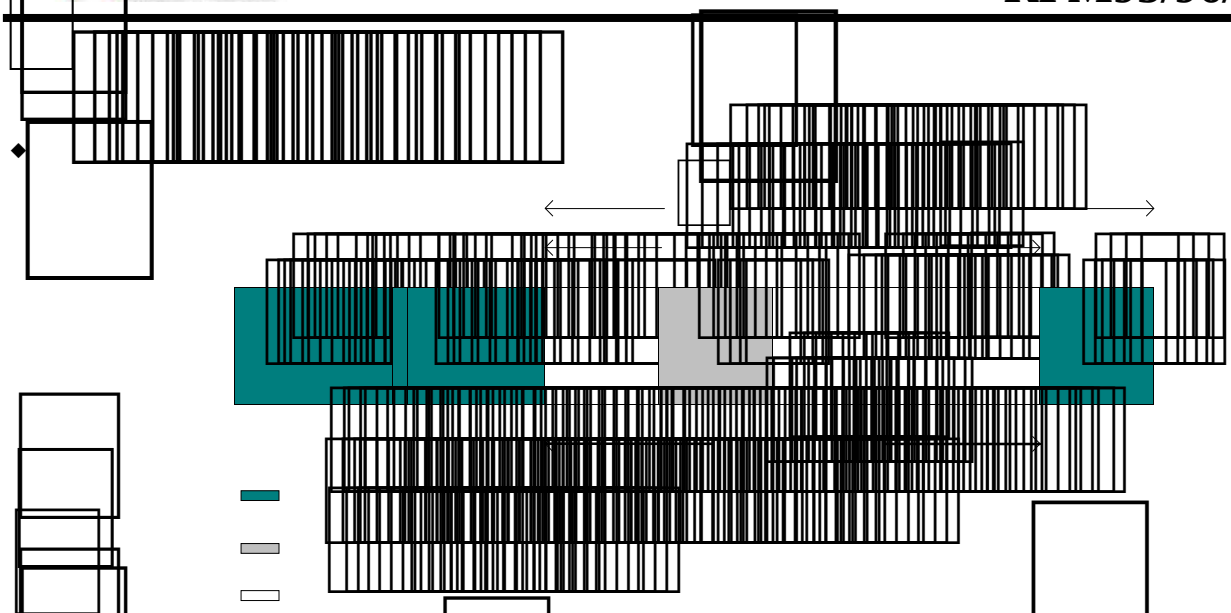


Figure 34. Variable Length Packet Format

Unlimited Length Packet Format (PacketFormat = 1)

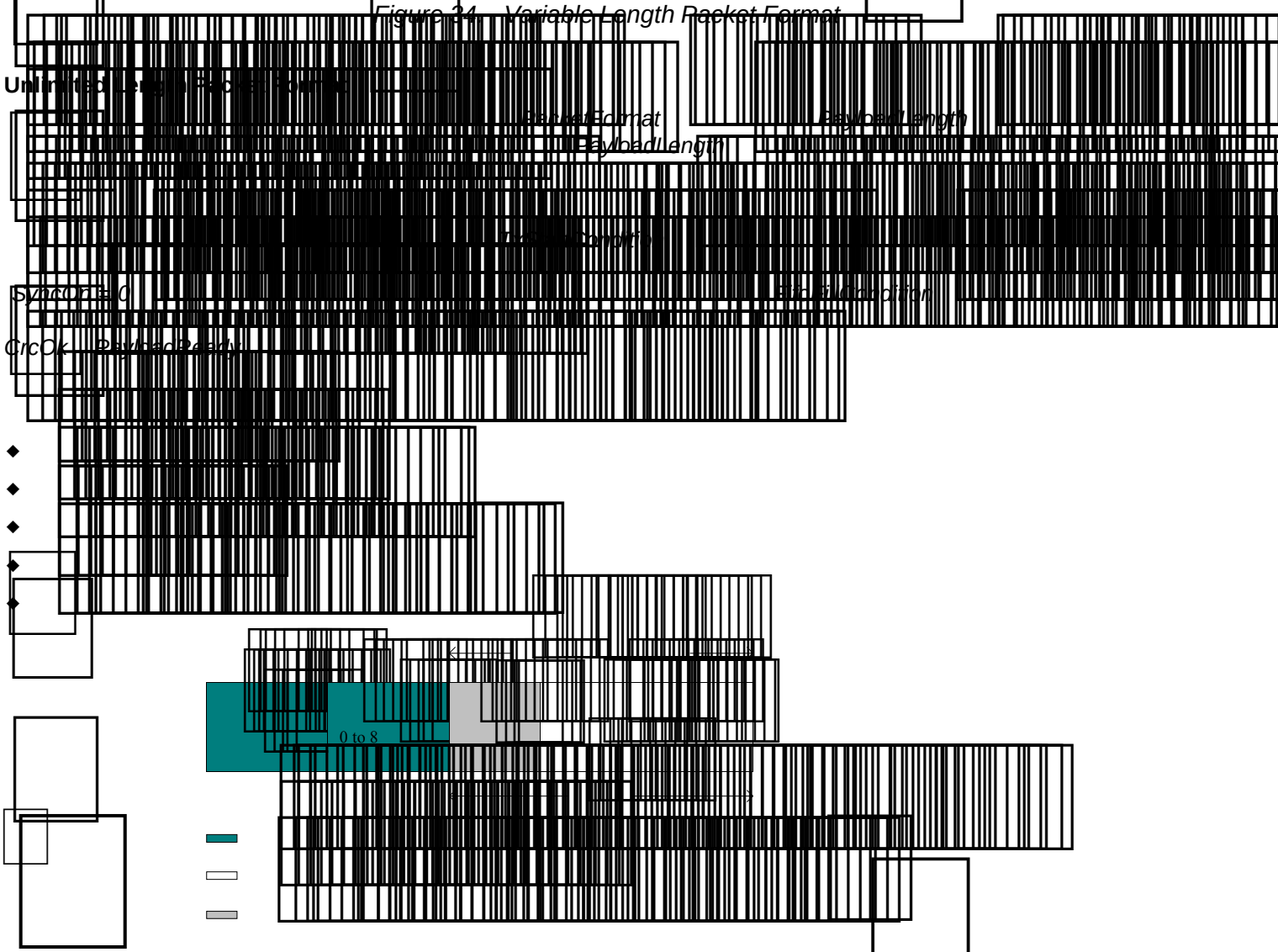
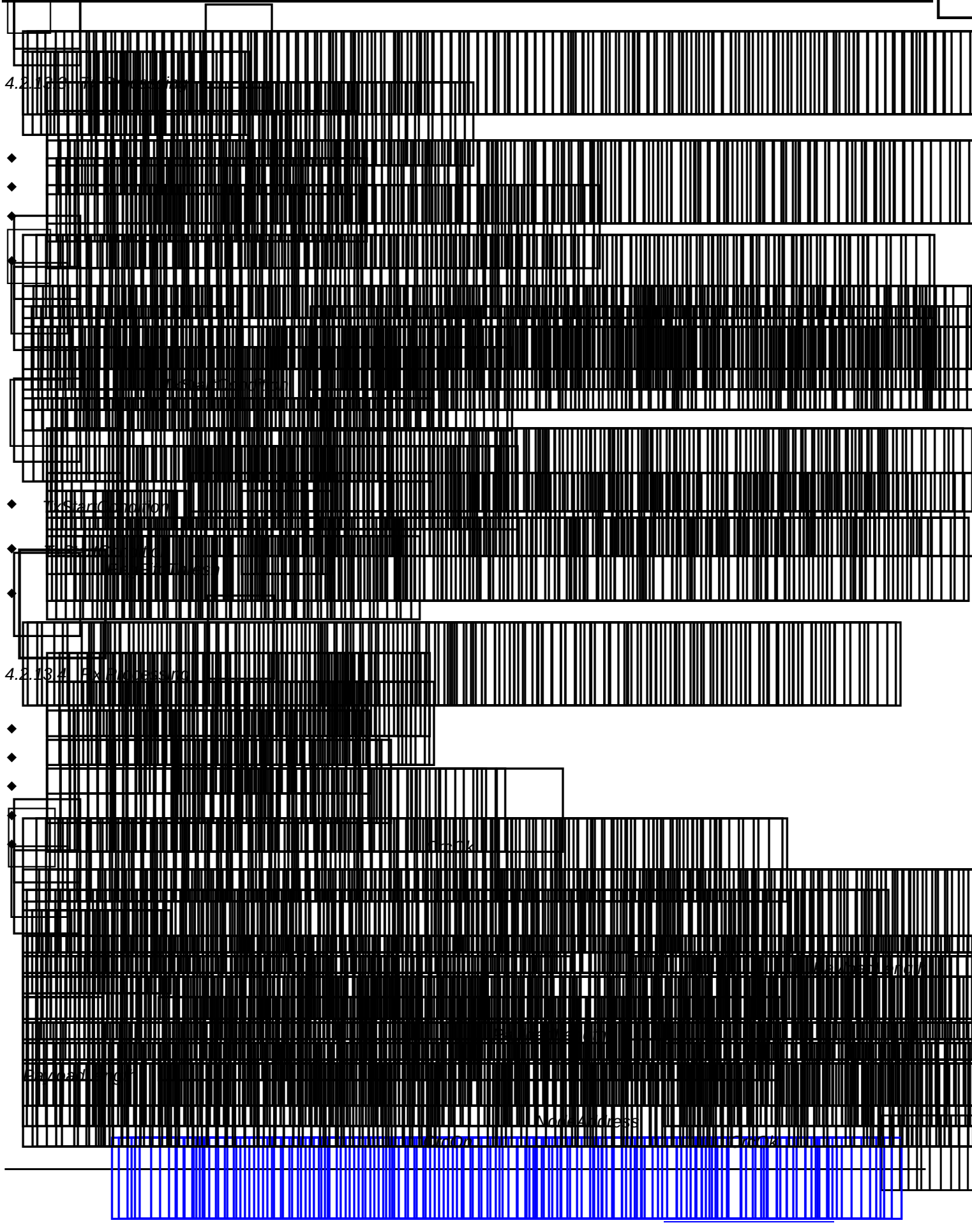


Figure 35. Unlimited Length Packet Format



PayloadReady
CrcAutoClearOff
PayloadReady

4.2.13.5. Handling Large Packets

- FifoFull
- PacketSent
- PayloadReady CrcOk

4.2.14.6. Packet Filtering

Sync Word

SyncAddressMatch

Note Sync Word values containing 0x00 byte(s) are forbidden

Address Based

AddressFiltering

- *AddressFiltering*
- *AddressFiltering*

BroadcastAddress

Length Based

PayloadLength

CRC Based

- *CrcOn*
- *CrcAutoClearOff*

CrcWhiteningType

Table 76 CRC Description

Crc Type	*CrcWhiteningType*	Polynomial	Seed Value	Complemented
CCITT				
IBM				

4.2.13.1. FIFO Data Packaging Methods

Note: Only one of the two methods can be enabled at a time.

Manchester Encoding

Figure 36. Manchester Encoding

Data Whitening

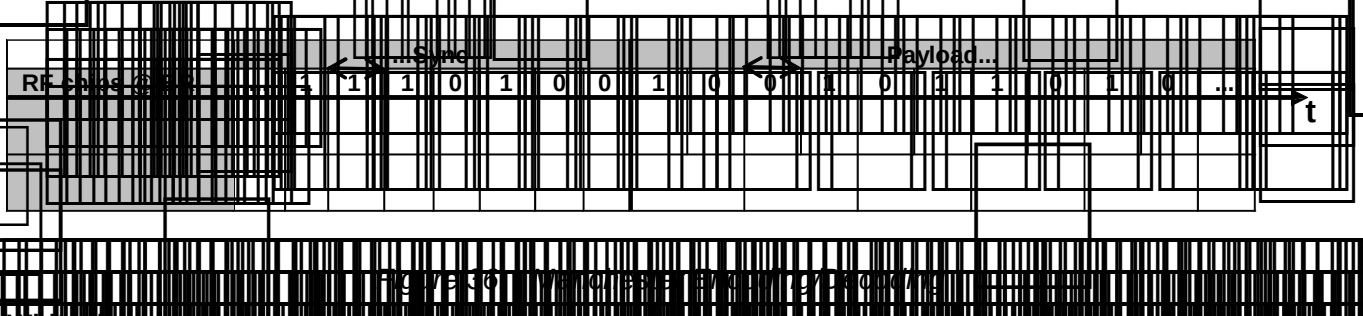


Figure 37. Whitening Packet Structure

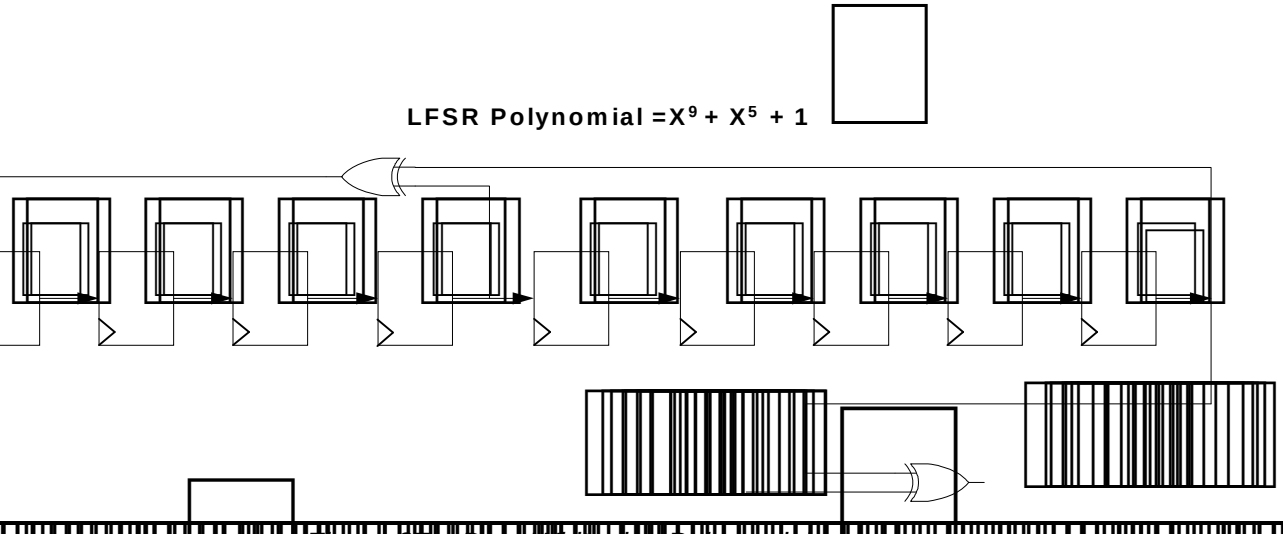


Figure 37. Data Whitening Polynomial

4.2.13.

Register 0x0F FifoRxCurrentAddr

Register 0x10 FifoTxBaseAddr

Register 0x11 FifoRxBaseAddr

RxCodingRate

FifoOverrun

4.2.14. ib-Homecontrol® Compatibility Mode

4.3. SPI Interface

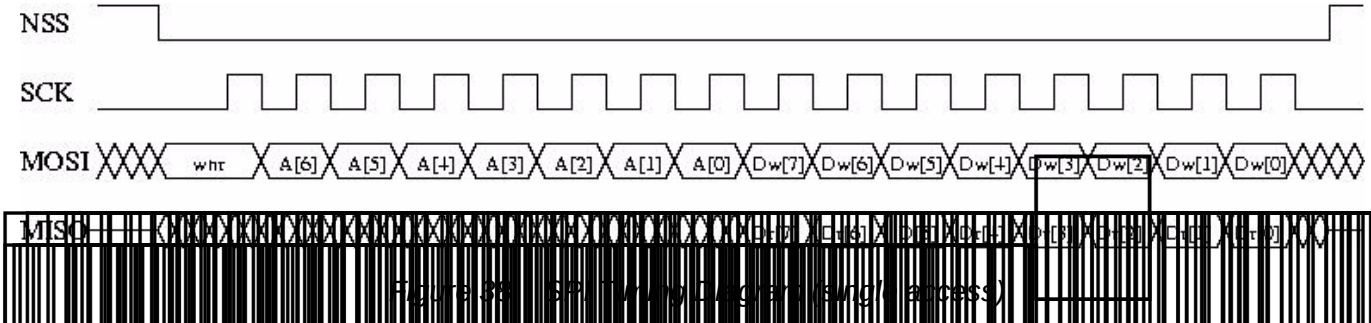


Figure 8: SPI Timing Diagram (single access)

5. RFM95/96/97/98(W) Analog & RF Frontend Electronics

5.1. Power Supply Strategy

5.2. Low Power Strategy

RegLowBat

RegDioMapping

5.3. Frequency Synthesis

5.3.1. Crystal Oscillator

5.3.2. Crystal Oscillator

- [illegible]
- [illegible]

Note *To minimize the current consumption of the RFM95/96/97/98(W), please ensure that the CLKOUT signal is disabled when not required.*

5.3.3. PLL

$$F_{STEP} = \frac{F_{XOSC}}{2^{19}}$$

RegFrf

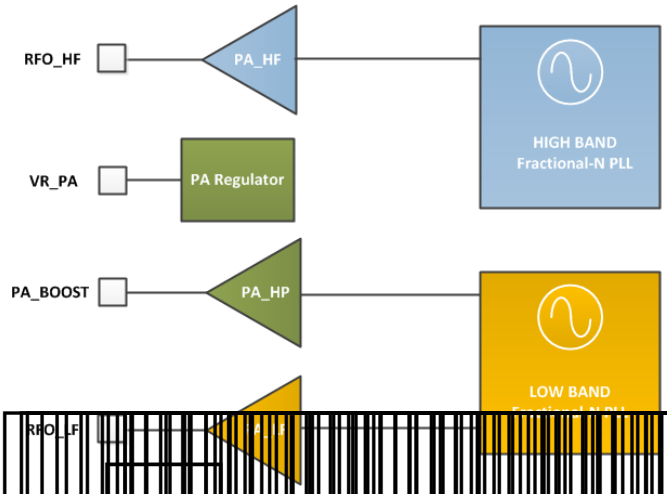
$$F_{RF} = F_{STEP} \times Frf(23,0)$$

Note *The Frf setting is split across 3 bytes. A change in the center frequency will only be taken into account when the least significant byte FrfLsb in RegFrfLsb is written. This allows the potential for user generation of m-ary FSK at very low bit rates. This is possible where frequency modulation is achieved by direct programming of the programmed RF centre frequency. To enable this functionality set the FastHopOn bit of register RegPllHop.*

5.3.4. RC Oscillator

5.4. Transmitter Description

5.4.1. Architecture Description



5.4.2. RF Power Amplifiers

Table 77 Power Amplifier Mode Selection Truth Table

PaSelect	Mode	Power Range	Pout Formula

Notes - For +20 dBm restrictions on operation please consult the following section.

- To ensure correct operation at the highest power levels ensure that the current limiter OcpTrim is adjusted to permit delivery of the requisite supply current.

- If the PA_BOOST pin is not used it may be left floating.

5.4.3. High Power +20 dBm Operation

Table 78 High Power Settings

Register	Address	Value for High Power	Default value PA_HF/LF or +17dBm	Description
RegPaDac				

Notes - High Power settings must be turned off when using PA_LF or PA_HF
- Over Current Protection limit should be adapted to the actual power level, in RegOcp

Table 79 Operating Range, +20dBm Operation

Symbol	Description	Min	Max	Unit

Table 80 Operating Range, +20dBm Operation

Symbol	Description	Min	Max	Unit

5.4.4. Overcurrent Protection

OcpTrim	RegOcp

Table 81 Trimming of the OCP Current

OcpTrim	I_{MAX}	Imax Formula
		OcpTrim
		OcpTrim
		240 mA

Note Imax sets a limit on the current drain of the Power Amplifier only, hence the maximum current drain of the is equal to Imax + I_{FS}

5.5. Receiver Description

5.5.1. Overview

5.5.2. Receiver Chain

5.5.6. Automatic Gain Control in FSK/OOK Mode

Table 82 LNA Gain Control and Performances

RX input level (Pin)	*Gain Setting*	*LnaGain*	*Relative LNA Gain [dB]*	NF Lower/Higher band [dB]	IIP3 Lower/Higher band [dBm]
Pin <= AgcThresh1					
AgcThresh1 < Pin <= AgcThresh2					
AgcThresh2 < Pin <= AgcThresh3					
AgcThresh3 < Pin <= AgcThresh4					
AgcThresh4 < Pin <= AgcThresh5					
AgcThresh5 < Pin					

5.5.4. RSSI

RssiValue

RssiOffset

$$RSSI\,[dBm] = -\frac{RssiValue}{2} \quad (RssiSmoothing)$$

RssiSmoothing

Table 83 RssiSmoothing Options

RssiSmoothing	Number of Samples	Estimated Accuracy	Response Time
			$\frac{2^{(RssiSmoothing+1)}}{4 \cdot RxBw[kHz]}[ms]$

5.5.5. RSSI in LoRa™ Mode

LoRa™

$$RSSI[dBm] = -137 + RSSI$$

5.5.6. Channel Activity Detection

Note Te respect sampling criterion in the decimation chain of the receiver, the communication bit rate cannot be set at a higher than twice the single sided receiver bandwidth (BitRate < 2 x RxBw)

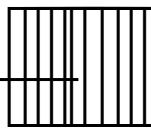
RxBw RxBwMant

RxBwExp RegRxBw

$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{(RxBwExp+2)}}$$

Table 84 Available RxBw Settings

RxBwMant (binary value)	RxBwExp (decimal)	RxBw (kHz) FSK / OOK



6. Description of the Registers

LoRa™

6.1. Register Table Summary

Table 85 Registers Summary

Address	Register Name		Reset (POR)	Default (FSK)	Description	
	FSK/OOK Mode	LoRa™ Mode			FSK/OOK Mode	LoRa™ Mode
						LoRa™
						LoRa™

Address	Register Name		Reset (POR)	Default (FSK)	Description	
	FSK/OOK Mode	LoRa^{TM} Mode			FSK Mode	LoRa^{TM} Mode
					Pay-	LoRa^{TM}
					loadReady	
					dress	
						LoRa^{TM}

Address	Register Name		Reset (POR)	Default (FSK)	Description	
	FSK/OOK Mode	LoRa™ Mode			FSK/OOK Mode	LoRa™ Mode

Note - Reset values are automatically refreshed in the chip at Power On Reset

- Default values are the Hope RF recommended register values, optimizing the device operation

*- Registers for which the Default value differs from the Reset value are denoted by a * in the tables of section 6.2*

6.2. FSK/OOK Mode Register Map

Table 86 Register Map

Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description

$$BitRate = \frac{FXOSC}{BitRate(15:0) + \frac{BitrateFrac}{16}}$$

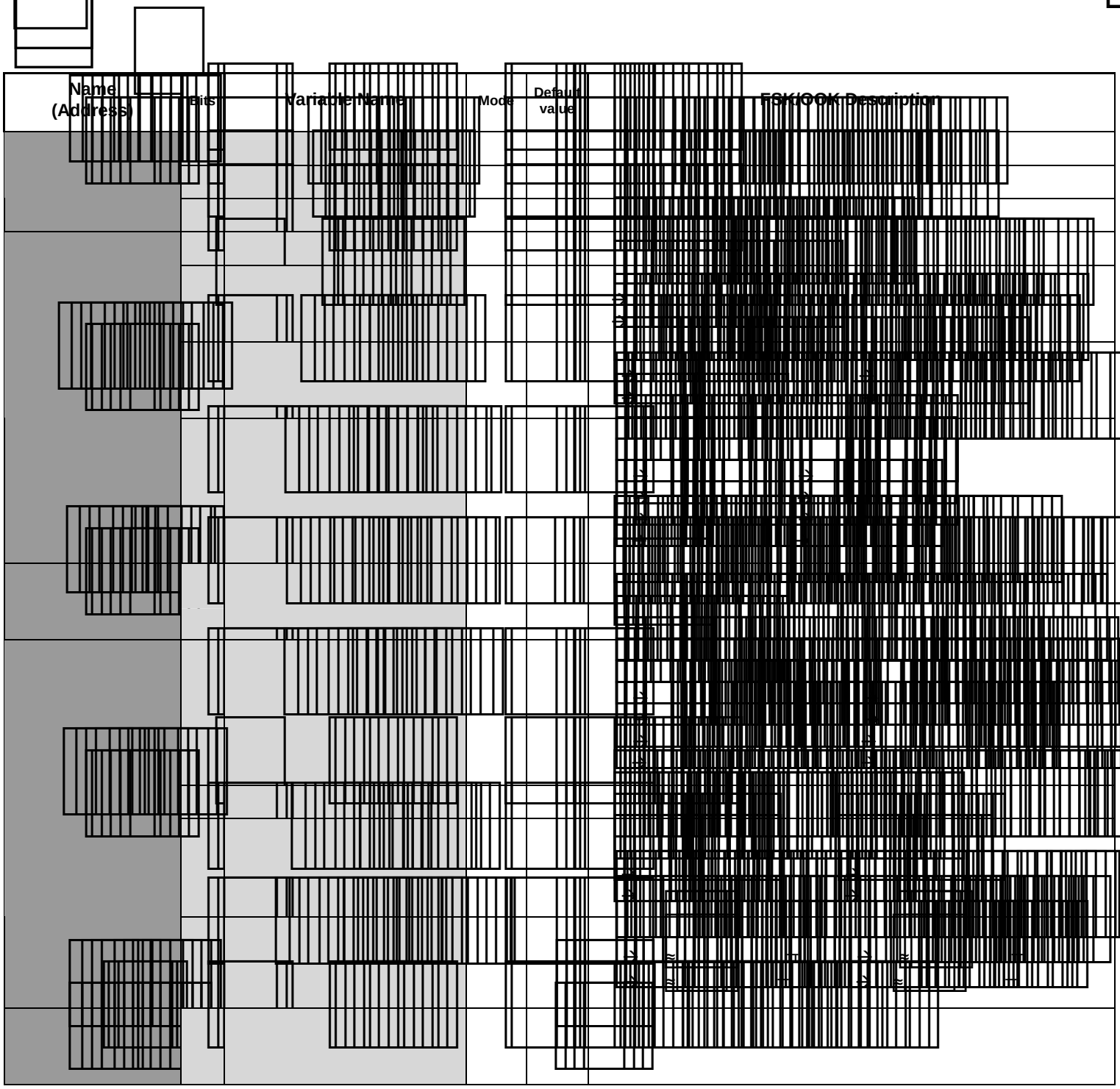
$$Fdev = Fstep \times Fdev(15:0)$$

Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description
					$Frf = FRF[23:0] \times F_{XOSC} / 2^{19}$

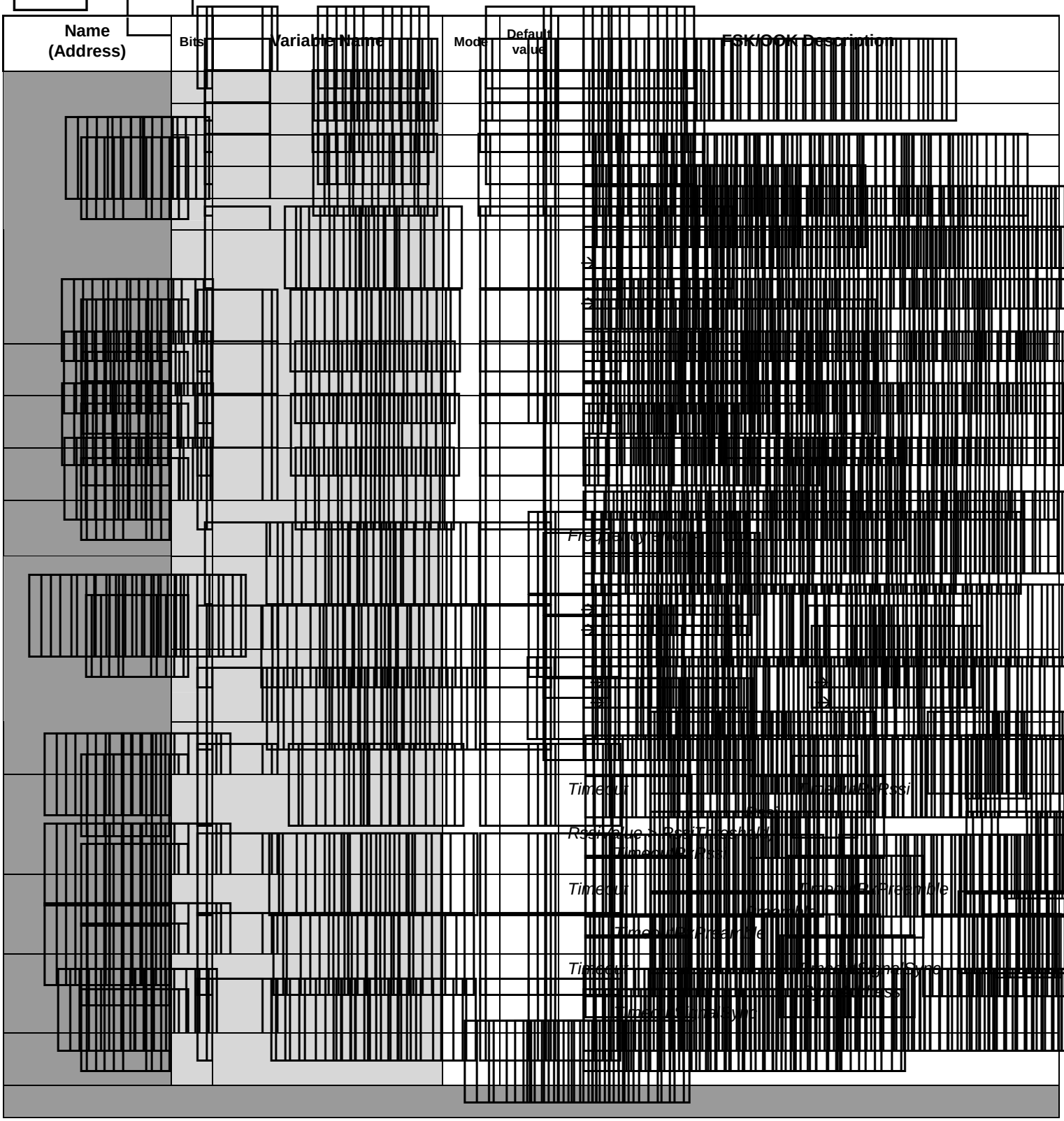
Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description

Name (Address)	Bits	Variable Name	Mode	Default value	Description

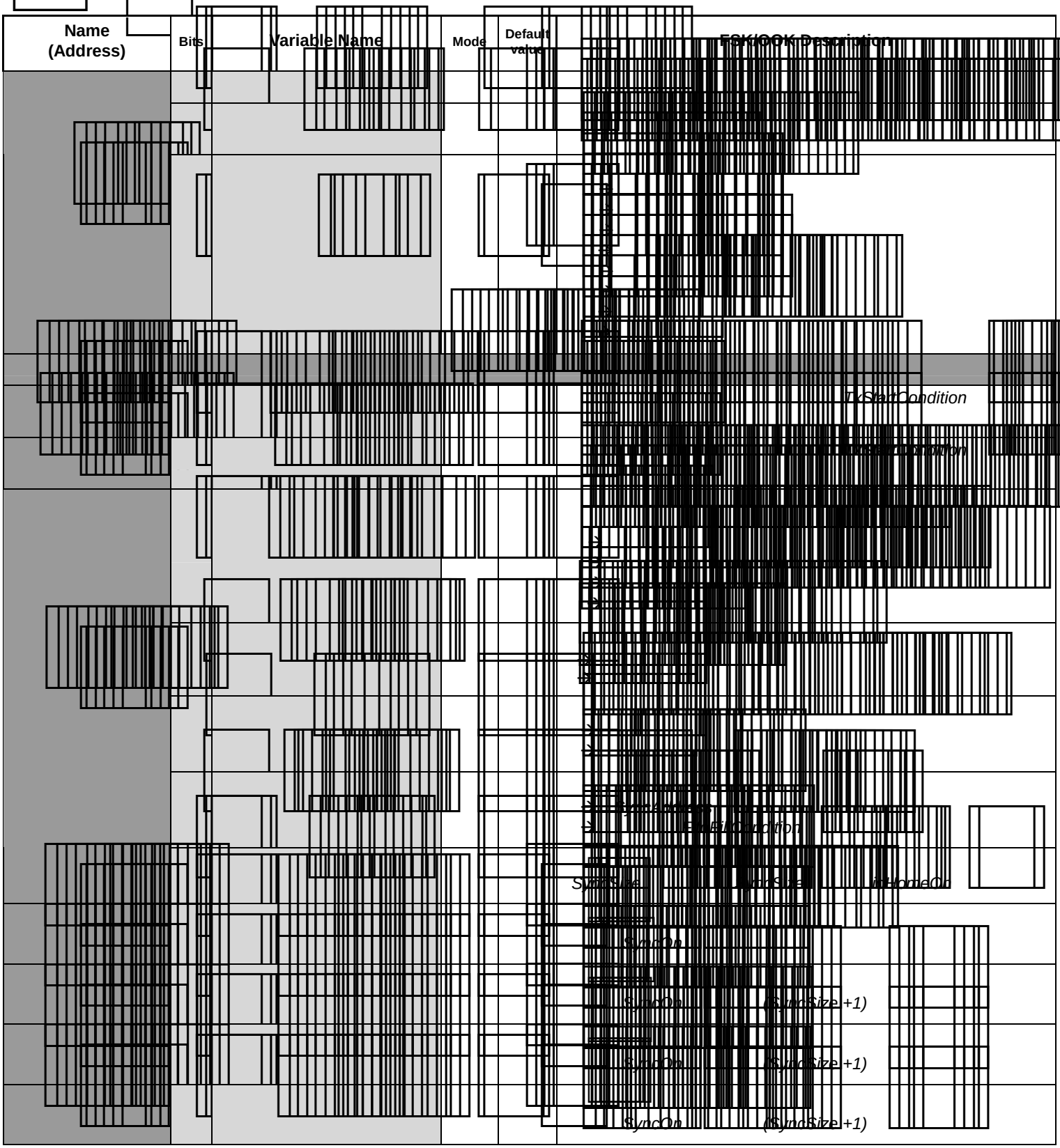
$$RxBw = \frac{FXOSC}{RxBwMant \times 2^{RxBwExp+2}}$$


Name (Address)
Bits
Variable Name
Mode
Default value
FSK/OOK Description

Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description



Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description

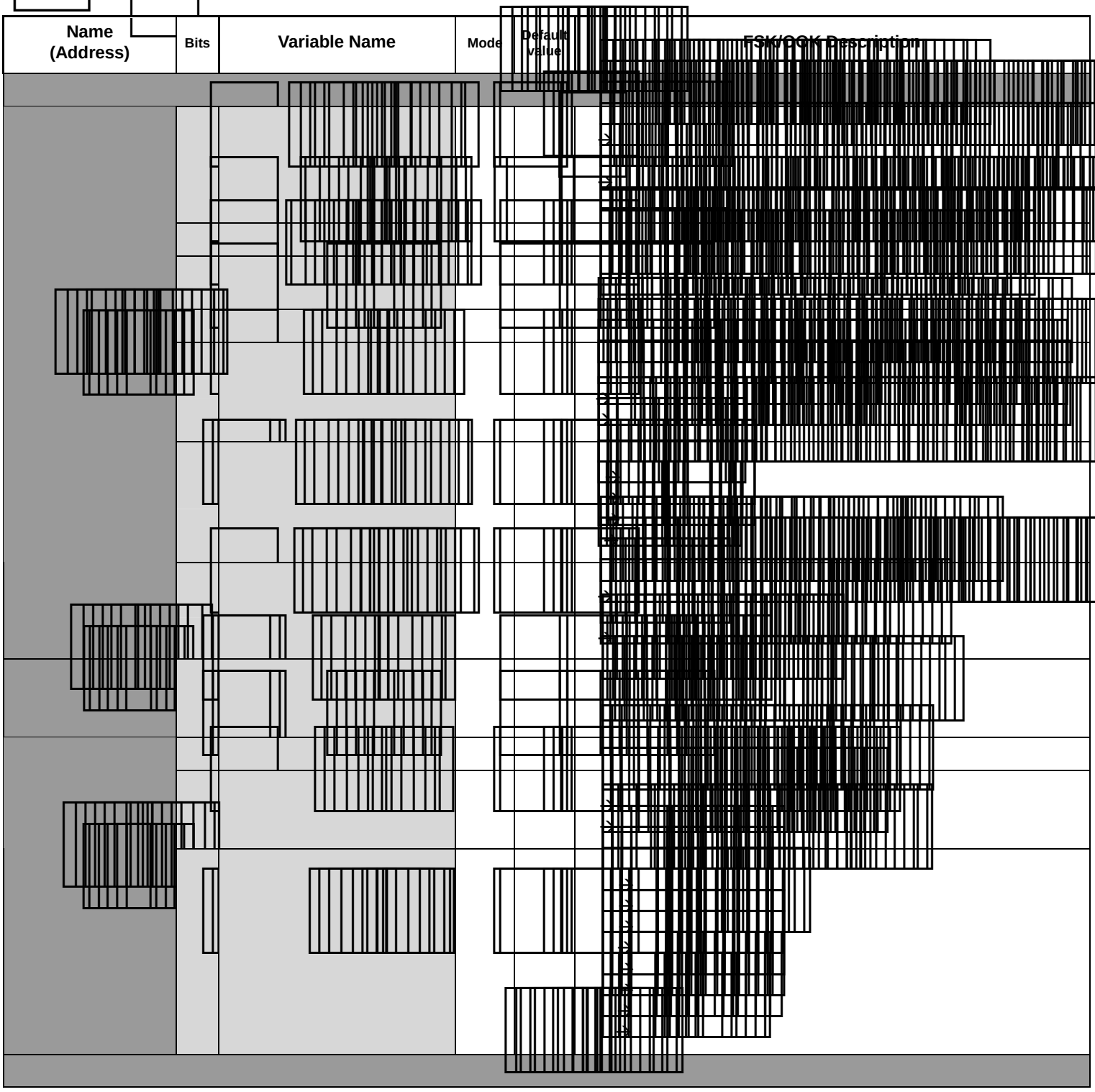


Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description
					SyncOn *(SyncSize +1)*
					SyncOn *(SyncSize +1)*
					SyncOn *(SyncSize +1)*
					SyncOn *(SyncSize +1)*
					PayloadReady *(PayloadLength)*
					NodeAddress
					NodeAddress
					BroadcastAddress

Name (Address)	Bits	Variable Name	Mode	Default value	PSK/OOK Description
					à (first part EirqThreshold)
					SequencerStart
					LowPowerSelect
					Standby *Sleep*
					IdleMode
					Note: mid mode is the chip LowPower mode at *Sequencer Start*
					PacketSent
					PacketSent

Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description
					PayloadReady PayloadReady CrcOk Rssi SyncAddress PreambleDetect CrcAutoClearOff ... PayloadReady
					RxTimeout ... PayloadReady Note: RxTimeout interrupt is a TimeoutRxRssi, TimeoutRxPreamble or TimeoutSignalSync interrupt

Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description



Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description
					Mode
	2				
					Filter bandwidth control during reception

Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible] PreambleDetect
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	→ Rssi → PreambleDetect
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible] TempValue [illegible] RegTemp [illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	BitRateFrac [illegible] $$BitRate = \frac{FXOSC}{BitRate(15,0) + \frac{BitrateFrac}{16}}$$

Name (Address)	Bits	Variable Name	Mode	Default value	FSK/OOK Description
	5				
	4:0				*AgcReferenceLevel*

6.3. [illegible]

Table 87 Low Frequency Additional Registers

Name (Address)	Bits	Variable Name	Mode	Default value	Low Frequency Additional Registers
	5				
	4:0				*AgcReferenceLevel*

Table 88 High Frequency Additional Registers

Name (Address)	Bits	Variable Name	Mode	Default value	Low Frequency Additional Registers
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	*RxBw* *AgcReferenceLevel*

6.4. LoRa™ Mode Register Map

Name (Address)	Bits	Variable Name	Mode	Reset	Data Description
LoRa™					

Name (Address)	Bits	Variable Name	Mode	Reset	LoRa[TM] Description
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
[illegible]	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]
	[illegible]	[illegible]	[illegible]	[illegible]	[illegible]

Name (Address)	Bits	Variable Name	Mode	Reset	LoRaTM Description
Lora					

Name (Address)	Bits	Variable Name	Mode	Reset	LoRa™ Description

$$SNR[dB] = \frac{Packet\ Snr[twos\ com\ plimen\ t]}{4}$$

Name (Address)	Bits	Variable Name	Mode	Reset	LoRa[TM] Description
					$RSSI[dBm] = -137 + PacketRssi$
					$RSSI[dBm] = -137 + Rssi$

Name (Address)	Bits	Variable Name	Mode	Reset	R/W Description

7. Application Information

7.1. Crystal Resonator Specification

Table 89 Crystal Specification

Symbol	Description	Conditions	Min	Typ	Max	Unit

Notes - the initial frequency tolerance, temperature stability and ageing performance should be chosen in accordance with the target operating temperature range and the receiver bandwidth selected.

- the loading capacitance should be applied externally, and adapted to the actual Cload specification of the XTAL.

7.2. Reset of the Chip

7.2.1. POR

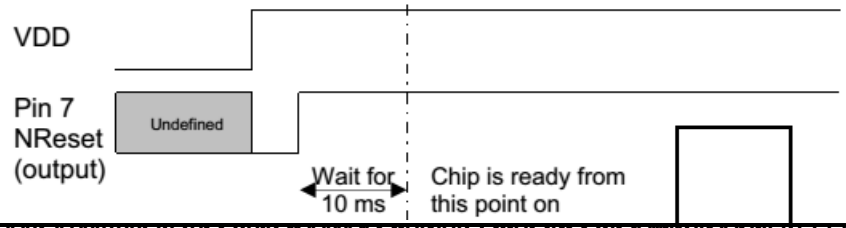


Figure 42. POR Timing Diagram

7.2.2. Manual Reset

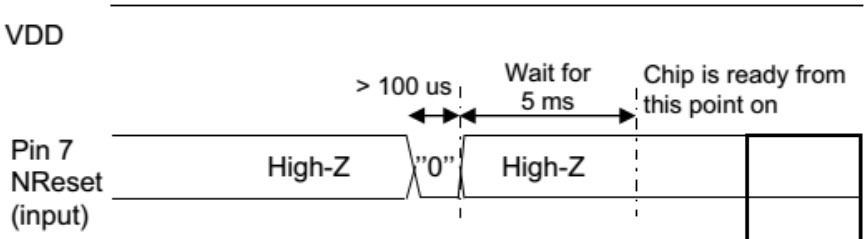


Figure 43. Manual Reset Timing Diagram

Note whilst pin 7 is driven low, an over current consumption of up to one milliampere can be seen on VDD.

7.3. [illegible]

7.3.1.1 Rx Packet Handling

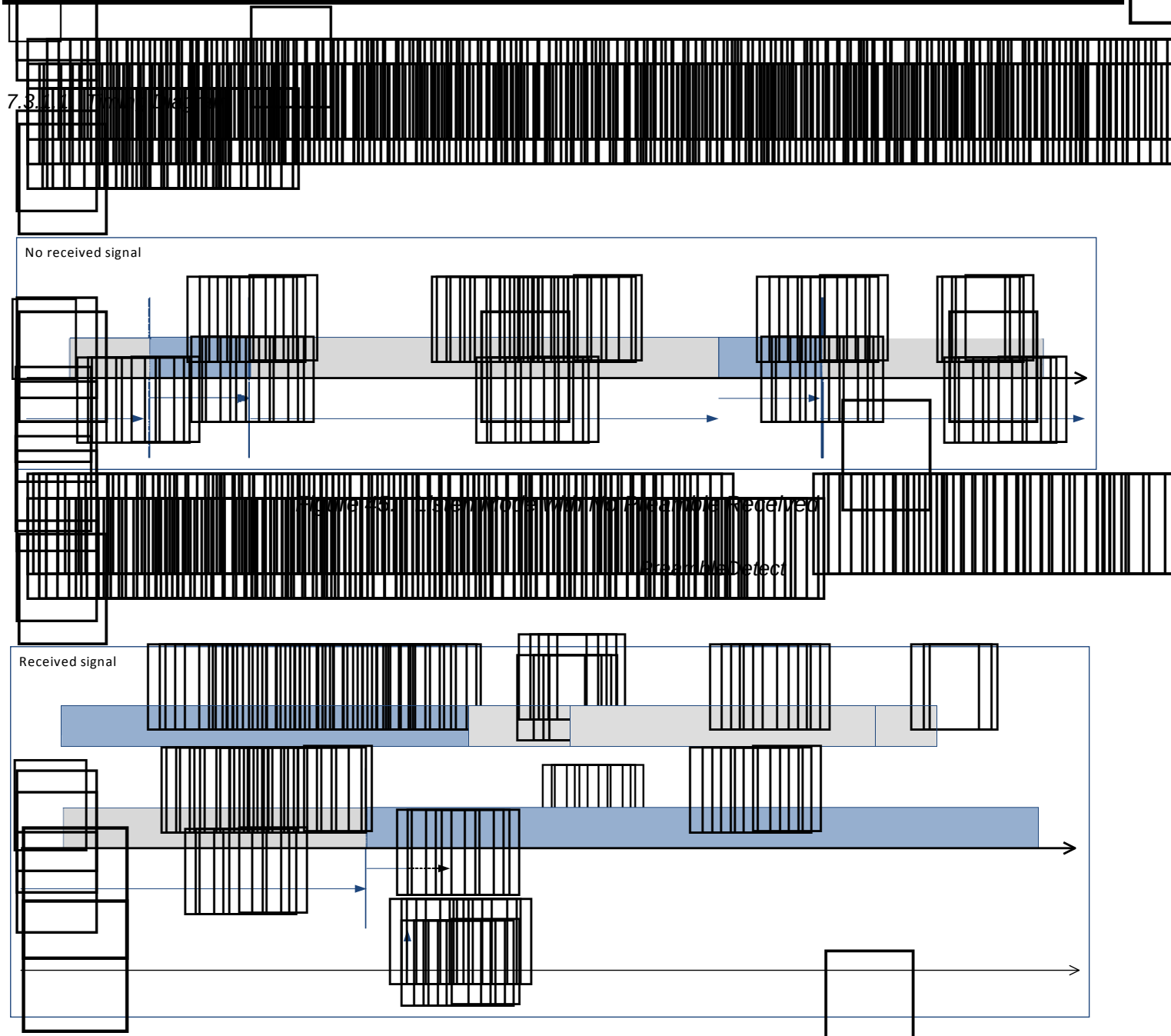
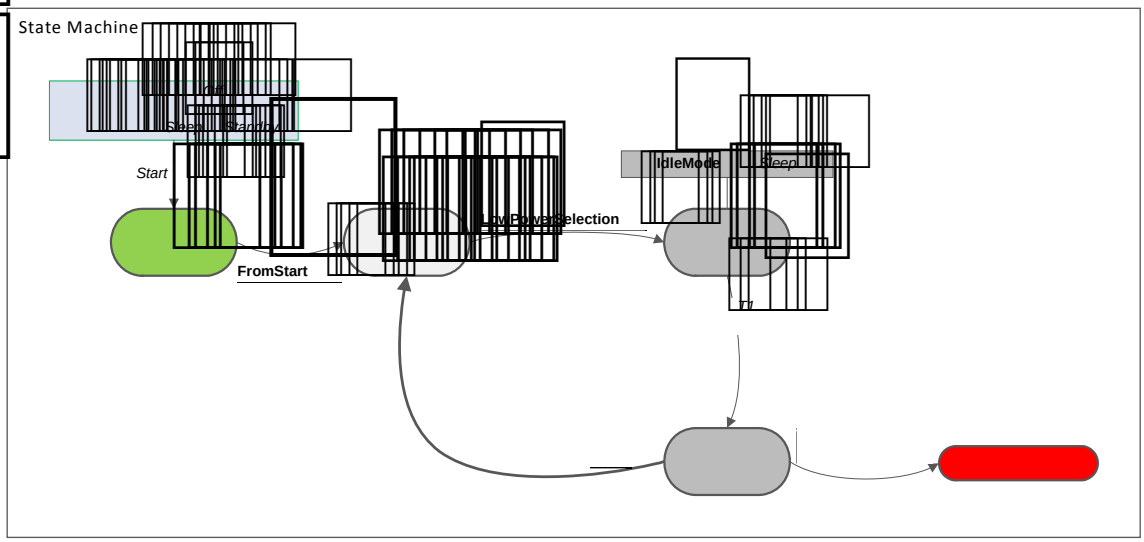


Figure 45. Listen Mode with Preamble Received

Figure 46. Listen Mode with Preamble Received

7.3.1.2. Sequencer Configuration

PreambleDetect



7.3.2. Wake on SyncAddress Mode

SyncAddress

7.3.2.1. Timing Sequence

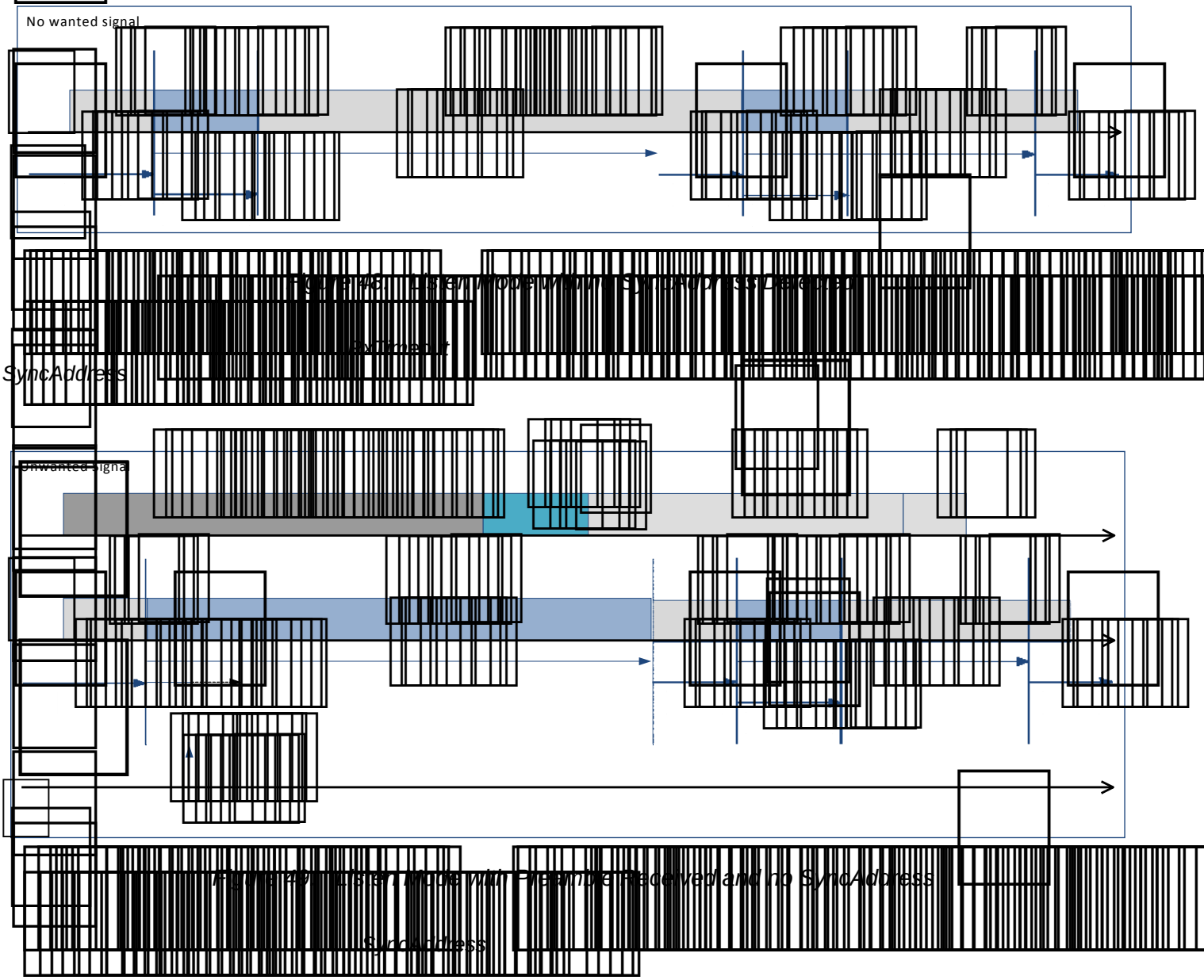


Figure 14. Listen Mode with SyncAddress Detected

Figure 15. Listen Mode with Preamble Received and no SyncAddress

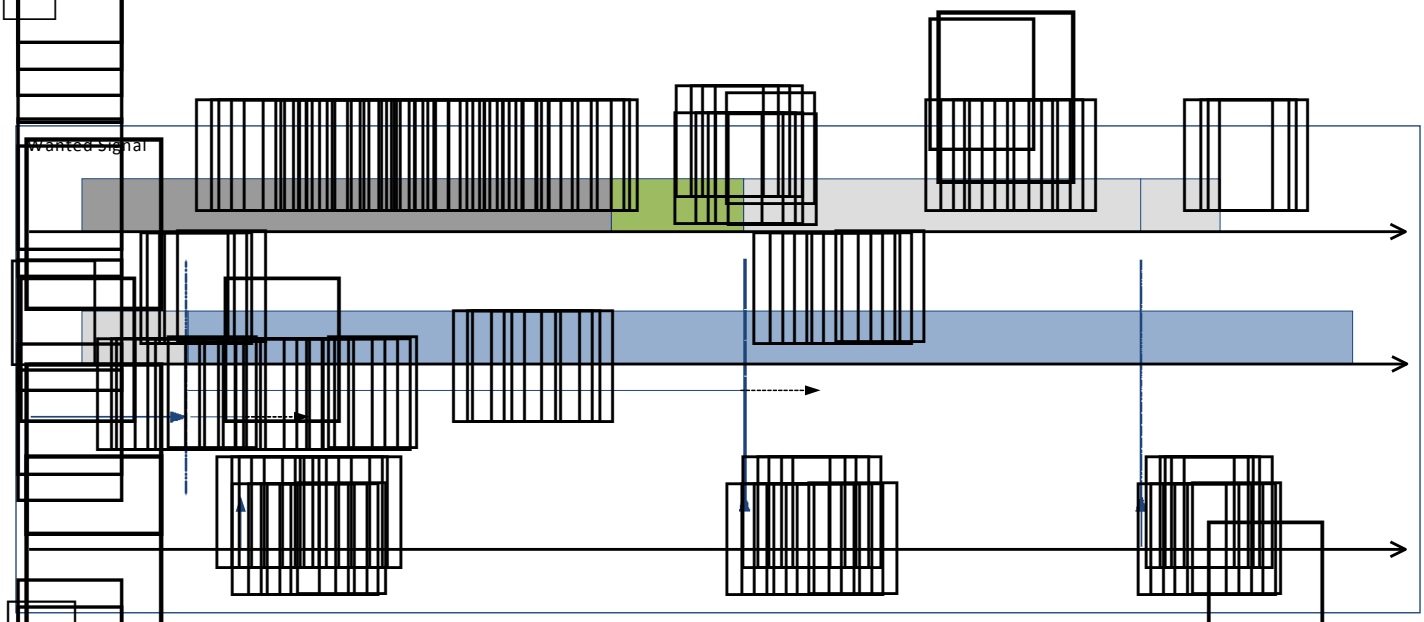


Figure 50. Listen Mode with Preamble Received & Valid SyncAddress

7.3.2.2. Sequencer Configuration

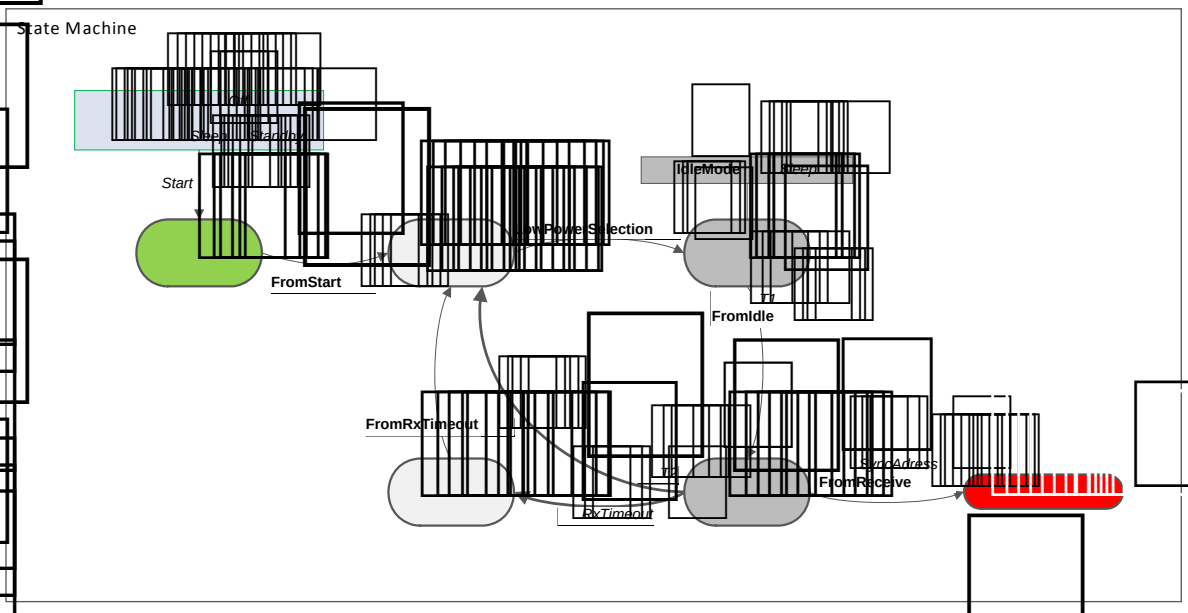


Figure 51. Wake On SyncAddress State Machine

Table 92 ListenMode with SyncAddress Condition Settings

Variable	Effect
	Set Receiver off
	Set Receiver off
	PreambleDetectSize
	SyncSize

Table 93 Listen Mode with PreambleDetect Condition Recommended DIO Mapping

DIO	Value	Description
		MapPreambleDetect

7.4. Top Sequencer [illegible]

PayloadLength [illegible] *BeaconOn* *RegPacketConfig2*

7.4.1. [illegible]

PacketSent

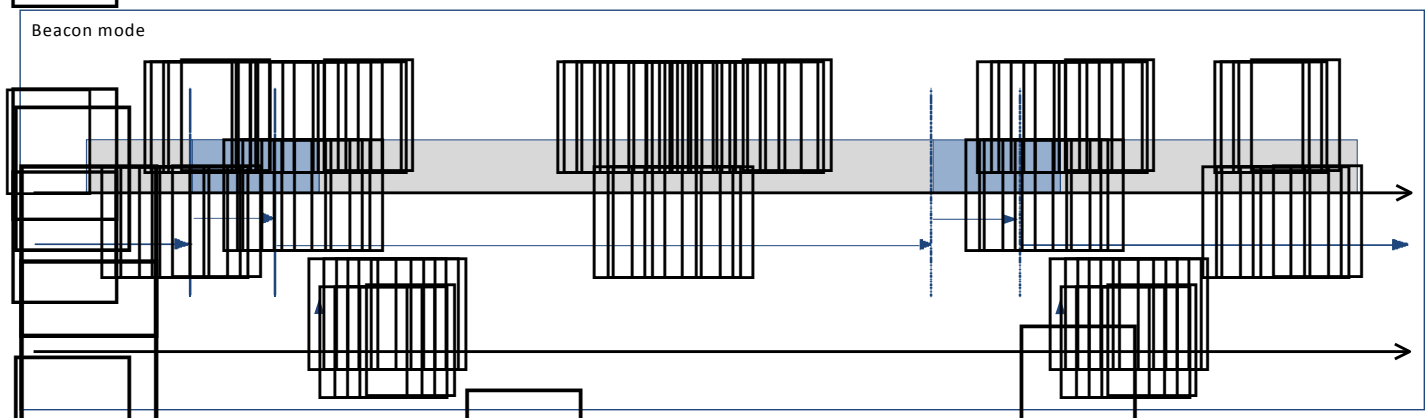


Figure 52. Beacon Mode Timing Diagram

7.4.2. Sequencer Configuration

SequencerStop *RegSeqConfig1*

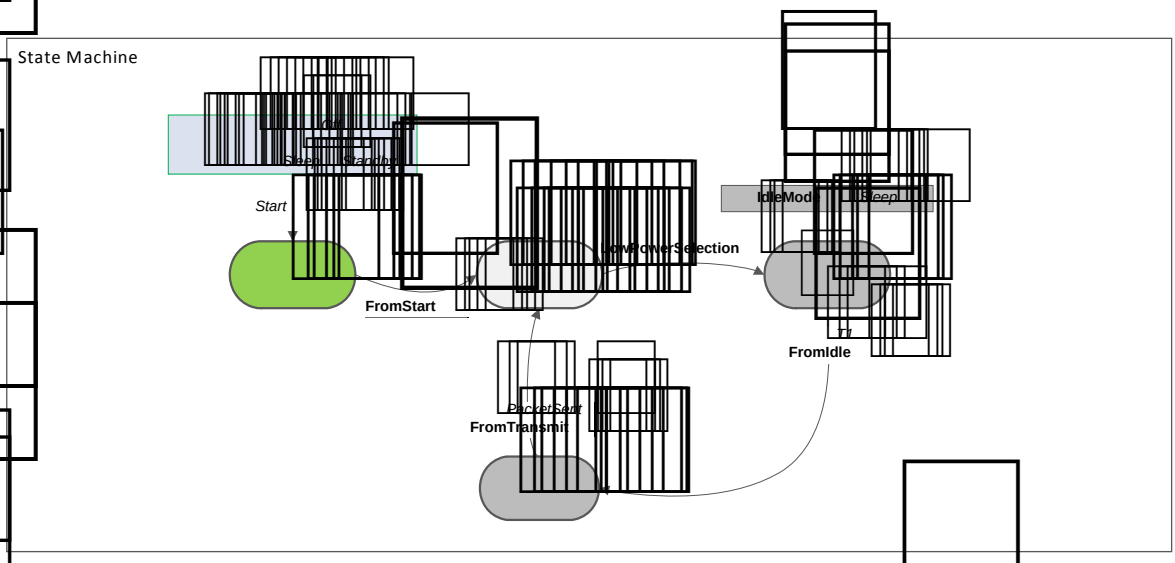


Figure 53. Beacon Mode State Machine

Table 94 Beacon Mode Settings

Variable	Effect
Start	LowPowerSelection
Idle	
LowPowerSelection	*PacketSent*

7.5. Example CRC Calculation

```
// CRC types
#define CRC_TYPE_CCITT                          0
#define CRC_TYPE_IBM                            1

// Polynomial = X^16 + X^12 + X^5 + 1
#define POLYNOMIAL_CCITT                        0x1021
// Polynomial = X^16 + X^15 + X^2 + 1
#define POLYNOMIAL_IBM                          0x8005

// Seeds
#define CRC_IBM_SEED                            0xFFFF
#define CRC_CCITT_SEED                          0x1D0F

/*
 * CRC algorithm implementation
 *
 * \param[IN] crc Previous CRC value
 * \param[IN] data New data to be added to the CRC
 * \param[IN] polynomial CRC polynomial selection [CRC_TYPE_CCITT, CRC_TYPE_IBM]
 *
 * \retval crc New computed CRC
 */
U16 ComputeCrc( U16 crc, U8 data, U16 polynomial )
{
    U8 i;
    for( i = 0; i < 8; i++ )
    {
        if( ( ( ( crc & 0x8000 ) >> 8 ) ^ ( data & 0x80 ) ) != 0 )
        {
            crc <<= 1;                  // shift left once
            crc ^= polynomial;          // XOR with polynomial
        }
        else
        {
            crc <<= 1;                  // shift left once
        }
        data <<= 1;                     // Next data bit
    }
    return crc;
}

/*
 * CRC algorithm implementation
 *
 * \param[IN] buffer Array containing the data
 * \param[IN] bufferLength Buffer length
 * \param[IN] crcType Selects the CRC polynomial [CRC_TYPE_CCITT, CRC_TYPE_IBM]
 *
 * \retval crc Buffer computed CRC
 */
U16 RadioPacketComputeCrc( U8 *buffer, U8 bufferLength, U8 crcType )
{
    U8 i;
    U16 crc;
    U16 polynomial;

    polynomial = ( crcType == CRC_TYPE_IBM ) ? POLYNOMIAL_IBM : POLYNOMIAL_CCITT;
    crc = ( crcType == CRC_TYPE_IBM ) ? CRC_IBM_SEED : CRC_CCITT_SEED;

    for( i = 0; i < bufferLength; i++ )
    {
        crc = ComputeCrc( crc, buffer[i], polynomial );
    }

    if( crcType == CRC_TYPE_IBM )
    {
        return crc;
    }
    else
    {
        return ( U16 )( ~crc );
    }
}
```

Figure 54 - Example CRC Code

7.6. Example Temperature Reading

Temperature.c

```
/*!
 * Reads the raw temperature
 * \retval temperature New raw temperature reading in 2's complement format
 */
S8 RadioGetRawTemp( void )
{
    S8 temp = 0;
    U8 regValue = 0;

    regValue = RadioRead( 0x3C );

    // 2's complements conversion
    temp = regValue & 0x7F;
    if( ( regValue & 0x80 ) == 0x80 )
    {
        temp *= -1;
    }
    return temp;
}

/*!
 * Computes the temperature compensation factor
 * \param [IN] actualTemp Actual temperature measured by an external device
 * \retval compensationFactor Computed compensation factor
 */
S8 RadioCalibrateTemp( S8 actualTemp )
{
    return actualTemp - RadioGetRawTemp( );
}

/*!
 * Gets the actual compensated temperature
 * \param [IN] compensationFactor Return value of the calibration function
 * \retval New compensated temperature value
 */
S8 RadioGetTemp( S8 compensationFactor )
{
    return RadioGetRawTemp( ) + compensationFactor;
}

/*!
 * Usage example
 */
void main( void )
{
    S8 temp;
    S8 actualTemp = 0;
    S8 compensationFactor = 0;

    // Ask user for the temperature during calibration
    actualTemp = AskUserTemperature( );
    compensationFactor = RadioCalibrateTemp( actualTemp );

    while( True )
    {
        temp = RadioGetTemp( compensationFactor );
    }
}
```

Figure 55. Example Temperature Reading

7.7. Reference Design

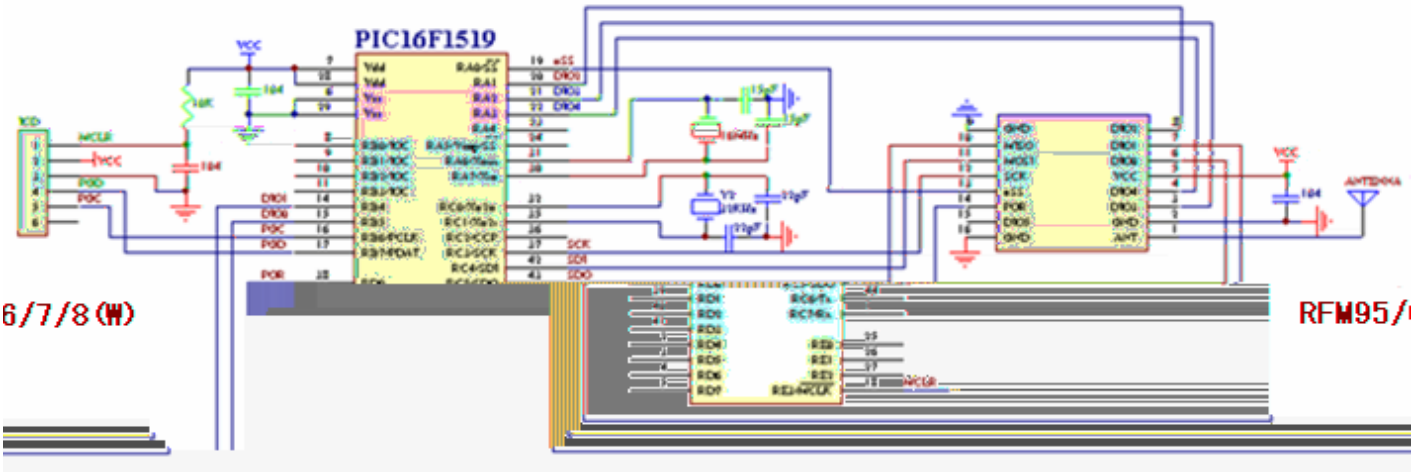
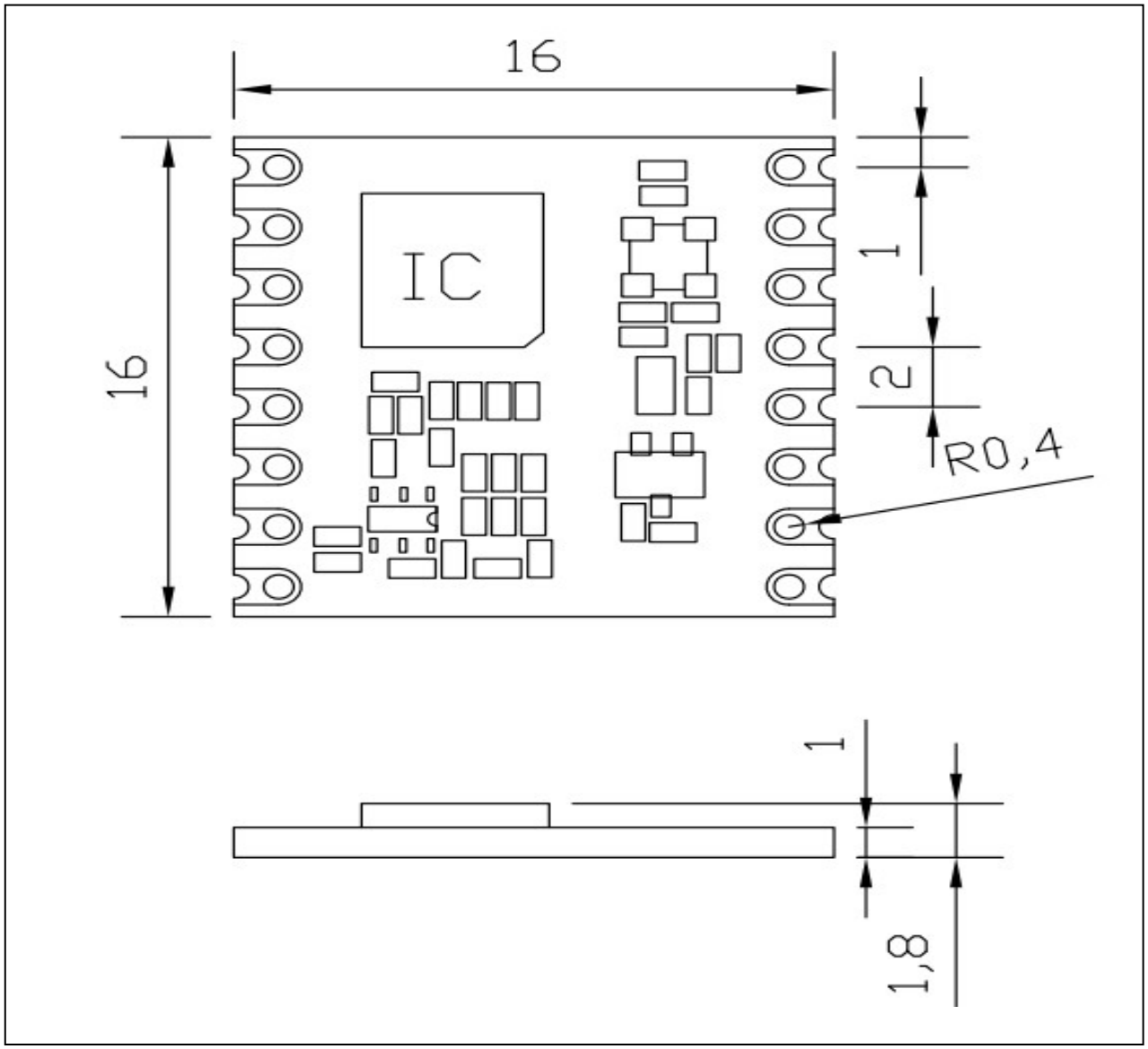


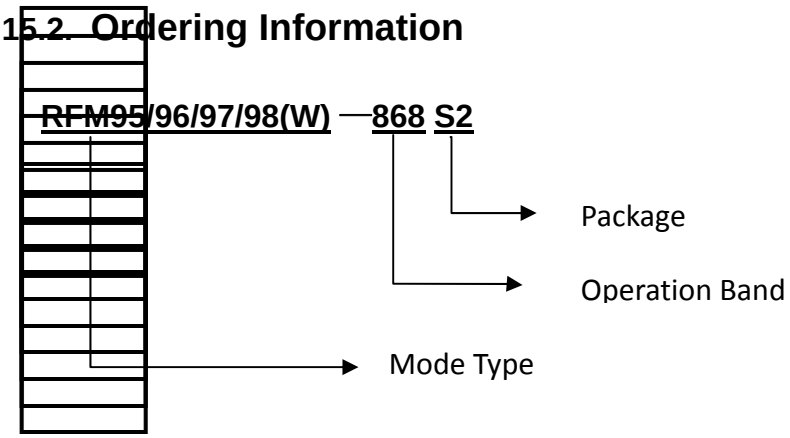
Figure 56:+20dBm Schematic

8. Packaging Information

8.1. Package Outline Drawing



15.2. Ordering Information



P/N: RFM95W-868S2
RFM95W module at 868MHz band, SMD Package
P/N: RFM95W-915S2
RFM95W module at 915MHz band, SMD Package
P/N: RFM96W-315S2
RFM96W module at 315MHz band, SMD Package
P/N: RFM96W-433S2
RFM96W module at 433MHz band, SMD Package
P/N: RFM97W-868S2
RFM97W module at 868MHz band, SMD Package
P/N: RFM97W-915S2
RFM97W module at 915MHz band, SMD Package
P/N: RFM98W-315S2
RFM98W module at 315MHz band, SMD Package
P/N: RFM98W-433S2
RFM98W module at 433MHz band, SMD Package