

Designing and Implementing an Audio Frequency Amplifier on a PCB

Bruno E. Gracia Villalobos

EE 4113

Professor Hansen

University of Texas at San Antonio

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Abstract

This paper explores the process for the design and implementation of an audio frequency amplifier on a custom-made Printed Circuit Board (PCB) with dimensions 4.7" x 3.4" for the final project of an analog circuits laboratory course. The circuit is designed to take in a signal from 0 to 2 V peak-to-peak, cutoff any frequencies outside the 200 to 18k Hz range, and output the filtered waveform to a 20Ω load with controllable gain in the range of -5 to 20 dB. In the mid-band, at 1.6kHz, the circuit displays only 1% Total Harmonic Distortion (THD). At 9 kHz, the circuit displays a Signal-to-Noise Ratio (SNR) of 48.6dB. The circuit was developed as a group effort of three laboratory students throughout a three-month period in three phases: the development and prototyping of the bandpass filter, the development and prototyping of a class A/B audio amplifier, and the development and assembly of a custom PCB; The lab reports for the project were all individually written. For the constraints of the hardware, the circuit relies on $\pm 15V$ supply rails and GND from a DC power supply and a function generator capable of outputting a sinusoidal waveform from 0-2Vpp in the range of 0 to 100kHz.

1 Introduction and Problem Description

1.1 The EE 4113 Class

This paper serves as the final exam for the EE 4113 – Electrical and Computer Engineering Laboratory course—commonly named “Lab 2”—required for the author’s fulfillment of a bachelor’s degree in Computer Engineering at the University of Texas at San Antonio. In Lab 2, students learn the following major topics:

- Complex electronic subsystem design
- Improvement of measurement system performance
- Impact of circuit parasitics
- Signal integrity
- Electromagnetic interference (EMI)
- Thermal analysis
- Printed circuit board (PCB) layout
- Technical communication

1.2 Description of Project

The project entails of the design and implementation of an electronic circuit on a custom PCB that amplifies and filters signals with frequency spectra in the range of human hearing (0 to 22000 Hz). Two +- 15V DC supply rails are used to power up the circuit from a DC Power supply. The input signal is sent to the circuit through a BNC connector, and the output is a 20Ω power resistor.

The design consists of two sub circuits, and the following list explains these to resemble the signal path from input to output:

1. An active, bandpass filter with the following specs:

- An active architecture using TL071 and TL072 op-amps
- Passband exists in [200, 18k] Hz
- Passband ripple < 2dB
- Low stopband is at 40 Hz with >22dB attenuation
- High stopband is at 90k Hz with >22dB attenuation
- 100 μ F electrolytic power supply bypass caps

- 0.1 μ F ceramic bypass caps on IC power pins
2. A volume controlled, pre-amped class AB audio power amp with the following specs:
- A push-pull architecture using an IRF510 and IRF9510 power MOSFETS
 - 0.01 μ F and 0.1 μ F ceramic bypass caps on power MOSFETS' drains
 - Passband gain exists in [-5, 20] dB
 - Gain of at least 10 for feedback network
 - Capable of a 20V peak-to-peak (Vpp) output into a 20 Ω load with an input 2Vpp sinewave at 1.6kHz
 - Given the last criteria point, the Total Harmonic Distortion (THD) should be <1%

The project was developed in three phases. The first phase (project 1A) consisted of designing and testing the active, bandpass filter on a protoboard. The second phase (project 1B) consisted of designing the volume controlled, pre-amped class AB audio power amp, testing the amp in isolation, and testing both the filter and amp in a protoboard together. The third and last phase (project 1C) consisted of designing a PCB using CAD for the overall amplifier, testing the board for manufacture errors, soldering and testing each sub-circuit using through-hole parts, and testing the final assembled PCB using oscilloscope measurements.

The paper is arranged in a different format. First, the design and Pspice simulation of both sub-circuits, the filter and the volume controlled, pre-amped class AB audio power are discussed. Secondly, the prototyping process is discussed, in the same order as the design and simulation process, that is, building a sub-circuit and testing it on the oscilloscope. Lastly, the PCB design process is discussed, including the CAD process, the soldering process, and the testing process. Although the project timeline and paper outline are similar in nature, the main difference is the separation of simulation and prototyping; the paper discusses the simulation of all phases then the prototyping of all phases, while the project was developed by simulating and prototyping a phase before moving on to the next phase.

2 Initial Design and Pspice Simulation

2.1 Filter Section

The first phase of this project laid out the requirements for the bandpass filter. To begin, the filter was designed using an online filter design tool called “Analog Filter Wizard” by Analog Devices (1). This tool can design low pass, high pass, and band pass filters given specifications such as maximum ripple, passband gain, stopband attenuation, filter architecture, operating conditions, and component tolerances.

For better quality control and for learning purposes, the bandpass filter for the audio amplifier was designed as a combination of a high pass filter and low pass filter. The former filter’s purpose is to serve as the lower “limit” of the audio frequency bandpass filter, and the latter filter’s purpose is to serve as the upper “limit” of the audio frequency bandpass filter. When combined, both high and low pass filters effectively model the bandpass filter requirements as laid out in section 1.2. Lastly, both high pass and low pass filter designs had in common the need to accommodate a 10% capacitor tolerance, and a 5% resistor tolerance through larger passband range and larger stopband attenuation gain.

2.1.1 Low pass filter design

The low pass filter was over-designed to cut at a larger frequency—at 22kHz—rather than 18kHz to keep the filter within spec when prototyping. This passband gain was set at -1dB to account for ripple and keep it within the spec of <2dB ripple. The filter’s design also set the stopband gain at -30dB—a -8dB increase over spec—to account for component tolerances. The Analog Filter Wizard can consider these over-designed specs and they are demonstrated in Figure 1.

Filter Requirements for Low-Pass, 3rd order Chebyshev

Specifications: Optimize for Specific Components; $+V_s = 15$; $-V_s = -15$

Gain: 0 dB

Passband: -1dB at 22kHz

Stopband: -30dB at 90kHz

Component Tolerances: Capacitor = 10%; Resistor = 5%; Inductor = 5%; Op Amp GBW = 20%

BOM: refer to BOM.csv file

Figure 1: Analog Filter Wizard - Low Pass Filter Report

As shown in Figure 1, given our over-designed specifications, the Analog Filter Wizard generated a 3rd order Chebyshev filter architecture split into two stages (2 poles per 1 stage). Figure 1 also demonstrates the + - 15V power supply requirement, as well as unity gain in the passband (not a boost/shelf filter).

Figure 2 displays the result of this design as reported by the Analog Filter Wizard. For the active components, the Wizard suggests the use of Analog Devices’ own IC’s (ADA 4096), but the amplifier’s design used TL071 and TL072’s from Texas Instruments. For the passive components, the Wizard was set to use standard E12 sizes. This section effectively served as the audio amplifier’s “upper” frequency limit.

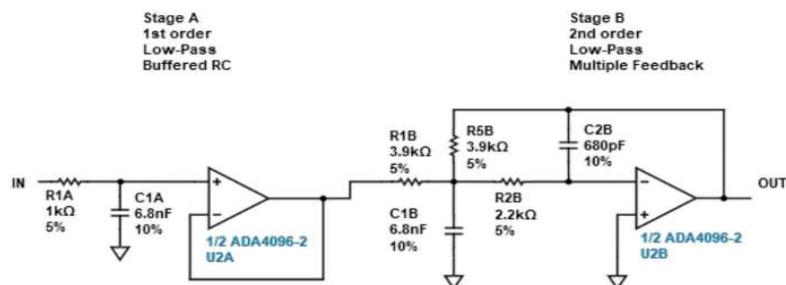


Figure 2: Analog Filter Wizard - Low Pass Filter Schematic

2.1.2 High pass filter design

The high pass filter was over designed as well to keep the overall bandpass filter within spec when prototyping. The main two specs of interest are: a passband at 150Hz, and a stopband at 35Hz. The passband, like the low pass design, was also specified to be at -1dB to account for ripple and the stopband at -30dB to account for component tolerances. Figure 3 demonstrates these specs through the Analog Filter Wizard design report.

Filter Requirements for High-Pass, 3rd order Chebyshev

Specifications: Optimize for Specific Components; $+Vs = 15$; $-Vs = -15$

Gain: 0 dB

Passband: -1dB at 150Hz

Stopband: -30dB at 35Hz

Component Tolerances: Capacitor = 10%; Resistor = 5%; Inductor = 5%; Op Amp GBW = 20%

BOM: refer to BOM.csv file

Figure 3: Analog Filter Wizard - High Pass Filter Report

Similar to the low pass design, this high pass filter consists of a two stage, 3rd order Chebyshev architecture. To keep unity gain and the filter within spec, a gain of 0db was chosen and the power supply to +/- 15V to prepare for the future PCB design. The passband also exhibits a -1dB gain like the low-pass design to keep <2dB ripple.

Figure 4 shows the filter architecture in schematic form. In this design, the same requirements for component tolerances and op-amp choices that applied for the low pass filter are included.

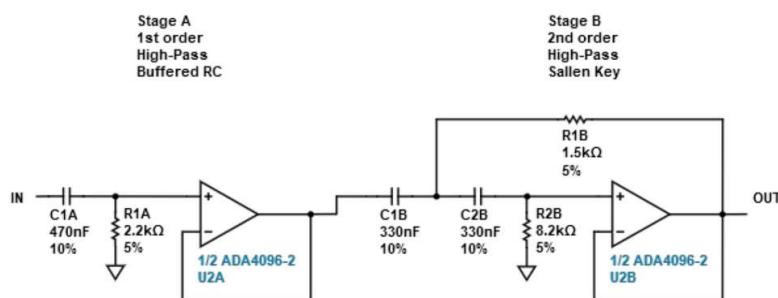
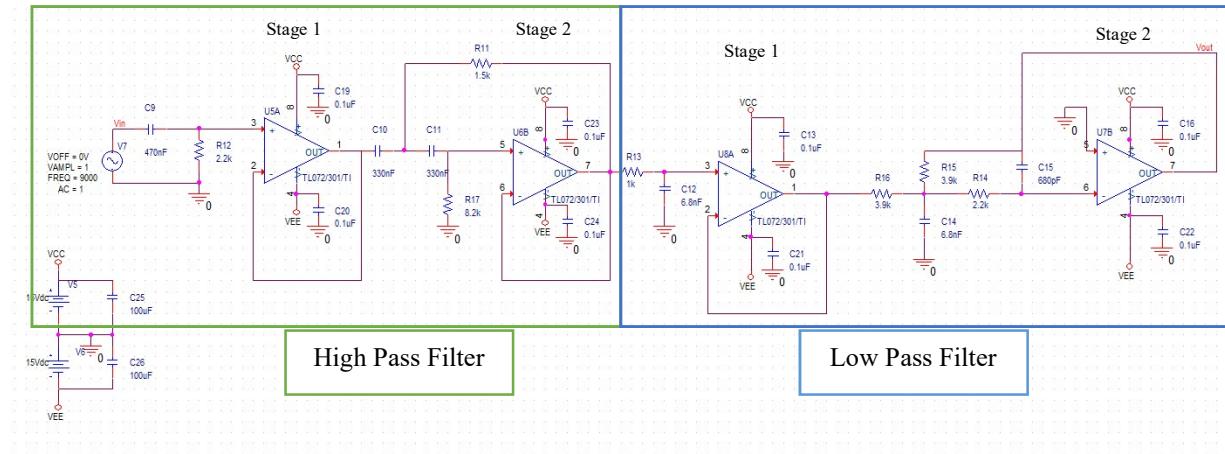


Figure 4: Analog Filter Wizard - High Pass Filter Schematic

2.1.3 OrCAD simulation

Both low pass and high pass filter designs were combined into a single design and simulated using OrCAD Capture CIS 17.2. To generate the bandpass filter, the high-pass filter is the “first” section embedded in a green rectangle and the low-pass filter is the “second” section embedded in a blue rectangle. The order of these considers the need for filtering noise as the high-pass filter has a DC decoupling capacitor at its effective input voltage node. At the output of the second stage of the high-pass filter, the input voltage node of the first stage of the low-pass filter section is connected. In essence, signal enters unfiltered through C9, the 470pF decoupling cap of the high pass filter section, and exits filtered from pin 7 of the 2nd stage of the low-pass filter section. The signal is filtered from all frequencies outside of [150, 22k] Hz (these bounds consider component tolerances). Figure 5 shows the resultant schematic.



2.1.3.1 Frequency domain simulation

Once the schematic was built using OrCAD, both frequency and time domain simulations were constructed to model the accuracy and behavior of the filter. To begin, a frequency simulation was developed using an AC sweep from 1Hz to 100kHz with 1000 points/decade using OrCAD's built in Pspice simulation software. Figure 6 displays the resultant Bode plot of the filter's response

The first expectation of unity gain in the passband is met as seen on Figure 6. Next, the lower and upper -3dB points were examined to obtain the conventional lower and upper bandpass limits of the filter. The simulation resulted in a lower frequency limit of 130.074Hz at around -3.0038dB and an upper frequency limit of 26.229kHz at -3.0273 dB.. Figures 7 and 8 showcase the lower and upper limits respectively calculated using cursors. These results meet expectation since the Analog Filter Wizard defined the passbands at the -1dB marks.

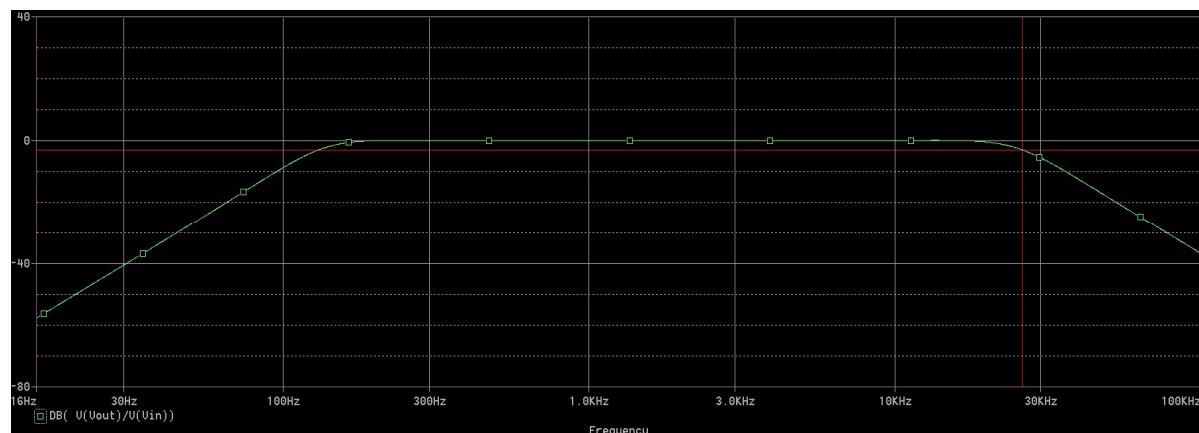


Figure 6: Frequency domain Pspice simulation of Bandpass Filter

Trace Color	Trace Name	Y1
	X Values	130.074
CURSOR 1,2	DB(V(Vout)/V(Vin))	-3.0038

Figure 7: Cursor at lower f3db = 130Hz

Trace Color	Trace Name	Y1
	X Values	26.229K
CURSOR 1,2	DB(V(Vout)/V(Vin))	-3.0273

Figure 8: Cursor at upper f3db = 26.2kHz

2.1.3.2 Time domain simulation

Before continuing, it is necessary to give a disclaimer for the chosen test input signal: to the author's misconception of "mid-band," as laid out in the project requirements, where a 1.6kHz 2Vpp tester sine wave should be used, a 9kHz 2Vpp sine wave was used instead. There are simulations available with 1.6kHz frequency as the tester signal, but to keep conformity through the paper, the 9kHz is chosen; Since 9kHz is within the passband, there should not be considerable errata with respect to the required filter specs.

To model phase delay and gain, a time domain simulation was constructed using a 2Vpp sinusoidal input running at 9kHz for 1000 μ s with a 10ns step size. Figure 9 displays the simulation from approx. 0 to 0.16ms or 3/2 period of the sine wave. Cursor 2 is placed on Vin and cursor 1 is placed on Vout. The cursor displacement shows there is a ~0.295dB increase in Figure 10 for Vout which meets spec. Figure 10 also shows there is a ~69 μ s lag for Vout compared to Vin.

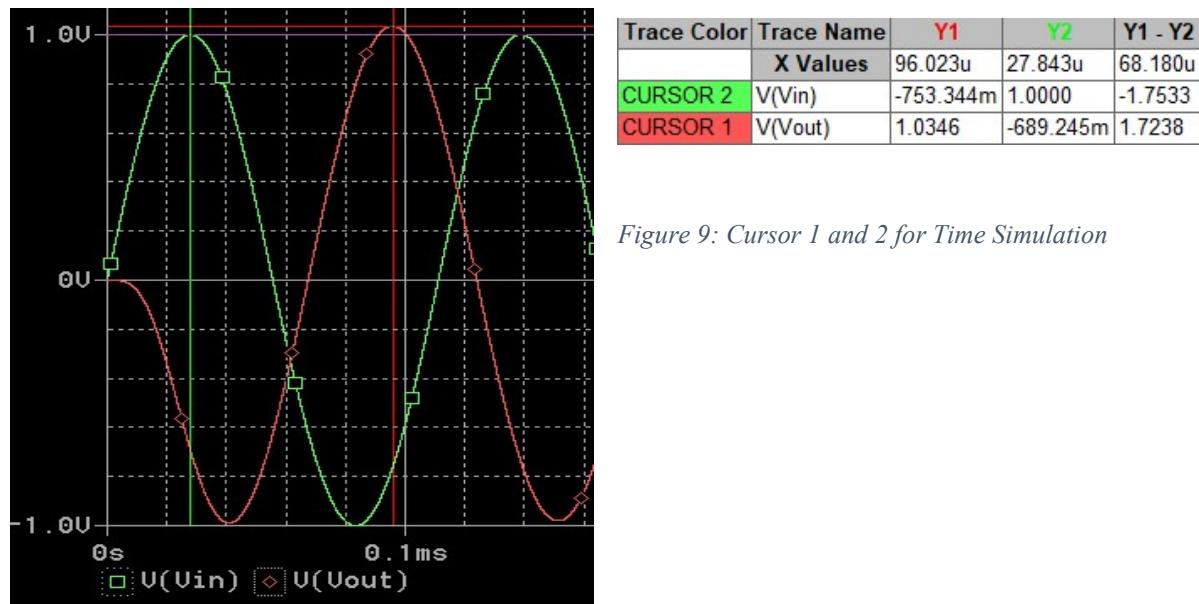


Figure 9: Cursor 1 and 2 for Time Simulation

Figure 10: Time domain simulation of filter

2.2 Class A/B Amp Section

Once the filter was simulated, a class A/B amp was designed to provide a volume control, pre-amp and amplification stage to the output of the bandpass filter. To achieve this goal, the class A/B Amp was designed and tested in isolation of the filter, and then appended to the output of the bandpass filter circuit. The class A/B amp consists of a push-pull MOSFET amplifier architecture and the design process followed a three-phase lifecycle:

1. derive open loop biasing method to put amplifier operation into full class B
2. re-bias amplifier into class A/B to remove cross-over distortion
3. derive closed loop model pre-amp with volume control stage

The first phase is discussed next in section 2.2.1.

2.2.1 Phase 1: Full Class B Operation

To begin the first phase of the design, the potentiometers were biased so that 0V appeared across them in simulation; This setting put the amplifier into full class B operation and the resulting circuit is shown in Figure 11-A. With this classification, the amplifier shows the defining characteristic of cross-over distortion as shown in Figure 11-B; this waveform is commonly named as “the Alamo” in the “Lab 2” class. Given the entire project’s design for audio waveforms, this distortion is something that is detrimental to the design. As a result, the amplifier needed to be rebiased into class A/B to remove the cross over distortion. This rebiasing is discussed next in Phase 2.

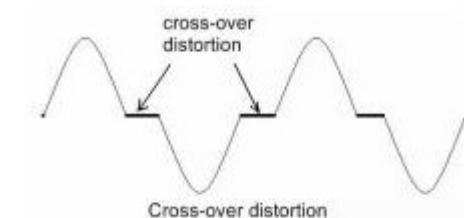
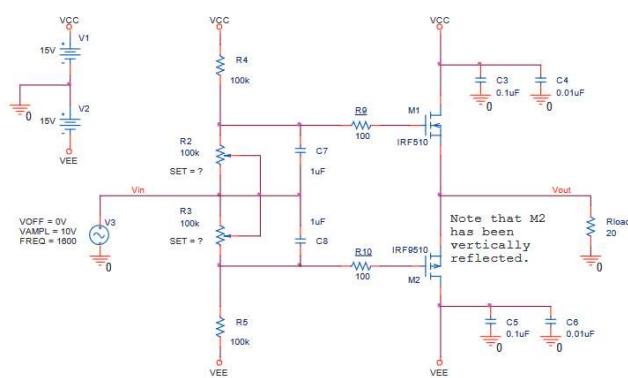


Figure 11-B: Cross Over Distortion in Vout (2)

Figure 11-A: Open Loop Class B Amplifier

2.2.2 Phase 2: Class A/B Operation

As part of the second phase of the design, the amplifier was re-biased to remove the cross-over distortion. To achieve this measure, the potentiometers were re-biased one by one, increasing the current through the MOSFETS until the cross-over distortion was gone. At this point, the amplifier is said to operate in a class A/B setting, and the form and shape of the output waveform is nearly identical to the input waveform, given it is of sinusoidal type. This step is important in the design of the amplifier sub-circuit because the full class B operation would have distorted the output audio of the design. Once the output waveform met expectation, the next step was to add a pre-amp and volume control. This is discussed in section 2.2.3.

2.2.3 Phase 3: Closed Loop Model with Pre-Amp and Volume Control

Once the amplifier is operating in class A/B, it is ready to be integrated in a closed loop model with volume control. The main function of the closed loop model is to add gain to the input signal by using a pre-amp built with the TL071. The volume control's function is to have control on the gain of the signal and is placed in the signal chain before the pre-amp to keep the closed loop model architecture.

First, the amplifier was put in a closed loop with a TL071 op-amp to give the amplifier a gain of 11. Secondly, the volume control potentiometer was added preceding the non-inverting pin of the op-amp. The final configuration of the amplifier sub-circuit can be seen in Figure 13.

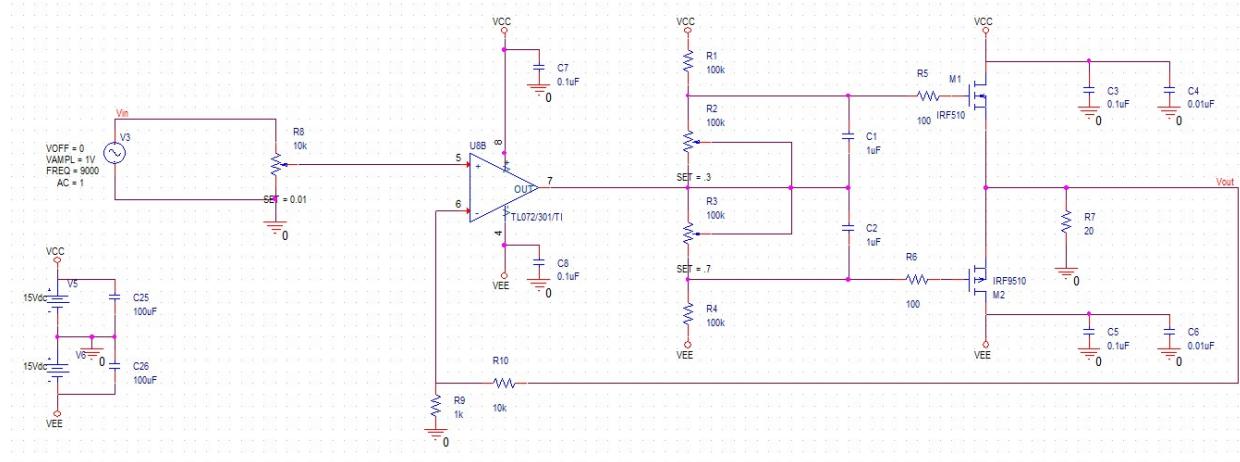


Figure 12: Class A/B Amp with Volume Control and Pre-Amp

Both volume control and pre-amp measures are designed to meet the required spec of having an adjustable passband gain in the range of at least [-5, 20] dB. To meet the desired range

spec, the volume control was chosen to be 10k Ω potentiometer. To meet the gain spec, the feedback resistors of the closed loop, R9 and R10 were chosen to be 10k Ω and 1k Ω to give a gain of

$$Av = (10k/1k + 1) = 11$$

for a non-inverting configuration.

Another design consideration was 100 Ω resistors R5 and R6; these are indeed optionally placed to reduce oscillations in the amplifier, but in this case, they seemed to have either prevented it or not helped at all. However, these are not large enough to impact performance for an audio power amp, and they are not discussed further. In the next section, Pspice simulations are discussed next to measure the performance of the audio power amp.

2.2.4 Voltage Simulations

After the completion of all three phases in the design of the audio power amp, it was necessary to visualize the input and output waveforms. To simulate the audio power amp configuration, two tests were conducted in the time domain with a 2Vpp, 9kHz sine wave. First off, to test the amplifier at full power, the volume control potentiometer was set at near 0Ω to put the noninverting pin at the full 2Vpp range of the input waveform as shown on Figure 14.

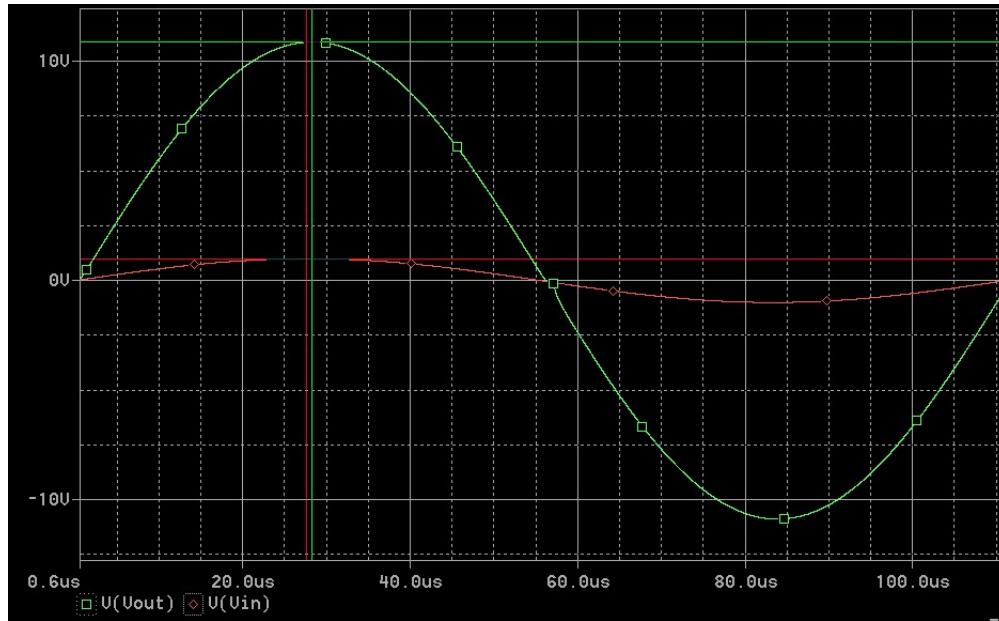


Figure 13: Time domain simulation of 2Vpp at Noninverting pin

For Vout, measured at the 20Ω load R7, the resulting output is

$$10.885V * 2 = 21.77 \text{ Vpp}$$

according to Cursor 2 under Y2 in Figure 15. The gain is then

$$\text{AvdB} = 20\log(21.77V / 2V) = 20.74\text{dB}.$$

The gain result shows the audio power amp meets the minimum 20dB gain spec.

Although not part of the spec requirement, the phase offset confirms the usefulness of the audio power amp since the peaks of both sine waves are aligned; this will allow the audio input will play back at the same time once it goes out of the audio frequency amplifier.

Trace Color	Trace Name	Y1	Y2	Y1 - Y2
	X Values	27.617u	28.263u	-645.901n
CURSOR 2	V(Vout)	10.877	10.885	-8.3795m
CURSOR 1	V(Vin)	1.0000	0.9996	320.771u

Figure 14: Cursors show time lag and voltage gain

For the second test, the same 9kHz, 2Vpp sine wave was used as the tester. However, the potentiometer was set at $10\text{k}\Omega$ so that the noninverting pin sees around 100nV. The resulting output at R7, 20Ω load is virtually insignificant at $1.1\mu\text{V}$. This is a gain of

$$\text{AvdB} = 20\log(1.1\mu\text{V} / 2\text{V}) = -140\text{dB},$$

which meets the minimum spec of -5dB. This result is showcased in Figure 16.

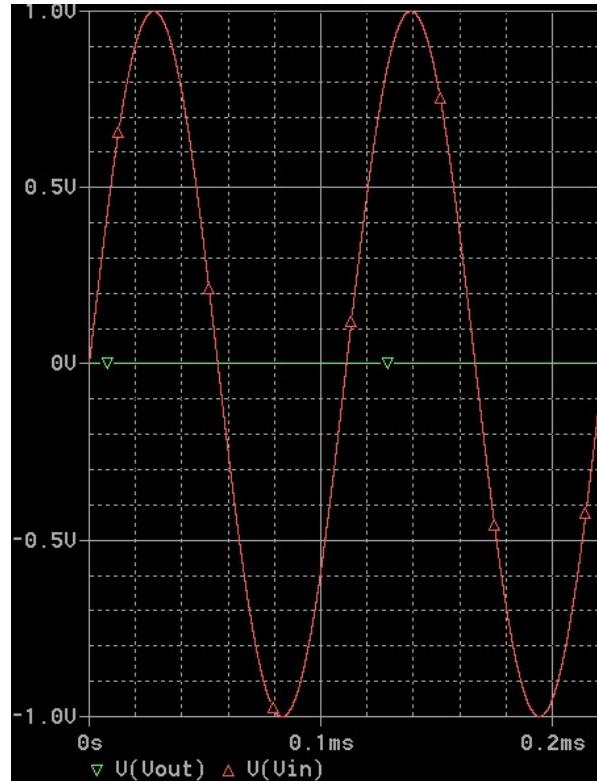


Figure 15: Time domain simulation of 100nV at noninverting pin

2.2.5 Power simulation

To test the power consumption of the full configuration of the audio amplifier, including the class A/B amp, the pre-amp, and volume control, a 9kHz 2Vpp sine wave was sent to the noninverting pin of the pre-amp. This effectively outputs a 21.77Vpp sine wave at the R7 load as demonstrated in 2.2.4. Figure 17 showcases an average of 3W consumption of the 20Ω load!



Figure 16: Average power consumption of load @ 21.77Vpp = 3W

To measure efficiency, Figure 18 showcases a combined -6W of generated power by the +15V DC supplies. Given the 9kHz 2Vpp sine wave consumes power in the negligible microwatts, the efficiency of the full audio power amp at the load is:

$$\% \text{ Efficiency} = 3/6 = \sim 50\%$$

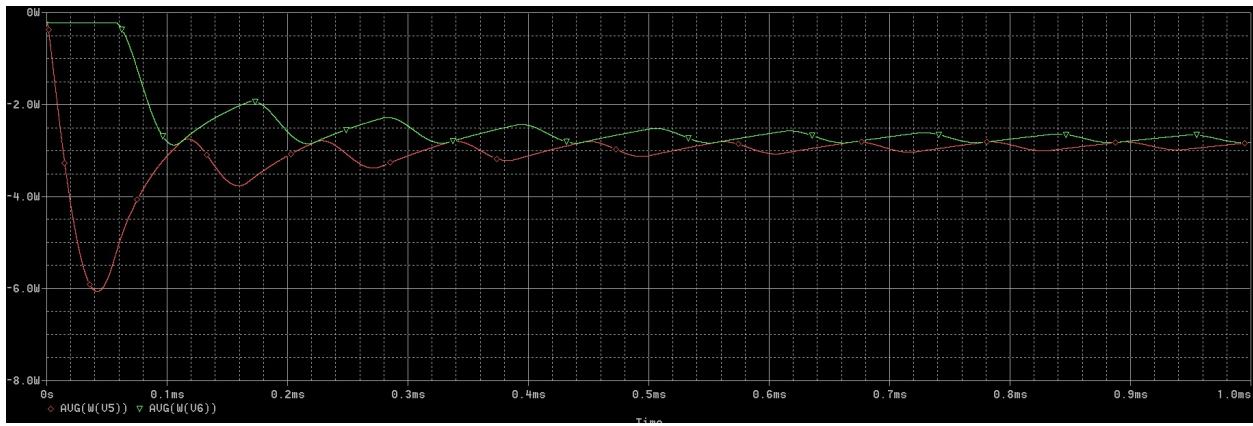


Figure 17: Power consumption of $\pm 15V$ supplies = -6W

Once both filter and audio power amp simulations were verified to pass the minimum required specifications, the next step was to prototype both sub-circuits as discussed in 3.1.

3 Protoboard Circuit

3.1 Bandpass Filter Prototyping

In this section, the filter prototyping process is discussed. After simulating the full bandpass filter in OrCAD Pspice, it was prototyped on a standard 830-pt breadboard as shown in Figure 18. The bill of materials (BOM) generated from OrCAD is shown in Figure 19. As mentioned in section 2, E12 values were used for both capacitors and resistors. In addition, capacitors had 5% tolerance and resistors had 10% tolerances; these were accounted for in the Analog Filter Wizard design. For the required 4 op-amps, 2 TL072's were used since each chip has two integrated op-amps. Lastly, to anticipate the prototyping of the audio power amp, the full bandpass filter was prototyped in 1/2 of the breadboard space.

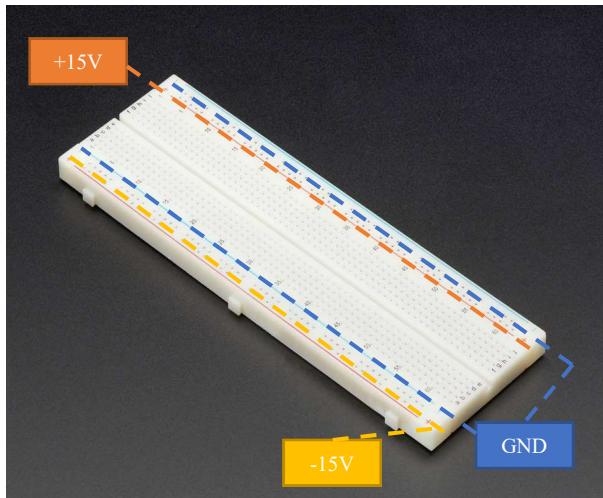


Figure 198: 830 pt breadboard (3)

Item	Quantity	Reference	Part
1	1	C9	470nF
2	2	C10,C11	330nF
3	2	C12,C14	6.8nF
4	8	C13,C16,C19,C20,C21,C22, C23,C24	0.1uF
5	1	C15	680pF
6	2	C25,C26	100uF
7	1	R11	1.5k
8	2	R12,R14	2.2k
9	1	R13	1k
10	2	R15,R16	3.9k
11	1	R17	8.2k
12	4	U5,U6,U7,U8	TL072/301/TI

Figure 19: Bandpass filter section BOM from OrCAD

To begin the prototyping process, a DC power supply was used to wire in +15V on the RED rail of the *right* part of the breadboard. Next, a -15V wire setup the RED rail of the *left* part of the breadboard. Lastly, GND was wired in on both BLUE rails of the breadboard. This configuration can be seen on the left side of Figure 18.

After wiring in the power rails, both 100uF electrolytic bypass capacitors, C25 and C26 were placed across both +- 15V rails to reduce AC noise on the DC lines. One of them was placed from +15V to GND, and the other from GND to -15V to account for polarity of electrolytic capacitors. In addition, the leads of all passive components were trimmed to reduce series inductance despite this not being a problem at audio frequencies.

3.1.1 Prototyping the High pass filter section

Given the signal enters the decoupling capacitor from the high pass filter, this section was naturally prototyped first. The first TL072 IC was placed on the breadboard and its VCC and VEE power pins were both coupled in parallel with 0.1uF ceramic capacitors to ground to reduce noise. Next, the passive components, with their short leads, were wired in the protoboard as following the guidelines of Figure 20.

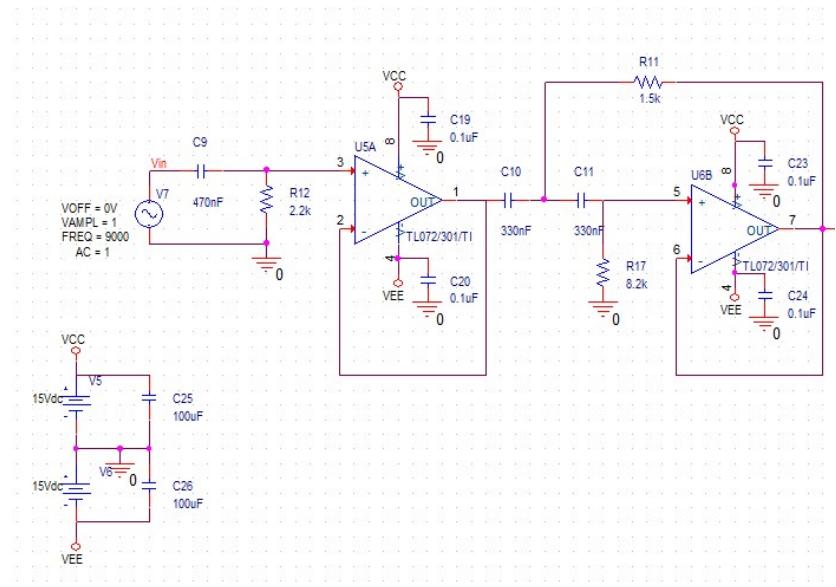


Figure 20: High pass filter section schematic

Once all parts were wired in the protoboard, the circuit was tested using an oscilloscope. A x10 probe measured signal on pin 7 of the TL072 as shown in Figure 20, and an alligator clip brought a 200Hz 2Vpp signal in from a function generator at C9, the 470nF's capacitor's lead.

To meet specs, the high pass filter must have a passband at 150 Hz with unity gain, and a stopband at 35Hz with an attenuation of -30dB. The Vin signal was “swept” from 1 Hz to 1kHz and Vout (pin 7 of TL072) was measured on the oscilloscope. The measurements proved correct and the low pass filter was wired next.

3.1.2 Prototyping the Low pass filter section

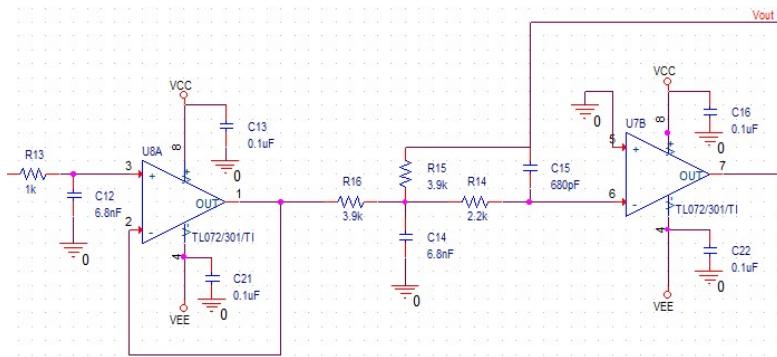


Figure 21: Low pass filter section schematic

the passive components were wired to their respective locations as dictated by Figure 21.

To test the low pass filter in isolation, the alligator clip was moved and placed next to R13, the $1\text{k}\Omega$ resistor feeding into the noninverting pin (#3) of the TL072 chip. The x10 scope probe was moved and placed in pin 7 of the TL072 chip of the low pass filter section. A 9kHz, 2Vpp signal was then injected to R13 through the alligator clip.

Both Vin and Vout were then observed in the oscilloscope to make sure the low pass filter meets the required passband of unity gain at 22kHz and below, as well as the stopband attenuation of -30dB at 90kHz. Once again, in the same way as testing the high pass filter section, the signal was swept from 9kHz to 1Hz, then back up to 22kHz all the way to 90kHz. The oscilloscope proved the measurements right and the low pass filter and high pass filter were combined next.

The low pass filter section was prototyped next. First, the second TL072 IC was placed on the breadboard. The $0.1\mu\text{F}$ bypass ceramic capacitors were also placed in a similar manner to the high pass filter section's TL072.

With the IC in place, the rest of

3.1.3 Testing the Bandpass Filter

Both high pass and low pass filter sections were then combined to complete the bandpass filter section. To meet specs, the bandpass filter must have

- a passband in the range of [200, 18k] Hz
- less than 2dB ripple in the passband
- at least 22dB attenuation in both 50 and 90k Hz stopbands.

Since the Analog Filter Wizard over-designed the filter to have specs of:

- a passband in the range of [150, 22k] Hz
- stopbands of -30dB attenuation at 35 and 90k Hz
- <1dB ripple in the passband

the prototyped circuit with component tolerances considered met these requirements and is demonstrated in the following demonstration sheet (Figure 22) for a grade in EE 4113.

The passband ripple should be less than or equal to 2dB. The low-frequency passband corner should be 200Hz. The high-frequency passband corner should be 18kHz.	Set up an 2.0Vpp 1600Hz input sine wave. Display input V _{pp} on scope channel 1. Display output V _{pp} on scope channel 2. Set the volume control to about a 10Vpp output level. Use the function generator knob to scroll across the passband from 200Hz to 18kHz and identify the peak-to-peak value of A _{p,max} . Record this value to the right. Also record the value 0.79*A _{p,max} to the right. Now scroll again across the passband from 200Hz to 18kHz and verify that the output is never lower than 0.79*A _{p,max} .		
The low-frequency stopband corner should be 40Hz. The stopband attenuation should be at least 22dB below A _{p,max} .	Keep the same input amplitude settings as the prior measurement that yielded the value of A _{p,max} . Calculate and record to the right the value 0.0794*A _{p,max} . Set the frequency to 40Hz and carefully measure V _{out,pp} . Trigger on the stronger input signal and use trace averaging if necessary. V _{out,pp} should be smaller than 0.0794*A _{p,max} .		✓ 3
The high-frequency stopband corner should be 90kHz. The stopband attenuation should be at least 22dB below A _{p,max} .	Keep the same input amplitude and volume control gain settings as the prior measurement that yielded the value of A _{p,max} . Calculate and record to the right the value 0.0794*A _{p,max} . Set the frequency to 90kHz and carefully measure V _{out,pp} . Trigger on the stronger input signal and use trace averaging if necessary. V _{out,pp} should be smaller than 0.0794*A _{p,max} .		✓ 3

Figure 22: Grading sheet for testing the bandpass filter for Project 1B

3.2 Audio Power Amp Prototyping

The audio power amp sub-circuit was prototyped next. Similar to the filter prototyping process, this sub-circuit was first simulated fully in OrCAD as specified in section 2.2. The sub-circuit was prototyped in the remaining $\frac{1}{2}$ of the protoboard that was used to build the bandpass filter in 3.1. The BOM as generated by OrCAD is shown in Figure 23.

Item	Quantity	Reference	Part
1	2	C1,C2	1uF
2	4	C3,C5,C7,C8	0.1uF
3	2	C4,C6	0.01uF
4	2	C25,C26	100uF
5	1	M1	IRF510
6	1	M2	IRF9510
7	4	R1,R2,R3,R4	100k
8	2	R5,R6	100
9	1	R7	20
10	2	R8,R10	10k
11	1	R9	1k
12	1	U8	TL072/301/TI

Figure 23: BOM for the Audio Power Amp

Since the filter prototyping process setup the power rails, power supply capacitors, and trimmed the leads on the passive components, the prototyping of the audio power amp was a more seamless process. In addition, the E12 components with the same respective tolerances for both capacitors and resistors were also used in this sub-circuit.

The prototyping of the audio power amp was split into phases like the simulation process described in 2.2. First, the open loop biasing was established to put the audio power amp in Full Class B. Next, the cross over distortion was remediated by configuring the potentiometers to put the audio power amp in Class A/B. In this step, the DC power supply was toggled to “Current mode” where instead of displaying both ± 15 V rails on the LCD displays, the DC power supply displayed the amount of current in amps being consumed by the circuit. To remove the cross-over distortion, the potentiometers were each dialed until their respective power rail measured around 170 mA on the LCD of the DC power supply. Lastly, the closed loop configuration with volume control and pre-amp is setup to complete the entire sub-circuit.

It is worth mentioning that this prototyping process did have a different step of the process compared to the simulation. Both IRF510 and IRF9510 MOSFETS each received a heatsink to remediate the heat when running the audio power amp at full power ($\sim 3W$ on 20Ω load). When running the circuit at full power without heatsinks, the IRF9510 or the IRF510 can burnout and therefore each MOSFET obtained a conventional heatsink to prevent this.

3.2.1 Audio Power Amp Testing

The operation of the audio power amp was successful and met the specs as outlined in section 1.2. Figure 24 showcases the fulfillment of specs as part of the grade received for the project in the EE 4113 class.

The passband voltage gain must be adjustable over the range -5dB to 20dB.	Set up an 2.0Vpp 1600Hz input sine wave. Display input Vpp on scope channel 1. Display output Vpp on scope channel 2. Adjust potentiometer for a 1.12Vpp output to test -5dB gain. (You must be able to go at least this low. Even lower is perfectly acceptable.)	N/A	<input checked="" type="checkbox"/>	2
The passband voltage gain must be adjustable over the range -5dB to 20dB.	Set up an 2.0Vpp 1600Hz input sine wave. Display input Vpp on scope channel 1. Display output Vpp on scope channel 2. Adjust potentiometer for a 20Vpp output to test 20dB gain. (You must be able to go at least this high. Even higher is perfectly acceptable.)	N/A	<input checked="" type="checkbox"/>	2
The output should not display spurious oscillations at any gain setting.	If the output displayed spurious oscillations during tests 14a and/or 14b (even if trace-averaged out), deduct points, otherwise give full credit.	N/A	<input checked="" type="checkbox"/>	3

Figure 24: Audio power amp spec fulfillment

3.3 Combining the Filter and Audio Power Amp

Once both sub-circuits were tested in isolation, the output of the bandpass filter was connected to the input of the volume control, 10kΩ potentiometer. There were no other steps needed in the process of combining both the audio power amp and the bandpass filter as these were already built and tested in isolation. To test the entire circuit, signal was injected into the same 470pF capacitor, C7 through the alligator clip, and the x10 scope probe was moved to the 20Ω load, R7. This configuration completes the entire circuit as shown in Figure 25.

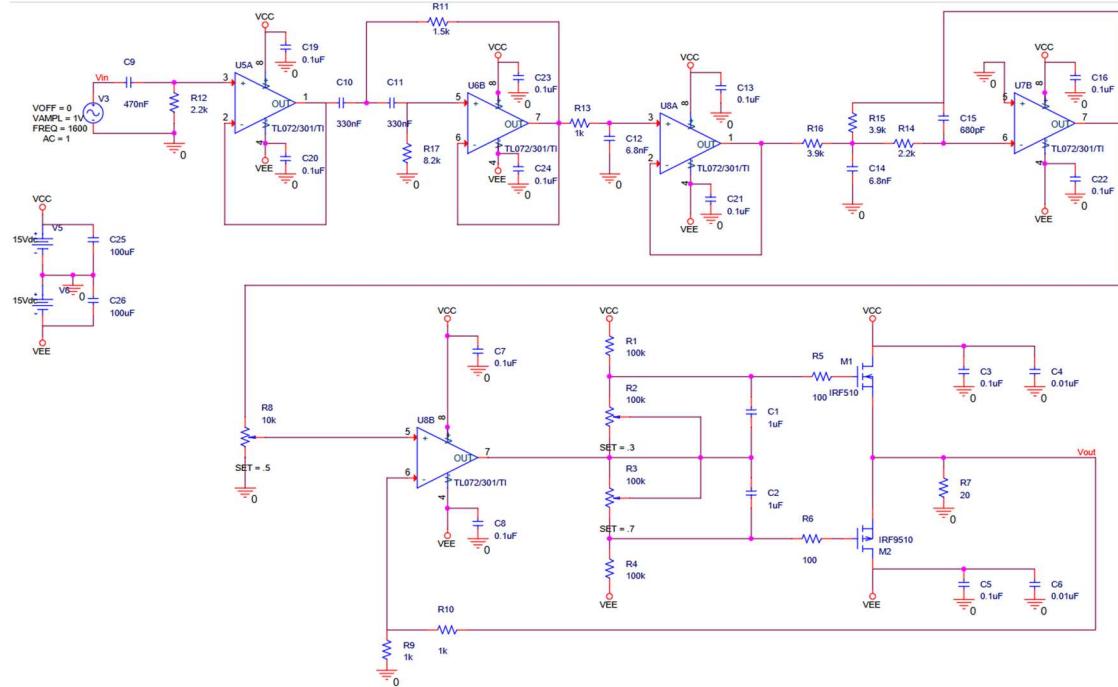


Figure 25: Complete circuit schematic of the audio frequency amplifier

4 PCB Design

The PCB Design process was completed in four phases. The first phase consisted of preparing the netlist in OrCAD for export to Allegro PCB Editor. The second phase consisted of designing the board layout in Allegro PCB Editor to obtain the gerber and drill files to print the PCB. The third and last phase consisted of soldering the components and testing each sub-circuit on the board. Next, the first phase will be discussed.

4.1 Netlist Preparation for Allegro PCB Editor

Before exporting the netlist to Allegro PCB Editor, simulation-only components such as Voltage sources had to be replaced with appropriate BNC and through-hole connectors. More specifically, the test sinusoidal source at the C9, DC decoupling capacitor was replaced by a BNC connector (BNC_5PIN) to input a signal from the function generator at the cost of the parasitics of the cable alone. In addition, through hole connections for DC power wires replaced the VDC voltage sources in the schematic with CON1 parts. Lastly, the power supply decoupling caps in the simulation schematic were replaced with CMAX components to account for electrolytic capacitors. These changes on the left part of the schematic in Figure 27.

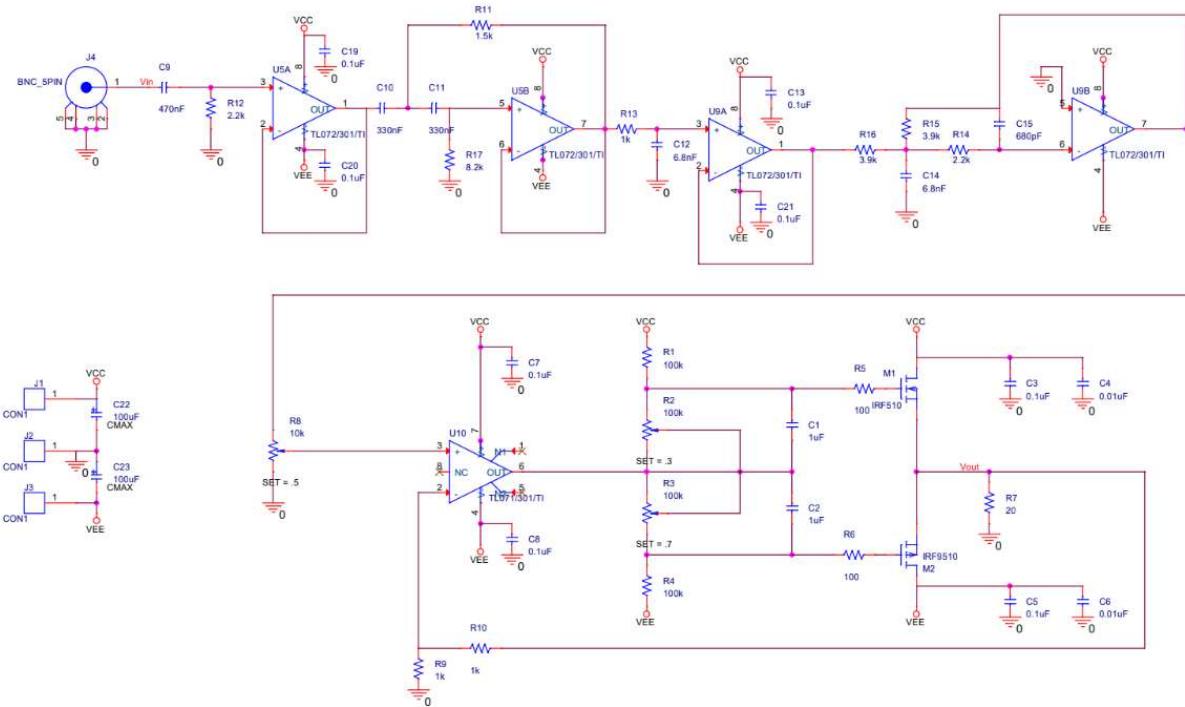


Figure 27: Schematic Prepared for Allegro PCB Editor

In addition to replacing the voltage sources in the schematic, the pinout configuration of the TL071 chip for the audio power amp had to be edited in OrCAD to account for unused pins. Since the pre-amp does not need a Voltage offset, pins 1, 8, and 5 on the TL071 chip were specified as NC (no connect) by editing the part in OrCAD. This measure was necessary to prevent errors when exporting the netlist to Allegro PCB Editor, because naturally, once the chip is soldered in the PCB, having a “floating” pin can cause undesired operation of the chip. Therefore, unused pins must be defined to prevent this. Figure 28 showcases the full BOM needed for the PCB.

Item	Quantity	Reference	Part
1	2	C1,C2	1uF
2	12	C3,C5,C7,C8,C13,C16,C19, C20,C21,C22,C23,C24	0.1uF
3	2	C4,C6	0.01uF
4	1	C9	470nF
5	2	C10,C11	330nF
6	2	C12,C14	6.8nF
7	1	C15	680pF
8	2	C25,C26	100uF
9	1	M1	IRF510
10	1	M2	IRF9510
11	4	R1,R2,R3,R4	100k
12	2	R5,R6	100
13	1	R7	20
14	1	R8	10k
15	3	R9,R10,R13	1k
16	1	R11	1.5k
17	2	R12,R14	2.2k
18	2	R15,R16	3.9k
19	1	R17	8.2k
20	4	U5,U9	TL072/301/TI
21	1	U10	TL071
22	1	J4	BNC_5PIN
23	3	J1,J2,J3	CON1

Figure 28: Full BOM for PCB

4.2 Board Layout through Allegro PCB Editor

Once the schematic was “prepared” in OrCAD Capture CIS, the netlist exported to Allegro PCB Editor. The main specifications of the PCB are as follows:

- board size of 4700 x 3400 mils
- top layer as ground plane and through hole parts
- bottom layer as ground plane and for signal traces
- 20 mil signal traces (component to component)
- 50 mil power traces (+15V for Vcc and -15V Vee)

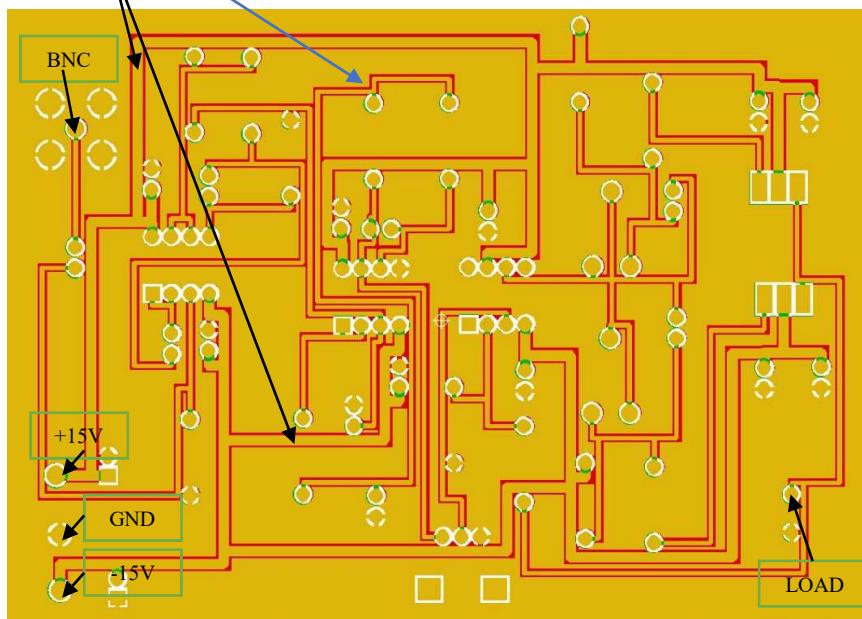


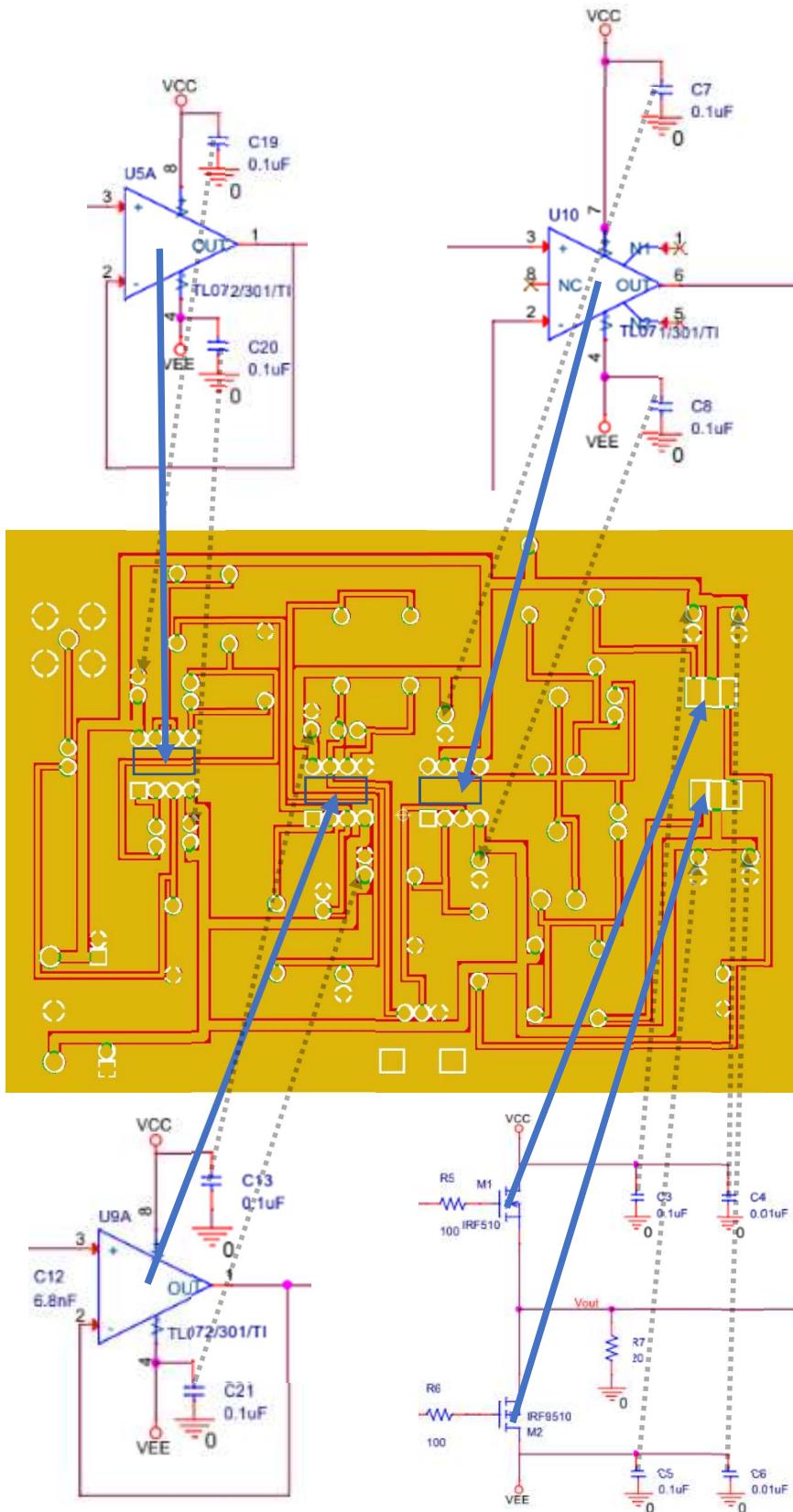
Figure 29: PCB Layout: Bottom Layer

The specs of key interest here are the 20 mil signal traces and 50 mil power traces. The latter were chosen to account for the high current needs of a +15 VDC rail which, with a greater width, reduce parasitic resistance and inductance. The width of the traces can be seen in Figure 29.

After configuring the PCB in Allegro PCB Editor to match the required specifications, each of the components were part placed on the board, following the signal path of the entire circuit. For example, the following input signal connectors were placed on the left side of the board for easy access as shown on the bottom layer of the PCB in Figure 29:

- The +15V through-hole connector is for the Vcc rail
- The -15V through-hole connector is for the Vee rail
- The GND through-hole connector is for earth ground (not chassis ground!)
- The BNC connector is for the input signal (9kHz, 2Vpp sin wave for testing)

Figure 30: Close placement of bypass capacitors to power pins



Another design choice of interest for part placement are the bypass capacitors. Both MOSFETS and IC's used bypass capacitors to reduce noise on the Vcc and Vee rails, and these were placed virtually adjacent to their respective power pins. The close placement of the 0.01uF and 0.1uF capacitors to the MOSFETS, TL072's and the TL071 is demonstrated in Figure 30 to the left.

Apart from the BNC, through-hole (J1-J3) power connectors, and bypass capacitors, the rest of the components were auto-routed by the Allegro PCB Editor software. Nevertheless, the board layout is analogous to the way the schematic is drawn out: signal comes in from the left and exits out the right. Before printing the PCB, the entire board was examined for coherency, and once all design rule check (DRC) tests were passed, the artwork files for the BOTTOM and TOP layers, as well as the OUTLINE (the border around the PCB) were generated (4).

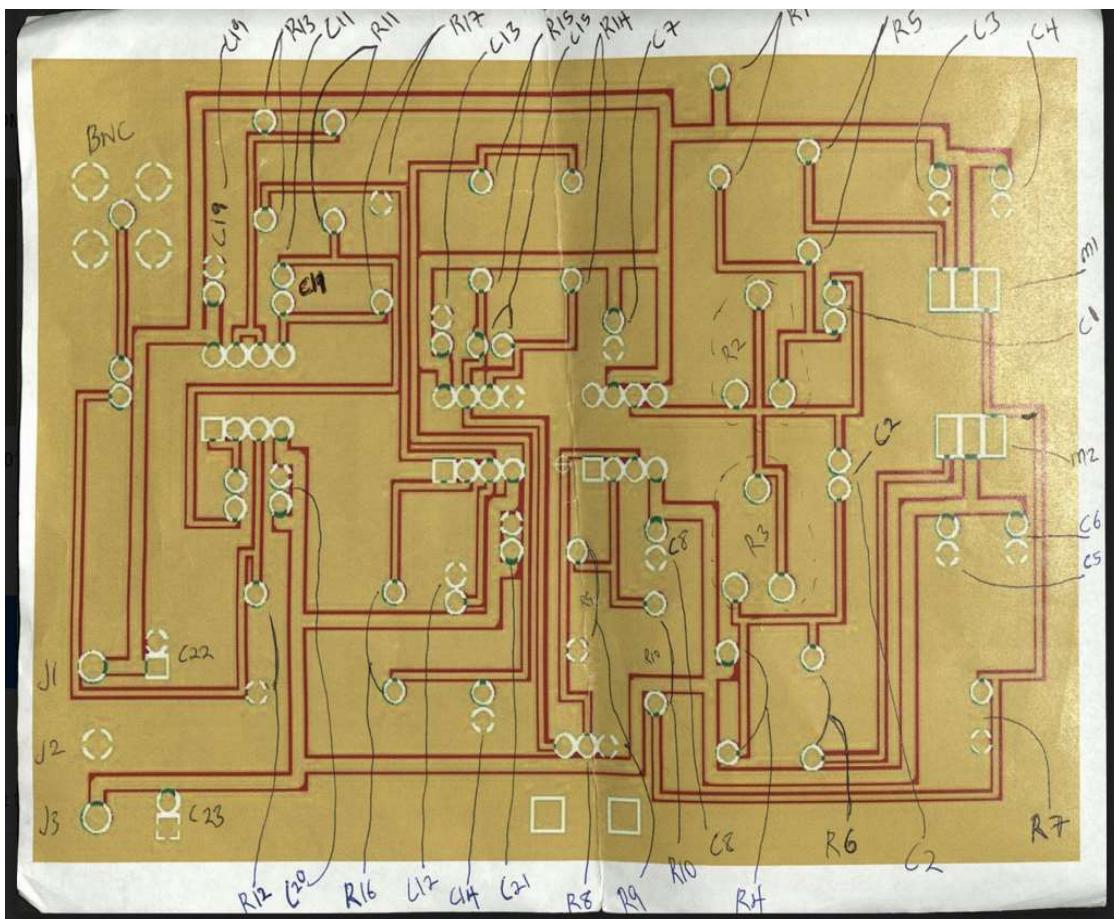
The addition of the drill file to the artwork files was the last step to print the PCB with the machine provided by the EE 4113 class.

4.3 PCB Soldering

After the board design with Allegro PCB Editor, the EE 4113 class delivered the PCB using FR-4 fiberglass as the board material. The first step in the PCB soldering process was to “ohm-out” the board to check for traces accidentally shorted to ground or places they shouldn’t be connected to (such as Vcc shorted to Vee, a capacitor’s pads shorted together, etc.).

Due to a mishap in properly making a backup copy of the artwork and drill files, the next step was to reverse engineer the board layout of the PCB to figure out which parts went where. Although time consuming, this step of the process was crucial for the author to learn not only of better documenting habits but primarily how to better understand the critical signal path of the circuit. The process was carried out by tracing the input signal from BNC all the way out to the load R7. Figure 31 showcases the reverse engineered PCB with accurate component markings.

Figure 261: Reverse engineered PCB layout

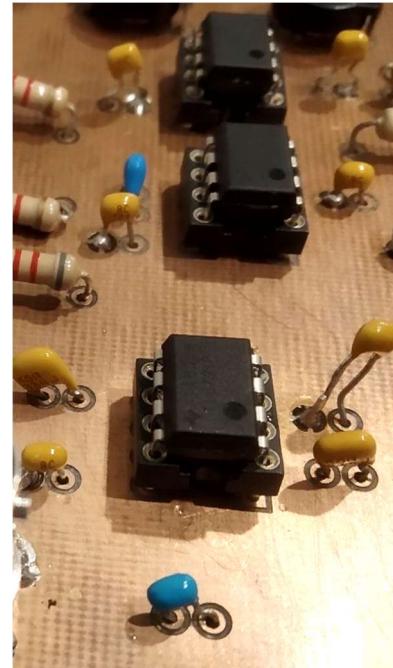


Once having a clear map of where components need to be, the second step in the soldering process was to make sure power is distributed in the board properly. To begin this process, the first soldered components were the power wires due to their critical nature in circuit operation. After the power wires, the 100uF electrolytic caps were soldered into the board. Then, all ceramic bypass capacitors (0.01uF and 0.1uF) were soldered. Lastly, all DIP sockets for use with the TL072 and TL071 chips were soldered into the board. Power was tested in the traces leading up to these components to ensure proper circuit operation. Figures 32 and 33 showcase the listed soldered components.

Figure 32: DIP sockets for IC's and 0.01uF/0.1uF bypass caps



Figure 33: 100uF power bypass caps and +15V (RED), -15V (YELLOW), GND (BLACK) wires



After checking proper power distribution, the volume controlled, and pre-amped class A/B audio amplifier was the first sub-circuit to be soldered and tested on the board. Similar to the simulation and prototyping processes, the class A/B power amp was built and tested in three phases: first the open loop configuration was soldered and tested to operate in full class B (crossover distortion visible); Secondly, the two bias potentiometers, R2 and R3, were modified in resistance by dialing them one by one until the output on the oscilloscope removed the cross over distortion and set the operation of the amplifier into class A/B; Thirdly, the pre-amp with a gain of 11 and the volume control 10k potentiometer were added to the configuration and tested with a 2Vpp 9kHz sine wave into pin 7 of the TL071.

Once the audio amp sub-circuit was performing up to spec, the filter was prototyped and soldered on next. The same process of prototyping the circuit on the protoboard took place for the filter stage: first solder and test the high pass filter; after expected operation is tested from the high pass filter, solder and test the low pass filter together. Figure 34 displays the finished PCB (top and mirrored bottom layer).

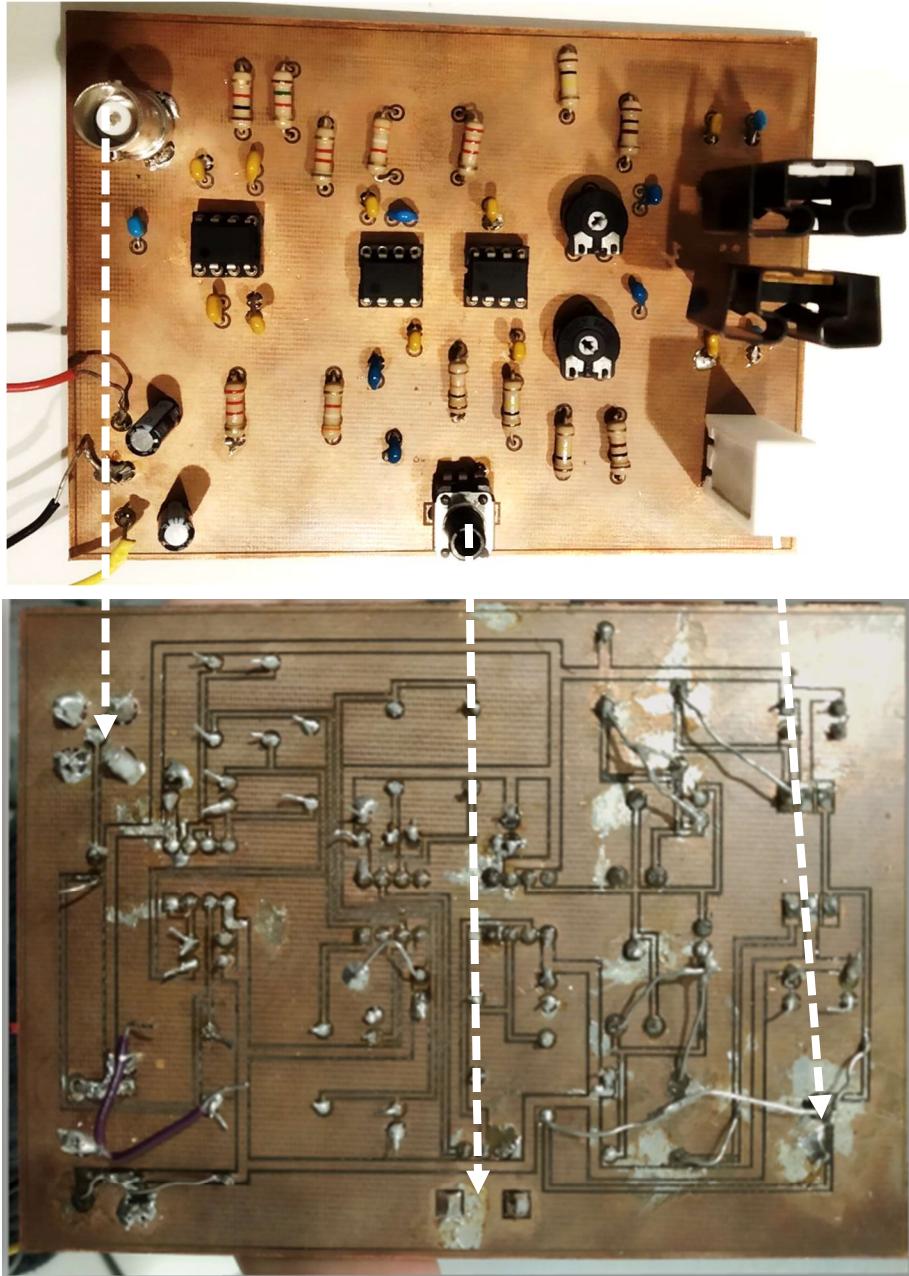


Figure 34: Top and bottom views of the completed PCB soldering process

4.4 Testing

Once the full audio frequency amplifier circuit was soldered in the board, the PCB testing phase went into effect. The board was tested to ensure it met the specifications outlined in section 1.2. The testing phase was divided into two methods:

- testing the output waveforms in the time domain with the oscilloscope
- testing the output waveform in the frequency domain with the oscilloscope's FFT

For the first test in the time domain, a 2Vpp sinusoidal signal was used to “sweep” the circuit for measuring the gain to validate the spec requirements.

For the second test in the frequency domain, a 2Vpp sinusoidal signal was also used to “sweep” the circuit for calculating the Total Harmonic Distortion (THD), and Signal to Noise Ratio (SNR). Sections 4.4.1 and 4.4.2 demonstrate both tests to complete the validation of the circuit’s performance.

4.4.1 Verifying Specifications in the Time Domain

The oscilloscope was used to test the full circuit in the time domain to verify it meets the required specifications. First, the DC power supply wired GND, +15V, and -15V into the circuit. Next, a 2Vpp sinusoidal waveform was input into the BNC connector from the function generator available. To probe the circuit, a x10 scope probe was affixed to the upper lead of the 20Ω load R7 and displayed on channel 1 (yellow) of the oscilloscope. The input sin wave from the function generator was probed with a x1 alligator clip probe and displayed on channel 2 (blue) of the oscilloscope. The ground clips of both scope probes were affixed to the same GND through-hole connector incoming from the DC power supply.

Now, with the volume control potentiometer at the highest setting to allow the full 2Vpp waveform to reach the input of the pre-amp, the function generator was used to “sweep” the circuit with the sine wave at the following frequencies:

- 40 Hz to test the stopband gain spec of >22dB
 - 200 Hz to test the gain in the pass band lower limit
 - 9 kHz to test the gain in the “mid band”
 - 18 kHz to test the gain in the passband upper limit
 - 90 kHz to test the stopband gain spec of >22dB

When the sweep reached 40Hz, the oscilloscope showed a gain of

$$\text{AvdB} = 20\log(1.60/2.16) = -2.6\text{dB}$$

at the load in Figure 35. However, since channel 1 is set to 10.0V of division, this measurement seems incorrect and the spec must have passed.

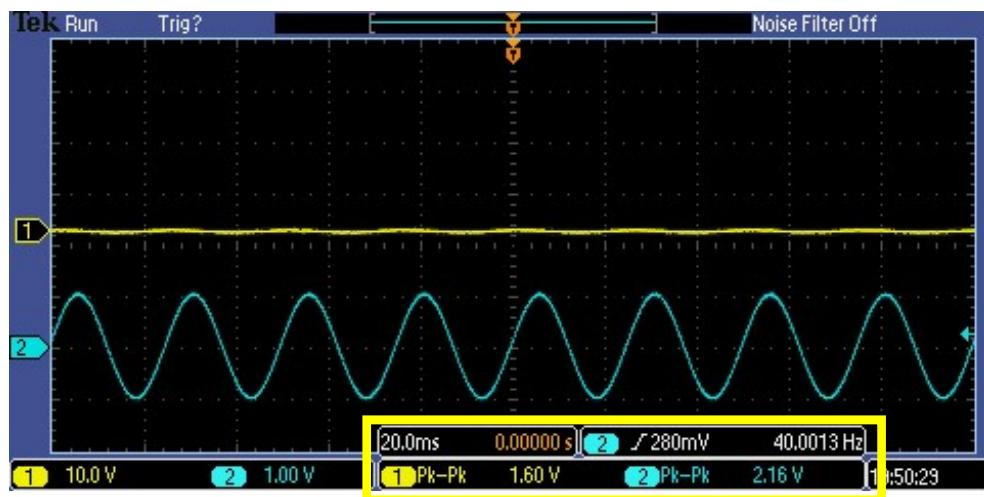


Figure 275: 2Vpp 40Hz input shows -2.6dB of gain

At 200 Hz, the passband lower limit, the oscilloscope displayed a gain of

$$\text{AvdB} = 20\log(22.4/2.08) = 20.644 \text{ dB}$$

at the load in Figure 36 which certainly meets spec! Interestingly, there seems to be a slight of phase difference in the output signal, which must be due to the 3rd order Chebyshev's high pass filter group delay graph.

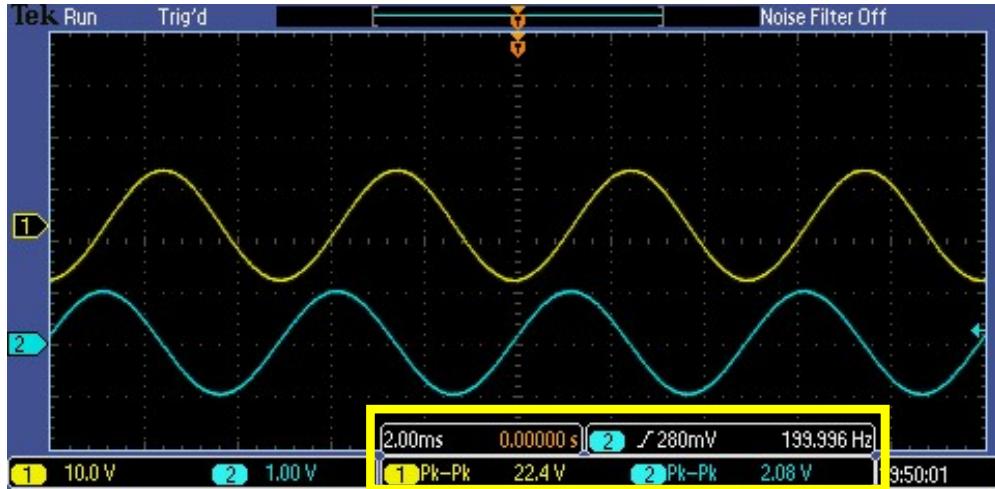


Figure 36: 2Vpp at 200Hz shows 20.644dB of gain at the load

Further sweeping the signal up to 9 kHz—the “mid-band”, the oscilloscope displayed a gain of

$$\text{AvdB} = 20\log(20.8/2.08) = 20\text{dB}.$$

The load certainly displays in Figure 37 that the audio frequency amplifier met spec at the “mid-band” frequency at full power. There is also less phase difference than at 200 Hz.

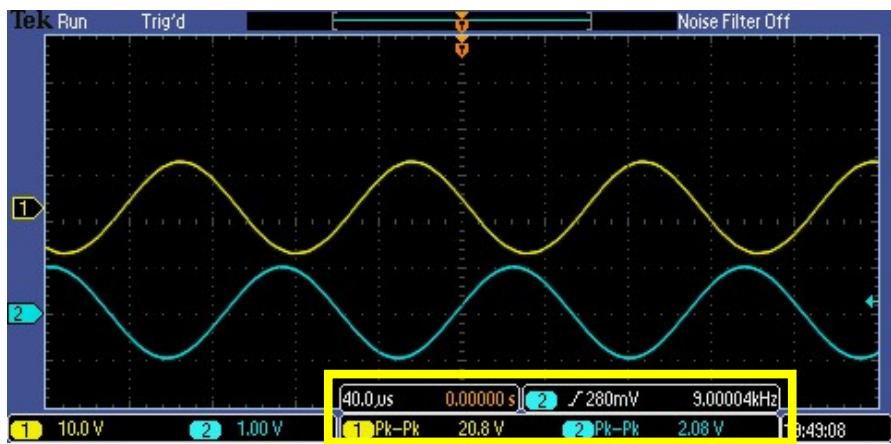


Figure 37: 2Vpp at 9kHz shows 20dB of gain at the load

Going up to 18kHz, the passband upper limit, the oscilloscope displayed a gain of

$$\text{AvdB} = (18.4/2.08) = 18.94 \text{ dB.}$$

This measurement does not meet spec of the minimum 20 dB as shown in Figure 38. However, it is likely there must not have been the correct volume control setting for the input of the pre-amp to see the full 2 Vpp since the rest of the frequencies have been meeting spec. There's also a phase difference due to the 3rd order Chebyshev's group delay response.

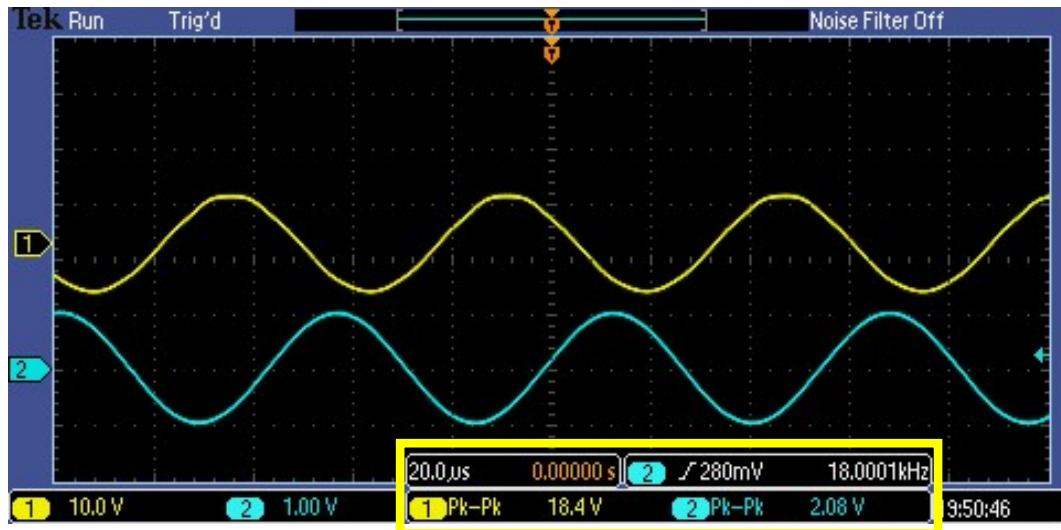


Figure 288: 2Vpp at 18 kHz shows a gain of 18.94dB at the load

Lastly, the function generator was swept to the stopband at 90 kHz, and the oscilloscope as shown in Figure 39 displayed a gain of

$$\text{AvdB} = 20\log(14.4/2.20) = 16.32 \text{ dB}$$

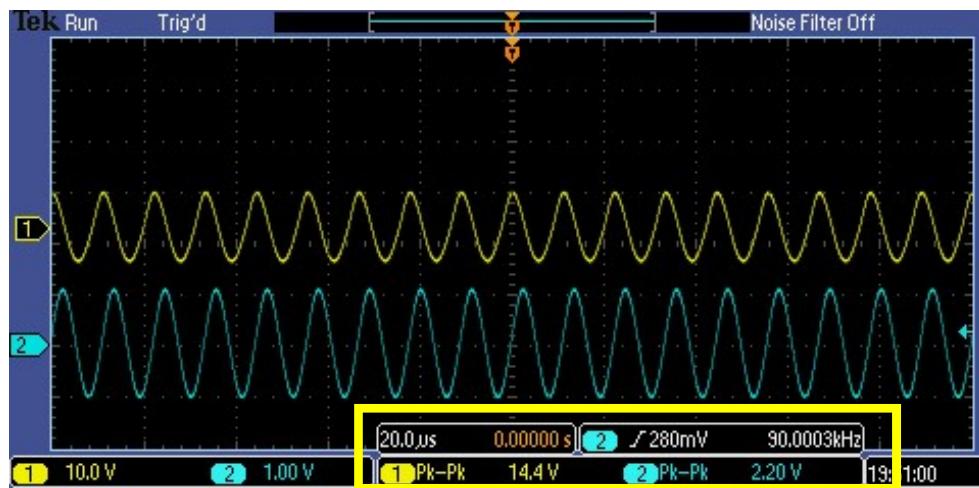


Figure 299: 2Vpp at 90 kHz shows 16.32 dB gain at the load

This measurement certainly does not meet the spec and further testing will need to be done to understand why it failed spec. When prototyping the board, every spec requirement was met. There must have been a “dead spot” where the filter does not operate as intended but the exact cause is still unknown.

4.4.2 THD and SNR Calculations in the Frequency Domain

To calculate the THD and SNR of the circuit, the same test signal frequencies that were used for 4.4.1 will be used in this section. The amplitude of the test signal will remain the same at 1V for a peak-to-peak voltage of 2Vpp. Vout remains connected to the oscilloscope's yellow, channel 1, and Vin remains connected to the blue, channel 2. However, some tests were erroneously conducted and their input Vpp might be subject to changes from the 2Vpp.

First the 40 Hz stopband was analyzed with the FFT function of the oscilloscope shown in Figure 40. Here, the input test signal was erroneously set to 160mV, which must have been the volume control knob at its lowest setting. Thus, no THD or SNR calculation can be made.

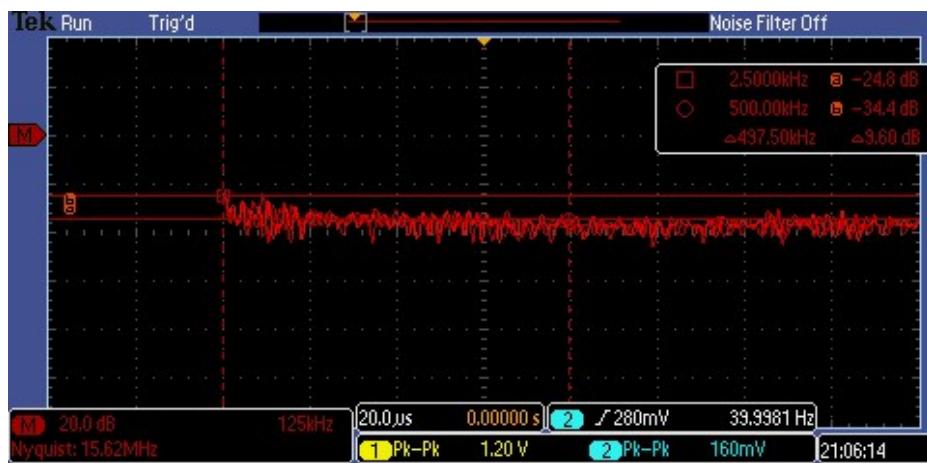


Figure 40: FFT of output signal at the load with a 160mV 40Hz input

To remediate this error, a 100 Hz, 560mV input signal is shown in Figure 41. Here, the SNR is 32.8dB and there are no other visible harmonics so THD cannot be computed.

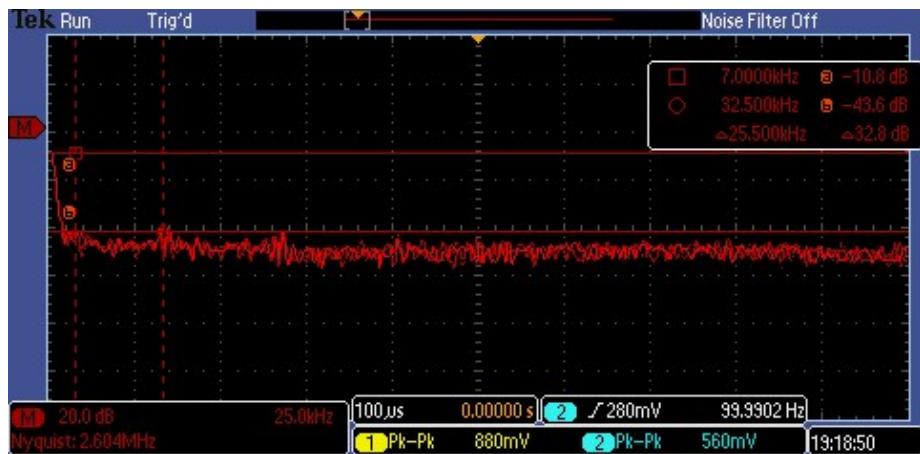


Figure 41: Input 560mV 100 Hz shows a 32.8dB SNR

Another test at 200 Hz was conducted as shown in Figure 42. This test shows a remarkable SNR that meets spec with 50.4dB. In addition, there is not a THD computed because there are no visible harmonics.

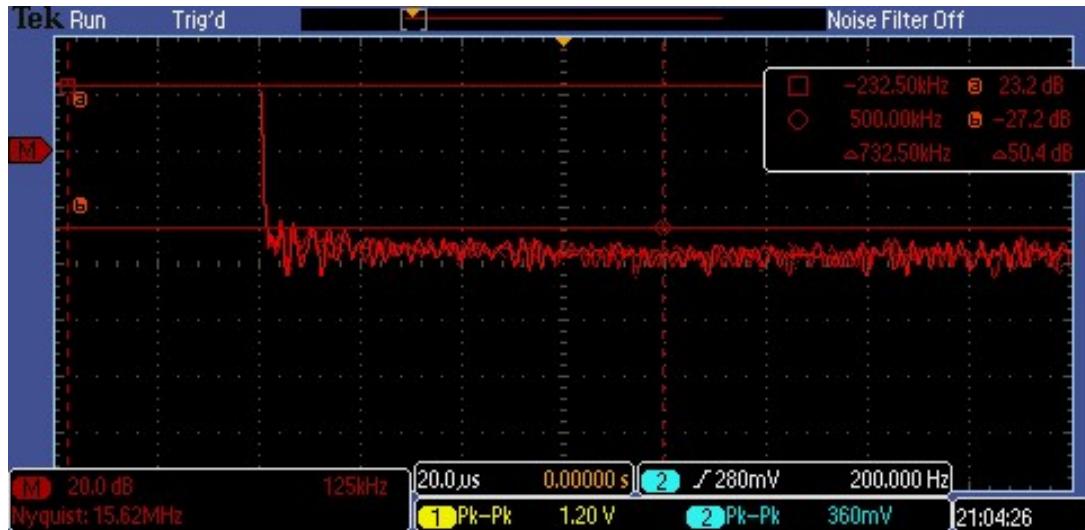


Figure 302: Input 200Hz 360mV shows a 50.4dB SNR

To test the “mid-band”, a 9 kHz, 2Vpp sine wave was used. Here, the SNR passes spec with 46.8dB and there are no visible harmonics shown in Figure 43.

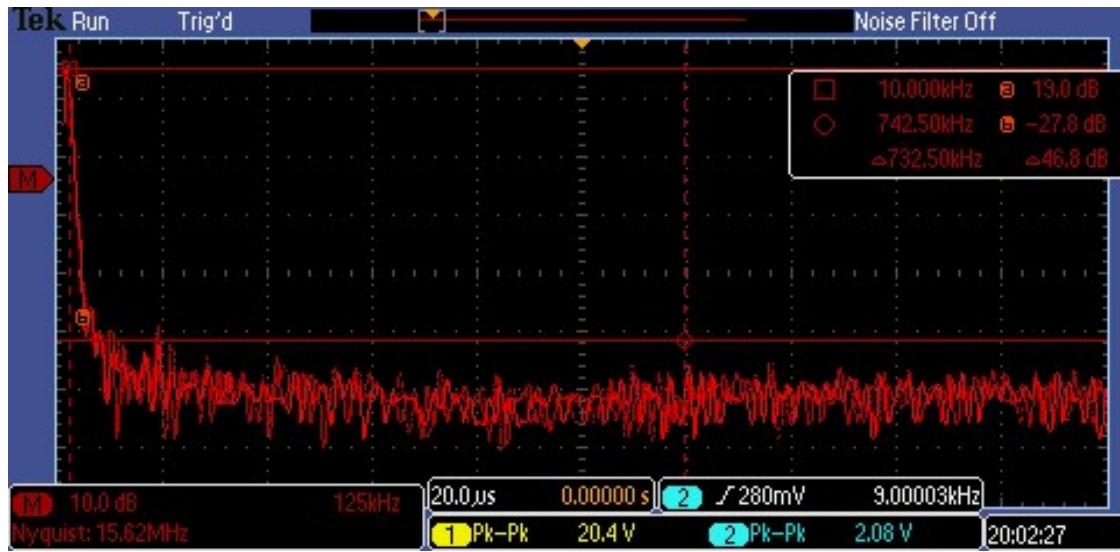


Figure 313: Input 2Vpp at 9 kHz shows a 46.8 dB SNR

To test the upper limit of the passband, an 18 kHz 2Vpp test sine wave was input to the circuit. Figure 44 displays a SNR of 38.4dB which meets spec. There are no visible harmonics, but there appears to be the formation of one three grid points to the right of the fundamental.

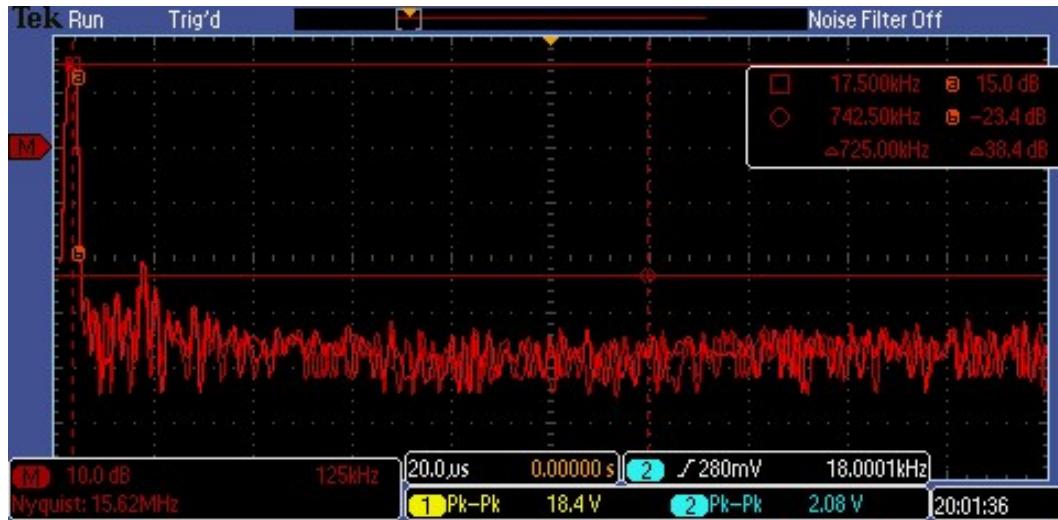


Figure 44: Input 18kHz 2Vpp shows 38.4dB of SNR

Lastly, to test the upper stopband at 90kHz, a 2Vpp 90 kHz sine wave was used as the input. First, the SNR is calculated in Figure 45. The oscilloscope shows an SNR of 47.2 dB which meets the minimum of 22dB attenuation spec.



Figure 45: Input 90kHz 2Vpp shows 47.2 dB of SNR

Furthermore, there are 3 visible harmonics. These are displayed in Figures 346-348. To calculate the THD, the voltage in amplitude for each of the harmonics will be calculated next.

- Fundamental: 18.0 kHz, $V_m = 2V_{pp} / 2 = 1.00 \text{ V}$
- 2nd harmonic: 172.5 kHz, $V_m = 10^{-(-10.4 \text{ dB} / 20)} = 0.302 \text{ V}$
- 3rd harmonic: 265 kHz, $V_m = 10^{-(-19.2 \text{ dB} / 20)} = 0.110 \text{ V}$
- 4th harmonic: 357.5 kHz, $V_m = 10^{-(-24.0 \text{ dB} / 20)} = 0.0631 \text{ V}$

$$\% \text{ THD} = 100 * (0.302^2 + 0.110^2 + 0.0631^2) / (1.00^2) = 10.7\%.$$

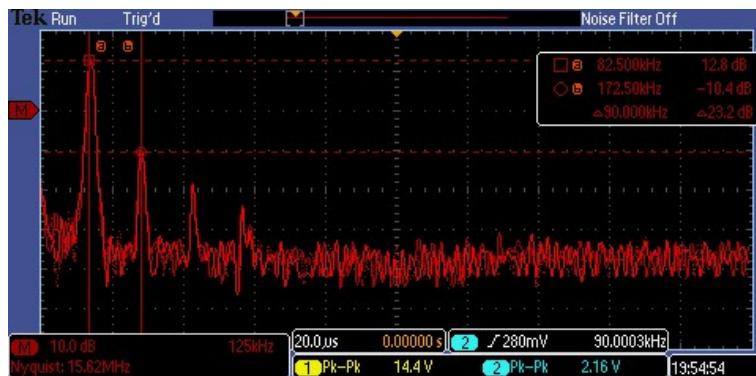


Figure 346: 23.2dB drop between fundamental and 2nd harmonic

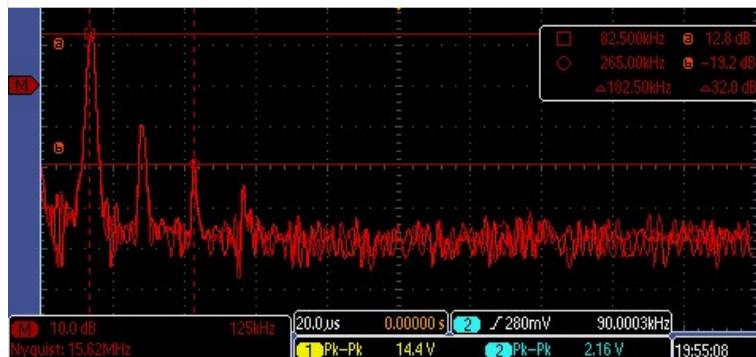


Figure 347: 32.0dB drop between fundamental and 3rd harmonic

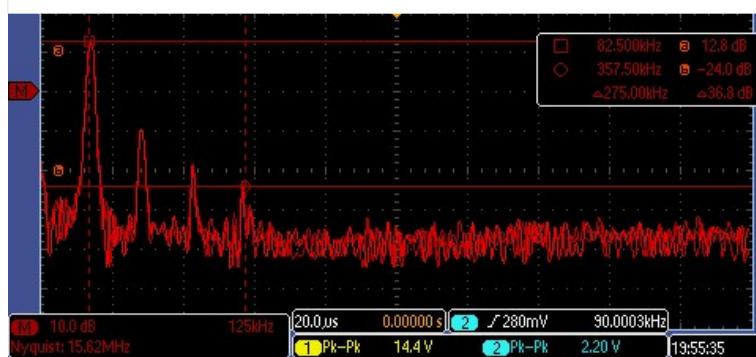


Figure 348: 35.8dB drop between fundamental and 4th harmonic

5 Conclusion and Reflections

Although the audio frequency amplifier met all the required specifications in both simulation and the prototyping phase, the PCB circuit provided several difficulties which impacted the testing phase in section 4. Further, the PCB circuit is supposed to provide huge performance increases primarily using ground planes which reduce parasitics in the circuit, but these did not reach their full fruition due to the reasons specified in 5.1 to 5.3. Besides the PCB performance, the author's personal thoughts on the project are elaborated in section 5.4

5.1 Broken Traces on the PCB

First, when soldering the components on the PCB, several traces were ripped off from the FR-4 fiberglass due to high temperature soldering and continuous switching of lead-based vs lead-free solder. There were also times that pins were “bridged” or shorted together by leaking solder from one of the component’s leads to the other. This caused for a need of solder wick, and continuous heating up of the fiberglass resulted in more broken traces. In other cases, the solder from the pad of a component’s lead would leak to the ground plane, and the whole trace leading up to the component would be shorted to ground as a result. Solder wick was used again to fix the trace which damaged the durability of the copper on the fiberglass.

In the worst cases, paths from the component lead to the rest of the trace were completely ripped off and left the lead “floating.” Short pieces of wire had to be soldered to the lead on one side and to the trace on the other. Fixes such as these contributed to the parasitics and reliability of the circuit, which caused the circuit to fail some tests as shown in section 4.

Most of the problems with ripped traces were caused by both the author’s erroneous technique and the usefulness of the soldering iron. After the tip of the iron was replaced, tinned, and always protected by being covered in solder, there was little to no difficulty heating up the solder pads on the PCB, which led to fewer bridged pins and broken traces.

5.2 Burned Out Components

Prior to compiling the SNR and THD calculation screenshots from the oscilloscope in section 4.4.2, the IRF9510 MOSFET overheated and eventually “burned out” when testing the circuit with a 200 Hz, 2Vpp input sine wave on the pre-amp. This made be due to the characteristics of the Chebyshev filters’ passband ripple, which caused the MOSFET to receive a little too much current, but further testing would need to be done to confirm this speculation. Despite the

MOSFET having a heatsink or “hat”, the volume had to be controlled when sweeping the input signal around 200 Hz to prevent another burn out after replacement.

5.3 Gain Glitch

During the testing phase of the final PCB circuit, the output voltage at the 20Ω load showed a “flatline” when increasing the volume from 10Vpp to 15Vpp. There are no known reasons for this glitch, but the best guess for this error was a manufacturing defect on the potentiometer: If the wiper in the 10k volume control potentiometer did not make proper contact at $\frac{1}{2}$ the volume setting to $\frac{3}{4}$ setting, the noninverting pin of the pre-amp would be left floating and no voltage would reach the load.

5.4 Final Thoughts

To say the least, this project challenged my engineering skills to the point of making me yearn to take another analog circuits lab. With this project alone, I learned how to design and simulate circuits using OrCAD, how to construct custom PCB’s for better circuit performance, soldering techniques, a deeper understanding of oscilloscope measurements, noise reduction techniques, the importance of controlled temperature for components, and above all, circuit debugging techniques.

The only thing I would like to have changed in the scope of the project would be to change to 20Ω load with an actual speaker to have some fun testing out the bandpass filter with music. Although this could easily be done by de-soldering the power resistor load and replacing it with a 20Ω , it would have been intriguing for it to be part of the actual project requirements for the grade in the class.

Lastly, as a Computer Engineering senior, I can truly say that EE 4113, or the “Lab 2” course made me deviate a little from my previous affinity for embedded systems. Given my concentration is in Digital Signal Processing due to my love for music equipment and production techniques, my future educational career seems to gear more towards an analog oriented approach rather than digital as a result of taking this course. Thank you Professor Hansen for your patience and instruction.

6 References

- (1) <https://www.analog.com/designtools/en/filterwizard/>
- (2) <http://www.myclassbook.org/harmonic-distortion-analyzers/>
- (3) <https://www.adafruit.com/product/239>
- (4) Complete PCB Design Using OrCAD® Capture and PCB Editor, by Kraig Mitzner, Newnes, 2009, ISBN 978-0-7506-8971-7.

7 Appendices

7.1.1 Further Images of Completed PCB

