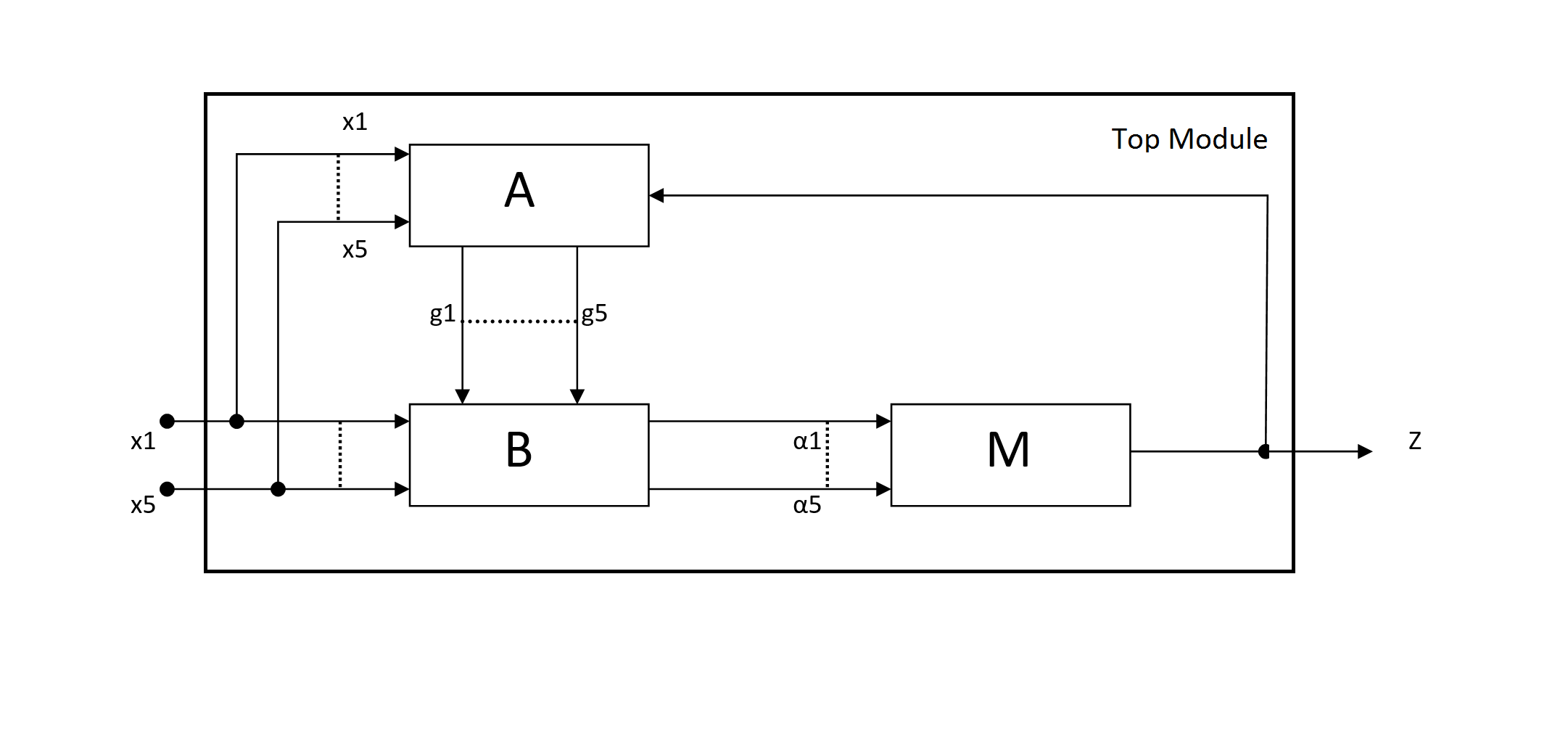
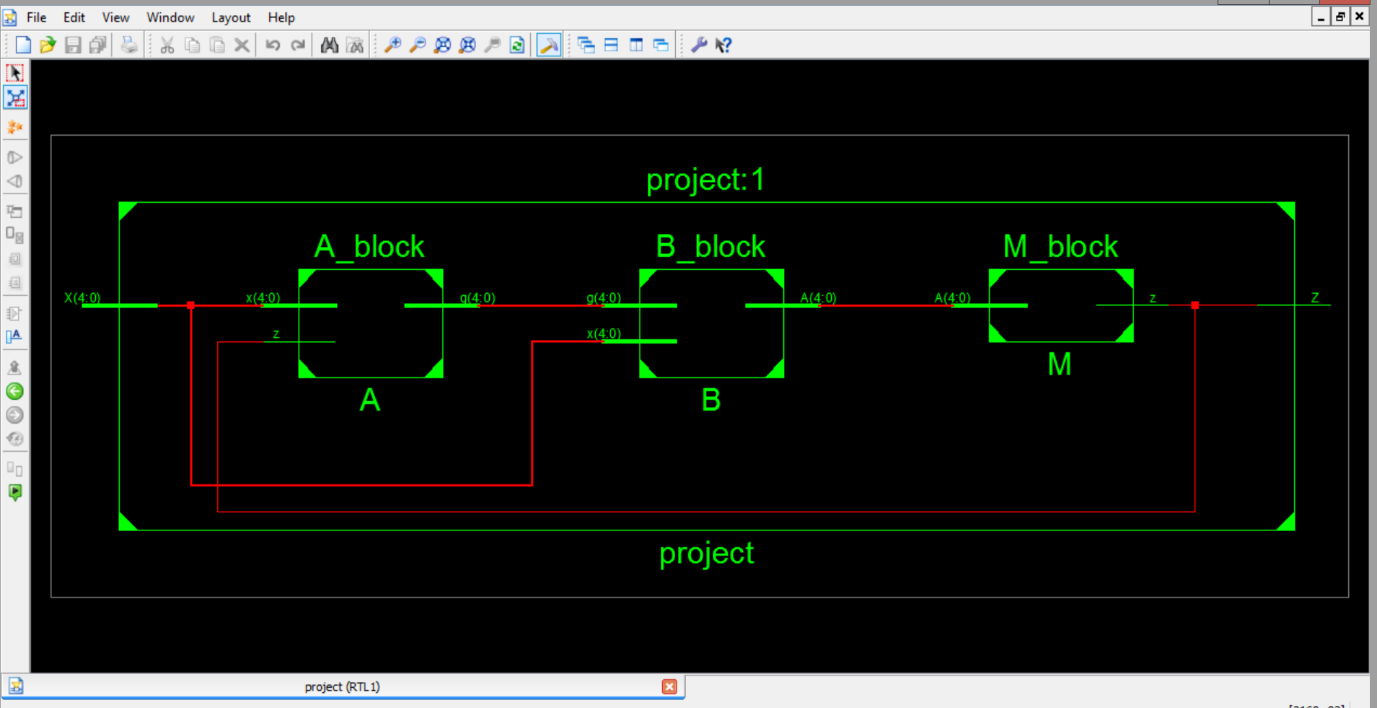
The complete system was designed by first dividing it into three blocks A, B and M with independent functions. The arrangement of the blocks was done as shown in the figure below. The entire module took five 1-bit input values and produced one 1-bit output. The detailed operation of individual blocks had to be described as modules using Verilog language code and combined together to form one complete module.



The values provided at primary input ports to the top module are the outputs from five copies of the system to which redundancy has to be provided. These input ports are connected to both A and B modules. The output at Z is the primary output port of the system, which gets its value from the output port of module M.

Module A is involved with generation of the intermediate output values by first comparing the five Figure RTL Schematic of Blocks A, B and M in the top module project. primary input values with the primary output value. These intermediate values, along with the primary inputs are used in the B module to provide another range of intermediate output values. The M module, basically performs the majority function to these intermediate values which produce the primary outputs.

The RTL schematic of the proposed 5MR with automatic reconfiguration is shown above.