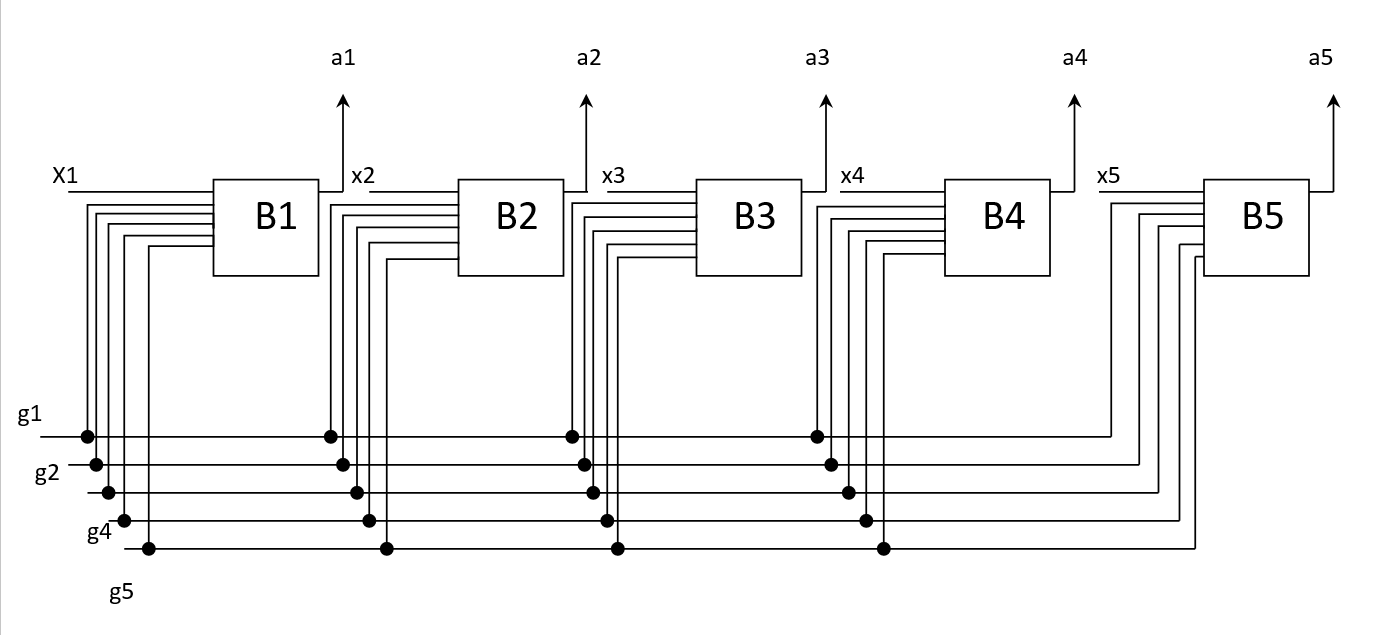
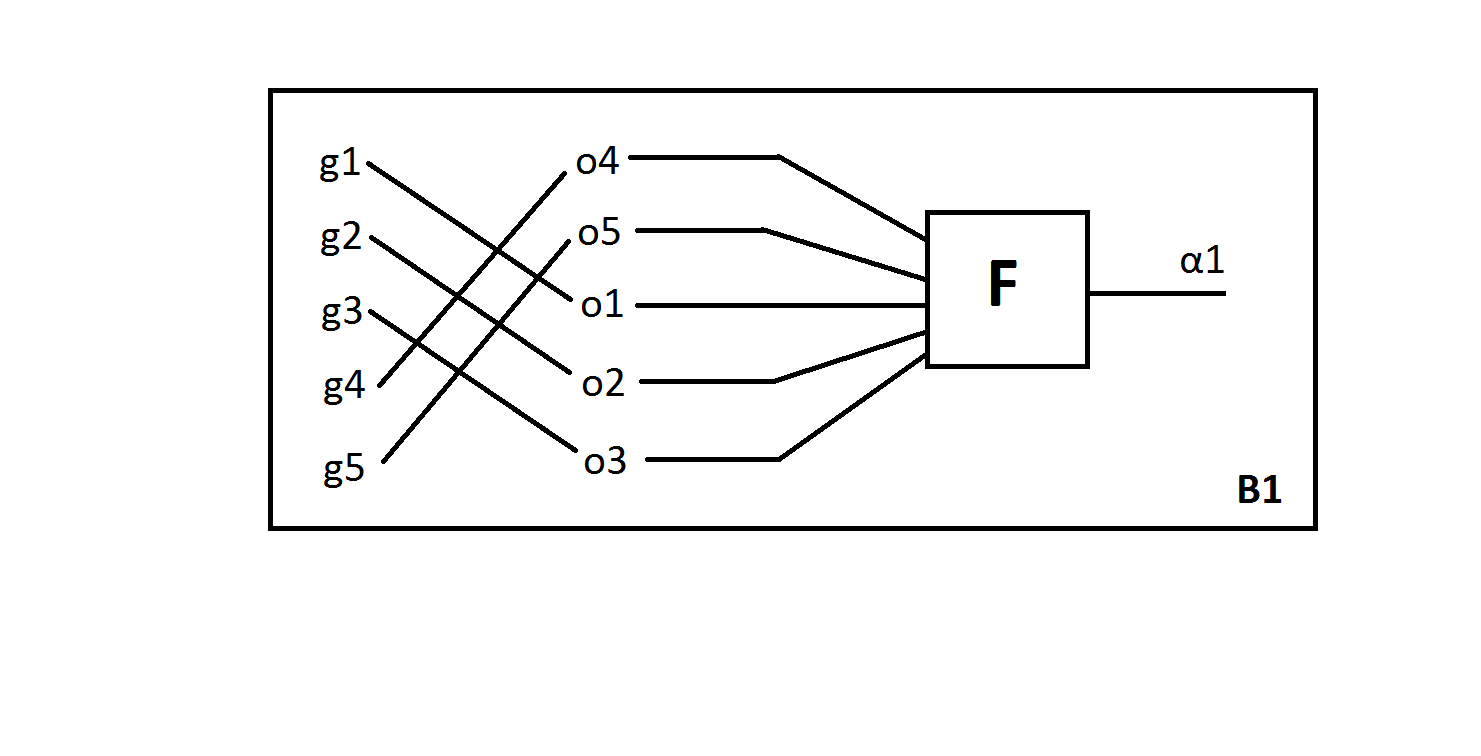
The task of designing the B block basically involved combinational circuits and describing a function (F) which took a 5-bit input to produce a 1-bit output. This block had to take the values from primary inputs as well as the intermediate outputs generated by the block A and produce the value of αi’s according to the equation below. Since we require five αi’s, we need to perform operations using five blocks which have the common function (F), however the order of the inputs would have to be changed for every block.

This equation is derived from the three conditions that are to be fulfilled for the successful reconfiguration of a 5MR into a TMR. The conditions are stated as follows. i) αi=0for the faulty ith input ii) αi+1=1 for the immediate next (i+1)th value and iii) αi =xi for every other value of i. This is a generalized equation which can be applied when there is one fault as well as the condition where there are two faults also. The basic functional diagram of the B block is given below.

At each block B which ranges from B1 to B5, we need to produce a different combination of the intermediate output (g) values and for the first module, it is described below. Upon rearrangement of inputs using the appropriate assignment of wires and intermediate registers, the resultant arrangement of the 5-bit wire will have the function (F) applied to it. After the application of the function, the output thus produced will be a 1-bit value. Four more blocks are to be created with the arrangement of the orders changing. For example, 12345 will be rearranged as 45123 in the B1 block and will be rearranged as 51234 in the B2 block and 12345 in the B3 block and this pattern continues till B5 block. The five outputs of these blocks are combined as the primary outputs of the block B itself. This ensures that the above conditions are satisfied.



The RTL schematics of the Block B are given below and provide an idea of the function (F) in the form of combinational gates.

