American International University- Bangladesh
Department of Electrical and Electronic Engineering
EEE2104: Digital Logic Design Laboratory

Title: Design of Multiplexer (MUX) and Demultiplexer (DEMUX).

Introduction:

In this experiment students will learn how to design and implement multiplexers (MUX) and demultiplexers (DeMUX) of different sizes using basic logic gates. They will also learn how to construct bigger multiplexer using smaller multiplexers.

Theory and Methodology:

A multiplexer (or mux) is a device that selects one of several inputs and forwards the selected input into a single line. A multiplexer of 2^n inputs has n selection lines, which are used to select which input has to be sent to the output. A multiplexer is also called a data selector.

A demultiplexer (or demux) is a device taking a single input and selecting one of many data-output-lines, which is connected to the single input.

Multiplexer:

In computer system, it is often necessary to choose data from exactly one of a number of possible sources. Suppose that there are four sources of data, provided as input signals D_0 ,D_1, D_2 and D_3. The values of these signals change in time, perhaps at regular intervals. We want to design a circuit that produces an output that has the same value as either D_0 or D_1 or D_2 or D_3, dependent on the values of two selection pins S_1 and S_0. Here, the number of selection pin is two. Four combinations are possible using these two selection pins S_1 and S_0, such as (S_1, S_0) = (0,0), (0,1), (1,0), (1,1). Each combination is dedicated for each input. Let us consider the output variable is f. Now if $S_1 = 0$ and $S_0 = 0$ then $f = D_0$, if $S_1 = 0$ and $S_0 = 1$ then $f = D_1$, if $S_1 = 1$ and $S_0 = 0$ then $f = D_2$ and if $S_1 = 1$ and $S_0 = 1$ then $f = D_3$.

It is important to know that there is a relationship between the number of input and the number of selection pins. If the number of selection pin of a MUX is n, then maximum 2^n inputs are possible for that MUX. And the MUX will be called as 2^nto1 line MUX. The MUX we are going to design is a 4to1 MUX. There could be also 2to1 MUX, 8to1 MUX, 16to1 MUX etc.

For our design, there are 4 inputs and 2 selection pins. So actually we have 6 inputs. Now if we draw the truth table for 6 different inputs, there will be 64 input combinations. But fortunately we can do it in a more convenient way as given below.

Table:1

S_1	S_0	f
0	0	D_0
0	1	D_1
1	0	D_2

1	1	D_3

From the above truth table, we can write the function as given below.

$$f = \bar{S_1}\bar{S_0}D_0 + \bar{S_1}S_0D_1 + S_1\bar{S_0}D_2 + S_1S_0D_3 \ldots (1)$$

The logic circuit of the equation (1) is given in figure 1.

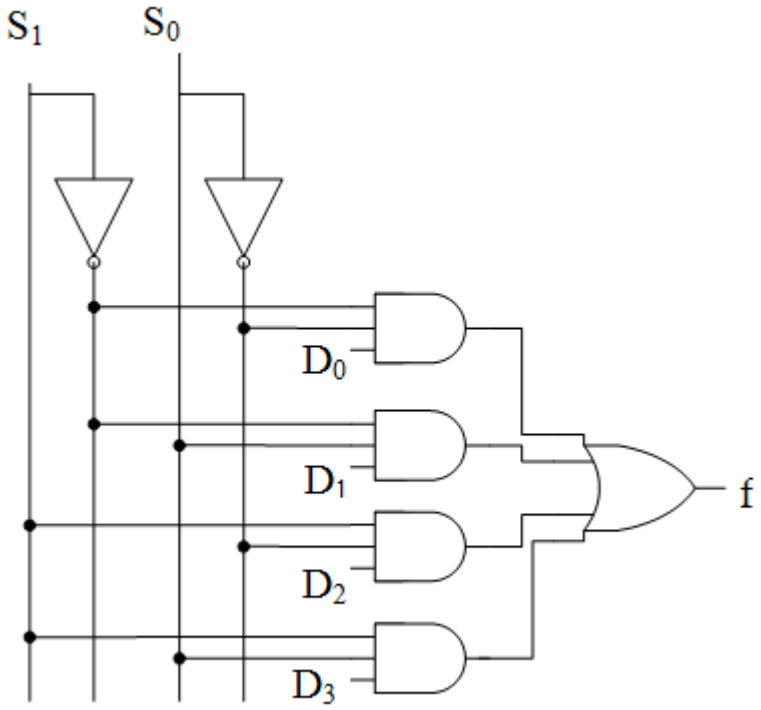

Figure1: 4to1 Multiplexer

Demultiplexer:

A Demultiplexer or Demux is opposite to the multiplexer. It has only one input and several outputs and one or more selection pins. Depending on the combination of selection input, the data input will be routed to one of many outputs. Other inputs will be low. Depending on the number of output, demultiplexers are termed as 1to2, 1to4 and 1to8 demultiplexers etc. If the number of selection pin is n, then maximum 2^n outputs can be accommodated.

We are going to design a 1to4 line demux having an input D_{in}, two selection pins S_1 and S_0 and four outputs D_0 ,D_1, D_2 and D_3. Now if $S_1 = 0$ and $S_0 = 0$ then $D_0 = D_{in}$, if $S_1 = 0$ and $S_0 = 1$ then $D_1 = D_{in}$, if $S_1 = 1$ and $S_0 = 0$ then $D_2 = D_{in}$ and if $S_1 = 1$ and $S_0 = 1$ then $D_3 = D_{in}$. We can draw the truth table as given below.

Table:2

S_1	S_0	D_0	D_1	D_2	D_3
0	0	D_{in}	0	0	0
0	1	0	D_{in}	0	0

1	0	0	0	D_{in}	0
1	1	0	0	0	D_{in}

From the above truth table we can write the functions for D_0 ,D_1, D_2 and D_3 as given below.

$D_0 = \overline{S_1}\overline{S_0}D_{in}$ … (2)

$D_1 = \overline{S_1}S_0D_{in}$ … (3)

$D_2 = S_1\overline{S_0}D_{in}$ … (4)

$D_0 = \overline{S_1}\overline{S_0}D_{in}$ … (5)

The circuit for 1to4 line demux is given below.

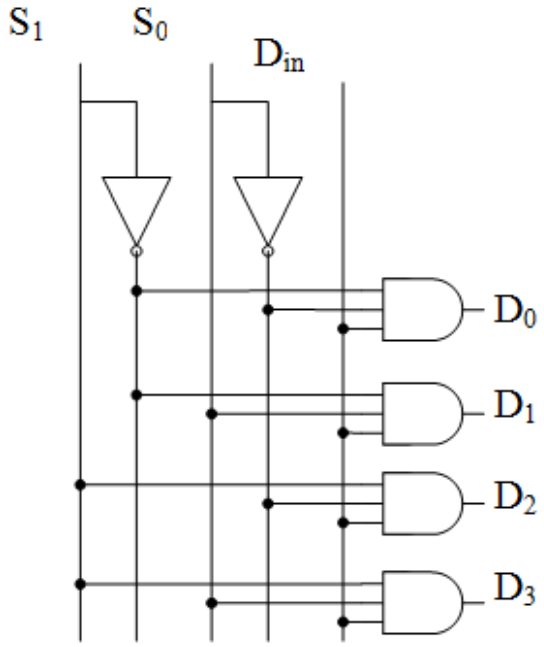

Figure 2: 1 to 4 Demultiplexer

It is also possible to construct 4to1 multiplexer (and 1to4 demultiplexer) using 2to1 multiplexers (1to2 demultiplexers) only. Figure 3 and figure 4 show the construction of 4to1 multiplexer using 2to1 multiplexers and 1to4 demultiplexer using 1to2 demultiplexers only.

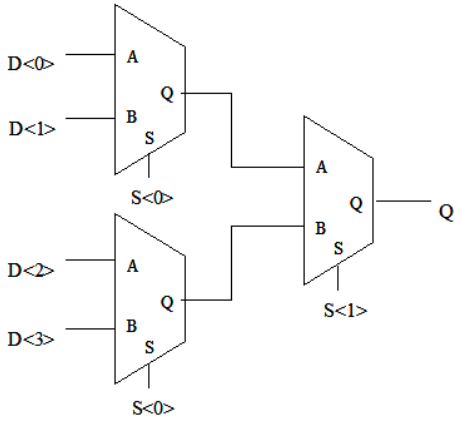

Figure 3: 4to1 multiplexer using 2to1 multiplexers.

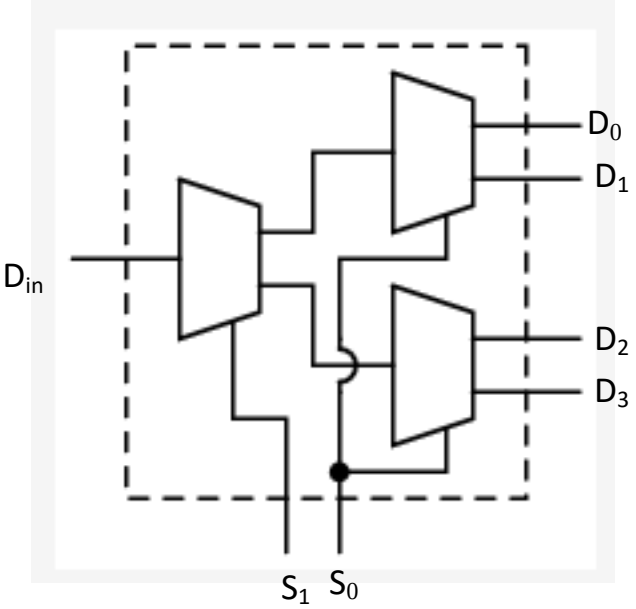

Figure 4: 1to4 demultiplexer using 1to2 dmultiplexers.

Pre-Lab Homework:

Read about the characteristics of Multiplexer and De-multiplexer circuits from any book or websites and use PSIM to generate the output of the circuits provided in this lab sheet. Save the simulation results and bring it to the lab.

Apparatus:

1. NOT Gate - IC 7404
2. AND Gate - IC 7408
3. OR Gate - IC 7408

Precautions:

Have your instructor check all your connections after you are done setting up the circuit and make sure that you apply only enough voltage to turn on the chip, otherwise it may get damaged.

Experimental Procedure:

1) Connect the circuit according to the figures.

2) Use the toggle switches on the trainer board for providing input signal to the circuits. Connect the outputs to the LEDs on the trainer board.

3) Apply the input signals and observe and note the corresponding output signals.

Simulation and Measurement:

Compare the simulation results with your experimental data and comment on the differences (if any).

Questions for report writing:

Design and simulate the following circuits.

1) 8to1 multiplexer using basic logic gates.
2) 8to1 multiplexer using 4to1 and/or 2to1 multiplexers.
3) 1to8 demultiplexer using basic logic gates.
4) 1to8 demultiplexer using 1to4 and/or 1to2 demultiplexers.

Discussion and Conclusion:

Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

Reference(s):

1. "Fundamentals of Digital Logic with verilog design" by – Brown & Vranesic