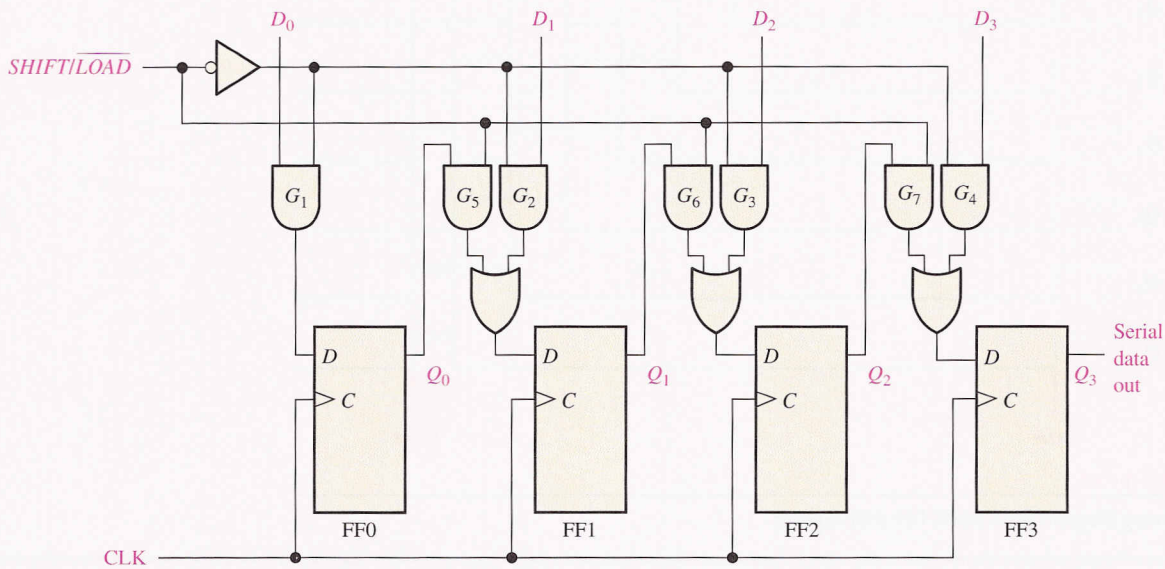
After completing this section, you should be able to

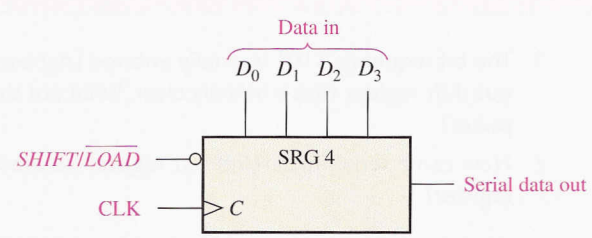
- Explain how data bits are entered into a shift register in parallel
- Compare serial input to parallel input
- Discuss the 74HC165 8-bit parallel-load shift register
- Develop and analyze timing diagrams for parallel in/serial out registers

For parallel data, multiple bits are transferred at one time.

Figure 9–12 illustrates a 4-bit parallel in/serial out shift register and a typical logic symbol. Notice that there are four data-input lines, D_0, D_1, D_2, and D_3, and a $SHIFT/\overline{LOAD}$ input, which allows four bits of data to **load** in parallel into the register. When $SHIFT/\overline{LOAD}$ is LOW, gates G_1 through G_4 are enabled, allowing each data bit to be applied to the D input of its respective flip-flop. When a clock pulse is applied, the flip-flops with $D = 1$ will set and those with $D = 0$ will reset, thereby storing all four bits simultaneously.



(a) Logic diagram



(b) Logic symbol

▲ FIGURE 9–12

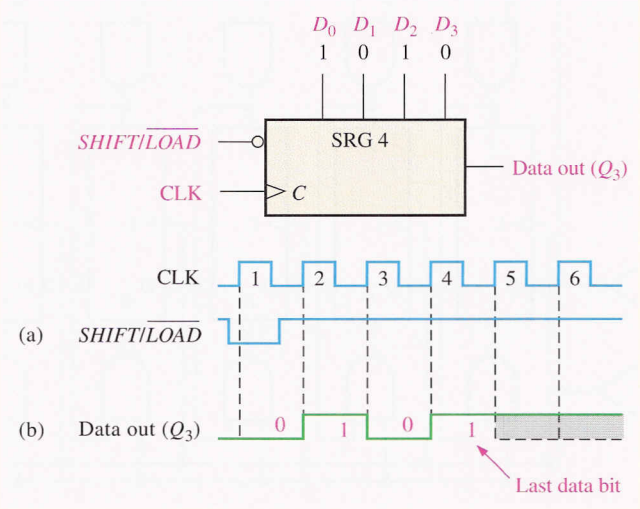
A 4-bit parallel in/serial out shift register. Open file F09-12 to verify operation.

When $SHIFT/\overline{LOAD}$ is HIGH, gates G_1 through G_4 are disabled and gates G_5 through G_7 are enabled, allowing the data bits to shift right from one stage to the next. The OR gates

allow either the normal shifting operation or the parallel data-entry operation, depending on which AND gates are enabled by the level on the *SHIFT*/$\overline{LOAD}$ input. Notice that FF0 has a single AND to disable the parallel input, D_0. It does not require an AND/OR arrangement because there is no serial data in.

EXAMPLE 9–3

Show the data-output waveform for a 4-bit register with the parallel input data and the clock and *SHIFT*/$\overline{LOAD}$ waveforms given in Figure 9–13(a). Refer to Figure 9–12(a) for the logic diagram.



▲ **FIGURE 9–13**

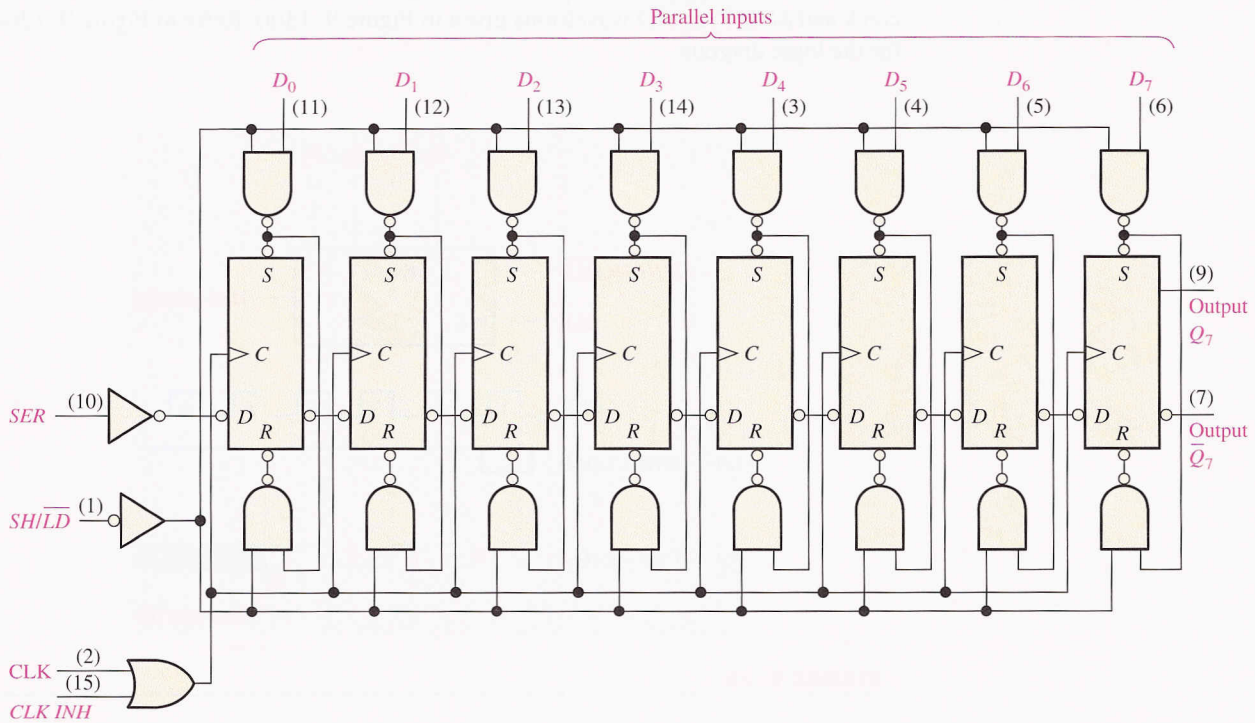
Solution On clock pulse 1, the parallel data ($D_0D_1D_2D_3 = 1010$) are loaded into the register, making Q_3 a 0. On clock pulse 2 the 1 from Q_2 is shifted onto Q_3; on clock pulse 3 the 0 is shifted onto Q_3; on clock pulse 4 the last data bit (1) is shifted onto Q_3; and on clock pulse 5, all data bits have been shifted out, and only 1s remain in the register (assuming the *D* input remains a 1). See Figure 9–13(b).

Related Problem Show the data-output waveform for the clock and *SHIFT*/$\overline{LOAD}$ inputs shown in Figure 9–13(a) if the parallel data are $D_0D_1D_2D_3 = 0101$.

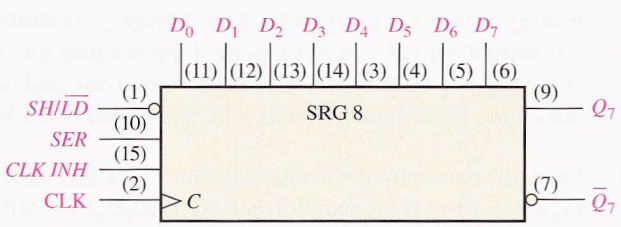
THE 74HC165 8-BIT PARALLEL LOAD SHIFT REGISTER

The 74HC165 is an example of an IC shift register that has a parallel in/serial out operation (it can also be operated as serial in/serial out). Figure 9–14(a) shows the internal logic diagram for this device, and part (b) shows a typical logic block symbol. A LOW on the *SHIFT*/$\overline{LOAD}$ input (*SH*/$\overline{LD}$) enables all the NAND gates for parallel loading. When an input data bit is a 1, the flip-flop is asynchronously set by a LOW out of the upper gate.

When an input data bit is a 0, the flip-flop is asynchronously reset by a LOW out of the lower gate. Additionally, data can be entered serially on the *SER* input. Also, the clock can be inhibited anytime with a HIGH on the *CLK INH* input. The serial data outputs of the register are Q_7 and its complement $\overline{Q}_7$. This implementation is different from the synchronous method of parallel loading previously discussed, demonstrating that there are usually several ways to accomplish the same function.



(a) Logic diagram

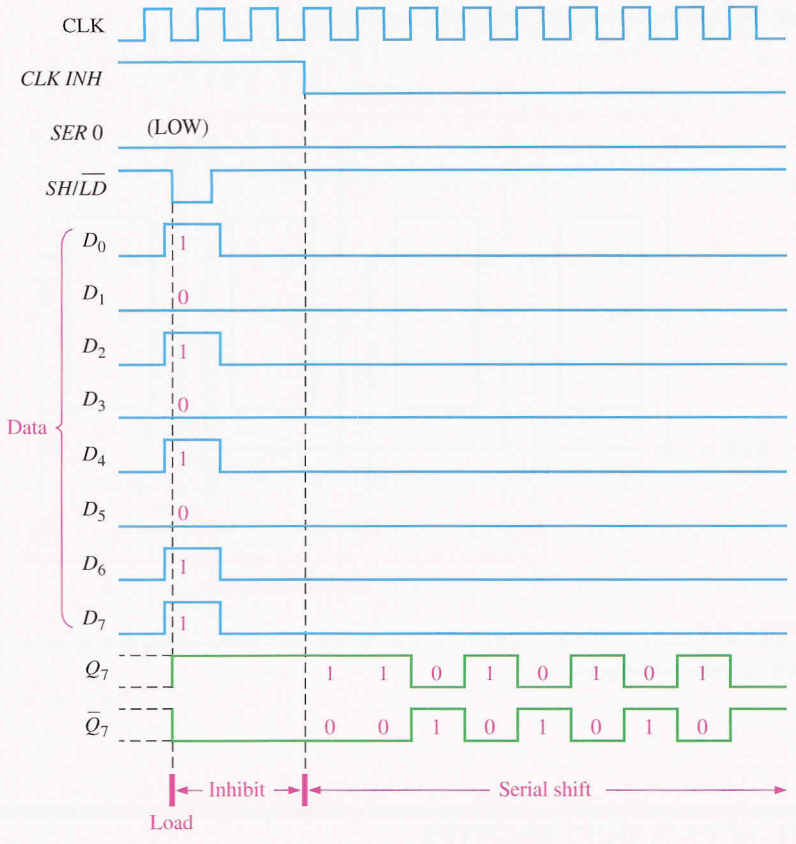


(b) Logic symbol

▲ FIGURE 9–14

The 74HC165 8-bit parallel load shift register.

Figure 9–15 is a timing diagram showing an example of the operation of a 74HC165 shift register.



▲ **FIGURE 9–15**

Sample timing diagram for a 74HC165 shift register.

SECTION 9–4 REVIEW

1. Explain the function of the *SHIFT*/$\overline{LOAD}$ input.
2. Is the parallel load operation in a 74HC165 shift register synchronous or asynchronous? What does this mean?

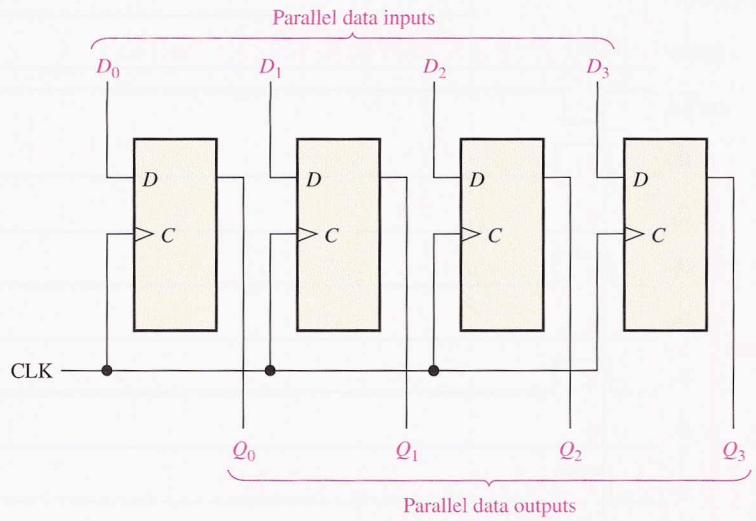
9–5 PARALLEL IN/PARALLEL OUT SHIFT REGISTERS

Parallel entry of data was described in Section 9–4, and parallel output of data has also been discussed previously. The parallel in/parallel out register employs both methods. Immediately following the simultaneous entry of all data bits, the bits appear on the parallel outputs.

After completing this section, you should be able to

■ Discuss the 74HC195 4-bit parallel-access shift register ■ Develop and analyze timing diagrams for parallel in/parallel out registers

Figure 9–16 shows a parallel in/parallel out register.



▲ **FIGURE 9–16**

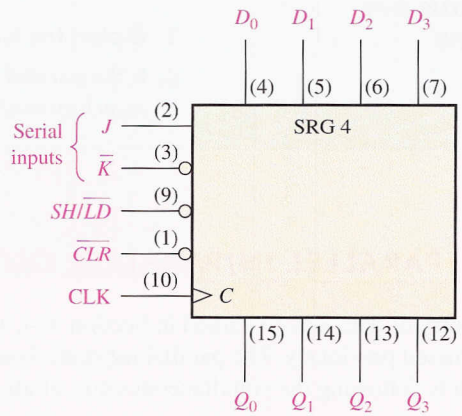
A parallel in/parallel out register.

THE 74HC195 4-BIT PARALLEL-ACCESS SHIFT REGISTER

The 74HC195 can be used for parallel in/parallel out operation. Because it also has a serial input, it can be used for serial in/serial out and serial in/parallel out operations. It can be used for parallel in/serial out operation by using Q_3 as the output. A typical logic block symbol is shown in Figure 9–17.

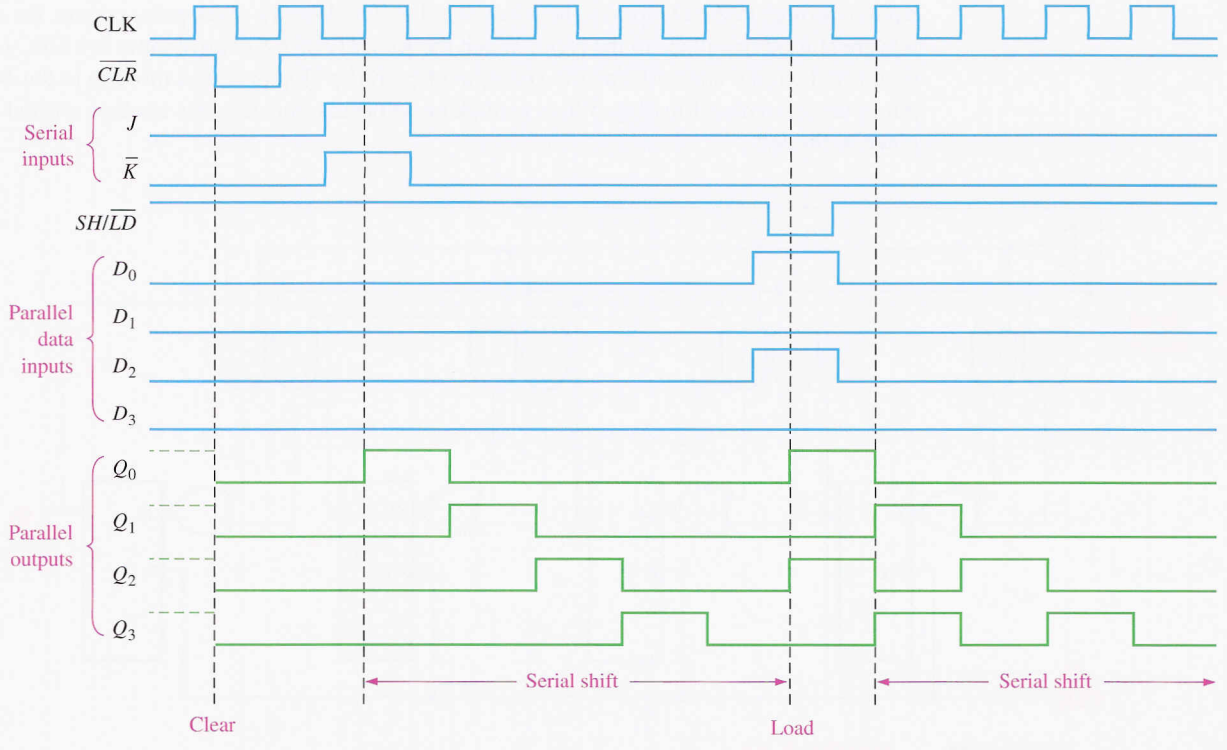
▶ **FIGURE 9–17**

The 74HC195 4-bit parallel access shift register.



When the $SHIFT/\overline{LOAD}$ input ($SH/\overline{LD}$) is LOW, the data on the parallel inputs are entered synchronously on the positive transition of the clock. When $SH/\overline{LD}$ is HIGH, stored data will shift right (Q_0 to Q_3) synchronously with the clock. Inputs J and $\overline{K}$ are the serial data inputs to the first stage of the register (Q_0); Q_3 can be used for serial output data. The active-LOW clear input is asynchronous.

The timing diagram in Figure 9–18 illustrates the operation of this register.



▲ **FIGURE 9–18**

Sample timing diagram for a 74HC195 shift register.

SECTION 9–5 REVIEW

1. In Figure 9–16, $D_0 = 1$, $D_1 = 0$, $D_2 = 0$, and $D_3 = 1$. After three clock pulses, what are the data outputs?
2. For a 74HC195, $SH/\overline{LD} = 1$, $J = 1$, and $\overline{K} = 1$. What is Q_0 after one clock pulse?

9–6 BIDIRECTIONAL SHIFT REGISTERS

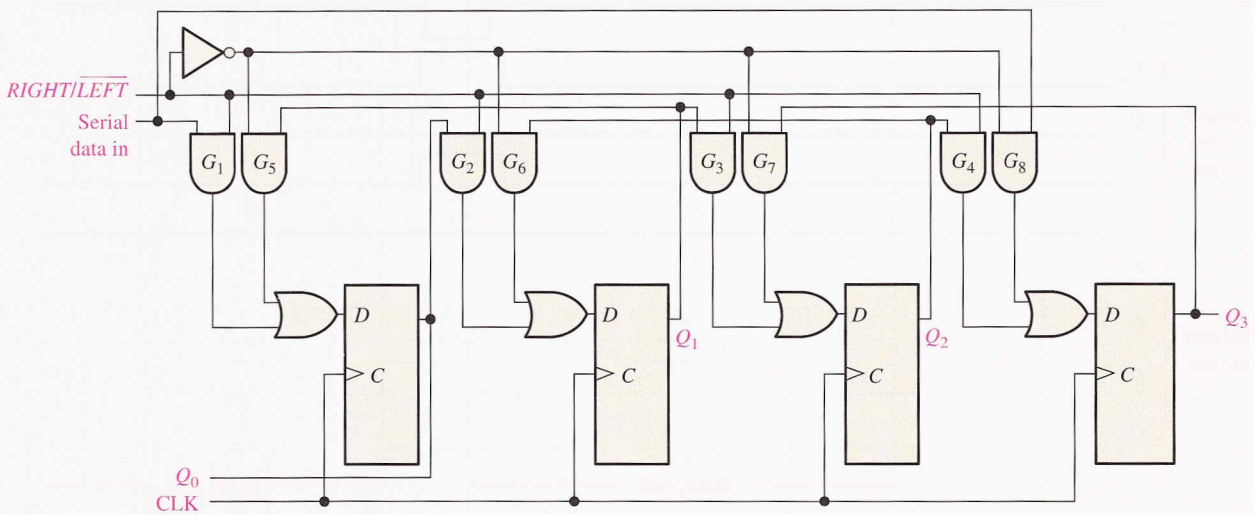
A bidirectional shift register is one in which the data can be shifted either left or right. It can be implemented by using gating logic that enables the transfer of a data bit from one stage to the next stage to the right or to the left, depending on the level of a control line.

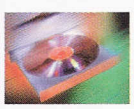
After completing this section, you should be able to

■ Explain the operation of a bidirectional shift register ■ Discuss the 74HC194 4-bit bidirectional universal shift register ■ Develop and analyze timing diagrams for bidirectional shift registers

A 4-bit **bidirectional** shift register is shown in Figure 9–19. A HIGH on the $RIGHT/\overline{LEFT}$ control input allows data bits inside the register to be shifted to the right, and a LOW enables data bits inside the register to be shifted to the left. An examination of the gating logic will make the operation apparent. When the $RIGHT/\overline{LEFT}$ control input is HIGH, gates G_1 through G_4 are enabled, and the state of the Q output of each flip-flop is

passed through to the D input of the *following* flip-flop. When a clock pulse occurs, the data bits are shifted one place to the *right*. When the $RIGHT/\overline{LEFT}$ control input is LOW, gates G_5 through G_8 are enabled, and the Q output of each flip-flop is passed through to the D input of the *preceding* flip-flop. When a clock pulse occurs, the data bits are then shifted one place to the *left*.





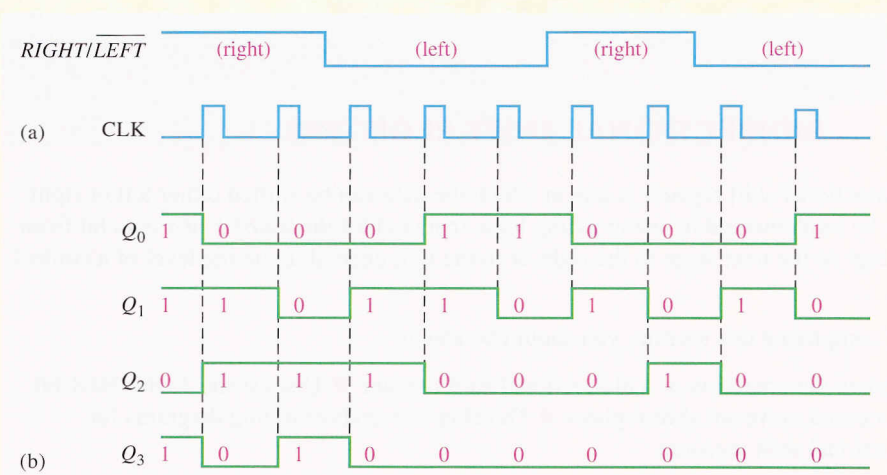
▲ **FIGURE 9–19**

Four-bit bidirectional shift register. Open file F09-19 to verify the operation.

EXAMPLE 9–4

Determine the state of the shift register of Figure 9–19 after each clock pulse for the given $RIGHT/\overline{LEFT}$ control input waveform in Figure 9–20(a). Assume that $Q_0 = 1$, $Q_1 = 1$, $Q_2 = 0$, and $Q_3 = 1$ and that the serial data-input line is LOW.

▶ **FIGURE 9–20**



Solution See Figure 9–20(b).

Related Problem Invert the $RIGHT/\overline{LEFT}$ waveform, and determine the state of the shift register in Figure 9–19 after each clock pulse.

THE 74HC194 4-BIT BIDIRECTIONAL UNIVERSAL SHIFT REGISTER

The 74HC194 is an example of a universal bidirectional shift register in integrated circuit form. A **universal shift register** has both serial and parallel input and output capability. A logic block symbol is shown in Figure 9–21, and a sample timing diagram is shown in Figure 9–22.

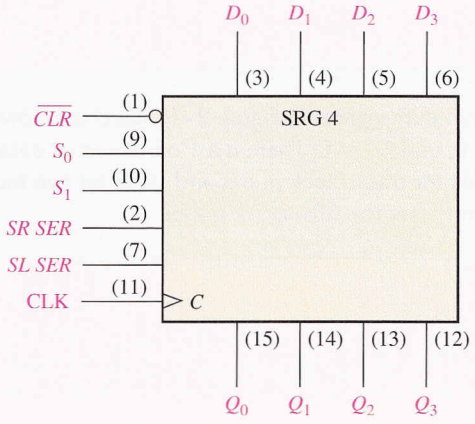


FIGURE 9–21

The 74HC194 4-bit bidirectional universal shift register.

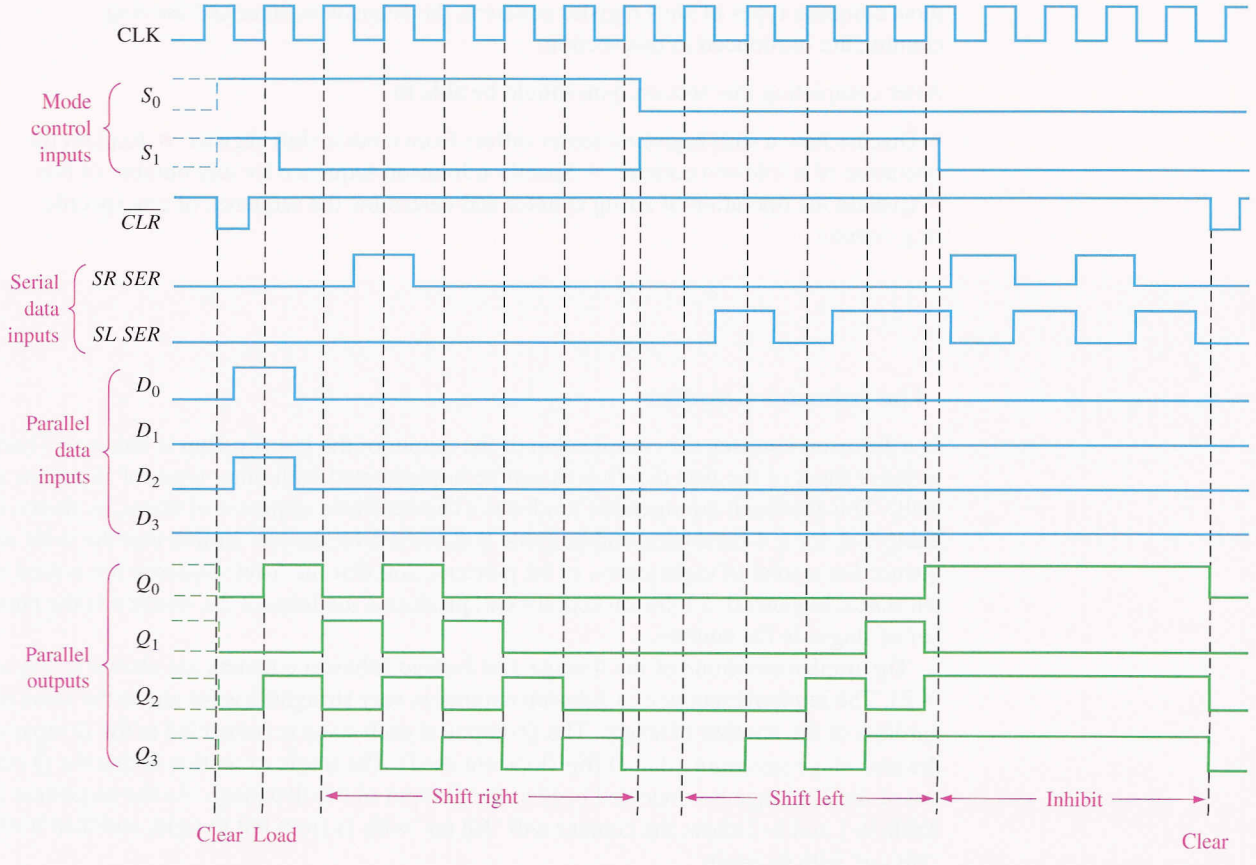


FIGURE 9–22

Sample timing diagram for a 74HC194 shift register.