# Encoder and Decoder:

1. **Design** a **2-line** to **4-line decoder** with **active low output**. State **how many input** and **output terminals** your device will have with **proper markings. For your design show** the **truth table**, **derive SOP output expressions**, **draw logic symbol/block diagram** and **combinational logic diagram**.
2. **Design** a **2-line** to **4-line decoder** with **active high output**. State **how many input** and **output terminals** your device will have with **proper markings. For your design show** the **truth table**, **derive SOP output expressions**, **draw logic symbol/block diagram** and **combinational logic diagram**.
3. **Design** a **3-line** to **8-line decoder** with **active high output**. State **how many input** and **output terminals** your device will have with **proper markings. For your design show** the **truth table**, **derive SOP output expressions**, **draw logic symbol/block diagram** and **combinational logic diagram**.
4. **Design** a **decimal** to **binary Priority encoder** with the following **priority sequence** (1, 0, 3, 2) with 1 having highest priority and 2 with the lowest priority. State **how many input** and **output terminals** your device will have with **proper markings. For your design show** the **truth table, derive SOP output expressions**, **draw logic symbol/block diagram** and **combinational logic diagram**.
5. **Design** a **decimal** to **binary Priority encoder** with the following **priority sequence** (5, 7, 4, 6, 1, 0, 3, 2) with 5 having highest priority and 2 with the lowest priority. State **how many input** and **output terminals** your device will have with **proper markings. For your design show** the **truth table, derive SOP output expressions**, **draw logic symbol/block diagram** and **combinational logic diagram**.
6. **Implement** the **function** $f$**(A,B,C,D)=(3, 5, 6,7, 9, 10, 11, 13)**, **using** a **4-bit decoder** and **necessary gates**.
7. **Implement** the **logic function** $f$**(A,B,C)=AB+$\overline{C}$**, using a **3-bit decoder** and **necessary gates**.
8. **Implement** a **Full Subtractor** using a **3-bit decoder** and **necessary gates.**

# Multiplexer and Demultiplexer:

1. **Design** a **4X1 Multiplexer**. State **how many input** and **output terminals** your device will have with **proper markings in a block diagram. For your design show** the **truth table, derive SOP output expressions** and **draw combinational logic diagram**.
2. **A drink dispenser machine has 7 different types of drinks that it can serve to it's customer. The machine is programed in such a way that only one of the drink is served at a time**. The input switch configuration is set in the following way. **0 for Coke, 1 for Sprite, 2 for Mirinda, 3 for Coffee, 4 for Lime, 5 for Water and 6 for Mountain Dew**. Design the system with the concept of Mux. State **how many input** and **output terminals** your device will have with **proper markings. For your design show** the **truth table, derive SOP output expressions**, draw logic symbol/block diagram
3. **Design** a **8X1 Multiplexer using 4X1 Multiplexer blocks only**. State **how many input** and **output terminals** your device will have with **proper markings. For your design show** the **truth table, derive SOP output expressions**, **draw logic symbol/block diagram**.
4. **Design** a **8X1 Multiplexer using 4X1 Multiplexer and 2X1 Multiplexer blocks**. State **how many input** and **output terminals** your device will have with **proper markings. For your design show,** the **truth table, derive SOP output expressions**, **draw logic symbol/block diagram**.
5. **Implement** the **function** $f$**(A,B,C)=(3, 5, 6, 7)** using **Multiplexer**. Show **which pins** you are choosing as **selector pin** in your truth table.
6. What do you **understand** by the term **Demultiplexer**?
7. **Design** a **1 to 2 Demultiplexer**. State **how many input** and **output terminals** your device will have with **proper markings in a block diagram. For your design show** the **truth table, derive SOP output expressions** and **draw combinational logic diagram**.

# Assignment-F1
## Digital Logic Design

8. **Design** a **1 to 4 Demultiplexer**. State **how many input** and **output terminals** your device will have with **proper markings in a block diagram**. **For your design show** the **truth table, derive SOP output expressions** and **draw combinational logic diagram**.

9. **Design** a **1 to 7 Demultiplexer with 1 of 2 Demux only**. State **how many input** and **output terminals** your device will have with **proper markings in a block diagram**. **For your design show** the **truth table, derive SOP output expressions**.

10. **Design** a **1 to 16 Demultiplexer using 1 to 2 Demultiplexer blocks only**. State **how many input** and **output terminals** your device will have with **proper markings in a block diagram**. **For your design show** the **truth table, derive SOP output expressions**.

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**Do not copy from your peers. If you do not understand anything, consult with them or me. Assignments copied will be considered obsolete. Assignment is <span style="color:red">due on quiz 4, in class</span>. Please do not drop your assignments in my office room.**