



American International University- Bangladesh

Department of Electrical and Electronic Engineering

EEE2206 Digital Logic Design Laboratory

Title: Implementation of Asynchronous and synchronous counters using flip-flops.

Introduction:

Counters are combinations of flip-flops arranged so that they can remember how many clock pulses have been applied over some specified interval. The flip-flops are often interconnected so that only a portion of their available binary states can be supported. If there are N flip-flops being used in a counter, the number of states available is $2N$. If the counter proceeds cyclically through K of these states, where $K \leq 2N$, it is said to be a modulo K (or MOD K) counter. Some applications will require a separate output to indicate each of the counters states, alternatively, other applications may require only one output pulse every K th state.

Counters are classified into two broad categories according to the way they are clocked: **asynchronous and synchronous**. In asynchronous counters, commonly called ripple counters, the first flip-flop is clocked by the external clock pulse and then each successive flip flop is clocked by the output of the preceding flip-flop. In synchronous counters, the clock input is connected to all of the flip-flops so that they are clocked simultaneously.

The objective of this experiment is designing of the following counters using J-K Flip-Flops (IC 74LS76)

- (a) n -bit Binary Asynchronous Counter
- (b) n -bit Binary Synchronous Counter

Theory and Methodology:

Asynchronous counter

A three-bit asynchronous counter is shown in the figure 9.1. The external clock is connected to the clock input of the first flip-flop (FF0) only. So, FF0 changes state at the falling edge of each clock pulse, but FF1 changes only when triggered by the falling edge of the Q output of FF0. Because of the inherent propagation delay through a flip-flop, the transition of the input clock pulse and a transition of the Q output of FF0 can never occur at exactly the same time. Therefore, the flip-flops cannot be triggered simultaneously, producing an asynchronous operation.

Figure 9.1 gives a three-bit counter capable of counting from 0 to 7. The clock inputs of the three flip-flops are connected in cascade. The T input of each flip-flop is connected to a constant 1, which means that the state of the flip-flop will be reversed (toggled) at each positive edge of its clock. We are assuming that the purpose of this circuit is to count the number of pulses that occur on the primary input called Clock. Thus the clock input of the first flip-flop is connected to the Clock line. The other two flip-flops have their clock inputs driven by the Q output of the preceding flip-flop. Therefore, they toggle their state whenever the preceding flip-flop changes its state from $Q = 1$ to $Q = 0$, which results in a positive edge of the Q signal.

Figure 9.1 shows a timing diagram for the counter. The value of Q_0 toggles once each clock cycle. The change takes place shortly after the positive edge of the Clock signal. The delay is caused by the propagation delay through the flip-flop. Since the second flip-flop is clocked by Q_0 , the value of Q_1 changes shortly after the negative edge of the Q_0 signal. Similarly, the

value of Q_2 changes shortly after the negative edge of the Q_1 signal. If we look at the values $Q_2Q_1Q_0$ as the count, then the timing diagram indicates that the counting sequence is 0, 1, 2, 3, 4, 5, 6, 7, 0, 1, and so on. This circuit is a modulo-8 counter. Because it counts in the upward direction, we call it an up-counter.

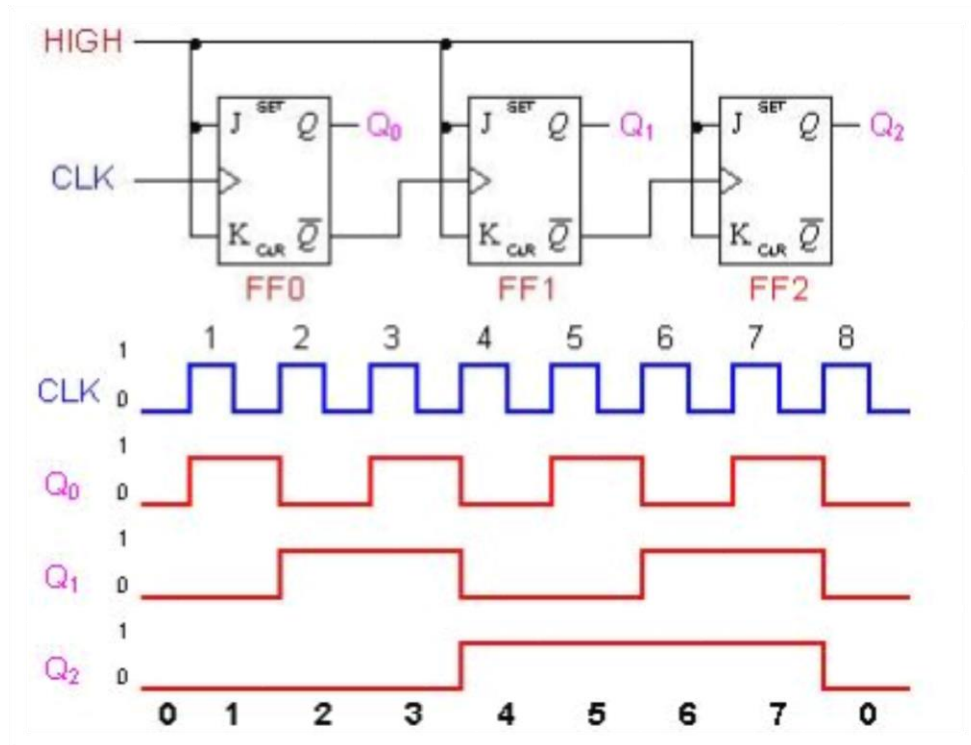


Figure 9.1: 3 bit Asynchronous counter and its timing diagram

Synchronous counter

In synchronous counters, the clock inputs of all the flip-flops are connected together and are triggered by the input pulses. Thus, all the flip-flops change state simultaneously (in parallel). The most important advantage of synchronous counters is that there is no cumulative time delay because all flip-flops are triggered in parallel. Thus, the maximum operating frequency for this counter will be significantly higher than for the corresponding ripple counter.

Table 9.1 shows the contents of a four-bit up-counter for eight consecutive clock cycles, assuming that the count is initially 0. Observing the pattern of bits in each row of the table, it is apparent that bit Q_0 changes on each clock cycle. Bit Q_1 changes only when $Q_0 = 1$. Bit Q_2 changes only when both Q_1 and Q_0 are equal to 1. In general, for an n -bit up-counter, a given flip-flop changes its state only when all the preceding flip-flops are in the state $Q = 1$.

Table 9.1

$T_0 = 1$
 $T_1 = Q_0$
 $T_2 = Q_0Q_1$
 $T_3 = Q_0Q_1Q_2$
 $T_4 = Q_0Q_1Q_2Q_3$
 \vdots
 $T_n = Q_0Q_1 \cdots Q_{n-1}$

Clock cycle	Q_2	Q_1	Q_0
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0
5	1	0	1
6	1	1	0
7	1	1	1
8	0	0	0

The Circuit diagram of a four-bit counter based on these expressions is given in Figure 9.2a. Figure 9.2b gives a timing diagram. It shows that the circuit behaves as a modulo-16 up-counter. Because all changes take place with the same delay after the active edge of the Clock signal, the circuit is called a synchronous counter.

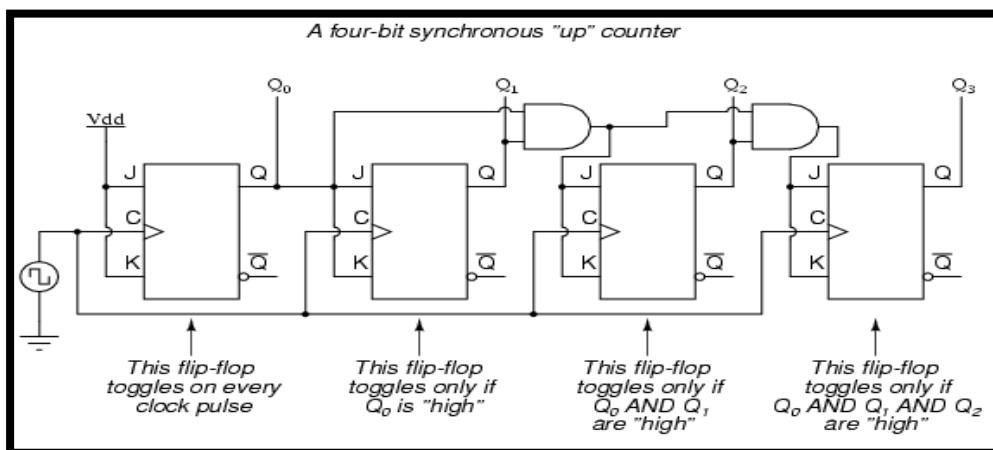


Figure 9.2a: A four-bit Synchronous Up Counter

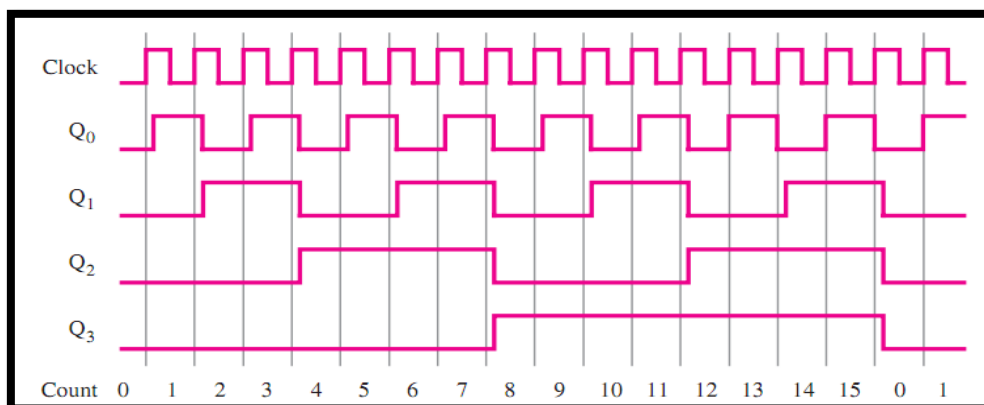


Figure 9.2b: The timing diagram of a four-bit Synchronous Up Counter

Pin Configuration of 74LS76 and 7408

There are 2 J-K Flip Flops in one IC. Here is the pin configuration of the IC 74LS76:

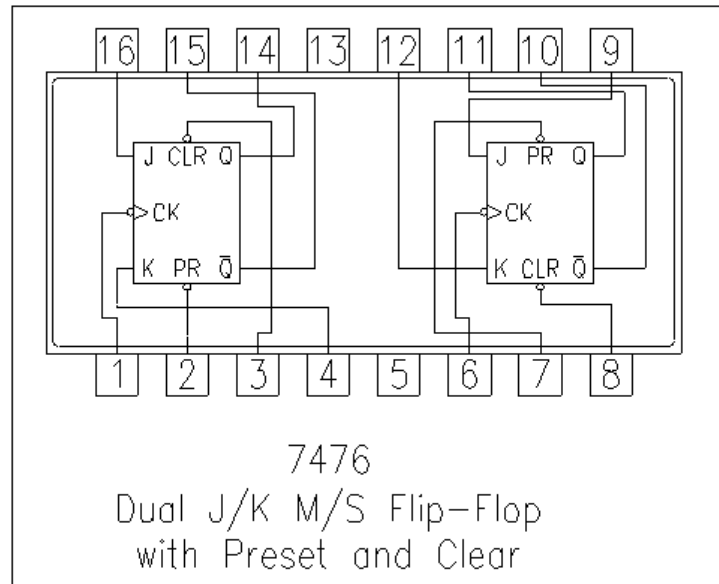


Figure 9.3: IC 74LS76

IC 7408 contains 4 AND gates in it. The pin configuration is shown below:

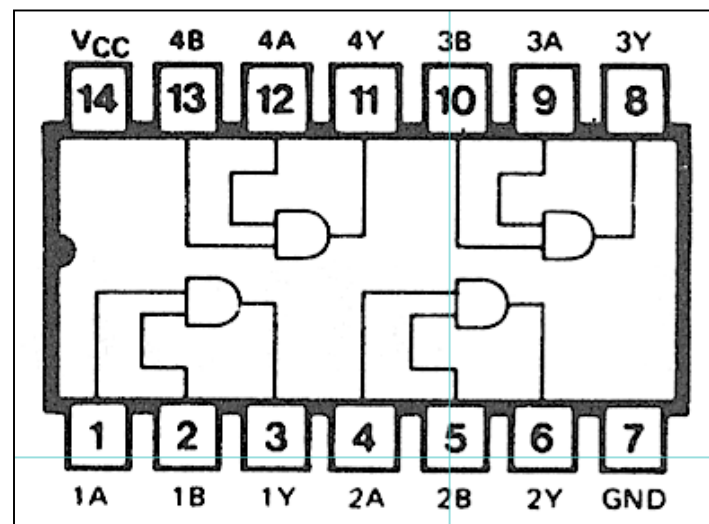


Figure 9.4: IC 7408

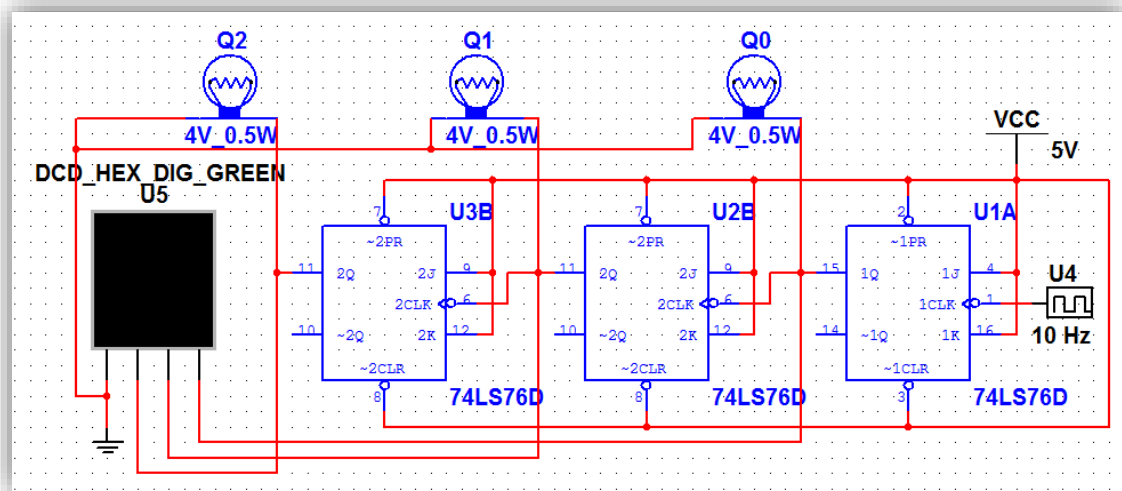


Fig 9.5: 3 bit Asynchronous Counter

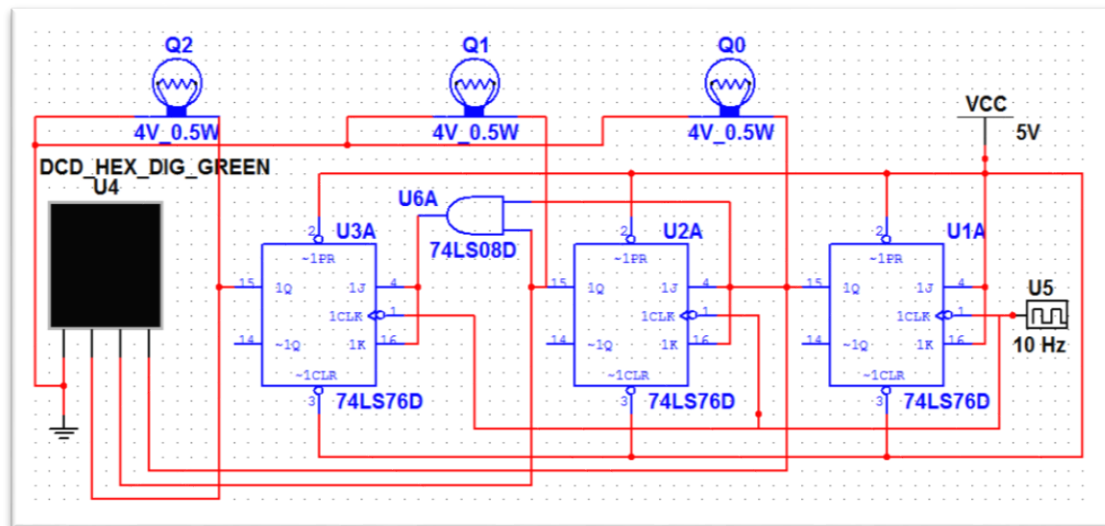


Fig 9.6: 3 bit Synchronous Counter

Pre-Lab Homework:

1. Write down in details the operation of JK Flip Flops mentioning its circuit diagram, truth table and timing diagram (also mention about the asynchronous inputs).
2. Also write down in brief the operations of other different types of Flip Flops.

Apparatus:

- IC 74LS76 (JK Flip Flop)
- IC 7408 (AND Gate)
- LED Lamps or Display
- Trainer Board
- Oscilloscope
- Connecting Wires

Precautions:

- Before preparing the circuits, check all the ICs(74LS76 & 7408) to make sure they are all working properly.

- Careful about the biasing of JK Flip Flops.
- Make sure you connected the preset and clear pins with Vcc.
- Try to use as less wire as possible. Make sure there is no loose connection.
- If you use a LED display then make sure you biased it properly.
- For Clock pulse, the trainer board's analog signal generator is a good choice. Use lower frequencies so that the change is slow enough to observe the outputs and take readings.

Experimental Procedure:

Part 1: 3 bit Asynchronous Counter

1. Design the circuit on the bread board as shown in Figure 9.5.
2. Use the trainer board's signal generator for the clock pulse and power supply for biasing the Flip Flops.
3. The output can also be viewed in oscilloscope, just connect the outputs to the different channels of the oscilloscope.
4. Observe the output results, record them and also take some pictures for your lab report.

3 bit Synchronous Counter

1. Design the circuit on the bread board as shown in Figure 9.6.
2. Use the trainer board's signal generator for the clock pulse and power supply for biasing the Flip Flops.
3. The output can also be viewed in oscilloscope, just connect the outputs to the different channels of the oscilloscope.
4. Observe the output results and take some pictures for your lab report.

Simulation and Measurement:

All the simulation should be done in Power Sim (PSIM). Compare the simulation results with your experimental data/ wave shapes and comment on the differences (if any).

Discussion and conclusion:

Interpret the data/findings and determine the extent to which the experiment was successful in complying with the goal that was initially set. Discuss any mistake you might have made while conducting the investigation and describe ways the study could have been improved.

Questions with answers for report writing:

1. Design a 4 bit Asynchronous Up- Counter.
2. Design a 4 bit Synchronous Up- Counter.

Bonus Mark

1. Design a 3 bit Asynchronous down counter.
2. Design a Mod 10 Synchronous up counter.

Reference(s):

- i) Thomas L. Floyd, "Digital Fundamentals", Ninth Edition.