Assignment-F3
Digital Logic Design

Counters:

a) Design a **4-bit Asynchronous binary counter** using **J-K flip-flops**. For your designed counter, **show** the **truth table** and **timing diagram for each outputs** with **respect** to **the clock signal**, **clearly mentioning** the **state where your device goes into recycle mode.**

b) Design an **Asynchronous Decade counter** using **J-K flip-flops**. For your designed counter, **show** the **truth table** and **timing diagram for each output** with **respect** to **the clock signal**, **clearly mentioning** the **state where your device goes into recycle mode and how the recycle operation is achieved.**

c) Design an **Asynchronous MOD-13 binary counter** using **J-K flip-flops**. For your designed counter, **show** the **truth table** and **timing diagram for each output** with **respect** to **the clock signal**, **clearly mentioning** the **state where your device goes into recycle mode and how the recycle operation is achieved.**

d) Design a **5-bit Synchronous binary counter** using **J-K flip-flops**. For your designed counter, **show** the **truth table** and **timing diagram for each output** with **respect** to **the clock signal**, **clearly mentioning** the **state where your device goes into recycle mode**.

e) Design a **Synchronous Decade counter** using **J-K flip-flops**. For your designed counter, **show** the **truth table** and **timing diagram for each output** with **respect** to **the clock signal**, **clearly mentioning** the **state where your device goes into recycle mode and how the recycle operation is achieved.**

f) Design a S**ynchronous MOD-13 binary counter** using **J-K flip-flops**. For your designed counter, **show** the **truth table** and **timing diagram for each output** with **respect** to **the clock signal**, **clearly mentioning** the **state where your device goes into recycle mode and how the recycle operation is achieved.**

g) **Design a 4-bit Synchronous UP/DOWN counter using J-K flip-flops.**

h) Design a S**ynchronous binary counter with the irregular sequence of 1, 9, 6, 3 and again back to 1, repeating the cycle,** using **J-K flip-flops**. For your designed counter, **show** the **state tables** for both present and next state **for each outputs** and derive K-Maps for the input signals. Your **design must include** the **finalized logic block diagram properly connected**.

i) Design a S**ynchronous binary counter with the irregular sequence of 0, 7, 2, 5, 4, 1 and again back to 0, repeating the cycle,** using **J-K flip-flops**. For your designed counter, **show** the **state tables** for both present and next state **for each outputs** and derive K-Maps for the input signals. Your **design must include** the **finalized logic block diagram properly connected**.

j) Design a S**ynchronous binary counter with the irregular sequence of 12, 9, 6, 3, 14, 5 and again back to 12, repeating the cycle,** using **J-K flip-flops**. For your designed counter, **show** the **state tables** for both present and next state **for each outputs** and derive K-Maps for the input signals. Your **design must include** the **finalized logic block diagram properly connected**.

Shift Registers:

k) Design a 4-bit PARALLEL IN/ PARALLEL OUT (PIPO) shift register **with the help of D flip-flop.**

l) Design a 4-bit Bidirectional Shift Register with the help of **D flip-flop** and **necessary gates/blocks.**

m) Design a 4-bit PARALLEL IN/ SERIAL OUT (PISO) shift register **with the help of D flip-flop.**

Do not copy from your peers. If you do not understand anything, consult with them or me. Assignments copied will be considered obsolete. Assignment is due on day of quiz 6. Please do not drop your assignments in my office room.