Assignment-F2

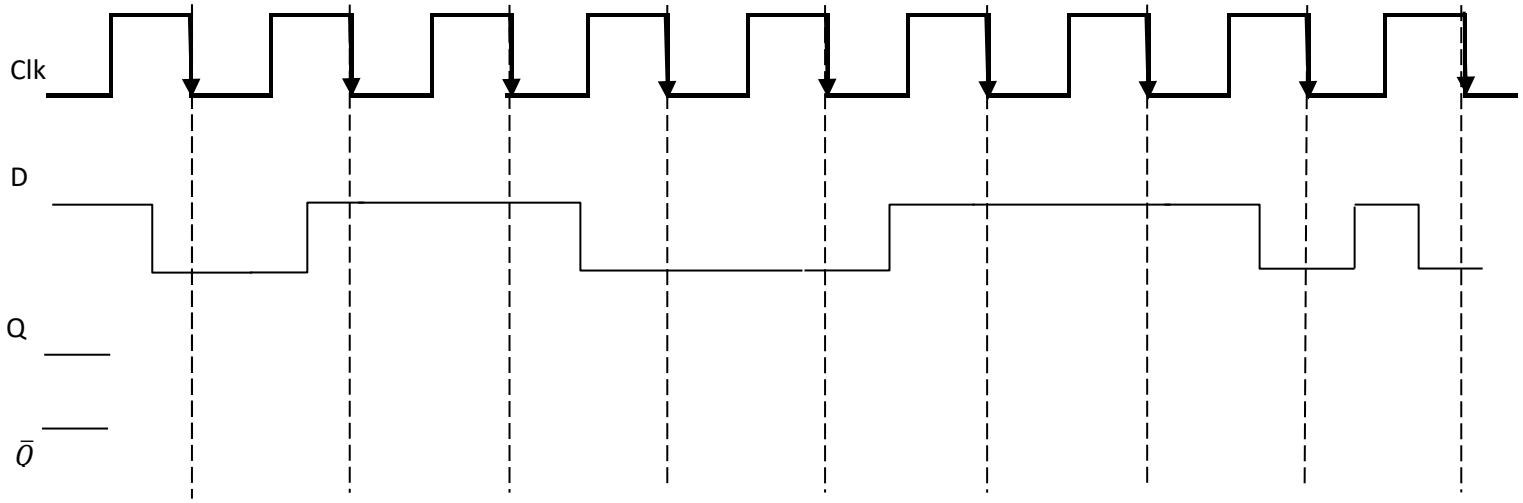
Digital Logic Design

Sequential Logic Design:

1. What is the **basic difference** between a **combinational logic circuit** and **sequential logic circuit**?
2. What is a **latch**?
3. **Design** an active high input **S-R latch**. **For the designed device**, **state** the **truth table** and **verify it** using the **present state assumption** and **next state table** process **discussed in class**, **draw logic symbol/block diagram** and **combinational logic diagram.**
4. **Design** an active low input **S-R latch**. **For the designed device**, **state** the **truth table** and **verify it** using the **present state assumption** and **next state table** process **discussed in class, draw logic symbol/block diagram** and **combinational logic diagram.**
5. **Design** an active high input gated **S-R latch**. **For the designed device**, **state** the **truth table** and **verify it** using the **present state assumption** and **next state table** process **discussed in class**, **draw logic symbol/block diagram** and **combinational logic diagram.**
6. What do you **understand by the term flip-flop**?
7. What is the **basic difference between** an **edge-triggered device** and **a level triggered device**? **Explain with the help of diagram**.
8. **Draw** the **logic symbol** of a **positive edge-triggered S-R flip-flop** along with the **truth table** for it. **Use the truth table and a timing diagram** to **explain** the **operation** of the **S-R flip-flop**.
9. **Draw** the **logic symbol** of a **positive edge-triggered D flip-flop** along with the **truth table** for it. **Use the truth table and a timing diagram** to **explain** the **operation** of the **D flip-flop.**
10. **Draw** the **logic symbol and logic diagram** of a **positive edge-triggered J-K flip-flop** along with the **truth table** for it. **Use the truth table and a timing diagram** to **explain** the **operation** of the **J-K flip-flop.**
11. **Draw** the **logic symbol** of a **positive edge-triggered T flip-flop** along with the **truth table** for it. **Use the truth table and a timing diagram** to **explain** the **operation** of the **T flip-flop**
12. **Draw** the **logic diagram** of a **Master-Slave J-K flip-flop**. **Explain** the **operation** of the **Master-Slave J-K flip-flop with the help of a timing diagram.**

Timing Diagram Problems:

a) Determine the output Q and $\bar{Q}$ of a negative edge triggered D-flip-flop if Q is initially at reset condition.



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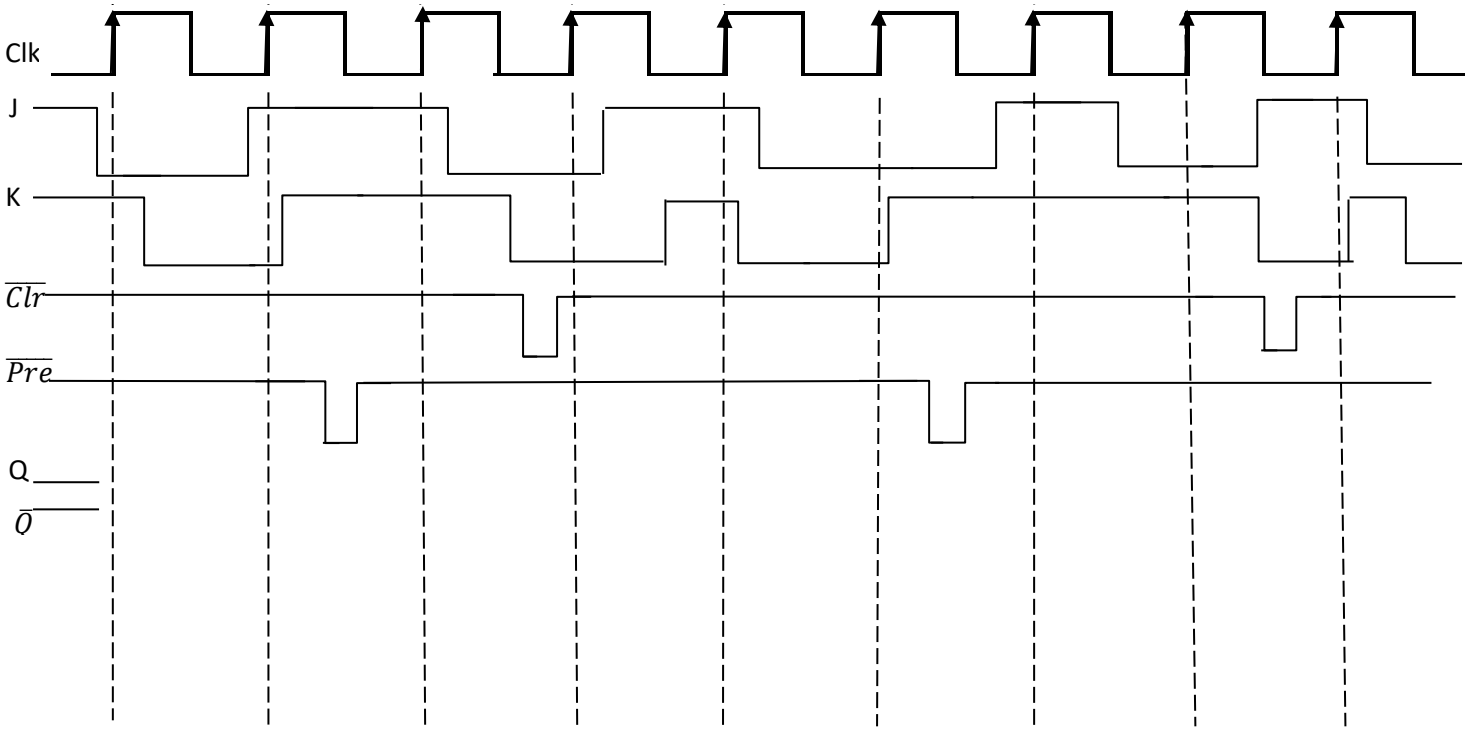
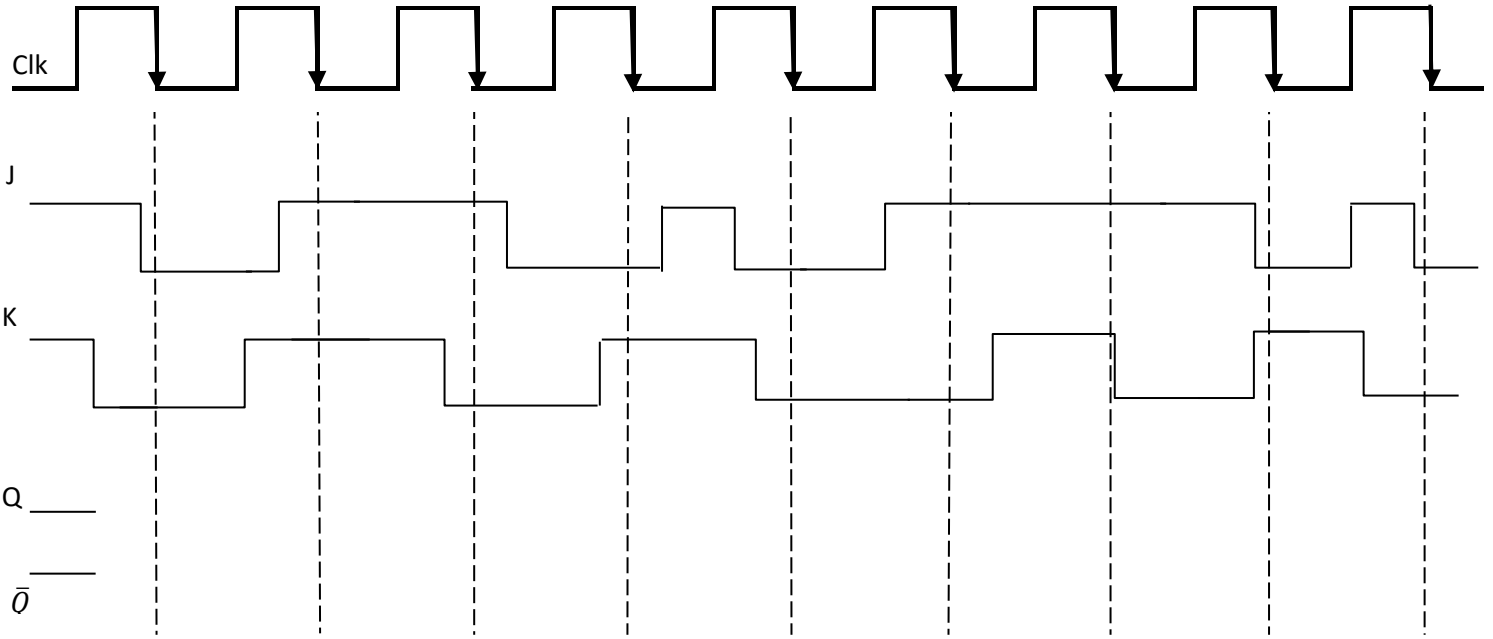
b) **Determine the output Q and $\overline{Q}$ of a positive edge triggered J-K-flip-flop if Q is initially at reset condition. Here $\overline{Clr}$ and $\overline{Pre}$ are active low inputs which corresponds to clear and preset respectively**.



c) Determine the output Q and $\overline{Q}$ of a negative edge triggered J-K-flip-flop if Q is initially at reset condition.



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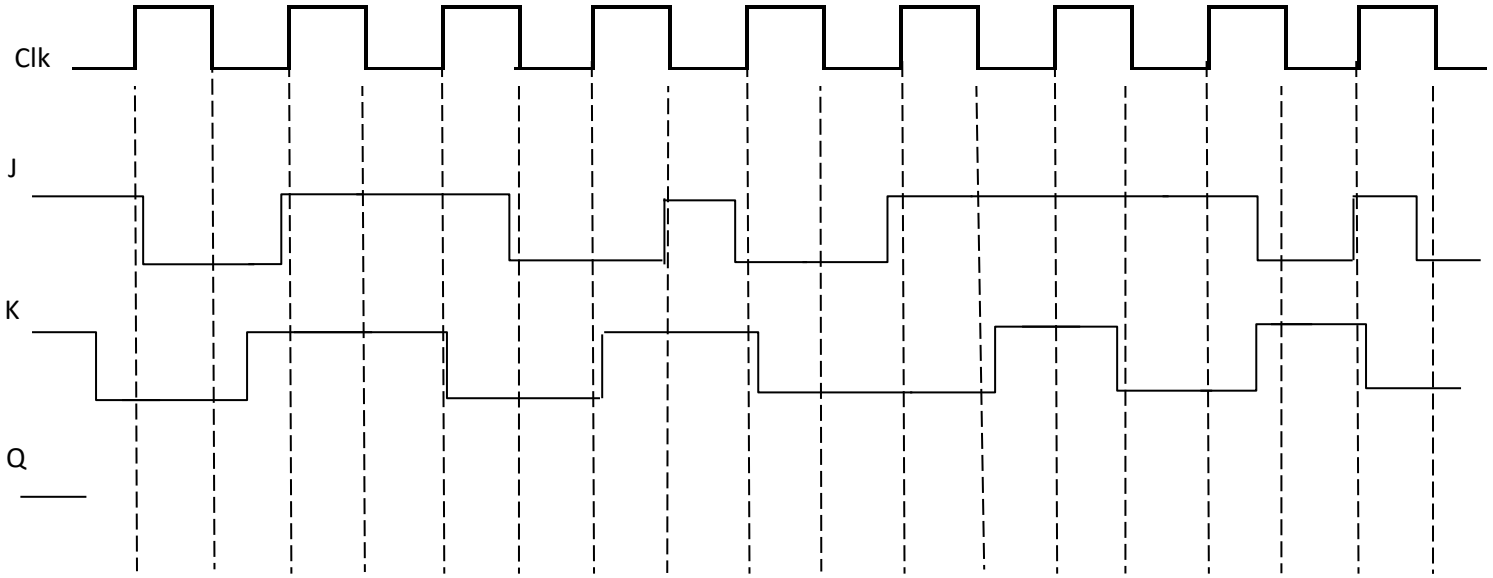
d. Determine the output Q and $\bar{Q}$ of a Master Slave-flip-flop if Q is initially at reset condition.



Answer the timing diagrams in the question and attach it to your assignment.

Do not copy from your peers. If you do not understand anything, consult with them or me. Assignments copied will be considered obsolete. Assignment is due on the day of quiz 5. Please do not drop your assignments in my office room.