SRM VALLIAMMAI ENGINEERING COLLEGE

SRM Nagar, Kattankulathur – 603 203

DEPARTMENT OF
COMPUTER SCIENCE AND ENGINEERING

QUESTION BANK

IV SEMESTER

1908006-COMPUTER ARCHITECTURE

Regulation – 2019

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SRM VALLIAMMAI ENGINEERING COLLEGE

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SUBJECT:1908006-COMPUTER ARCHITECTURE
SEM/ YEAR : IV Sem / IIYear

UNIT I-BASIC STRUCTURE OF A COMPUTER SYSTEM				
Functional Units–Basic Operational Concepts–Performance–Instructions: Language of the Computer Operations, Operands–Instruction representation–Logical operations–decision making–MIPS Addressing–Bus structure–Bus operation				
PART–A				
Q.No	**Questions**		**BT Level**	**Competence**
1	**Define** Computer Architecture.		BTL 1	Remember
2	**Interpret** the instruction set Architecture.		BTL 2	Understand
3	**Identify** general characteristics of Relative addressing mode with an example.		BTL 4	Analyze
4	**Define** Computer Architecture.		BTL 1	Remember
5	**Tabulate** the components of computer system.		BTL 1	Remember
6	**Give** the addressing modes in MIPS.		BTL 2	Understand
7	What are the fields in an MIPS instruction?		BTL 1	Remember
8	What are called Instruction?		BTL 1	Remember
9	**Discuss** the use of bus in computer architecture.		BTL 2	Understand
10	**Differentiate** register direct and indirect addressing.		BTL 4	Analyze
11	**Give** the difference between auto increment and auto decrement addressing mode.		BTL 2	Understand
12	**Discuss** the functions of control unit?		BTL 2	Understand
13	Differentiate DRAM and SRAM.		BTL 4	Analyze
14	**Calculate** throughput and response time.		BTL 3	Apply
15	**Compose** the CPU performance equation.		BTL 6	Create
16	Measure the performance of the computers: If computer A runs a program in 10 seconds, and computer B runs the same program in 15 seconds, how much faster is A over B?		BTL 5	Evaluate
17	**Formulat**e the equation of CPU execution time for a program.		BTL 6	Create
18	**Show** the formula for CPU clock cycles required for a program.		BTL 3	Apply
19	**Describe** about the various logical operators.		BTL 1	Apply
20	**What** are the various types of decision making instructions?		BTL 1	Remember
21	**Compare** address bus and memory bus structure.		BTL 4	Analyze
22	**Assess** the instructions based on the operations they perform and give one example to each category**.**		BTL 5	Evaluate

<table>
<tr><td>23</td><td>Examine control Line in Bus Structure.</td><td></td><td>BTL 3</td><td>Apply</td></tr>
<tr><td>24</td><td>Consider the following performance measurements for a program
<table>
<tr><th>Measurement</th><th>Computer A</th><th>Computer B</th></tr>
<tr><td>Instruction Count</td><td>10 billion</td><td>8 billion</td></tr>
<tr><td>Clock rate</td><td>4GHz</td><td>4GHz</td></tr>
<tr><td>CPI</td><td>1.0</td><td>1.1</td></tr>
</table>
Which computer has the higher MIPS rating?</td><td></td><td>BTL 5</td><td>Evaluate</td></tr>
<tr><td colspan="5">PART B</td></tr>
<tr><td>1</td><td>Evaluate the various techniques to represent instructions in a computer system.</td><td>(13)</td><td>BTL 5</td><td>Evaluate</td></tr>
<tr><td>2</td><td>List the various components of computer system and explain with neat diagram</td><td>(8)</td><td>BTL 1</td><td>Remember</td></tr>
<tr><td>3</td><td>i).What is an addressing mode in a computer?
ii).Describe the MIPS addressing modes with suitable examples to each category</td><td>(4)
(9)</td><td>BTL 1</td><td>Remember</td></tr>
<tr><td>4.</td><td>i). Identify the various operations in computer system.
ii). Examine the operands of computer hardware.</td><td>(6)
(7)</td><td>BTL 1</td><td>Remember</td></tr>
<tr><td>5</td><td>i).Discuss the logical operations and control operations of computer.
ii).Explain the concept of Arithmetic operation with examples</td><td>(7)
(6)</td><td>BTL 2</td><td>Understand</td></tr>
<tr><td>6</td><td>Consider three different processors P1, P2, and P3 executing the same instruction set. P1 has a 3 GHz clock rate and a CPI of 1.5. P2 has a 2.5 GHz clock rate and a CPI of 1.0. P3 has a 4.0 GHz clock rate and has a CPI of 2.2.
i).Which processor has the highest performance expressed in instructions per second?
ii).If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions?
iii).We are trying to reduce the execution time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?</td><td>
(3)
(5)
(5)</td><td>BTL 4</td><td>Analyze</td></tr>
<tr><td>7</td><td>Assess the various instruction formats and illustrate with an example</td><td>(13)</td><td>BTL5</td><td>Evaluate</td></tr>
<tr><td>8</td><td>Illustrate in detail about Technologies for Building Processors and Memory</td><td>(13)</td><td>BTL3</td><td>Apply</td></tr>
<tr><td>9</td><td>Describe the branching operations in detail with suitable example.</td><td>(13)</td><td>BTL 2</td><td>Understand</td></tr>
<tr><td>10</td><td>i).Formulate the performance of CPU.
ii).Compose the factors that affect performance.</td><td>(9)
(4)</td><td>BTL 6</td><td>Create</td></tr>
<tr><td>11</td><td>i).Illustrate the different types of instruction set architecture in detail
ii).Examine the basic instruction types with examples</td><td>(7)
(6)</td><td>BTL 3</td><td>Apply</td></tr>
<tr><td>12</td><td>What is Bus? Describe in detail the bus structure.</td><td>(13)</td><td>BTL 1</td><td>Remember</td></tr>
<tr><td>13</td><td>Examine performance of a computer in detail</td><td>(13)</td><td>BTL 3</td><td>Apply</td></tr>
<tr><td>14</td><td>i)If computer A runs a program in 10 seconds and computer B</td><td>(4)</td><td>BTL 4</td><td>Analyze</td></tr>
</table>

	runs the same program in 15 seconds, how much faster is A than B? ii)Suppose we have two implementations of the same instruction set architecture. Computer A has a clock cycle time of 250ps and a CPI of 2.0 for some program, and computer B has a clock cycle time of 500ps and CPI of 1.2 for the same program. Which computer is faster for this program and by how much?	(9)		
15	**Analyze** the various instruction formats and illustrate with an example.	**(13)**	BTL 4	Analyze
16	Consider two different implementation of the same instruction set architecture, The instruction can be divided into four classes according to their CPI (class A,B,C and D). P1 with clock rate 2.5 Ghz and CPI s of 1,2,3, and 3 respectively and P2 with clock rate 3 Ghz and CPI s of 2,2,2and 2 respectively. Given a program with a dynamic instruction count of $1.0*10^6$ instruction divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster? What is the global CPI for each implementation? Find the clock cycles required in both cases.	**(13)**	BTL 2	Understand
17	Explain the centralized and distributed bus system in computer organization.	**(13)**	BTL2	Understand
PART-C				
1	**Evaluate** a MIPS assembly instruction in to a machine instruction, for the add $to, $s1,$s2 MIPS instruction.	**(15)**	BTL 5	Evaluate

2	Assume a two address format specified as source, destination. Examine the following sequence of instructions and explain the addressing modes used and the operation done in every instruction.(15)
	MOVE (R5)+, R0
	ADD (R5)+, R0
	MOVE R0, (R5)
	MOVE16(R5),R3
	ADD#40,R5
		(15)	BTL 6	Create

3	**Assume** that the variables f and g are assigned to register $s0 and $s1 respectively. Assume that base address of the array A is in register $s2. Assume f is zero initially. F=g – A[4] A[5]=f + 100 Translate the above C statement into MIPS code .how many MIPS assembly instructions are needed to perform the C statements and how many different registers are needed to carry out the C statements?	**(15)**	BTL 6	Create
4	**Evaluate** which code sequence will execute faster according to execution time for the following conditions: c The computer with three instruction classes and CPI measurements as given below and instruction counts for each instruction class for the same program from two different compilers are given. Assume that the computer's clock rate is 1GHZ. Code from CPI for the instruction class	**(15)**	BTL 5	Evaluate

	A B C CPI 1 2 3 Code from CPI for the instruction class A B C Compiler1 2 1 2 Compiler2 2 1 1			
5	Summarize the functional units of a computer? Explain the functions of each unit?	**(15)**	BTL5	Evaluate

UNIT II-ARITHMETIC FOR COMPUTERS

ALU–Addition and subtraction–Multiplication–Division–Floating Point Representation and operation-Sub word parallelism

Q.No	**Questions**		**BT Level**	**Competence**
1	**Calculate** the following: Add 5_{10} to 6_{10} in binary and Subtract -6_{10} from 7_{10} in binary.		BTL 3	Apply
2	**Analyze** overflow conditions for addition and subtraction.		BTL 4	Analyze
3	**Construct** the Multiplication hardware diagram.		BTL 3	Apply
4	x=0000 1011 1110 1111 and y= 1111 0010 1001 1101 **Examine** x-y		BTL 1	Remember
5	**What** is fast multiplication?		BTL 1	Remember
6	Subtract $(11011)_2$–$(10011)_2$ using 1's complement and 2's complement method.		BTL 2	Understand
7	**Illustrate** scientific notation and normalization with example.		BTL 3	Apply
8	**Analyze** and Multiply 100011 * 100010		BTL 4	Analyze
9	**Give** the representation of double precision floating point number.		BTL 2	Understand
10	For the following C statement, **Develop** MIPS assembly code. f = g + (h − 5).		BTL 6	Create
11	**Name** the floating point instructions in MIPS.		BTL 1	Remember
12	**Formulate** the steps of floating point addition.		BTL 6	Create
13	**Evaluate** the sequence for floating point multiplication.		BTL 5	Evaluate
14	**Define** guard bit. What are the ways to truncate the guard bits?		BTL 1	Remember
15	**Express** the IEEE 754 floating point format. Represent $(63.25)_{10}$ in single precision		BTL 2	Understand
16	**State** sub-word parallelism.		BTL 1	Remember
17	**Interpret** single precision floating point number representation with example.		BTL 2	Understand
18	Analyze the normalization notation and perform the same for the following number $10.015_{10} * 10^{1}$		BTL 4	Analyze
19	**List** the steps in division algorithm.		BTL 1	Remember

20	For the following MIPS assembly instructions above, **what** is a corresponding C statement?
	add f, g, h
	add f, i, f
			BTL 5	Evaluate

21	Subtract $(11011)_2$ –$(10011)_2$ using 2's complement.		BTL 3	Apply
22	Divide $(1001010)_2$ by $(1000)_2$		BTL 5	Evaluate
23	Interpret the representation of double precision floating point number		BTL2	Understand
24	Add the Binary numbers 1110 and 1011.		BTL 4	Analyze

PART B				
1	i).**Discuss** the multiplication algorithm in detail with diagram. ii).Express the steps to Multiply $2_{10}*3_{10}$ using the sequential version multiplication algorithm.	**(6)** **(7)**	BTL 2	Understand
2	**Discuss** about the fast multiplication algorithm with hardware block and refined version of multiplication hardware.	**(13)**	BTL 2	Understand
3	**Describe** about basic concepts of ALU design.	**(13)**	BTL 1	Remember
4	**Develop** algorithm to implement A*B. calculate the product of octal unsigned 6-bit integers. Assume A and B with values: A=101 000_2, B=010 011_2	**(13)**	BTL 6	Create
5	i) .**State** the integer division algorithm with diagram. ii).Divide 50 by 23 and show the content of registers Assume both the inputs are unsigned 6-bit integers	**(6)** **(7)**	BTL 1	Remember
6	i).**Express** in detail about Carry look ahead Adder. **Analyze** the overflow in addition and in subtraction.	**(6)** **(7)**	BTL 2	Understand
7	State the integer division algorithm with diagram. ii) Divide $(12)_{10}$ by $(3)_{10}$.	**(7)** **(6)**	BTL 4	Analyze
8	Explain the multiplication of signed 2's complement numbers. Give algorithm with example.	**(13)**	BTL 5	Evaluate
9	i).**Examine**, how floating point addition is carried out in a computer system? ii).Give an example for a binary floating point addition.	**(8)** **(5)**	BTL 1	Remember
10	**i) How** floating point numbers are represented in IEEE 752. ii) Tabulate the IEEE 752 binary representation of the number $5.00736125 * 10^{5}$ in single precision and double precision.	**(7)** **(6)**	BTL 1	Remember
11	i).Design an arithmetic element to perform the basic floating point operations. ii).**Discuss** sub word parallelism.	**(7)** **(6)**	BTL 2	Understand
12	i).**Explain** floating point addition algorithm with diagram. ii). Assess the result of the numbers $(0.5)_{10}$ and $(-0.4375)_{10}$ using binary Floating point Addition algorithm.	**(6)** **(7)**	BTL 5	Evaluate
13	**Calculate** using single precision IEEE 754 representation. i). 32.75 ii).18.125	 **(6)** **(7)**	BTL 4	Analyze
14	**Arrange** the given number 0.0625 i). Single precision. ii). Double precision formats.	 **(6)** **(7)**	BTL 4	Analyze
15	**Solve** using Floating point multiplication algorithm A= $1.110_{10} * 10^{10}$ B= $9.200*10^{-5}$	**(13)**	BTL 3	Apply
16	Multiply $0.5_{10} * - 0.4375_{10}$ using floating point Algorithm.	**(13)**	BTL 3	Apply
17	Calculate the division of A=3.264×10^3 and 6.52×10^2	**(13)**	BTL 3	Apply
PART C				
1	Multiply the following signed numbers A=$(-34)_{10}$ =$(1011110)_2$ and B=$(22)_{10}$= $(0010110)_2$ where B is multiplicand and A is multiplier.	**(15)**	BTL 6	Create
2.	**Evaluat**e the sum of 2.6125 * 101 and 4.150390625 * 101 by hand, assuming A and B are stored in the 16-bit half precision. Assume 1 guard, 1 round bit and 1 sticky bit and round to the nearest even. Show all the steps.	**(15)**	BTL 5	Evaluate

3	**Summarize** 4 bit numbers to save space, which implement the multiplication algorithm for 0010_2 , 0011_2 with hardware design.	**(15)**	BTL 5	Evaluate
4	Design 4 bit version of the algorithm to save pages, for dividing 00000111_2 by 0010_2 with hardware design.	**(15)**	BTL 6	Create
5	Assess the floating point instructions in MIPS.	**(15)**	BTL5	Evaluate

UNIT III–PROCESSOR AND CONTROL UNIT

A Basic MIPS implementation –Building a Data path–Control Implementation Scheme – Pipelining–Pipelined data path and control–Handling Data Hazards & Control Hazards– Exceptions

PART– A

Q.No	Questions		BT Level	Competence
1	Express the control signals required to perform arithmetic operations.		BTL2	Understand
2	Define hazard. Give an example for data hazard.		BTL 2	Understand
3	Recall pipeline bubble.		BTL 1	Remember
4	List the state elements needed to store and access an instruction.		BTL1	Remember
5	Draw the diagram of portion of data path used for fetching instruction.		BTL 2	Understand
6	Distinguish Sign Extend and Vector interrupts.		BTL2	Understand
7	Interpret the R-type instructions.		BTL 2	Understand
8	Evaluate branch taken and branch not taken in instruction execution.		BTL5	Evaluate
9	State the two steps that are common to implement any type of instruction.		BTL 1	Remember
10	Design the instruction format for the jump instruction.		BTL 6	Create
11	Classify the different types of hazards with examples.		BTL 4	Analyze
12	Illustrate data forwarding method to avoid data hazards.		BTL3	Apply
13	Assess the methods to reduce the pipelines tall.		BTL5	Evaluate
14	Articulate the use of branch prediction buffer.		BTL 3	Apply
15	Show the 5 stages pipeline.		BTL 3	Apply
16	Point out the concept of exceptions and interrupts.		BTL4	Analyze
17	What is pipelining?		BTL1	Remember
18	Illustrate the various phases in executing an instruction.		BTL 3	Apply
19	Classify the types of instruction classes and their instruction formats.		BTL4	Analyze
20	Generalize what is exception. Give one example for MIPS exception.		BTL6	Create
21	Assess the need of I type instructions.		BTL5	Evaluate
22	What is meant by branch prediction?		BTL 1	Remember
23	Identify the Structural Hazards in pipelining.		BTL 4	Analyze
24	What is meant by Control Hazard?		BTL 1	Remember
PART B				
1	Discuss the basic MIPS implementation of instruction set.	**(13)**	BTL 2	Understand
2	State and draw a simple MIPS data path with control unit and explain the execution of ALU instruction.	**(13)**	BTL1	Remember

3	i)List the types of hazards ii)Describe the methods for dealing with the control hazards.	**(5)** **(8)**	BTL1	Remember
4	Design and develop an instruction pipeline working under various situations of pipeline stall.	**(13)**	BTL6	Create
5	What is datahazard? How do you over come it?What are its side effects?	**(15)**	BTL1	Remember
6	i)Summarize control implementation scheme. ii)Distinguish the data and control path methods in pipelining.	**(7)** **(6)**	BTL 2	Understand
7	i)Differentiate sequential execution and pipelining ii)Select the model for building a data path.	**(7)** **(6)**	BTL4	Analyze
8	Recommend the techniques for i)Dynamic branch prediction. ii)Static branch prediction.	**(7)** **(6)**	BTL5	Evaluate
9	Examine the approaches would you use to handle exceptions in MIPS.	**(13)**	BTL 3	Apply
10	i)Analyze the hazards caused by unconditional branching statements. ii)Describe operand forwarding in a pipeline processor with a diagram.	**(7)** **(6)**	BTL4	Analyze
11	Express the modified data path to accommodate pipelined executions with a diagram.	**(13)**	BTL 2	Understand
12	i)Explain single cycle and pipelined performance with examples. ii)Point out the advantages of pipeline over single cycle.	**(7)** **(6)**	BTL4	Analyze
13	i)Tabulate the ALU control with suitable truthtable. ii)Differentiate R-type instruction and memory instruction.	**(7)** **(6)**	BTL1	Remember
14	With a suitable set of sequence of instructions show what happens when the branch is taken, assuming the pipeline is optimized for branches that are not taken and that we moved the branch execution to the ID stage.	**(13)**	BTL 3	Apply
15	Explain in detail about the Exceptions.	**(13)**	BTL 2	Understand
16	Sketch the Implementing Jumps and Finalizing Control.	**(13)**	BTL 3	Apply
17	Evaluate the two stage instruction pipeline with neat diagram illustration.	**(13)**	BTL5	Evaluate
PART-C				
1	Assume the following sequence of instructions are executed on a 5 stage pipelined data path: add r5, r2, r1lw r3, 4(r5)lw r2, 0(r2)or r3, r5, r3swr3, 0(r5) If there is no forwarding or hazard detection, insert NOPS to ensure correct execution. i)If the processor has forwarding, but we forgot to implement the hazard detection unit, what if happens when this code executes? ii)If there is forwarding, for the first five cycles, compose which signals are asserted in each cycle. iii)If there is no forwarding, what if new inputs and output signals do we need for the hazard detection unit.	**(5)** **(5)** **(5)**	BTL6	Create
2	Explain in detail about the laundry process through which the pipelining techniques can be established.	**(15)**	BTL5	Evaluate

3	Consider the following loop: Loop:lwr1,0(r1) and r1,r1,r2lw r1,0(r1)lw r1,0(r1) beqr1,r0,loop Assume that perfect branch prediction is used (no stalls) that there are no delay slots, and that the pipeline has full forwarding support. Also assume that many iterations of this loop are executed before the loop exits. i)Assess a pipeline execution diagram for the third iteration of this loop. ii)Show all instructions that are in the pipeline during these cycles (for all iterations).	**(8)** **(7)**	BTL5	Evaluate
4	Plan the pipelining in MIPS architecture and generate the exceptions handled in MIPS.	**(15)**	BTL6	Create
5	Write in detail how exceptions are handled in MIPS architecture.	**(15)**	BTL6	Create

UNIT IV- MEMORY & I/O SYSTEMS

Memory Hierarchy - memory technologies – cache memory – measuring and improving cache performance– virtual memory, TLB's– Accessing I/O Devices–Interrupts–Direct MemoryAccess –Bus structure–Bus operation–Arbitration.

PART– A

Q.No	**Questions**		**BT Level**	**Competence**
1	Distinguish the types of localityof references.		BTL 2	Understand
2	Draw the structure of memory hierarchy		BTL1	Remember
3	Give the definition of memory–mapped I/O.		BTL 2	Understand
4	Compare and contrast SRAM and DRAM.		BTL4	Analyze
5	What is the need to implement memory as a hierarchy ?		BTL1	Remember
6	Define Rotational Latency.		BTL1	Remember
7	Criticize direct-mapped cache.		BTL5	Evaluate
8	Evaluate the following instance where in the cache size is 64 blocks and block size is 16 bytes.What block number does byte address 1200 map?		BTL5	Evaluate
9	Formulate, how many total bits are required for a direct-mapped cache with 16 KB of data and 4-word blocks, assuming a 32-bitaddress ?		BTL6	Create
10	Analyze the writing strategies in cache memory.		BTL4	Analyze
11	Integrate the functional steps required in an instruction cache miss.		BTL6	Create
12	Articulate hitrate and missrate.		BTL 3	Apply
13	Summarize the various block placement schemes in cache memory.		BTL 2	Understand
14	Quote the purpose of Dirty/Modified bit in Cache memory.		BTL1	Remember
15	Point out how DMA can improve I/O speed.		BTL4	Analyze
16	Show the role of TLB in virtual memory.		BTL 3	Apply
17	Illustrate the advantages of virtual memory.		BTL 3	Apply
18	Assess the relationship between physical address and logical address.		BTL5	Evaluate
19	Differentiate Programmed I/O and InterruptI/O.		BTL 2	Understand
20	Demonstrate the sequence of events involved in handling an		BTL 3	Apply

	interrupt request froma single device.			
21	Summarize the various memory technologies ?		BTL 2	Understand
22	Define Hit Ratio.		BTL1	Remember
23	Illustrate a busmaster?		BTL4	Analyze
24	What is an Interrupt?		BTL1	Remember
	PART B			
1	i)List the various memory technologies and examine its relevance in architecture design. ii)Identify the characteristics of memory system.	**(7)** **(6)**	BTL1	Remember
2	Elaborate in detail the memory hierarchy with neat diagram.	**(13)**	BTL1	Remember
3	i)Give the advantages of cache. ii)Identify the basic operations of cache in detail with diagram.	**(7)** **(6)**	BTL 2	Understand
4	Express the following various mapping schemes used in cache design. i)Direct. ii)Associative. iii)Set associative.	 **(4)** **(4)** **(5)**	BTL 2	Understand
5	Analyze the given problem: A byte addressable computer has a small data cache capable of holding eight 32-bit words.Each cache block contains 132-bit word. When a given program is executed, the processor reads data from the following sequence of hex addresses – 200, 204, 208, 20C, 2F4, 2F0, 200,204,218, 21C, 24C, 2F4. The pattern is repeated four times. Assuming that the cache is initially empty, show the contents of the cache at the end of each pass, and compute the hit rate for a direct mapped cache. What are the methods used to measure and improve the performance of the cache.	**(15)**	BTL4	Analyze
6	i)Define virtual memory and its importance. ii)Examine TLB with necessary diagram.	**(7)** **(6)**	BTL1	Remember
7	i)Demonstrate the DMAcontroller. ii)Illustrate how DMA controller isused for direct data transfer between memory and peripherals ?	**(7)** **(6)**	BTL 3	Apply
8	i)Evaluate the advantages of interrupts. ii)Summarize the concept of interrupts with neat diagrams.	**(7)** **(6)**	BTL5	Evaluate
9	Design standard input and output interfaces required to connect the I/O device to the bus.	**(13)**	BTL6	Create
10	Classify the bus arbitration techniques of DMA in detail.	**(13)**	BTL4	Analyze
11	Point out the following in detail i)Programmed I/O. ii)Instructions executed by IOP.	 **(7)** **(6)**	BTL4	Analyze
12	Describe in detail about the methods used to reduce cache misses.	**(13)**	BTL1	Remember
13	Discuss virtual memory address translation in detailwith necessary diagram.	**(13)**	BTL 2	Understand
14	Calculate the performance the processor: Assume the miss rate of an instruction cache is 2% and the miss rate of the data cache is 4%. If a processor has a CPI of 2	**(13)**	BTL 3	Apply

	without any memory stalls and the miss penalty is 100 cycles for all misses, estimate how much faster a processor would run with a perfect cache that never missed. Assume the frequency of all loads and stores is 36%..			
15	Examine about Interrupts and its use.	**(13)**	BTL 3	Apply
16	Describe in detail about the Cache Basics (CacheMemory).	**(13)**	BTL1	Remember
17	Explain in detail about the Interface Circuits.	**(13)**	BTL 2	Understand
	PART-C			
1	Mean Time Between Failures (MTBF), Mean Time To Replacement (MTTR)and Mean Time To Failure (MTTF) are useful metrics for Evaluate thereliability and availability of a storage resource. Explore these concepts byansweringthe questions aboutdevices with the following metrics: MTTF:3 years MTTR: 1 day i)Develop and calculate the MTBF for each of the devices. ii)Develop and calculate the availability for each of the devices. iii)What if happens to availability as the MTTR approaches ? iv)What if happens to availability as the MTTR gets very high?	**(4)** **(4)** **(4)** **(3)**	BTL6	Create
2	Design and explain parallel priority interrupt hardware for a system with eight interrupt sources.	**(15)**	BTL6	Create
3	For a direct mapped cache design with a 32 bit address, the following bits of the address are used to access the cache. Tag:31-10Index:9-5Offset:4-0 i)Judge what is the cache block size? ii)Decide how many entries does the cache have ? iii)Assess what is the ratio between total bits required for such a cache implementation over the data storage bits?	**(5)** **(5)** **(5)**	BTL5	Evaluate
4	Summarize by considering web application. Assuming both client and servers are involved in the process of web browsing application, where can caches be placed to speed upthe process.Design a memory hierarchy forthe system. Show the typical size and latency at various levels of the hierarchy. What is the relationship between the cache size and its access latency?What are the units of data transfers between hierarchies? What is the relationship between data location,data size and transfer latency?	**(15)**	BTL5	Evaluate
5	Formulate in detail about USB.	**(15)**	BTL 6	Create
	UNIT V-PARALLELISM			
Instruction-level-parallelism - Parallel processing challenges – Flynn‘s classification – SISD, MIMD, SIMD, SPMD, and Vector Architectures – Multi-core processors and other Shared Memory Multiprocessors.				
	PART– A			
Q.No	**Questions**		**BT Level**	**Competence**
1	State the main idea of ILP.		BTL 2	Understand
2	Illustrate the overall speedup if a webserver is to be enhanced with a new CPU which is10 times faster on computation than		BTL 3	Apply

	an old CPU.The original CPU spent 40% of its time processing and 60% of its time waiting for I/O.			
3	Illustrate the three important properties of vector instructions.		BTL4	Analyze
4	Analyze the main characteristics of SMT processor.		BTL4	Analyze
5	Quote the importance of loop unrolling technique.		BTL1	Remember
6	Define VLIW processor.		BTL1	Remember
7	Express anti-dependence.How is it removed ?		BTL 2	Understand
8	State the efficiency of super scalar processor.		BTL1	Remember
9	Differentiate between strong scaling and weak scaling.		BTL 2	Understand
10	Show the performance of cluster organization.		BTL 3	Apply
11	Compare SMT and hardware multithreading.		BTL5	Evaluate
12	Define the Flynn classification.		BTL1	Remember
13	Integrate the idea so fin-order execution and out-of-order execution.		BTL6	Create
14	Discriminate UMA and NUMA.		BTL5	Evaluate
15	Quote fine grained multithreading.		BTL1	Remember
16	Express the need for instruction level parallelism.		BTL 2	Understand
17	Formulate the various approaches to hardware multithreading.		BTL6	Create
18	Categorize the various multithreading options.		BTL4	Analyze
19	Differentiate fine grained multithreading and coarse-grained multithreading.		BTL4	Analyze
20	Classify shared memory multiprocessor based on the memory access latency		BTL 3	Apply
21	State Amdahl's law.		BTL1	Remember
22	Criticize the styles of vector architectures ?		BTL5	Evaluate
23	Brief about Multithreading.		BTL 3	Apply
24	Interpret Warehouse-scale computer ?		BTL 2	Understand
PART-B				
1	i)Define parallelism and its types. ii)List the main characteristics of Instruction level parallelism.	**(7)** **(6)**	BTL1	Remember
2	i)Give the concept of parallel processing. ii)Summarize the challenges faced by parallel processing.	**(7)** **(6)**	BTL 2	Understand
3	Express in detail about hardware multithreading.	**(13)**	BTL 2	Understand
4	Solve: suppose you want to achieve a speed up to 90 times faster with100 processors. What percentage of the original computation can be sequential?	**(13)**	BTL 3	Apply
5	List the software and hardware techniques to achieve Instruction Level Parallelism.	**(13)**	BTL1	Remember
6	i)Point out how will you use shared memory concept in multi-processor ? ii)Compare and contrast Fine grained and Coarse grained multithreading.	**(7)** **(6)**	BTL4	Analyze
7	i)Evaluate the features of Multi core processors. ii)How message passing is implemented in Multiprocessors	**(7)** **(6)**	BTL5	Evaluate
8	Classify the types of multithreading and nalyze the advantages of multithreading.	**(13)**	BTL4	Analyze
9	Formulate the ideas of Flynn's classification.	**(13)**	BTL6	Create
10	Sketch in detail about the following i)SISD	**(6)**	BTL3	Apply

	ii)MIMD	**(7)**		
11	Explain simultaneous Multithreading with example.	**(13)**	BTL4	Analyze
12	i)Describe about Graphics Processing unit. ii)Discuss about cluster and warehouse architecture.	**(7)** **(6)**	BTL1	Remember
13	Illustrate the following in detail i)Data Dependence ii)Name Dependence iii)Control dependence	 **(5)** **(4)** **(4)**	BTL3	Apply
14	Discuss the following in detail i)Vector processor. ii)Super scalar processor.	 **(7)** **(6)**	BTL 2	Understand
15	Elaborate in detail about the following i)SIMD ii)SPMD	 **(7)** **(6)**	BTL2	Understand
16	Explain in detail about i)Vector Registers ii)Vector Functional Units iii)Vector Load Store Units.	 **(3)** **(5)** **(5)**	BTL5	Evaluate
17	Describe in detail about the warehouse-scale computers.	**(13)**	BTL1	Remember
	PART-C			
1	Explain how would this loop be scheduled on a static two issue pipeline for MIPS? Loop: lw $t0,0($s1) #$t0=array element Addu $t0,$t0,$s2 #add scalar in $s2 Sw $t0, 0($s1) #storeresult Addi; %s1,$s1, -4 #decrementpointer Bne $s1,$zero,loop # branch $s1!=0 Decide and reorder the instruction to avoid as many pipeline stalls as possible. Assume branches are predicted, so that control hazards are handled by the hardware.	**(15)**	BTL6	Create
2	A pipelined processor uses delayed branch technique. Recommend any one ofthe following possibility for the design of the processor. In the first possibility,the processor has a 4-satge pipeline and one delay slot. In the second possibility, it has a 6-stage pipeline and two delay slots. Compare the performance of these two alternatives, taking only the branch penalty into account. Assume that 20% of the instructions are branch instructions and thatan optimizing compiler has an 80% success rate in filling in the single delayslot.For these cond alternative,the compiler is able to fill the seconds lot 25% of the time.	**(15)**	BTL5	Evaluate
3	Consider the following portions of two different programs running at the same time on four processors in a symmetric multicore processor (SMP). Assume that before this code is run,both x and yare 0? Core 1: x=2; Core 2: y=2; Core 3: w= x + y +1;		BTL6	Create

	Core4: z= x+y; i) What if all the possible resulting values of w, x, y, z ? For each possible outcome,explain how we might arrive at those values. ii)Develop the execution more deterministic so that only one set of values is possible?	**(8)** **(7)**		
4	Suppose we want to perform 2 sums: one is a sum of 10 scalar variables and one is a matrix sum of a pair of two dimensional arrays, with dimensions 10 by10. For now let's assume only the matrix sum is parallelizable. What if the speed up do you get with 10 versus 40 processors and next calculate the speed up assuming the matrices grow to 20 by 20.	**(15)**	BTL5	Evaluate
5	Write about the Cluster Architecture and the types of clusters.	**(15)**	BTL6	Create