

[illegible]

Reserved for EMI

CLINOUT R272 R0402 NSM1 CLIN

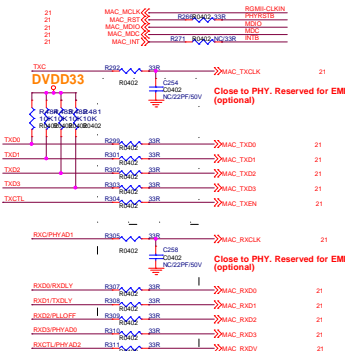
C042
C0402
C022P

VCC

PLL Free run clock output.

SMA Connector is reserved for measurement.
(optional)

CAP close to PHY. Reserved for EMI. (optional)



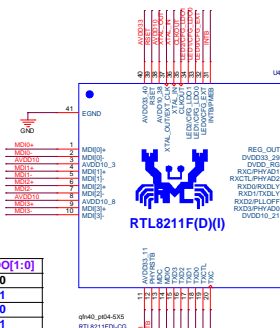
DVDD33

R273 4.7K R0402 INTB

R276 4.7K R0402 PHYRSTB

Pull-up to disable PLL @ ALDPS mode.

Pull-up for additional 2ns delay to TXC/RXC for data latching.

[illegible]

RGMII Power Source	CFG_EXT	CFG_LDO[1:0]
External 3.3V (default)	1'b1	2'b00
External 2.5V	1'b1	2'b01
External 1.8V	1'b1	2'b10
External 1.5V	1'b1	2'b11
Internal 2.5V	1'b0	2'b01
Internal 1.8V	1'b0	2'b10
Internal 1.5V	1'b0	2'b11

PHY Address	PHYAD[2:0]
0	3'b000
1 (default)	3'b001
2	3'b010
3	3'b011
4	3'b100
5	3'b101
6	3'b110
7	3'b111

DVDDQ33

R1706
R1707
DVPDDR3

C299
C300
C301

Note 1: R1705 is not needed for ONLY 3.3V RGMII application, and DVPDDR3 can be connected directly to DVDDQ33.

Note 2: DVPDDR3 must be short (or R1705 be mounted) to DVDDQ33 if the external RGMII 3.3V is selected.

Note 3: R6 must be removed if the internal or external 2.5V/1.8V/1.5V RGMII is selected.

Note 4: CAPs must be closely to pin2 for EMI consideration.

Figure 10: PCB layout for the DVS module. The diagram shows two main sections: "For LDO mode" and "For SWR mode". In LDO mode, a trace from REGOUT goes through capacitors C51 (100nF) and C42 (100nF) to the LDO pin. In SWR mode, a trace from SWR goes through capacitors C52 (100nF) and C43 (100nF) to the SWR pin. Both modes include a 2.2mH inductor L1 and a 1.4uF capacitor C41. The output is connected to a 100nF capacitor C50 and a 100nF capacitor C44. The output voltage is labeled DVDD10 and AVDD10. A note indicates that the trace length from L1 and PHY Pin 30 must be within 0.5 cm, and C6 and C7 to L1 must be within 0.5 cm. Another note states that bypass caps close to PHY DVDD10/AVDD10 power pins are required. A third note mentions that any inductance or dead accept less than 1 nF is not allowed on the path from REGOUT to DVDD10/AVDD10. A fourth note states that R3 is reserved to change the DVDD10/AVDD10 supply source to LDO mode (RTL211FD). A fifth note states that no design change of PCB model is needed if R3 is reserved. A sixth note states that if RTL211FD is selected, the CS should be replaced as 10uF X7R capacitor for industrial grade application. A seventh note states that if RTL211FD is selected, the CS should be replaced for industrial grade application and the value is still under testing.