

Rockchip Developer Guide Linux GMAC Mode Configuration

文件标识: RK-XX-XX-nnn

发布版本: V1.0.0

日期: 2021-01-16

文件密级: ☐绝密 ☐秘密 ☐内部资料 ☒公开

免责声明

本文档按“现状”提供，瑞芯微电子股份有限公司（“本公司”，下同）不对本文档的任何陈述、信息和内容的准确性、可靠性、完整性、适销性、特定目的性和非侵权性提供任何明示或暗示的声明或保证。本文档仅作为使用指导的参考。

由于产品版本升级或其他原因，本文档将可能在未经任何通知的情况下，不定期进行更新或修改。

商标声明

“Rockchip”、“瑞芯微”、“瑞芯”均为本公司的注册商标，归本公司所有。

本文档可能提及的其他所有注册商标或商标，由其各自拥有者所有。

版权所有 © 2020 瑞芯微电子股份有限公司

超越合理使用范畴，非经本公司书面许可，任何单位和个人不得擅自摘抄、复制本文档内容的部分或全部，并不得以任何形式传播。

瑞芯微电子股份有限公司

Rockchip Electronics Co., Ltd.

地址: 福建省福州市铜盘路软件园A区18号

网址: www.rock-chips.com

客户服务电话: +86-4007-700-590

客户服务传真: +86-591-83951833

客户服务邮箱: fae@rock-chips.com

前言

概述

本文提供 Rockchip 平台以太网 GMAC 接口不同模式下的配置用例，用于解决以太网配置问题。

产品版本

芯片名称	内核版本
ROCKCHIP 芯片	3.10/4.4/4.19

读者对象

本文档（本指南）主要适用于以下工程师：

技术支持工程师

软件开发工程师

修订记录

版本号	作者	修改日期	修改说明
V1.0.0	吴达超	2021-01-16	初始版本

目录

Rockchip Developer Guide Linux GMAC Mode Configuration

1. PX30
 - 1.1 RMII Clock Output
 - 1.2 RMII Clock Input
2. RK1808
 - 2.1 RMII Clock Output
 - 2.2 RMII Clock Input
 - 2.3 RGMII Clock Output
 - 2.4 RGMII Clock Input
3. RK3128
 - 3.1 RMII Clock Output
 - 3.2 RMII Clock Input
 - 3.3 RGMII Clock Input
4. RK3228
 - 4.1 RMII Clock Output
 - 4.2 RMII Clock Input
 - 4.3 RGMII Clock Output
 - 4.4 RGMII Clock Input
 - 4.5 Internal EPHY
5. RK3288
 - 5.1 RMII Clock Output
 - 5.2 RMII Clock Input
 - 5.3 RGMII Clock Input
6. RK3328
 - 6.1 RMII Clock Output
 - 6.2 RMII Clock Input
 - 6.3 RGMII Clock Input
 - 6.4 Internal EPHY
7. RK3368
 - 7.1 RMII Clock Output
 - 7.2 RMII Clock Input
 - 7.3 RGMII Clock Input
8. RK3399
 - 8.1 RMII Clock Output
 - 8.2 RMII Clock Input
 - 8.3 RGMII Clock Input
9. RK3568
 - 9.1 RMII Clock Output
 - 9.2 RMII Clock Input
 - 9.3 RGMII PLL output 25M for PHY, PLL output 125M for TX_CLK
 - 9.4 RGMII PLL output 25M for PHY, RGMII_CLK input 125M for TX_CLK
 - 9.5 RGMII Crystal 25M for PHY, PLL output 125M for TX_CLK
 - 9.6 RGMII Crystal 25M for PHY, RGMII_CLK input 125M for TX_CLK
 - 9.7 SGMII
 - 9.8 QSGMII
10. RV1108
 - 10.1 RMII Clock Input
 - 10.2 RMII Clock Output
11. RV1126
 - 11.1 RGMII PLL output 25M for PHY, PLL output 125M for TX_CLK
 - 11.2 RGMII PLL output 25M for PHY, RGMII Clock input 125M for TX_CLK

11.3 RGMII Crytal 25M for PHY, PLL output 125M for TX_CLK

11.4 RGMII Crytal 25M for PHY, RGMII_CLK input 125M for TX_CLK

11.5 RMII Clock Output

11.6 RMII Clock Input

不同模式下的配置主要包含了 phy mode, clock 和 pinctrl 的配置, 这些配置都是关联的, 需要同时配置, 否则无法工作。以下是各芯片不同模式下, 以 SDK 板级 DTS 为例的不同配置方式的参考。

1. PX30

1.1 RMII Clock Output

```
1  &gmac {
2      phy-supply = <&vcc_phy>;
3      clock_in_out = "output";
4      assigned-clocks = <&cru SCLK_MAC>;
5      assigned-clock-rates = <50000000>;
6      snps,reset-gpio = <&gpio2 13 GPIO_ACTIVE_LOW>;
7      snps,reset-active-low;
8      snps,reset-delays-us = <0 50000 50000>;
9      pinctrl-names = "default";
10     pinctrl-0 = <&rmii_pins &mac_refclk_12ma>;
11     status = "okay";
12 };
```

1.2 RMII Clock Input

```
1  &gmac_clkkin {
2      clock-frequency = <50000000>;
3  };
4
5  &gmac {
6      phy-supply = <&vcc_phy>;
7      clock_in_out = "input";
8      assigned-clocks = <&cru SCLK_MAC>;
9      assigned-clock-parents = <&gmac_clkkin>;
10     snps,reset-gpio = <&gpio2 13 GPIO_ACTIVE_LOW>;
11     snps,reset-active-low;
12     snps,reset-delays-us = <0 50000 50000>;
13     pinctrl-names = "default";
14     pinctrl-0 = <&rmii_pins &mac_refclk>;
15     status = "okay";
16 };
```

2. RK1808

2.1 RMII Clock Output

```
1  &gmac {
2      phy-supply = <&vcc_phy>;
3      phy-mode = "rmii";
4      clocks = <&cru SCLK_GMAC>, <&cru SCLK_GMAC_RX_TX>,
5                <&cru SCLK_GMAC_RX_TX>, <&cru SCLK_GMAC_REF>,
6                <&cru SCLK_GMAC_REFOUT>, <&cru ACLK_GMAC>,
7                <&cru PCLK_GMAC>, <&cru SCLK_GMAC_RMII_SPEED>;
8      clock-names = "stmmaceth", "mac_clk_rx",
9                    "mac_clk_tx", "clk_mac_ref",
10                   "clk_mac_refout", "aclk_mac",
11                   "pclk_mac", "clk_mac_speed";
12      assigned-clocks = <&cru SCLK_GMAC_RX_TX>;
13      assigned-clock-parents = <&cru SCLK_GMAC_RMII_SPEED>;
14      snps,reset-gpio = <&gpio0 10 GPIO_ACTIVE_LOW>;
15      snps,reset-active-low;
16      snps,reset-delays-us = <0 50000 50000>;
17      pinctrl-names = "default";
18      pinctrl-0 = <&rmii_pins>;
19      status = "okay";
20  };
```

2.2 RMII Clock Input

```

1  &gmac_clkin {
2      clock-frequency = <50000000>;
3  };
4
5  &gmac {
6      phy-supply = <&vcc_phy>;
7      phy-mode = "rmii";
8      clock_in_out = "input";
9      clocks = <&cru SCLK_GMAC>, <&cru SCLK_GMAC_RX_TX>,
10             <&cru SCLK_GMAC_RX_TX>, <&cru SCLK_GMAC_REF>,
11             <&cru SCLK_GMAC_REFOUT>, <&cru ACLK_GMAC>,
12             <&cru PCLK_GMAC>, <&cru SCLK_GMAC_RMII_SPEED>;
13      clock-names = "stmmaceth", "mac_clk_rx",
14                   "mac_clk_tx", "clk_mac_ref",
15                   "clk_mac_refout", "aclk_mac",
16                   "pclk_mac", "clk_mac_speed";
17      assigned-clocks = <&cru SCLK_GMAC_RX_TX>, <&cru SCLK_GMAC>;
18      assigned-clock-parents = <&cru SCLK_GMAC_RMII_SPEED>, <&gmac_clkin>;
19      snps,reset-gpio = <&gpio0 10 GPIO_ACTIVE_LOW>;
20      snps,reset-active-low;
21      snps,reset-delays-us = <0 50000 50000>;
22      pinctrl-names = "default";
23      pinctrl-0 = <&rmii_pins>;
24      status = "okay";
25  };

```

2.3 RGMII Clock Output

```

1  &gmac {
2      phy-supply = <&vcc_phy>;
3      phy-mode = "rgmii";
4      clock_in_out = "output";
5      assigned-clocks = <&cru SCLK_MAC>;
6      assigned-clock-rates = <125000000>;
7      snps,reset-gpio = <&gpio0 10 GPIO_ACTIVE_LOW>;
8      snps,reset-active-low;
9      /* Reset time is 20ms, 100ms for rtl8211f */
10     snps,reset-delays-us = <0 20000 100000>;
11     tx_delay = <0x50>;
12     rx_delay = <0x3a>;
13     status = "okay";
14 };

```

2.4 RGMII Clock Input

```

1  &gmac {
2      phy-supply = <&vcc_phy>;
3      phy-mode = "rgmii";
4      clock_in_out = "input";
5      assigned-clocks = <&cru SCLK_GMAC>;
6      assigned-clock-parents = <&gmac_clkin>;
7      snps,reset-gpio = <&gpio0 10 GPIO_ACTIVE_LOW>;
8      snps,reset-active-low;
9      /* Reset time is 20ms, 100ms for rtl8211f */
10     snps,reset-delays-us = <0 20000 100000>;
11     tx_delay = <0x50>;
12     rx_delay = <0x3a>;
13     status = "okay";
14 };

```

3. RK3128

3.1 RMII Clock Output

```

1  &gmac {
2      assigned-clocks = <&cru SCLK_MAC_SRC>;
3      assigned-clock-rates = <50000000>;
4      clock_in_out = "output";
5      pinctrl-names = "default";
6      pinctrl-0 = <&rmii_pins>;
7      phy-supply = <&vcc_phy>;
8      phy-mode = "rmii";
9      snps,reset-active-low;
10     snps,reset-delays-us = <0 10000 50000>;
11     snps,reset-gpio = <&gpio2 24 GPIO_ACTIVE_LOW>;
12     status = "okay";
13 };

```

3.2 RMII Clock Input


```

1  &clkin_gmac {
2      clock-frequency = <50000000>;
3  };
4
5  &gmac {
6      assigned-clocks = <&cru SCLK_MAC>;
7      assigned-clock-parents = <&clkin_gmac>;
8      clock_in_out = "input";
9      pinctrl-names = "default";
10     pinctrl-0 = <&rmii_pins>;
11     phy-supply = <&vcc_phy>;
12     phy-mode = "rmii";
13     snps,reset-active-low;
14     snps,reset-delays-us = <0 10000 50000>;
15     snps,reset-gpio = <&gpio2 24 GPIO_ACTIVE_LOW>;
16     status = "okay";
17 };

```

3.3 RGMII Clock Input

```

1  &gmac {
2      assigned-clocks = <&cru SCLK_MAC>;
3      assigned-clock-parents = <&clkin_gmac>;
4      clock_in_out = "input";
5      pinctrl-names = "default";
6      pinctrl-0 = <&rgmii_pins>;
7      phy-supply = <&vcc_phy>;
8      phy-mode = "rgmii";
9      snps,reset-active-low;
10     snps,reset-delays-us = <0 20000 100000>;
11     snps,reset-gpio = <&gpio2 24 GPIO_ACTIVE_LOW>;
12     tx_delay = <0x30>;
13     rx_delay = <0x16>;
14     status = "okay";
15 };

```

4. RK3228

4.1 RMII Clock Output

```

1  &gmac {
2      assigned-clocks = <&cru SCLK_MAC_EXTCLK>, <&cru SCLK_MAC>;
3      assigned-clock-parents = <&ext_gmac>, <&cru SCLK_MAC_EXTCLK>;
4      assigned-clock-rates = <0>, <50000000>;
5      clock_in_out = "output";
6      phy-supply = <&vcc_phy>;
7      phy-mode = "rmii";
8      pinctrl-names = "default";
9      pinctrl-0 = <&rmii_pins>;
10     snps,reset-gpio = <&gpio2 RK_PD0 GPIO_ACTIVE_LOW>;
11     snps,reset-active-low;
12     snps,reset-delays-us = <0 20000 100000>;
13     status = "okay";
14 };

```

4.2 RMII Clock Input

```

1  &ext_gmac: external-gmac-clock {
2      clock-frequency = <50000000>;
3  }
4
5  &gmac {
6      assigned-clocks = <&cru SCLK_MAC_EXTCLK>, <&cru SCLK_MAC>;
7      assigned-clock-parents = <&ext_gmac>, <&cru SCLK_MAC_EXTCLK>;
8      clock_in_out = "input";
9      phy-supply = <&vcc_phy>;
10     phy-mode = "rmii";
11     pinctrl-names = "default";
12     pinctrl-0 = <&rmii_pins>;
13     snps,reset-gpio = <&gpio2 RK_PD0 GPIO_ACTIVE_LOW>;
14     snps,reset-active-low;
15     snps,reset-delays-us = <0 20000 100000>;
16     status = "okay";
17 };

```

4.3 RGMII Clock Output

```

1  &gmac {
2      assigned-clocks = <&cru SCLK_MAC_EXTCLK>, <&cru SCLK_MAC>;
3      assigned-clock-parents = <&ext_gmac>, <&cru SCLK_MAC_EXTCLK>;
4      assigned-clock-rates = <0>, <125000000>;
5      clock_in_out = "output";
6      phy-supply = <&vcc_phy>;
7      phy-mode = "rgmii";
8      pinctrl-names = "default";
9      pinctrl-0 = <&rgmii_pins>;
10     snps,reset-gpio = <&gpio2 RK_PD0 GPIO_ACTIVE_LOW>;
11     snps,reset-active-low;
12     snps,reset-delays-us = <0 20000 100000>;
13     tx_delay = <0x30>;
14     rx_delay = <0x10>;
15     status = "okay";
16 };

```

4.4 RGMII Clock Input

```

1  &gmac {
2      assigned-clocks = <&cru SCLK_MAC_EXTCLK>, <&cru SCLK_MAC>;
3      assigned-clock-parents = <&ext_gmac>, <&cru SCLK_MAC_EXTCLK>;
4      clock_in_out = "input";
5      phy-supply = <&vcc_phy>;
6      phy-mode = "rgmii";
7      pinctrl-names = "default";
8      pinctrl-0 = <&rgmii_pins>;
9      snps,reset-gpio = <&gpio2 RK_PD0 GPIO_ACTIVE_LOW>;
10     snps,reset-active-low;
11     snps,reset-delays-us = <0 20000 100000>;
12     tx_delay = <0x30>;
13     rx_delay = <0x10>;
14     status = "okay";
15 };

```

4.5 Internal EPHY

```

1  &gmac {
2      assigned-clocks = <&cru SCLK_MAC_SRC>;
3      assigned-clock-rates = <50000000>;
4      clock_in_out = "output";
5      phy-supply = <&vcc_phy>;
6      phy-mode = "rmii";
7      phy-handle = <&phy>;
8      status = "okay";
9
10     mdio {
11         compatible = "snps,dwmac-mdio";
12         #address-cells = <1>;
13         #size-cells = <0>;
14
15         phy: ethernet-phy@0 {
16             compatible = "ethernet-phy-id1234.d400", "ethernet-phy-
ieee802.3-c22";
17             reg = <0>;
18             clocks = <&cru SCLK_MAC_PHY>;
19             resets = <&cru SRST_MACPHY>;
20             phy-is-integrated;
21         };
22     };
23 };

```

5. RK3288

5.1 RMII Clock Output

```

1  &gmac {
2      phy-supply = <&vcc_phy>;
3      phy-mode = "rmii";
4      clock_in_out = "output";
5      assigned-clocks = <&cru SCLK_MAC>;
6      assigned-clock-rates = <50000000>;
7      snps,reset-gpio = <&gpio4 RK_PA7 GPIO_ACTIVE_HIGH>;
8      snps,reset-active-low;
9      snps,reset-delays-us = <0 20000 1000000>;
10     pinctrl-names = "default";
11     pinctrl-0 = <&rmii_pins>;
12     status = "okay";
13 };

```

5.2 RMII Clock Input

```

1  &ext_gmac: external-gmac-clock {
2      clock-frequency = <50000000>;
3  }
4
5  &gmac {
6      phy-supply = <&vcc_phy>;
7      phy-mode = "rmii";
8      clock_in_out = "input";
9      assigned-clocks = <&cru SCLK_MAC>;
10     assigned-clock-parents = <&ext_gmac>;
11     snps,reset-gpio = <&gpio4 RK_PA7 GPIO_ACTIVE_HIGH>;
12     snps,reset-active-low;
13     snps,reset-delays-us = <0 20000 1000000>;
14     pinctrl-names = "default";
15     pinctrl-0 = <&rmii_pins>;
16     status = "okay";
17 };

```

5.3 RGMII Clock Input

```

1  &gmac {
2      phy-supply = <&vcc_phy>;
3      phy-mode = "rgmii";
4      clock_in_out = "input";
5      snps,reset-gpio = <&gpio4 RK_PA7 GPIO_ACTIVE_HIGH>;
6      snps,reset-active-low;
7      snps,reset-delays-us = <0 20000 1000000>;
8      assigned-clocks = <&cru SCLK_MAC>;
9      assigned-clock-parents = <&ext_gmac>;
10     pinctrl-names = "default";
11     pinctrl-0 = <&rgmii_pins>;
12     tx_delay = <0x30>;
13     rx_delay = <0x10>;
14     status = "okay";
15 };

```

6. RK3328

6.1 RMII Clock Output

```

1  &gmac2io {
2      phy-supply = <&vcc_phy>;
3      phy-mode = "rmii";
4      clock_in_out = "output";
5      assigned-clocks = <&cru SCLK_MAC2IO>;
6      assigned-clock-rates = <50000000>;
7      snps,reset-gpio = <&gpio1 RK_PC2 GPIO_ACTIVE_LOW>;
8      snps,reset-active-low;
9      snps,reset-delays-us = <0 20000 100000>;
10     pinctrl-names = "default";
11     pinctrl-0 = <&rmii1_pins>;
12     status = "okay";
13 };

```

6.2 RMII Clock Input

```

1  &clkin_gmac {
2      clock-frequency = <50000000>;
3  };
4
5  &gmac2io {
6      phy-supply = <&vcc_phy>;
7      phy-mode = "rmii";
8      clock_in_out = "input";
9      assigned-clocks = <&cru SCLK_MAC2IO>, <&cru SCLK_MAC2IO_EXT>;
10     assigned-clock-parents = <&gmac_clkin>, <&gmac_clkin>;
11     snps,reset-gpio = <&gpio1 RK_PC2 GPIO_ACTIVE_LOW>;
12     snps,reset-active-low;
13     snps,reset-delays-us = <0 20000 100000>;
14     pinctrl-names = "default";
15     pinctrl-0 = <&rmii1_pins>;
16     status = "okay";
17 };

```

6.3 RGMII Clock Input

```

1  &gmac2io {
2      phy-supply = <&vcc_phy>;
3      phy-mode = "rgmii";
4      clock_in_out = "input";
5      assigned-clocks = <&cru SCLK_MAC2IO>, <&cru SCLK_MAC2IO_EXT>;
6      assigned-clock-parents = <&gmac_clkin>, <&gmac_clkin>;
7      snps,reset-gpio = <&gpio1 RK_PC2 GPIO_ACTIVE_LOW>;
8      snps,reset-active-low;
9      snps,reset-delays-us = <0 20000 100000>;
10     pinctrl-names = "default";
11     pinctrl-0 = <&rgmiim1_pins>;
12     tx_delay = <0x26>;
13     rx_delay = <0x11>;
14     status = "okay";
15 };

```

6.4 Internal EPHY

```

1  &gmac2phy {
2      phy-supply = <&vcc_phy>;
3      clock_in_out = "output";
4      assigned-clocks = <&cru SCLK_MAC2PHY_SRC>;
5      assigned-clock-rate = <50000000>;
6      assigned-clocks = <&cru SCLK_MAC2PHY>;
7      assigned-clock-parents = <&cru SCLK_MAC2PHY_SRC>;
8      status = "okay";
9  };

```

7. RK3368

7.1 RMII Clock Output

```

1  &gmac {
2      phy-supply = <&vcc_lan>;
3      phy-mode = "rmii";
4      clock_in_out = "output";
5      assigned-clocks = <&cru SCLK_MAC>;
6      assigned-clock-rates = <50000000>;
7      snps,reset-gpio = <&gpio3 12 0>;
8      snps,reset-active-low;
9      snps,reset-delays-us = <0 20000 100000>;
10     pinctrl-names = "default";
11     pinctrl-0 = <&rmii_pins>;
12     status = "ok";
13 };

```

7.2 RMII Clock Input

```
1  &ext_gmac {
2      clock-frequency = <50000000>;
3  }
4
5  &gmac {
6      phy-supply = <&vcc_lan>;
7      phy-mode = "rmii";
8      clock_in_out = "input";
9      assigned-clocks = <&cru SCLK_MAC>;
10     assigned-clock-parents = <&ext_gmac>;
11     snps,reset-gpio = <&gpio3 12 0>;
12     snps,reset-active-low;
13     snps,reset-delays-us = <0 20000 100000>;
14     pinctrl-names = "default";
15     pinctrl-0 = <&rmii_pins>;
16     status = "ok";
17 };
```

7.3 RGMII Clock Input

```
1  &gmac {
2      phy-supply = <&vcc_lan>;
3      phy-mode = "rmii";
4      clock_in_out = "input";
5      assigned-clocks = <&cru SCLK_MAC>;
6      assigned-clock-parents = <&ext_gmac>;
7      snps,reset-gpio = <&gpio3 12 0>;
8      snps,reset-active-low;
9      snps,reset-delays-us = <0 20000 100000>;
10     pinctrl-names = "default";
11     pinctrl-0 = <&rmii_pins>;
12     status = "okay";
13 };
```

8. RK3399

8.1 RMII Clock Output


```

1  &gmac {
2      assigned-clocks = <&cru SCLK_MAC>;
3      assigned-clock-rates = <500000000>;
4      clock_in_out = "output";
5      phy-supply = <&vcc_phy>;
6      phy-mode = "rmii";
7      pinctrl-names = "default";
8      pinctrl-0 = <&rmii_pins>;
9      snps,reset-gpio = <&gpio3 RK_PB7 GPIO_ACTIVE_LOW>;
10     snps,reset-active-low;
11     snps,reset-delays-us = <0 20000 100000>;
12     status = "okay";
13 };

```

8.2 RMII Clock Input

```

1  &clkin_gmac {
2      clock-frequency = <500000000>;
3  };
4
5  &gmac {
6      assigned-clocks = <&cru SCLK_RMII_SRC>;
7      assigned-clock-parents = <&clkin_gmac>;
8      clock_in_out = "input";
9      phy-supply = <&vcc_phy>;
10     phy-mode = "rmii";
11     pinctrl-names = "default";
12     pinctrl-0 = <&rmii_pins>;
13     snps,reset-gpio = <&gpio3 RK_PB7 GPIO_ACTIVE_LOW>;
14     snps,reset-active-low;
15     snps,reset-delays-us = <0 20000 100000>;
16     status = "okay";
17 };

```

8.3 RGMII Clock Input

```

1  &gmac {
2      assigned-clocks = <&cru SCLK_RMII_SRC>;
3      assigned-clock-parents = <&clkin_gmac>;
4      clock_in_out = "input";
5      phy-supply = <&vcc_phy>;
6      phy-mode = "rgmii";
7      pinctrl-names = "default";
8      pinctrl-0 = <&rgmii_pins>;
9      snps,reset-gpio = <&gpio3 RK_PB7 GPIO_ACTIVE_LOW>;
10     snps,reset-active-low;
11     snps,reset-delays-us = <0 20000 100000>;
12     tx_delay = <0x28>;
13     rx_delay = <0x11>;
14     status = "okay";
15 };

```

9. RK3568

9.1 RMII Clock Output

- gmac0

```

1  &gmac0 {
2      phy-mode = "rmii";
3      clock_in_out = "output";
4      assigned-clocks = <&cru SCLK_GMAC0_RX_TX>, <&cru SCLK_GMAC0>;
5      aassigned-clock-parents = <&cru SCLK_GMAC0_RMII_SPEED>;
6      assigned-clock-rates = <0>, <50000000>;
7
8      snps,reset-gpio = <&gpio3 RK_PC2 GPIO_ACTIVE_LOW>;
9      snps,reset-active-low;
10     snps,reset-delays-us = <0 20000 100000>;
11     pinctrl-names = "default";
12     pinctrl-0 = <&gmac0_miim &gmac0_clkinout &gmac0_rx_bus2 &gmac0_tx_bus2
&gmac0_rx_er>;
13
14     phy-handle = <&rmii_phy0>;
15     status = "okay";
16 };
17
18 &mdio0 {
19     rgmii_phy0: phy@0 {
20         compatible = "ethernet-phy-ieee802.3-c22";
21         reg = <0x0>;
22     };
23 };

```

- gmac1m0:

```
1  &gmac1 {
2      phy-mode = "rmii";
3      clock_in_out = "output";
4      assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>;
5      assigned-clock-parents = <&cru SCLK_GMAC1_RMII_SPEED>;
6      assigned-clock-rates = <0>, <50000000>;
7
8      snps,reset-gpio = <&gpio3 RK_PC2 GPIO_ACTIVE_LOW>;
9      snps,reset-active-low;
10     snps,reset-delays-us = <0 20000 100000>;
11
12     pinctrl-names = "default";
13     pinctrl-0 = <&gmac1m0_miim &gmac1m0_clkout &gmac1m0_rx_bus2
&gmac1m0_tx_bus2 &gmac1m0_rx_er>;
14
15     phy-handle = <&rmii_phy1>;
16     status = "okay";
17 };
18
19 &mdio1 {
20     rgmii_phy1: phy@0 {
21         compatible = "ethernet-phy-ieee802.3-c22";
22         reg = <0x0>;
23     };
24 };
```

- gmac1m1:

```

1  &gmac1 {
2      phy-mode = "rmii";
3      clock_in_out = "output";
4      assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>;
5      assigned-clock-parents = <&cru SCLK_GMAC1_RMII_SPEED>;
6      assigned-clock-rates = <0>, <50000000>;
7
8      snps,reset-gpio = <&gpio3 RK_PC2 GPIO_ACTIVE_LOW>;
9      snps,reset-active-low;
10     snps,reset-delays-us = <0 20000 100000>;
11
12     pinctrl-names = "default";
13     pinctrl-0 = <&gmac1m1_miim &gmac1m1_clkinout &gmac1m1_rx_bus2
&gmac1m1_tx_bus2 &gmac1m1_rx_er>;
14
15     phy-handle = <&rmii_phy1>;
16     status = "okay";
17 };
18
19 &mdio1 {
20     rmii_phy1: phy@0 {
21         compatible = "ethernet-phy-ieee802.3-c22";
22         reg = <0x0>;
23     };
24 };

```

9.2 RMII Clock Input

- gmac0

```

1  &gmac0_clkln{
2      clock-frequency = <50000000>;
3  };
4
5  &gmac0 {
6      phy-mode = "rmii";
7      clock_in_out = "input";
8
9      snps,reset-gpio = <&gpio3 RK_PC2 GPIO_ACTIVE_LOW>;
10     snps,reset-active-low;
11     snps,reset-delays-us = <0 20000 100000>;
12
13     assigned-clocks = <&cru SCLK_GMAC0_RX_TX>, <&cru SCLK_GMAC0>;
14     aassigned-clock-parents = <&cru SCLK_GMAC0_RMII_SPEED>;
15     assigned-clock-rates = <0>, <50000000>;
16
17     pinctrl-names = "default";
18     pinctrl-0 = <&gmac0_miim &gmac0_clklnout &gmac0_rx_bus2 &gmac0_tx_bus2
&gmac0_rx_er>;
19
20     phy-handle = <&rmii_phy0>;
21     status = "okay";
22 };
23
24 &mdio0 {
25     rgmii_phy0: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28     };
29 };

```

- gmac1m0:

```

1  &gmac1_clkln{
2      clock-frequency = <50000000>;
3  };
4
5  &gmac1 {
6      phy-mode = "rmii";
7      clock_in_out = "input";
8
9      snps,reset-gpio = <&gpio3 RK_PC2 GPIO_ACTIVE_LOW>;
10     snps,reset-active-low;
11     snps,reset-delays-us = <0 20000 100000>;
12     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>;
13     assigned-clock-parents = <&cru SCLK_GMAC0_RMII_SPEED>, <&gmac1_clkni>;
14
15     pinctrl-names = "default";
16     pinctrl-0 = <&gmac1m0_miim &gmac1m0_clklnout &gmac1m0_rx_bus2
&gmac1m0_tx_bus2 &gmac1m0_rx_er>;
17
18     phy-handle = <&rmii_phy1>;
19     status = "okay";
20 };
21 &mdio1 {
22     rmii_phy1: phy@0 {
23         compatible = "ethernet-phy-ieee802.3-c22";
24         reg = <0x0>;
25     };
26 };

```

- gmac1m1:

```

1  &gmac1_clkln{
2      clock-frequency = <50000000>;
3  };
4
5  &gmac1 {
6      phy-mode = "rmii";
7      clock_in_out = "input";
8
9      snps,reset-gpio = <&gpio3 RK_PC2 GPIO_ACTIVE_LOW>;
10     snps,reset-active-low;
11     snps,reset-delays-us = <0 20000 100000>;
12     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>;
13     assigned-clock-parents = <&cru SCLK_GMAC0_RMII_SPEED>, <&gmac1_clkln>;
14
15     pinctrl-names = "default";
16     pinctrl-0 = <&gmac1m1_miim &gmac1m1_clklnout &gmac1m1_rx_bus2
&gmac1m1_tx_bus2 &gmac1m1_rx_er>;
17
18     phy-handle = <&rmii_phy1>;
19     status = "okay";
20 };
21
22 &mdio1 {
23     rmii_phy1: phy@0 {
24         compatible = "ethernet-phy-ieee802.3-c22";
25         reg = <0x0>;
26     };
27 };

```

9.3 RGMII PLL output 25M for PHY, PLL output 125M for TX_CLK

- gmac0

```

1  &gmac0 {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4      assigned-clocks = <&cru SCLK_GMAC0_RX_TX>, <&cru SCLK_GMAC0>, <&cru
CLK_MAC0_OUT>;
5      assigned-clock-parents = <&cru SCLK_GMAC0_RGMII_SPEED>;
6      assigned-clock-rates = <0>, <125000000>, <25000000>;
7
8      snps,reset-gpio = <&gpio2 RK_PD3 GPIO_ACTIVE_LOW>;
9      snps,reset-active-high;
10     /* Reset time is 20ms, 100ms for rtl8211f */
11     snps,reset-delays-us = <0 20000 100000>;
12
13     pinctrl-names = "default";
14     pinctrl-0 = <&gmac0_miim
15                 &gmac0_tx_bus2
16                 &gmac0_rx_bus2
17                 &gmac0_rgmii_clk
18                 &gmac0_rgmii_bus
19                 &eth0_pins>;
20
21     tx_delay = <0x3c>;
22     rx_delay = <0x2f>;
23     phy-handle = <&rgmii_phy0>;
24     status = "okay";
25 };
26
27 &mdio0 {
28     rgmii_phy0: phy@0 {
29         compatible = "ethernet-phy-ieee802.3-c22";
30         reg = <0x0>;
31         clocks = <&cru CLK_MAC0_OUT>;
32     };
33 };

```

- gmac1m0


```

1  &gmac1 {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio2 RK_PD1 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>, <&cru
CLK_MAC1_OUT>;
11     assigned-clock-parents = <&cru SCLK_GMAC1_RGMII_SPEED>;
12     assigned-clock-rates = <0>, <125000000>, <25000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac1m0_miim
16                 &gmac1m0_tx_bus2
17                 &gmac1m0_rx_bus2
18                 &gmac1m0_rgmii_clk
19                 &gmac1m0_rgmii_bus
20                 &eth1m0_pins>;
21
22     tx_delay = <0x4f>;
23     rx_delay = <0x26>;
24
25     phy-handle = <&rgmii_phy1>;
26     status = "okay";
27 };
28
29 &mdio1 {
30     rgmii_phy1: phy@0 {
31         compatible = "ethernet-phy-ieee802.3-c22";
32         reg = <0x0>;
33         clocks = <&cru CLK_MAC1_OUT>;
34     };
35 };

```

- gmac1m1

```

1  &gmac1 {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio2 RK_PD1 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>, <&cru
CLK_MAC1_OUT>;
11     assigned-clock-parents = <&cru SCLK_GMAC1_RGMII_SPEED>;
12     assigned-clock-rates = <0>, <125000000>, <25000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac1m1_miim
16                 &gmac1m1_tx_bus2
17                 &gmac1m1_rx_bus2
18                 &gmac1m1_rgmii_clk
19                 &gmac1m1_rgmii_bus
20                 &eth1m1_pins>;
21
22     tx_delay = <0x4f>;
23     rx_delay = <0x26>;
24
25     phy-handle = <&rgmii_phy1>;
26     status = "okay";
27 };
28
29 &mdio1 {
30     rgmii_phy1: phy@0 {
31         compatible = "ethernet-phy-ieee802.3-c22";
32         reg = <0x0>;
33         clocks = <&cru CLK_MAC1_OUT>;
34     };
35 };

```

9.4 RGMII PLL output 25M for PHY, RGMII_CLK input 125M for TX_CLK

- gmac0

```

1  &gmac0 {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4      assigned-clocks = <&cru SCLK_GMAC0_RX_TX>, <&cru SCLK_GMAC0>, <&cru
CLK_MAC0_OUT>;
5      assigned-clock-parents = <&cru SCLK_GMAC0_RGMII_SPEED>, <&gmac0_clkin>;
6      assigned-clock-rates = <0>, <125000000>, <25000000>;
7
8      snps,reset-gpio = <&gpio2 RK_PD3 GPIO_ACTIVE_LOW>;
9      snps,reset-active-high;
10     /* Reset time is 20ms, 100ms for rtl8211f */
11     snps,reset-delays-us = <0 20000 100000>;
12
13     pinctrl-names = "default";
14     pinctrl-0 = <&gmac0_miim
15                 &gmac0_tx_bus2
16                 &gmac0_rx_bus2
17                 &gmac0_rgmii_clk
18                 &gmac0_rgmii_bus
19                 &eth0_pins
20                 &gmac0_clkinout>;
21
22     tx_delay = <0x3c>;
23     rx_delay = <0x2f>;
24     phy-handle = <&rgmii_phy0>;
25     status = "okay";
26 };
27
28 &mdio0 {
29     rgmii_phy0: phy@0 {
30         compatible = "ethernet-phy-ieee802.3-c22";
31         reg = <0x0>;
32         clocks = <&cru CLK_MAC0_OUT>;
33     };
34 };

```

- gmac1m0

```

1  &gmac1 {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4
5      snps,reset-gpio = <&gpio2 RK_PD1 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>, <&cru
CLK_MAC1_OUT>;
11     assigned-clock-parents = <&cru SCLK_GMAC1_RGMII_SPEED>, <&gmac1_clkin>;
12     assigned-clock-rates = <0>, <125000000>, <25000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac1m0_miim
16                 &gmac1m0_tx_bus2
17                 &gmac1m0_rx_bus2
18                 &gmac1m0_rgmii_clk
19                 &gmac1m0_rgmii_bus
20                 &eth1m0_pins
21                 &gmac1m0_clkinout>;
22
23     tx_delay = <0x4f>;
24     rx_delay = <0x26>;
25
26     phy-handle = <&rgmii_phy1>;
27     status = "okay";
28 };
29
30 &mdio0 {
31     rgmii_phy1: phy@0 {
32         compatible = "ethernet-phy-ieee802.3-c22";
33         reg = <0x0>;
34         clocks = <&cru CLK_MAC0_OUT>;
35     };
36 };

```

- gmac1m1

```

1  &gmac1 {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4
5      snps,reset-gpio = <&gpio2 RK_PD1 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>, <&cru
CLK_MAC1_OUT>;
11     assigned-clock-parents = <&cru SCLK_GMAC1_RGMII_SPEED>, <&gmac1_clkin>;
12     assigned-clock-rates = <0>, <125000000>, <25000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac1m1_miim
16                 &gmac1m1_tx_bus2
17                 &gmac1m1_rx_bus2
18                 &gmac1m1_rgmii_clk
19                 &gmac1m1_rgmii_bus
20                 &eth1m1_pins
21                 &gmac1m1_clkinout>;
22
23     tx_delay = <0x4f>;
24     rx_delay = <0x26>;
25
26     phy-handle = <&rgmii_phy1>;
27     status = "okay";
28 };
29
30 &mdio1 {
31     rgmii_phy1: phy@0 {
32         compatible = "ethernet-phy-ieee802.3-c22";
33         reg = <0x0>;
34         clocks = <&cru CLK_MAC1_OUT>;
35     };
36 };

```

9.5 RGMII Crystal 25M for PHY, PLL output 125M for TX_CLK

- gmac0

```

1  &gmac0 {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4      assigned-clocks = <&cru SCLK_GMAC0_RX_TX>, <&cru SCLK_GMAC0>;
5      assigned-clock-parents = <&cru SCLK_GMAC0_RGMII_SPEED>;
6      assigned-clock-rates = <0>, <125000000>;
7
8      snps,reset-gpio = <&gpio2 RK_PD3 GPIO_ACTIVE_LOW>;
9      snps,reset-active-high;
10     /* Reset time is 20ms, 100ms for rtl8211f */
11     snps,reset-delays-us = <0 20000 100000>;
12
13     pinctrl-names = "default";
14     pinctrl-0 = <&gmac0_miim
15                 &gmac0_tx_bus2
16                 &gmac0_rx_bus2
17                 &gmac0_rgmii_clk
18                 &gmac0_rgmii_bus>;
19
20     tx_delay = <0x3c>;
21     rx_delay = <0x2f>;
22     phy-handle = <&rgmii_phy0>;
23     status = "okay";
24 };
25
26 &mdio0 {
27     rgmii_phy0: phy@0 {
28         compatible = "ethernet-phy-ieee802.3-c22";
29         reg = <0x0>;
30     };
31 };

```

- gmac1m0

```

1  &gmac1 {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio2 RK_PD1 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>;
11     assigned-clock-parents = <&cru SCLK_GMAC1_RGMII_SPEED>;
12     assigned-clock-rates = <0>, <125000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac1m0_miim
16                 &gmac1m0_tx_bus2
17                 &gmac1m0_rx_bus2
18                 &gmac1m0_rgmii_clk
19                 &gmac1m0_rgmii_bus>;
20
21     tx_delay = <0x4f>;
22     rx_delay = <0x26>;
23
24     phy-handle = <&rgmii_phy1>;
25     status = "okay";
26 };
27
28 &mdio1 {
29     rgmii_phy1: phy@0 {
30         compatible = "ethernet-phy-ieee802.3-c22";
31         reg = <0x0>;
32     };
33 };

```

- gmac1m1

```

1  &gmac1 {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio2 RK_PD1 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>;
11     assigned-clock-parents = <&cru SCLK_GMAC1_RGMII_SPEED>;
12     assigned-clock-rates = <0>, <125000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac1m1_miim
16                 &gmac1m1_tx_bus2
17                 &gmac1m1_rx_bus2
18                 &gmac1m1_rgmii_clk
19                 &gmac1m1_rgmii_bus>;
20
21     tx_delay = <0x4f>;
22     rx_delay = <0x26>;
23
24     phy-handle = <&rgmii_phy1>;
25     status = "okay";
26 };
27
28 &mdio1 {
29     rgmii_phy1: phy@0 {
30         compatible = "ethernet-phy-ieee802.3-c22";
31         reg = <0x0>;
32     };
33 };

```

9.6 RGMII Crystal 25M for PHY, RGMII_CLK input 125M for TX_CLK

- gmac0


```

1  &gmac0 {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4      assigned-clocks = <&cru SCLK_GMAC0_RX_TX>, <&cru SCLK_GMAC0>;
5      assigned-clock-parents = <&cru SCLK_GMAC0_RGMII_SPEED>, <&gmac0_clkin>;
6      assigned-clock-rates = <0>, <125000000>;
7
8      snps,reset-gpio = <&gpio2 RK_PD3 GPIO_ACTIVE_LOW>;
9      snps,reset-active-high;
10     /* Reset time is 20ms, 100ms for rtl8211f */
11     snps,reset-delays-us = <0 20000 100000>;
12
13     pinctrl-names = "default";
14     pinctrl-0 = <&gmac0_miim
15                 &gmac0_tx_bus2
16                 &gmac0_rx_bus2
17                 &gmac0_rgmii_clk
18                 &gmac0_rgmii_bus
19                 &gmac0_clkinout>;
20
21     tx_delay = <0x3c>;
22     rx_delay = <0x2f>;
23     phy-handle = <&rgmii_phy0>;
24     status = "okay";
25 };
26
27 &mdio0 {
28     rgmii_phy0: phy@0 {
29         compatible = "ethernet-phy-ieee802.3-c22";
30         reg = <0x0>;
31     };
32 };

```

- gmac1m0

```

1  &gmac1 {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4
5      snps,reset-gpio = <&gpio2 RK_PD1 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>;
11     assigned-clock-parents = <&cru SCLK_GMAC1_RGMII_SPEED>, <&gmac1_clkin>;
12     assigned-clock-rates = <0>, <125000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac1m0_miim
16                 &gmac1m0_tx_bus2
17                 &gmac1m0_rx_bus2
18                 &gmac1m0_rgmii_clk
19                 &gmac1m0_rgmii_bus
20                 &gmac1m0_clkinout>;
21
22     tx_delay = <0x4f>;
23     rx_delay = <0x26>;
24
25     phy-handle = <&rgmii_phy1>;
26     status = "okay";
27 };
28
29 &mdio1 {
30     rgmii_phy1: phy@0 {
31         compatible = "ethernet-phy-ieee802.3-c22";
32         reg = <0x0>;
33     };
34 };

```

- gmac1m1

```

1  &gmac1 {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4
5      snps,reset-gpio = <&gpio2 RK_PD1 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>, <&cru SCLK_GMAC1>;
11     assigned-clock-parents = <&cru SCLK_GMAC1_RGMII_SPEED>, <&gmac1_clkin>;
12     assigned-clock-rates = <0>, <125000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac1m1_miim
16                 &gmac1m1_tx_bus2
17                 &gmac1m1_rx_bus2
18                 &gmac1m1_rgmii_clk
19                 &gmac1m1_rgmii_bus
20                 &gmac1m1_clkinout>;
21
22     tx_delay = <0x4f>;
23     rx_delay = <0x26>;
24
25     phy-handle = <&rgmii_phy1>;
26     status = "okay";
27 };
28
29 &mdio1 {
30     rgmii_phy1: phy@0 {
31         compatible = "ethernet-phy-ieee802.3-c22";
32         reg = <0x0>;
33     };
34 };

```

9.7 SGMII

DTS 除了配置 gmac 和 mac phy 节点外，还需要配置 xpcs 和 combophy 节点。

- combophy

其中属性 `rockchip,sgmii-mac-sel` 表示使用的是哪个 gmac:

```

1  &combophy1_usq {
2      rockchip,sgmii-mac-sel = <0>; /* Use gmac0 as sgmii */
3      status = "okay";
4  };

```

- xpcs

```

1  &xpcs {
2      status = "okay";
3  };

```

- gmac0

```

1  &gmac0 {
2      phy-mode = "sgmii";
3
4      rockchip,pipegrf = <&pipegrf>;
5      rockchip,xpcs = <&xpcs>;
6
7      snps,reset-gpio = <&gpio2 RK_PC2 GPIO_ACTIVE_LOW>;
8      snps,reset-active-low;
9      snps,reset-delays-us = <0 20000 100000>;
10
11     assigned-clocks = <&cru SCLK_GMAC0_RX_TX>;
12     assigned-clock-parents = <&gmac0_xpcsclock>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac0_miim>;
16
17     power-domains = <&power RK3568_PD_PIPE>;
18     phys = <&combphy1_usq PHY_TYPE_SGMII>;
19     phy-handle = <&sgmii_phy>;
20     status = "okay";
21 };
22
23 &mdio0 {
24     sgmii_phy: phy@1 {
25         compatible = "ethernet-phy-ieee802.3-c22";
26         reg = <0x1>;
27     };
28 };

```

- gmac1

```

1  &gmac1 {
2      phy-mode = "sgmii";
3
4      rockchip,pipegrf = <&pipegrf>;
5      rockchip,xpcs = <&xpcs>;
6
7      snps,reset-gpio = <&gpio2 RK_PC2 GPIO_ACTIVE_LOW>;
8      snps,reset-active-low;
9      snps,reset-delays-us = <0 20000 100000>;
10
11     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>;
12     assigned-clock-parents = <&gmac1_xpcsclock>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&gmac1_miim>;
16
17     power-domains = <&power RK3568_PD_PIPE>;
18     phys = <&combphy1_usq PHY_TYPE_SGMII>;
19     phy-handle = <&sgmii_phy>;
20     status = "okay";
21 };
22
23 &mdio1 {
24     sgmii_phy: phy@1 {
25         compatible = "ethernet-phy-ieee802.3-c22";
26         reg = <0x1>;
27     };
28 };

```

9.8 QSGMII

同SGMII类似，DTS除了配置gmac和mac phy节点外，还需要配置xpcs和combophy节点。

- combophy

```

1  &combphy2_psq {
2      status = "okay";
3  };

```

- xpcs

```

1  &xpcs {
2      status = "okay";
3  };

```

```

1  &gmac0 {
2      phy-supply = <&pcie20_3v3>;
3      phy-mode = "qsgmii";
4      rockchip,xpcs = <&xpcs>;
5
6      snps,reset-gpio = <&gpio2 RK_PC2 GPIO_ACTIVE_LOW>;
7      snps,reset-active-low;
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru SCLK_GMAC0_RX_TX>;
11     assigned-clock-parents = <&gmac0_xpcsclock>;
12
13     pinctrl-names = "default";
14     pinctrl-0 = <&gmac0_miim>;
15
16     power-domains = <&power RK3568_PD_PIPE>;
17     phys = <&combphy2_psq PHY_TYPE_QSGMII>;
18     phy-handle = <&qsgmii_phy0>;
19
20     status = "okay";
21 };
22
23 &gmac1 {
24     phy-supply = <&pcie20_3v3>;
25     phy-mode = "qsgmii";
26
27     assigned-clocks = <&cru SCLK_GMAC1_RX_TX>;
28     assigned-clock-parents = <&gmac1_xpcsclock>;
29
30     power-domains = <&power RK3568_PD_PIPE>;
31     phy-handle = <&qsgmii_phy1>;
32
33     status = "okay";
34 };
35
36 &mdio0 {
37     qsgmii_phy0: phy@0 {
38         compatible = "ethernet-phy-id001c.c942", "ethernet-phy-ieee802.3-c22";
39         reg = <0x0>;
40     };
41     qsgmii_phy1: phy@1 {
42         compatible = "ethernet-phy-id001c.c942", "ethernet-phy-ieee802.3-c22";
43         reg = <0x1>;
44     };
45     qsgmii_phy2: phy@2 {
46         compatible = "ethernet-phy-id001c.c942", "ethernet-phy-ieee802.3-c22";
47         reg = <0x2>;
48     };
49     qsgmii_phy3: phy@3 {
50         compatible = "ethernet-phy-id001c.c942", "ethernet-phy-ieee802.3-c22";
51         reg = <0x3>;
52     };
53 };

```

10. RV1108

10.1 RMII Clock Input

```
1 gmac_clkin: gmac_clkin {
2     compatible = "fixed-clock";
3     clock-output-names = "gmac_clkin";
4     clock-frequency = <50000000>;
5     #clock-cells = <0>;
6 };
7
8 &gmac {
9     phy-mode = "rmii";
10    clock_in_out = "input";
11    assigned-clocks = <&cru SCLK_MAC>;
12    assigned-clock-parents = <&gmac_clkin>;
13    snps,reset-gpio = <&gpio3 12 0>;
14    snps,reset-active-low;
15    snps,reset-delays-us = <0 20000 100000>;
16    pinctrl-names = "default";
17    pinctrl-0 = <&rmii_pins>;
18    status = "ok";
19 };
```

10.2 RMII Clock Output

```
1 &gmac {
2     phy-mode = "rmii";
3     clock_in_out = "output";
4     assigned-clocks = <&cru SCLK_MAC>;
5     assigned-clock-rates = <50000000>;
6     snps,reset-gpio = <&gpio3 12 0>;
7     snps,reset-active-low;
8     snps,reset-delays-us = <0 20000 100000>;
9     pinctrl-names = "default";
10    pinctrl-0 = <&rmii_pins>;
11    status = "ok";
12 };
```

11. RV1126

11.1 RGMII PLL output 25M for PHY, PLL output 125M for TX_CLK

- gmac m0

```
1  &gmac {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio3 RK_PA0 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>, <&cru
CLK_GMAC_ETHERNET_OUT>;
11     assigned-clock-parents = <&cru CLK_GMAC_SRC_M0>, <&cru RGMII_MODE_CLK>;
12     assigned-clock-rates = <125000000>, <0>, <25000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&rgmiim0_miim &rgmiim0_bus2 &rgmiim0_bus4 &clk0_out_ethernet>;
16
17     tx_delay = <0x2a>;
18     rx_delay = <0x1a>;
19
20     phy-handle = <&phy>;
21     status = "okay";
22 };
23
24 &mdio {
25     phy: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28         clocks = <&cru CLK_GMAC_ETHERNET_OUT>;
29     };
30 };
```

- gmac m1


```

1  &gmac {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio3 RK_PA0 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>, <&cru
CLK_GMAC_ETHERNET_OUT>;
11     assigned-clock-parents = <&cru CLK_GMAC_SRC_M1>, <&cru RGMII_MODE_CLK>;
12     assigned-clock-rates = <125000000>, <0>, <25000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&rgmiim1_miim &rgmiim1_bus2 &rgmiim1_bus4 &clkml_out_ethernet>;
16
17     tx_delay = <0x2a>;
18     rx_delay = <0x1a>;
19
20     phy-handle = <&phy>;
21     status = "okay";
22 };
23
24 &mdio {
25     phy: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28         clocks = <&cru CLK_GMAC_ETHERNET_OUT>;
29     };
30 };

```

11.2 RGMII PLL output 25M for PHY, RGMII Clock input 125M for TX_CLK

- gmac m0

```

1  &gmac {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4
5      snps,reset-gpio = <&gpio3 RK_PA0 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>, <&cru
CLK_GMAC_ETHERNET_OUT>;
11     assigned-clock-parents = <&cru CLK_GMAC_SRC_M0>, <&cru RGMII_MODE_CLK>;
12     assigned-clock-rates = <125000000>, <0>, <25000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&rgmiim0_miim &rgmiim0_bus2 &rgmiim0_bus4 &clk0_out_ethernet>;
16
17     tx_delay = <0x2a>;
18     rx_delay = <0x1a>;
19
20     phy-handle = <&phy>;
21     status = "okay";
22 };
23
24 &mdio {
25     phy: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28         clocks = <&cru CLK_GMAC_ETHERNET_OUT>;
29     };
30 };

```

- gmac m1

```

1  &gmac {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4
5      snps,reset-gpio = <&gpio3 RK_PA0 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>, <&cru
CLK_GMAC_ETHERNET_OUT>;
11     assigned-clock-parents = <&cru CLK_GMAC_SRC_M1>, <&cru RGMII_MODE_CLK>;
12     assigned-clock-rates = <125000000>, <0>, <25000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&rgmiim1_miim &rgmiim1_bus2 &rgmiim1_bus4 &clkml_out_ethernet>;
16
17     tx_delay = <0x2a>;
18     rx_delay = <0x1a>;
19
20     phy-handle = <&phy>;
21     status = "okay";
22 };
23
24 &mdio {
25     phy: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28         clocks = <&cru CLK_GMAC_ETHERNET_OUT>;
29     };
30 };

```

11.3 RGMII Crytal 25M for PHY, PLL output 125M for TX_CLK

- gmac m0

```

1  &gmac {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio3 RK_PA0 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>;
11     assigned-clock-parents = <&cru CLK_GMAC_SRC_M0>, <&cru RGMII_MODE_CLK>;
12     assigned-clock-rates = <125000000>, <0>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&rgmiim0_miim &rgmiim0_bus2 &rgmiim0_bus4 &clkm0_out_ethernet>;
16
17     tx_delay = <0x2a>;
18     rx_delay = <0x1a>;
19
20     phy-handle = <&phy>;
21     status = "okay";
22 };
23
24 &mdio {
25     phy: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28     };
29 };

```

- gmac m1

```

1  &gmac {
2      phy-mode = "rgmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio3 RK_PA0 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>;
11     assigned-clock-parents = <&cru CLK_GMAC_SRC_M1>, <&cru RGMII_MODE_CLK>;
12     assigned-clock-rates = <125000000>, <0>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&rgmiim1_miim &rgmiim1_bus2 &rgmiim1_bus4 &clkml_out_ethernet>;
16
17     tx_delay = <0x2a>;
18     rx_delay = <0x1a>;
19
20     phy-handle = <&phy>;
21     status = "okay";
22 };
23
24 &mdio {
25     phy: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28     };
29 };

```

11.4 RGMII Crytal 25M for PHY, RGMII_CLK input 125M for TX_CLK

- gmac m0

```

1  &gmac {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4
5      snps,reset-gpio = <&gpio3 RK_PA0 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru CLK_GMAC_RGMII_M0>, <&cru CLK_GMAC_SRC_M0>, <&cru
CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>;
11     assigned-clock-parents = <&gmac_clkin_m0>, <&cru CLK_GMAC_RGMII_M0>, <&cru
CLK_GMAC_SRC_M0>, <&cru RGMII_MODE_CLK>;
12
13     pinctrl-names = "default";
14     pinctrl-0 = <&rgmiim0_miim &rgmiim0_bus2 &rgmiim0_bus4>;
15
16     tx_delay = <0x2a>;
17     rx_delay = <0x1a>;
18
19     phy-handle = <&phy>;
20     status = "okay";
21 };
22
23 &mdio {
24     phy: phy@0 {
25         compatible = "ethernet-phy-ieee802.3-c22";
26         reg = <0x0>;
27     };
28 };

```

- gmac m1

```

1  &gmac {
2      phy-mode = "rgmii";
3      clock_in_out = "input";
4
5      snps,reset-gpio = <&gpio3 RK_PA0 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      /* Reset time is 20ms, 100ms for rtl8211f */
8      snps,reset-delays-us = <0 20000 100000>;
9
10     assigned-clocks = <&cru CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>, <&cru
CLK_GMAC_ETHERNET_OUT>;
11     assigned-clock-parents = <&cru CLK_GMAC_SRC_M1>, <&cru RGMII_MODE_CLK>;
12     assigned-clock-rates = <125000000>, <0>, <25000000>;
13
14     pinctrl-names = "default";
15     pinctrl-0 = <&rgmiim1_miim &rgmiim1_bus2 &rgmiim1_bus4>;
16
17     tx_delay = <0x2a>;
18     rx_delay = <0x1a>;
19
20     phy-handle = <&phy>;
21     status = "okay";
22 };
23
24 &mdio {
25     phy: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28     };
29 };

```

11.5 RMII Clock Output

- gmac m0

```

1  &gmac {
2      phy-mode = "rmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio3 RK_PC5 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      snps,reset-delays-us = <0 50000 50000>;
8
9      assigned-clocks = <&cru CLK_GMAC_SRC_M0>, <&cru CLK_GMAC_SRC>, <&cru
CLK_GMAC_TX_RX>;
10     assigned-clock-rates = <0>, <500000000>;
11     assigned-clock-parents = <&cru CLK_GMAC_RGMII_M0>, <&cru CLK_GMAC_SRC_M0>,
<&cru RMII_MODE_CLK>;
12
13     pinctrl-names = "default";
14     pinctrl-0 = <&rmii0_miim &rgmiim0_rxer &rmii0_bus2 &rgmiim0_mclkinout>;
15
16     phy-handle = <&phy>;
17     status = "okay";
18 };
19
20 &mdio {
21     phy: phy@0 {
22         compatible = "ethernet-phy-ieee802.3-c22";
23         reg = <0x0>;
24     };
25 };

```

- gmac m1


```

1  &gmac {
2      phy-mode = "rmii";
3      clock_in_out = "output";
4
5      snps,reset-gpio = <&gpio3 RK_PC5 GPIO_ACTIVE_LOW>;
6      snps,reset-active-low;
7      snps,reset-delays-us = <0 50000 50000>;
8
9      assigned-clocks = <&cru CLK_GMAC_SRC_M1>, <&cru CLK_GMAC_SRC>, <&cru
CLK_GMAC_TX_RX>;
10     assigned-clock-rates = <0>, <500000000>;
11     assigned-clock-parents = <&cru CLK_GMAC_RGMII_M1>, <&cru CLK_GMAC_SRC_M1>,
<&cru RMII_MODE_CLK>;
12
13     pinctrl-names = "default";
14     pinctrl-0 = <&rmii1_miim &rgmii1_rxer &rmii10_bus2 &rgmii1_mclkinout>;
15
16     phy-handle = <&phy>;
17     status = "okay";
18 };
19
20 &mdio {
21     phy: phy@0 {
22         compatible = "ethernet-phy-ieee802.3-c22";
23         reg = <0x0>;
24     };
25 };

```

11.6 RMII Clock Input

- gmac m0

```

1  &gmac_clkin_m0 {
2      clock-frequency = <50000000>;
3  };
4
5  &gmac {
6      phy-mode = "rmii";
7      clock_in_out = "input";
8
9      snps,reset-gpio = <&gpio3 RK_PC5 GPIO_ACTIVE_LOW>;
10     snps,reset-active-low;
11     snps,reset-delays-us = <0 50000 50000>;
12
13     assigned-clocks = <&cru CLK_GMAC_RGMII_M0>, <&cru CLK_GMAC_SRC_M0>, <&cru
CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>;
14     assigned-clock-rates = <0>, <0>, <50000000>;
15     assigned-clock-parents = <&gmac_clkin_m0>, <&cru CLK_GMAC_RGMII_M0>, <&cru
CLK_GMAC_SRC_M0>, <&cru RMII_MODE_CLK>;
16
17     pinctrl-names = "default";
18     pinctrl-0 = <&rmii0_miim &rgmiim0_rxer &rmii0_bus2
&rgmiim0_mclkinout_level0>;
19
20     phy-handle = <&phy>;
21     status = "okay";
22 };
23
24 &mdio {
25     phy: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28     };
29 };

```

- gmac m1

```

1  &gmac_clkin_m1 {
2      clock-frequency = <50000000>;
3  };
4
5  &gmac {
6      phy-mode = "rmii";
7      clock_in_out = "input";
8
9      snps,reset-gpio = <&gpio3 RK_PC5 GPIO_ACTIVE_LOW>;
10     snps,reset-active-low;
11     snps,reset-delays-us = <0 50000 50000>;
12
13     assigned-clocks = <&cru CLK_GMAC_RGMII_M1>, <&cru CLK_GMAC_SRC_M1>, <&cru
CLK_GMAC_SRC>, <&cru CLK_GMAC_TX_RX>;
14     assigned-clock-rates = <0>, <0>, <50000000>;
15     assigned-clock-parents = <&gmac_clkin_m1>, <&cru CLK_GMAC_RGMII_M1>, <&cru
CLK_GMAC_SRC_M1>, <&cru RMII_MODE_CLK>;
16
17     pinctrl-names = "default";
18     pinctrl-0 = <&rmii1_miim &rgmii1_rxer &rmii1_bus2
&rgmii1_mclkinout_level0>;
19
20     phy-handle = <&phy>;
21     status = "okay";
22 };
23
24 &mdio {
25     phy: phy@0 {
26         compatible = "ethernet-phy-ieee802.3-c22";
27         reg = <0x0>;
28     };
29 };

```