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SOICbite Programming/Debug Connector Footprint

This PCB footprint allows you to use 3mm x 6mm edge of PCB and a SOIC-8 clip as a cheap and space-efficient connector

Simon Merrett

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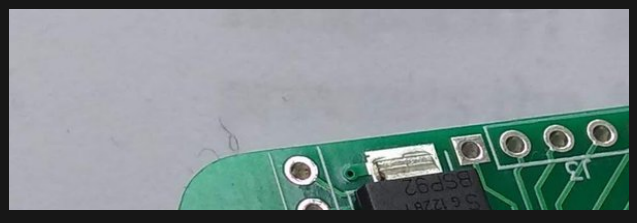

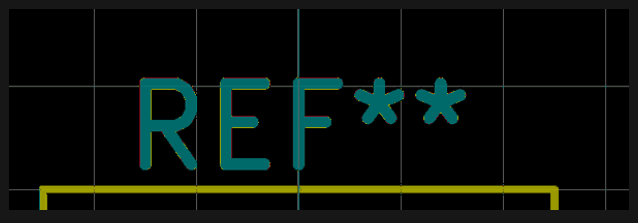

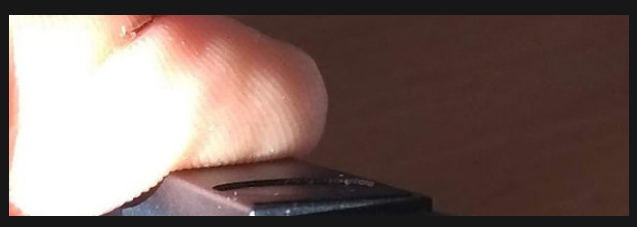

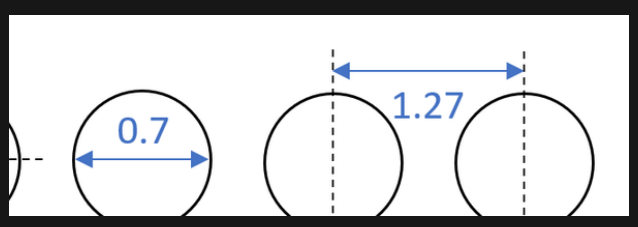

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Simon Merrett

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PCB PROGRAMMING SOIC DEBUG CONNECTOR PROGRAMMER

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THIS PROJECT IS SUBMITTED FOR

- Hackaday.com Tip Line

This project was created on 06/03/2019 and last updated 5 years ago.

DESCRIPTION

It's cheaper than a Tag Connect and may even be smaller.

This has been tested as a SPI programmer on AVRs, a UART programmer on ESP32 and SWD programmer @2MHz on SAMD51.
The footprints are available as a Kicad mod footprint file under downloads. On the Github repo there's now an Eagle version too. If anyone converts them to other EDA footprint formats, I'll happily add them here or host them in the Github repo.

You do need to adjust your SOIC-8 test clip so that it will close enough to press the contact pins against the PCB pads. See the photos - about 1mm will do to start with. Depending on your pin configuration, you need to make sure opposing contacts don't touch each other when no PCB is between them.

Also, you may need to use short sections of thin traces to escape the pads between the NPTH.

DETAILS

UPDATE 14 Aug 19: Github now has a USB suggested pinout and a converter board from USB micro to SOICbite USB, thanks to @Patrick Fenner !

UPDATE 29 Jul 19: Now confirmed working as SWD link to programme UF2 bootloader on SAMD51 at 2MHz SWD clock.

UPDATE 13 Jul 19: An unchecked dimensional drawing is available in the project images for generating other EDA package footprints. Would be great if someone can check this drawing, either against the existing kicad/eagle footprints or building in another EDA, sending to PCB fab and confirming connection with the SOIC clip.

UPDATE 17 Jun 19: The Github repo now includes an Eagle version! Please test and check it works.

UPDATE 14 Jun 19: The Github repo readme.md now has suggested pad mapping for a variety of interfaces, thanks to @Jens Hauke .

FILES

SOIC_clipProg.kicad_mod

This has longer pads. Not recommended because it takes up more PCB area but was the first design I tried.

kicad_mod - 1.58 kB - 06/03/2019 at 17:19

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SOIC_clipProgSmall.kicad_mod

This is the recommended footprint for now. Has been tested and is the version in the project photos

kicad_mod - 1.88 kB - 06/03/2019 at 17:19

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DISCUSSIONS

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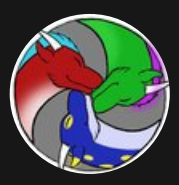


Xasin wrote 03/06/2021 at 16:55

Time to use this in my own projects now!
Just added it to my WIP Smart Home board, and it seems to fit well so far :>

The eight pins work great for the ESP's UART, I might even have enough free to squeeze JTAG alongside it.

Thanks <3

Simon Merrett wrote 03/06/2021 at 17:03

Great! Let me know if you can think of any way to improve it.

SamGurdus1 wrote 05/11/2020 at 05:28

I love this idea and am planning on using it on a project soon. I have a question about the thin traces used to escape the NPTH. What trace width have you had success with? I am planning on using the SOICbite to program an ATtiny85. Thanks for creating this!

Simon Merrett wrote 05/11/2020 at 07:03

Hi Sam, I have used 0.17mm traces to escape the centre pads "as-is". However, if you open the part in the footprint editor you can change the pad clearance for the holes to something smaller. This should let you use wider traces. I

may need to do a design revision to make this standard.

SamGurdus1 wrote 05/20/2020 at 21:18

I'm not sure I understand what you mean regarding the pad clearance. I am running into an issue because JLCPCB says that their minimum NPTH to Track clearance is 0.25mm. My EDA seems to think that with .17mm traces, there is a clearance of around 0.195m.

Simon Merrett wrote 05/20/2020 at 21:24

@SamGurdus1 if you open the SOICbite footprint in the kicad footprint editor (or whatever your EDA equivalent is) and go into the clearances on the NPTHs (select one NPTH and press "e" in kicad, then I think it's the third tab along in the pad edit window).

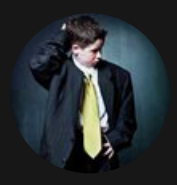
I've used 0.17mm on several boards with SOICbite from JLCPCB and haven't had any issues with that design rule.

Sam Ettinger wrote 03/09/2020 at 21:02

Thank you so much for this! I used the SOICbite on my latest project (https://hackaday.io/project/170302-12-switches-1-led-1-sao) and it made programming (and reprogramming, and re-reprogramming) a breeze! I'll definitely use it for future projects as well!

Simon Merrett wrote 03/09/2020 at 21:14

Hi @Sam Ettinger thanks for taking the time to try this and let me know how it helped you - made me smile! I love your project. Just wish the "S" in SAO stood for something else!

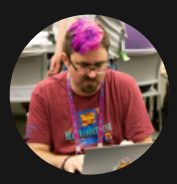


akohlsmith wrote 02/21/2020 at 23:12

This is so much better than that Tag-Connect garbage. multi-source, inexpensive, configurable... great job!

Simon Merrett wrote 02/21/2020 at 23:19

Thanks @akohlsmith . It's not perfect but it has a lot going for it. Please contribute to the github repository if you do any mods or breakouts with it. Even verifying the layout drawing would be useful!



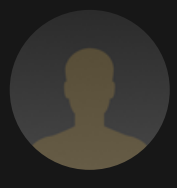
siddacious wrote 10/09/2019 at 15:47

FYI I successfully used the Eagle footprint on my newest board. Works great but the clip I used needed more than a bit of modification to work properly and probably needs a stiffer spring.

All told it's lived up to it's promise! Great job

Simon Merrett wrote 10/09/2019 at 20:13

@siddacious I'm so pleased and it's great that you took the time to let me know it helped you. Thanks. I have noticed a stiffer spring would be better but that it often improves if you go back and cut out a bit further/cleaner into the hinge section. Most of the resistance to closing on my three clips (I don't take them off the programmers now!) is usually a sliver of plastic that hasn't been cleanly cut away in the hinge area.



Peter Elliot wrote 07/11/2019 at 16:49

Very clever. I just bought two clips to try it out.

Do you have a PDF/Image with a dimensions for the recommended holes and pad sizes and spacing (looks to be on a 25mil grid), as I don't use either Kicad or Eagle. If not I'll install Kicad and then look at your footprint, but a document would be helpful for future reference.

furry [illegible] wrote [illegible] at 20:50

Wh[illegible] for me" rather than anything canonical.

https://www.amazon.com/Ximimark-SOIC8-Socket-Adpter-Programmer/dp/B07BRSVRXV
/ref=sr_1_5?keywords=soic+test+clip&qid=1561491531&s=gateway&sr=8-5

Lloyd Konneker wrote 06/20/2019 at 12:30

But the clip doesn't clamp down far enough to actually grab onto a normal circuit board.

Does the clip register before it makes contact? IOW, can the clip contacts short two pads while you are connecting the clip? (I don't have a SOIC test clip so I can't measure or experiment.) The TagConnect registers before making contact. Wouldn't be a problem if board and clip are unpowered, but something to think about. Since I only need four pins, I could separate the pads more, rip out every other contact on the clip.

Simon Merrett wrote 06/20/2019 at 12:40

Clip spring contacts do touch the PCB pads before the claws/teeth resister (or not) so it's possible that you could short the pads together. If the pad space were greater than the clip contacts, you'd find this much less of a risk. Most SOIC clip assemblies seem to have a cable with an IDC connector on the other end, so I just disconnect that, attach the clip and then attach the IDC connection.

You absolutely could make your pads sparse and customise your clip. I would recommend against having VCC and GND on "diagonally opposite" pads (e.g. 1 and 5 or 4 and 8) so you can't reverse power the board if you get the clip on the wrong way round. I think this is unlikely because the ribbon cables attached to SOIC clips usually have an index wire of a different colour (e.g. red instead of grey) which you can use as Pin 1, lined up with the Pad 1 of the footprint (denoted by the silkscreen partial outline round the pad).

Lloyd Konneker wrote 06/25/2019 at 18:44

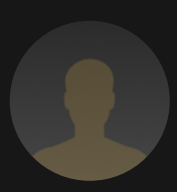
Also, I see that the contacts don't mate while the clip is not attached. Which is good. But one must be careful not to hack the clip so much that they do. Then one might need to be more careful about connecting: connect to board, then connect to programmer, as you have already stated you do. In my case (4 pins), I want to put Vcc opposite ground (so as you say, they are not diagonal) but if they do mate, and are plugged into the probe, they would short the probe power supply. Stuff to think about.

Lloyd Konneker wrote 06/19/2019 at 18:41

Clever, nice work. I use TagConnect, this seems better. For SBW (SpiByWire), you only need two pads on each side. I wanted to hack at my TagConnect, now I will do this instead.

Simon Merrett wrote 06/19/2019 at 20:23

Thanks, looking forward to seeing the results.



technophile.sw wrote 06/19/2019 at 16:18

Great idea, thanks!

Seems like the holes wouldn't need to be NPTH, if that removes a PCB build step and mfg cost. Just make the pads the same size as or about 0.002" larger than the holes.

Keying: could leave out some holes or use additional key holes or slots (with longer pegs added) to either side. Board edge notches perhaps, making the connector easier to find.

Simon Merrett wrote 06/19/2019 at 18:37

Good thoughts, and thanks for thanking! Although, I'm not sure I understand you correctly. The holes are staggered, relative to the pads, so I don't know if your suggestion would work how you imagine. As I said, I may have missed what you mean though! Also, this is two sided, so a PTH would possibly connect two different signals together. I haven't found NPTH to be an added cost on the board houses I use but if you'd like to submit a version with your changes to the Github repo, I'll host it with the others.

Ref keying, since publishing this I do wonder whether an edge-notch would be a good way to quickly line up, just as you have. I think it would require more modification to the clip, so I haven't done anything with it for now. Willing to take EDA footprint files as suggestions though!

I'd be happy to add project team members who'd like to work on this aspect.

I know of at least one engineer who is interested in e.g. SWD and more than one ground pad. His "ideal" would require 10 pads but the next size up SOIC test clip that I'm aware of is 14 pins, so we'd need to cut one of those down. They also don't appear to be available as cheaply as the SOIC 8 format, understandably.

Contributors and team members welcome!

Simon Merrett wrote

thanks, hope it helps!

Daninamiri wrote 06/13/2019 at 08:08

That is just ingenious!!!

BTW why do you need vias (NPTH)?

Simon Merrett wrote 06/13/2019 at 08:17

Well it's just a way to mechanically align and retain the spring contact with the pads. There are teeth/claws on the SOIC clip that engage with these NPTH to align the clip with the footprint and hold it in place. If you wanted to remove them, that would be fine. I have been pondering removing the middle three holes and seeing if the outer two could achieve the same function - this would require another physical modification to the SOIC test clip, as you would need to cut or abrade down the top and bottom middle three (six total) "claws", leaving just the outer ones to engage. One benefit of removing the middle three NPTH would be easier escaping of traces. Feel free to push a new version on the Github!

Jeff Epler wrote 06/13/2019 at 12:48

If you make the pattern asymmetrical (e.g., omit just the 3rd and 4th out of 5 NPTHs), you've now got a keyed connector

Simon Merrett wrote 06/13/2019 at 15:03

@jepler that's a nice idea. If you look in the side profile of the SOIC clip I modified in the project photos, you'll see that the spring conductors of the clip are closer to the PCB, so I don't think this keyed design would save you from VCC touching the wrong pads but visually it might help you line stuff up.

FWIW, I unplug my IDC connector on the other end of the ribbon cable, then connect the SOICbite and then replug the IDC in. Only takes a second but makes me feel better!

Gerben wrote 06/04/2019 at 13:23

That's really clever.

Thank you for sharing.

Simon Merrett wrote 06/04/2019 at 19:51

You're welcome!

SIMILAR PROJECTS

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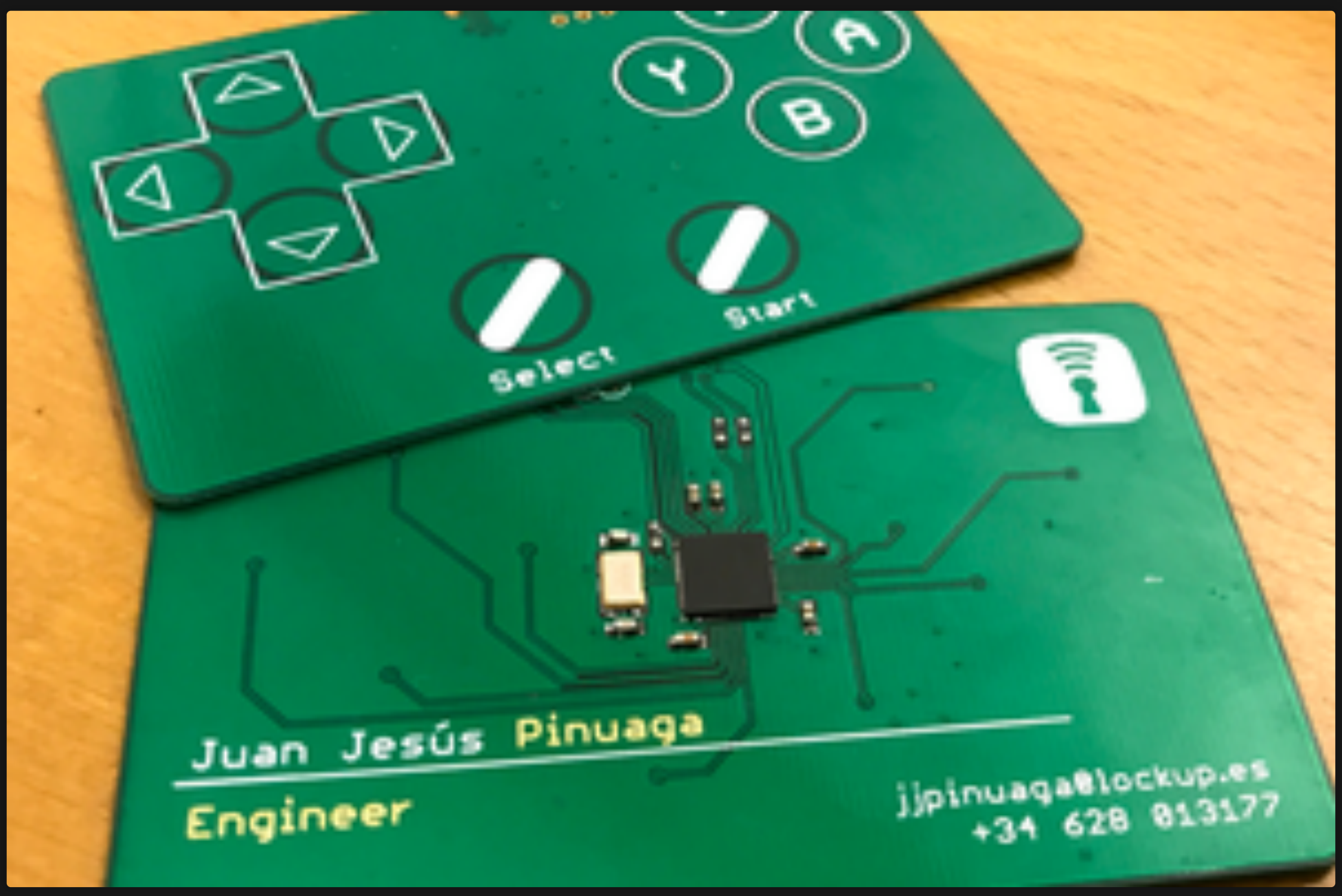
Pedro Minatel



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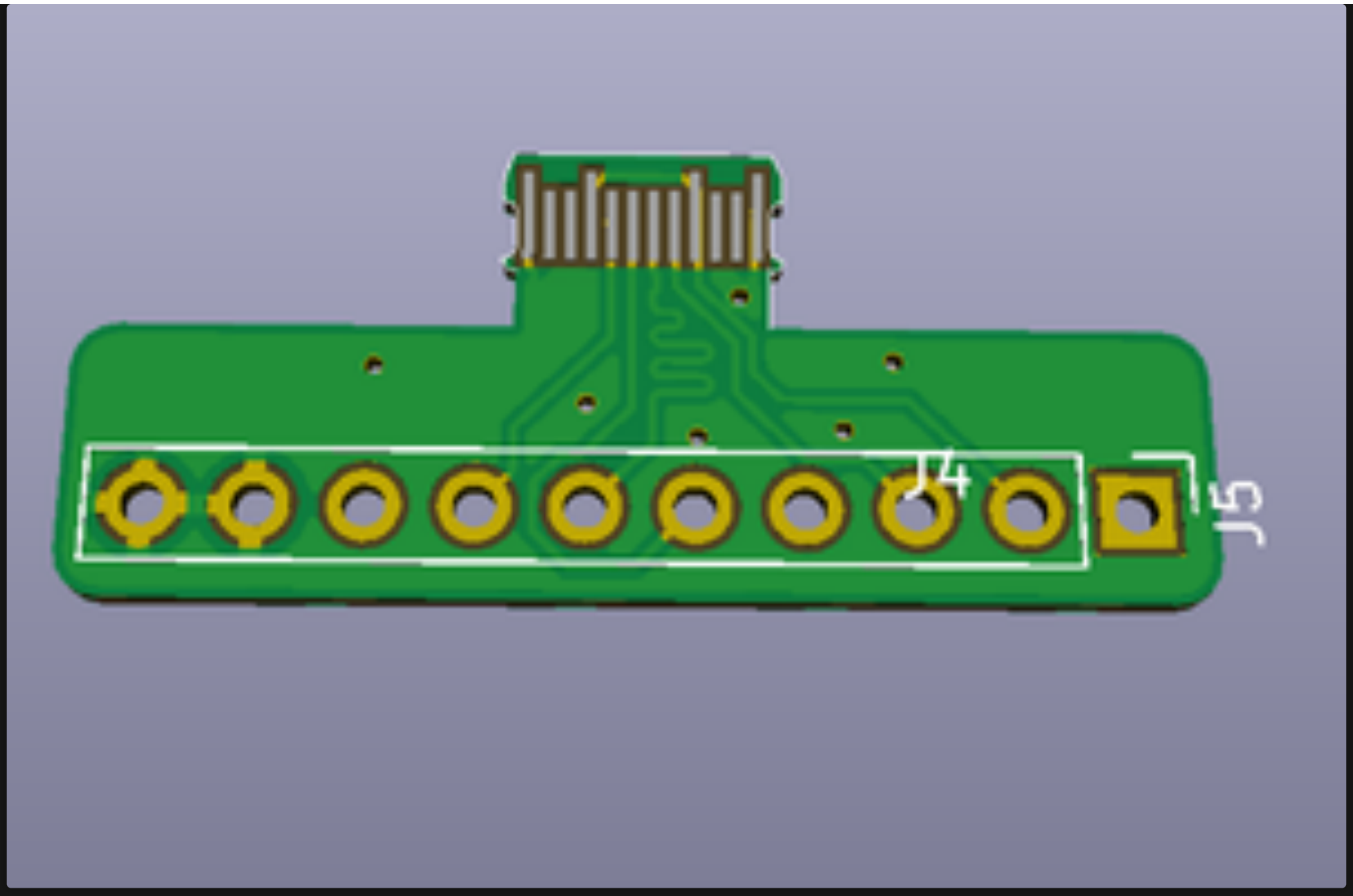

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