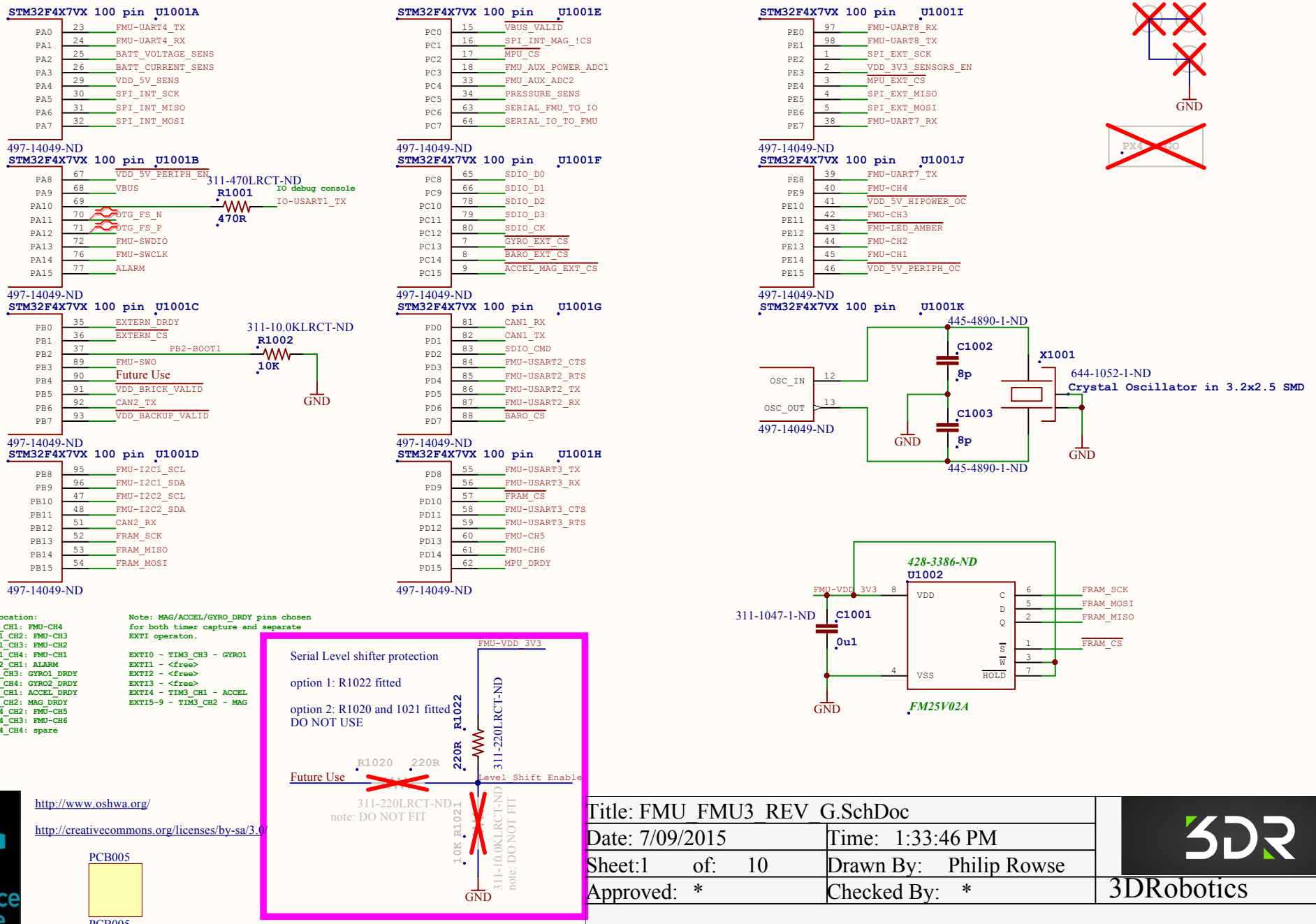
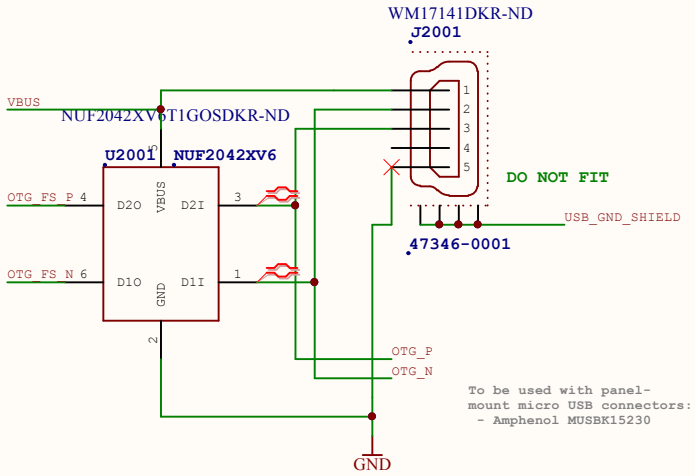
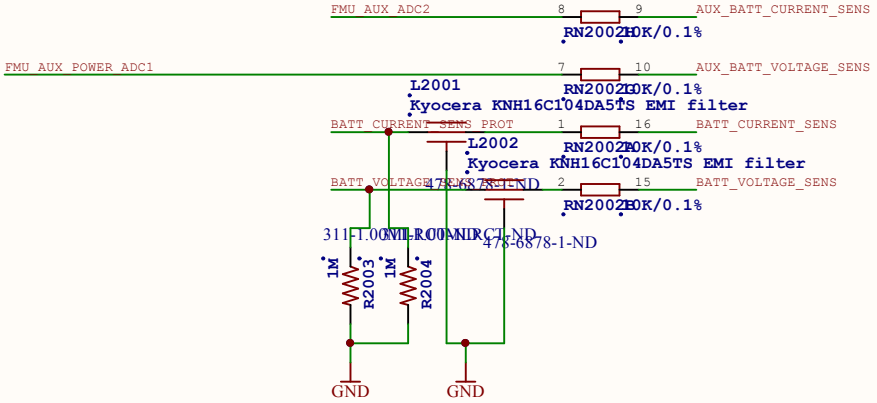
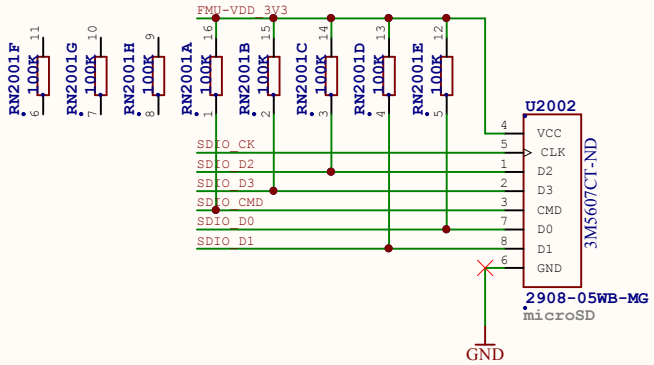
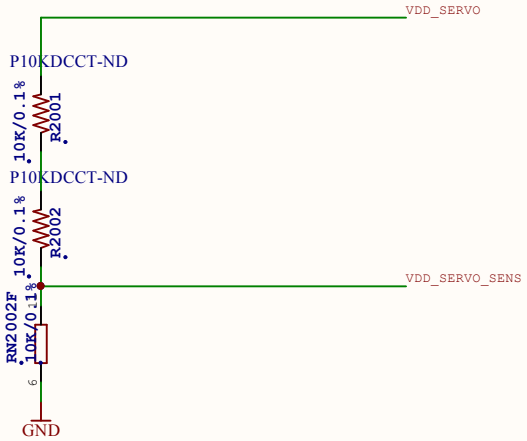
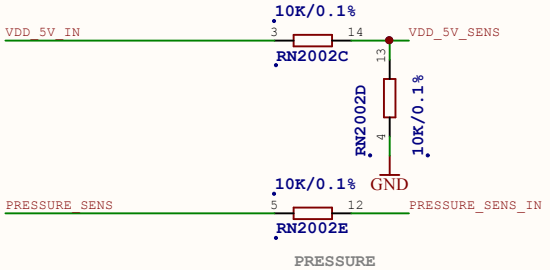

STM32F4X7VX 100 pin U1001A
PA0 23 FMU-UART4_TX
PA1 24 FMU-UART4_RX
PA2 25 BATT_VOLTAGE_SENS
PA3 26 BATT_CURRENT_SENS
PA4 29 VDD_5V_SENS
PA5 30 SPI_INT_SCK
PA6 31 SPI_INT_MISO
PA7 32 SPI_INT_MOSI
497-14049-ND
STM32F4X7VX 100 pin U1001B
PA8 67 VDD_5V_PERIPH_EN
PA9 68 VBUS
PA10 69
PA11 70 OTG_FS_N
PA12 71 OTG_FS_P
PA13 72 FMU-SWDIO
PA14 76 FMU-SWCLK
PA15 77 ALARM
311-470LRCT-ND
R1001
470R
IO debug console
IO-USART1_TX
497-14049-ND
STM32F4X7VX 100 pin U1001C
PB0 35 EXTERN_DRDY
PB1 36 EXTERN_CS
PB2 37 PB2-BOOT1
PB3 89 FMU-SWO
PB4 90 Future Use
PB5 91 VDD_BRICK_VALID
PB6 92 CAN2_TX
PB7 93 VDD_BACKUP_VALID
311-10.0KLRCT-ND
R1002
10K
GND
497-14049-ND
STM32F4X7VX 100 pin U1001D
PB8 95 FMU-I2C1_SCL
PB9 96 FMU-I2C1_SDA
PB10 47 FMU-I2C2_SCL
PB11 48 FMU-I2C2_SDA
PB12 51 CAN2_RX
PB13 52 FRAM_SCK
PB14 53 FRAM_MISO
PB15 54 FRAM_MOSI
497-14049-ND
STM32F4X7VX 100 pin U1001E
PC0 15 VBUS_VALID
PC1 16 SPI_INT_MAG_!CS
PC2 17 MPU_CS
PC3 18 FMU_AUX_POWER_ADC1
PC4 33 FMU_AUX_ADC2
PC5 34 PRESSURE_SENS
PC6 63 SERIAL_FMU_TO_IO
PC7 64 SERIAL_IO_TO_FMU
497-14049-ND
STM32F4X7VX 100 pin U1001F
PC8 65 SDIO_D0
PC9 66 SDIO_D1
PC10 78 SDIO_D2
PC11 79 SDIO_D3
PC12 80 SDIO_CK
PC13 7 GYRO_EXT_CS
PC14 8 BARO_EXT_CS
PC15 9 ACCEL_MAG_EXT_CS
497-14049-ND
STM32F4X7VX 100 pin U1001G
PD0 81 CAN1_RX
PD1 82 CAN1_TX
PD2 83 SDIO_CMD
PD3 84 FMU-USART2_CTS
PD4 85 FMU-USART2_RTS
PD5 86 FMU-USART2_TX
PD6 87 FMU-USART2_RX
PD7 88 BARO_CS
497-14049-ND
STM32F4X7VX 100 pin U1001H
PD8 55 FMU-USART3_TX
PD9 56 FMU-USART3_RX
PD10 57 FRAM_CS
PD11 58 FMU-USART3_CTS
PD12 59 FMU-USART3_RTS
PD13 60 FMU-CH5
PD14 61 FMU-CH6
PD15 62 MPU_DRDY
497-14049-ND
STM32F4X7VX 100 pin U1001I
PE0 97 FMU-UART8_RX
PE1 98 FMU-UART8_TX
PE2 1 SPI_EXT_SCK
PE3 2 VDD_3V3_SENSORS_EN
PE4 3 MPU_EXT_CS
PE5 4 SPI_EXT_MISO
PE6 5 SPI_EXT_MOSI
PE7 38 FMU-UART7_RX
497-14049-ND
STM32F4X7VX 100 pin U1001J
PE8 39 FMU-UART7_TX
PE9 40 FMU-CH4
PE10 41 VDD_5V_HIPOWER_OC
PE11 42 FMU-CH3
PE12 43 FMU-LED_AMBER
PE13 44 FMU-CH2
PE14 45 FMU-CH1
PE15 46 VDD_5V_PERIPH_OC
497-14049-ND
STM32F4X7VX 100 pin U1001K
445-4890-1-ND
C1002
8p
X1001
644-1052-1-ND
Crystal Oscillator in 3.2x2.5 SMD
OSC_IN 12
OSC_OUT 13
497-14049-ND
GND
C1003
8p
GND
445-4890-1-ND
GND
428-3386-ND
U1002
FMU-VDD_3V3 8
311-1047-1-ND
C1001
0u1
VDD
VSS
C 6
D 5
Q 2
S 1
WP 3
HOLD 7
FRAM_SCK
FRAM_MOSI
FRAM_MISO
FRAM_CS
GND
FM25V02A
Timer allocation:
PE9: TIM1_CH1: FMU-CH4
PE11: TIM1_CH2: FMU-CH3
PE13: TIM1_CH3: FMU-CH2
PE14: TIM1_CH4: FMU-CH1
PA15: TIM2_CH1: ALARM
PB0: TIM3_CH3: GYRO1_DRDY
PB1: TIM3_CH4: GYRO2_DRDY
PB4: TIM3_CH1: ACCEL_DRDY
PB5: TIM3_CH2: MAG_DRDY
PD13: TIM4_CH2: FMU-CH5
PD14: TIM4_CH3: FMU-CH6
PD15: TIM4_CH4: spare
Note: MAG/ACCEL/GYRO_DRDY pins chosen for both timer capture and separate EXTI operaton.
EXTI0 - TIM3_CH3 - GYRO1
EXTI1 - <free>
EXTI2 - <free>
EXTI3 - <free>
EXTI4 - TIM3_CH1 - ACCEL
EXTI5-9 - TIM3_CH2 - MAG
Serial Level shifter protection
option 1: R1022 fitted
option 2: R1020 and 1021 fitted
DO NOT USE
FMU-VDD_3V3
R1022
220R
311-220LRCT-ND
R1020
220R
Future Use
Level_Shift_Enable
311-220LRCT-ND
note: DO NOT FIT
R1021
10K
311-10.0KLRCT-ND
note: DO NOT FIT
GND
http://www.oshwa.org/
http://creativecommons.org/licenses/by-sa/3.0/
PCB005
PCB005
Title: FMU_FMU3_REV_G.SchDoc
Date: 7/09/2015
Time: 1:33:46 PM
Sheet:1 of: 10
Drawn By: Philip Rowse
Approved: *
Checked By: *
3DRobotics





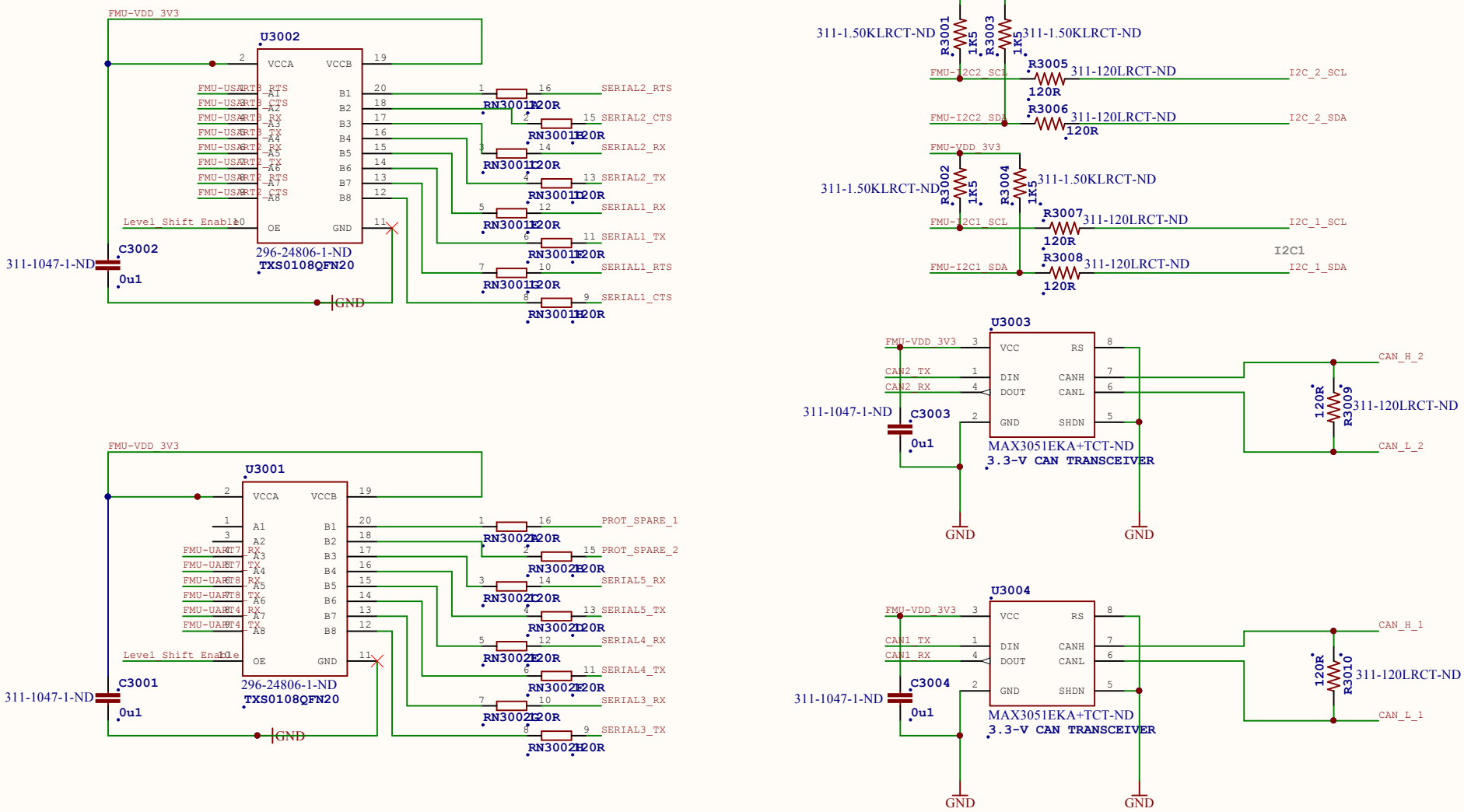






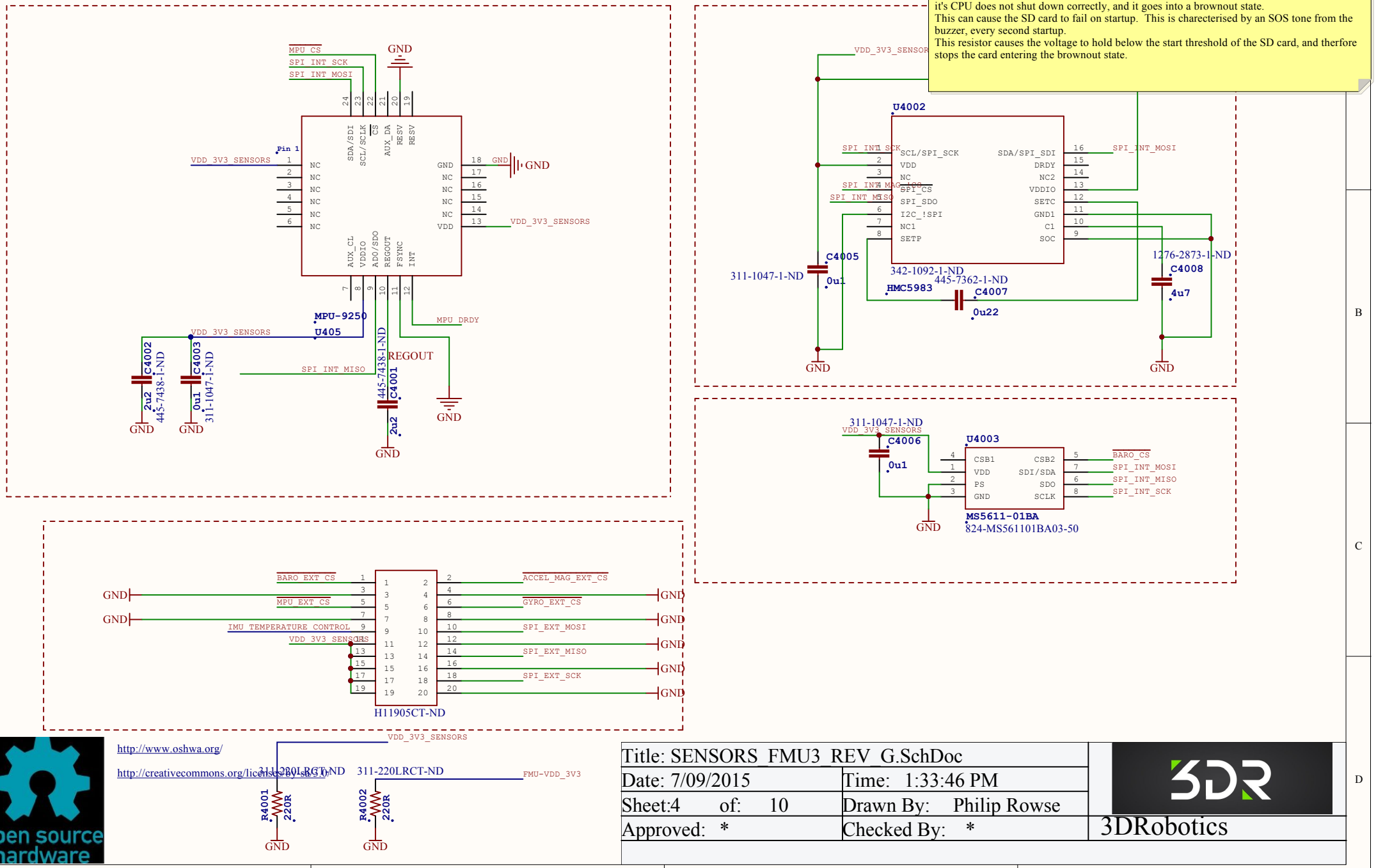
Title: SD_USB_FMU3_REV_G.SchDoc	
Date: 7/09/2015	Time: 1:33:46 PM
Sheet:2 of: 10	Drawn By: Philip Rowse
Approved: *	Checked By: *

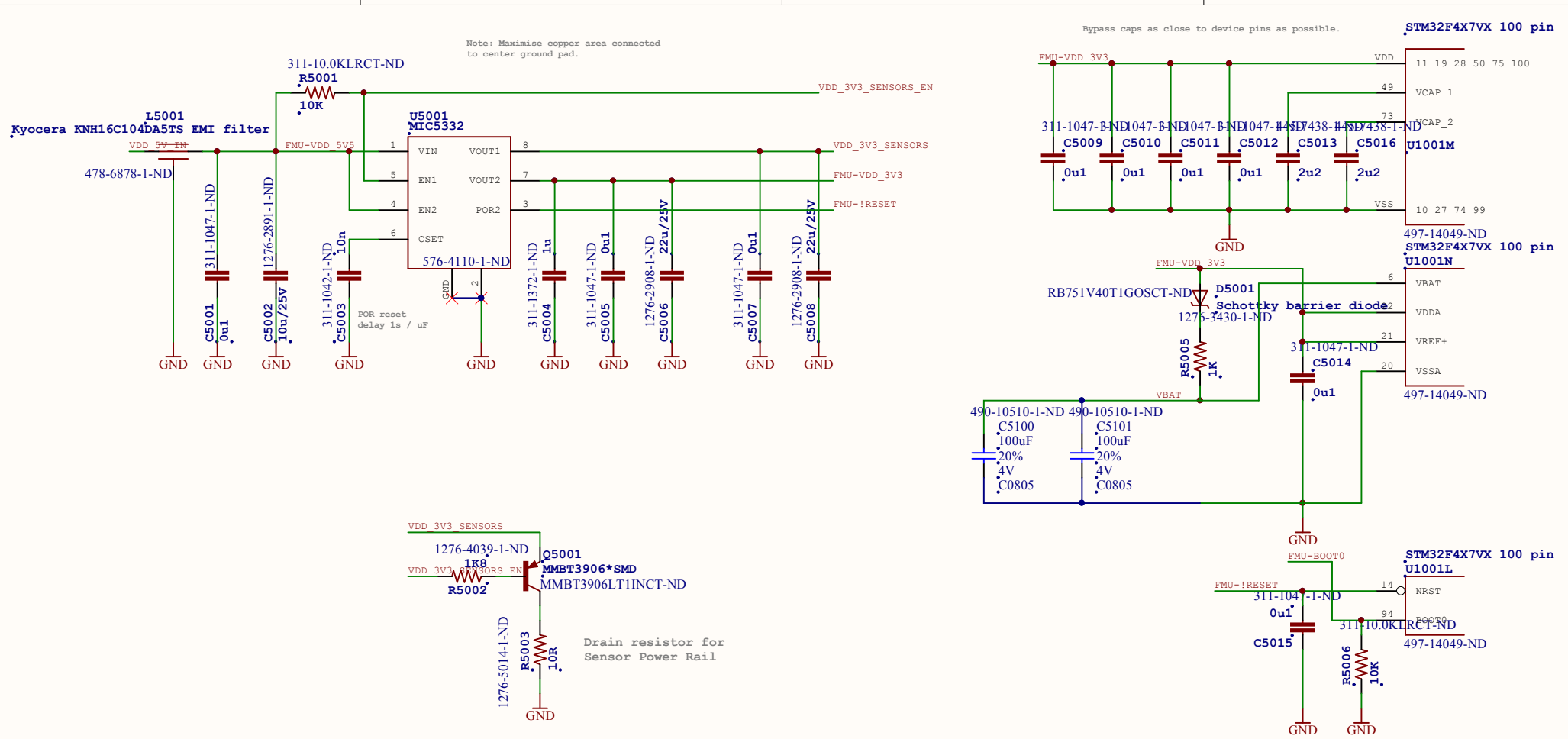
3DRobotics



Title: SERIAL_FMU3_REV_G.SchDoc	
Date: 7/09/2015	Time: 1:33:46 PM
Sheet:3 of: 10	Drawn By: Philip Rowse
Approved: *	Checked By: *

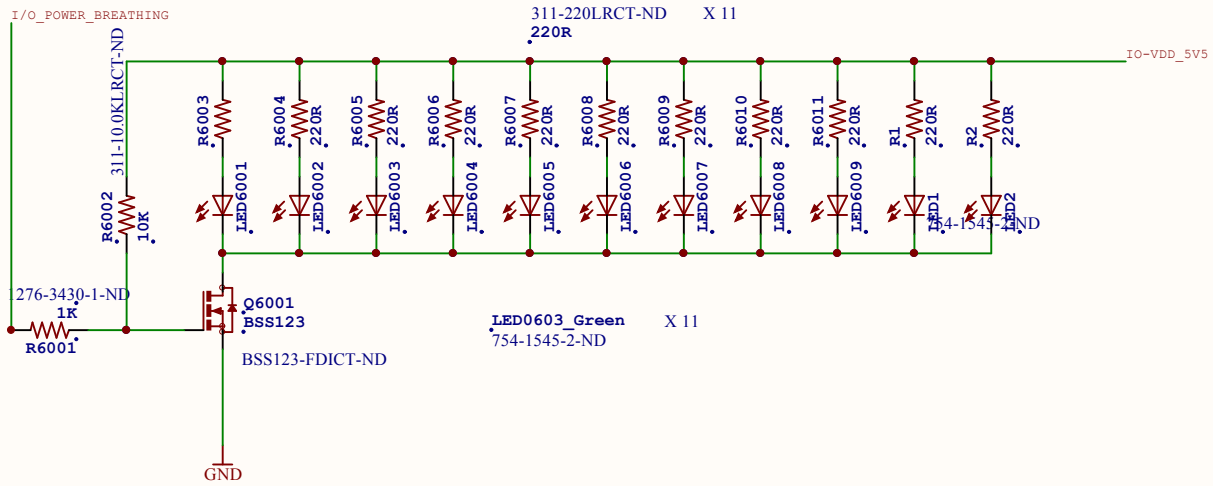
3DRobotics

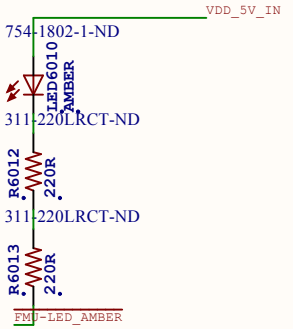

due to the serial lines being able to back power the cpu, The SD card can end up in a state where it's CPU does not shut down correctly, and it goes into a brownout state.
This can cause the SD card to fail on startup. This is charecterised by an SOS tone from the buzzer, every second startup.
This resistor causes the voltage to hold below the start threshold of the SD card, and therfore stops the card entering the brownout state.
MPU-9250
U405
REGOUT
MPU_DRDY
SPI_INT_MISO
VDD_3V3_SENSORS
GND
U4002
HMC5983
U4003
MS5611-01BA
824-MS561101BA03-50
H11905CT-ND
http://www.oshwa.org/
http://creativecommons.org/licenses/by-sa/3.0/
Title: SENSORS_FMU3_REV_G.SchDoc
Date: 7/09/2015
Time: 1:33:46 PM
Sheet:4 of: 10
Drawn By: Philip Rowse
Approved: *
Checked By: *
3DRobotics

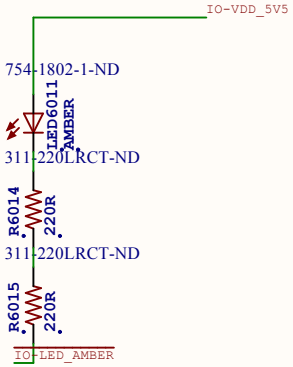


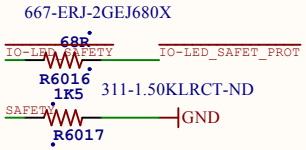
Title: FMU_Power_FMU3_REV_G.SchDoc	
Date: 7/09/2015	Time: 1:33:47 PM
Sheet:5 of: 10	Drawn By: Philip Rowse
Approved: *	Checked By: *

3DRobotics



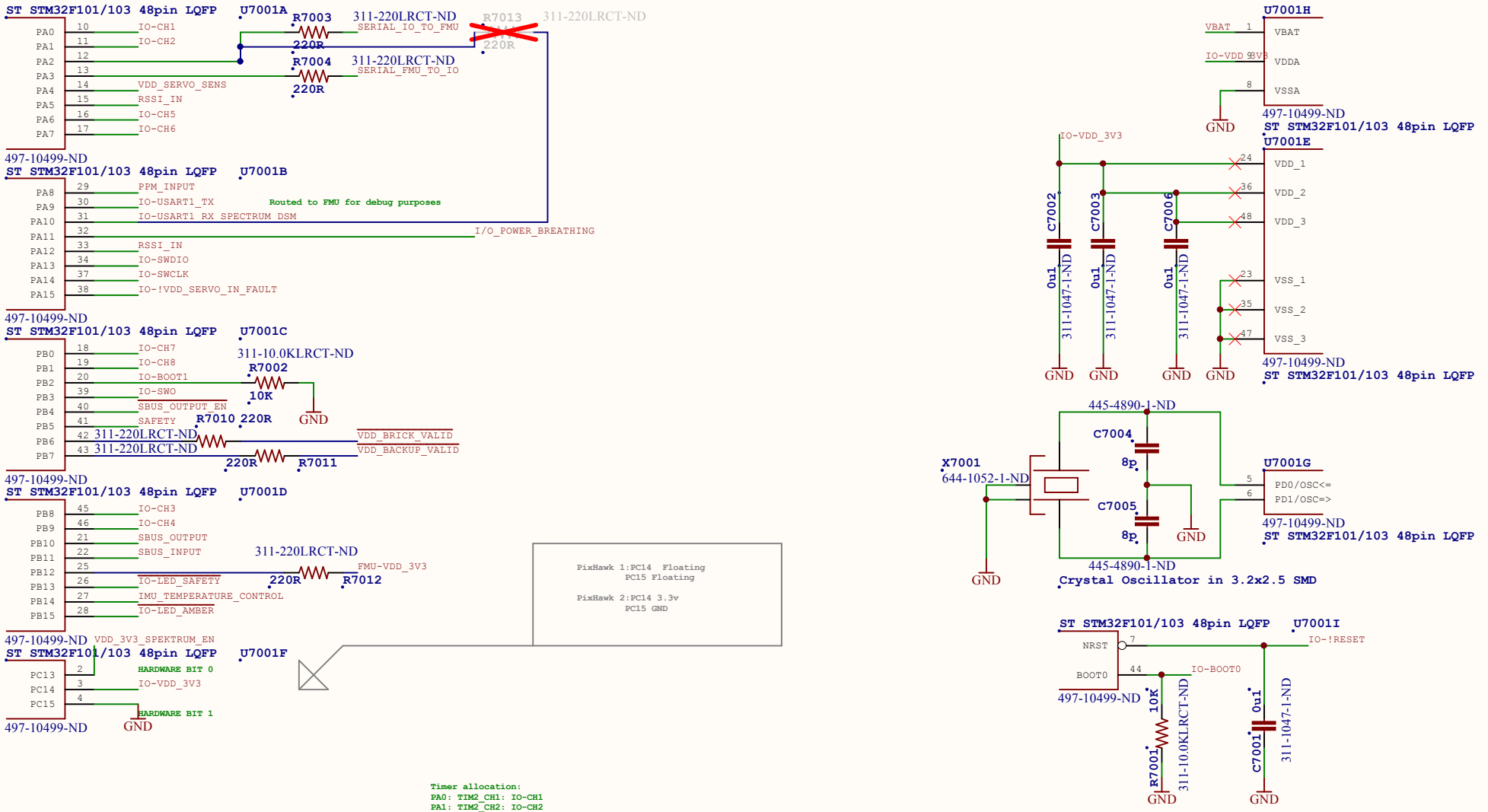






Title: LEDs_FMU3_REV_G.SchDoc	
Date: 7/09/2015	Time: 1:33:47 PM
Sheet:6 of: 10	Drawn By: Philip Rowse
Approved: *	Checked By: *

3DRobotics



Title: IO_FMU3_REV_G.SchDoc	
Date: 7/09/2015	Time: 1:33:47 PM
Sheet:7 of: 10	Drawn By: Philip Rowse
Approved: *	Checked By: *

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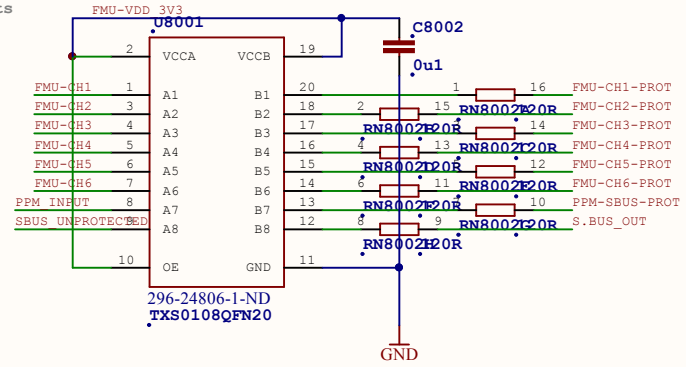
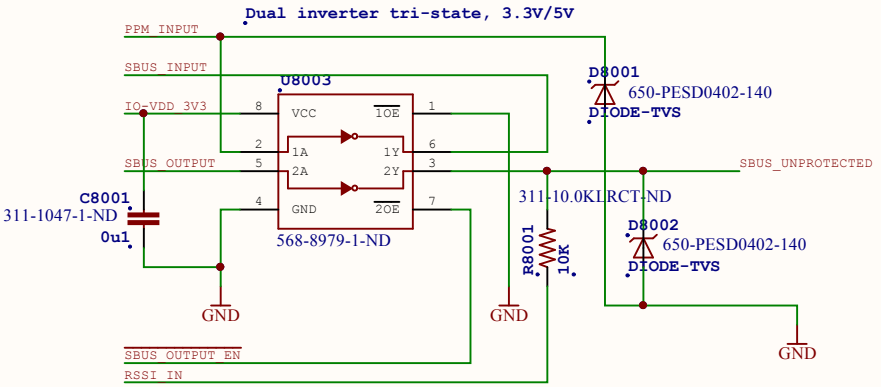
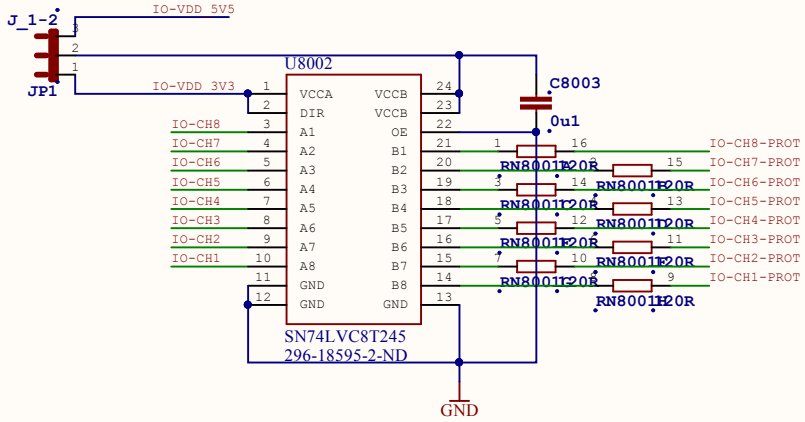
Servo outputs



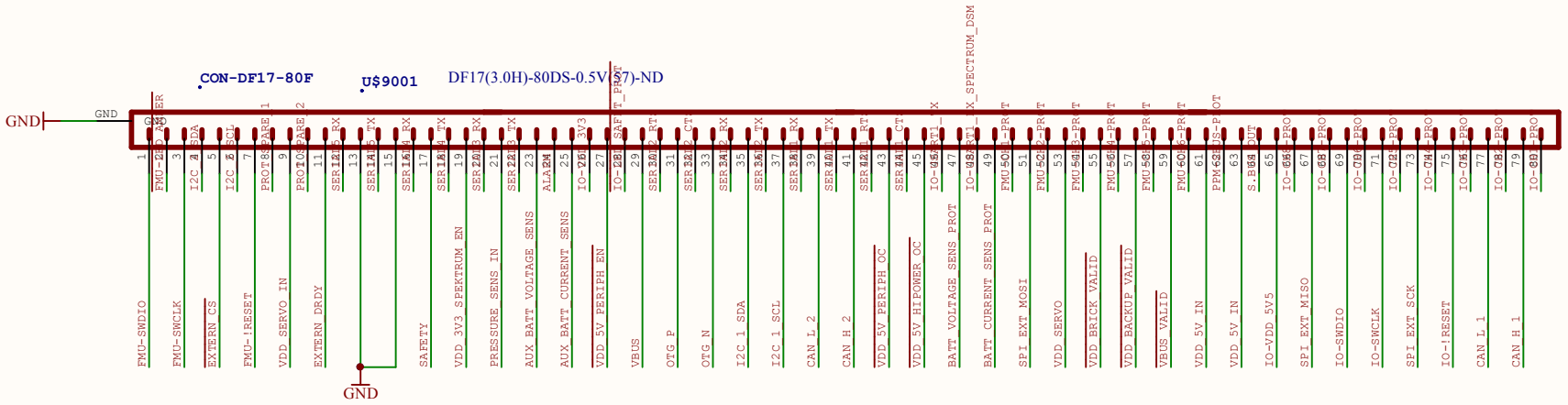
S.Bus in/out

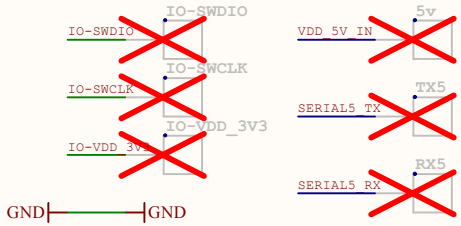


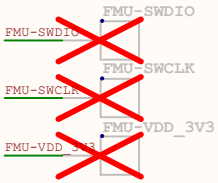


Title: PWM_PPM_FMU3_REV_G.SchDoc	
Date: 7/09/2015	Time: 1:33:47 PM
Sheet:8 of: 10	Drawn By: Philip Rowse
Approved: *	Checked By: *

3DRobotics

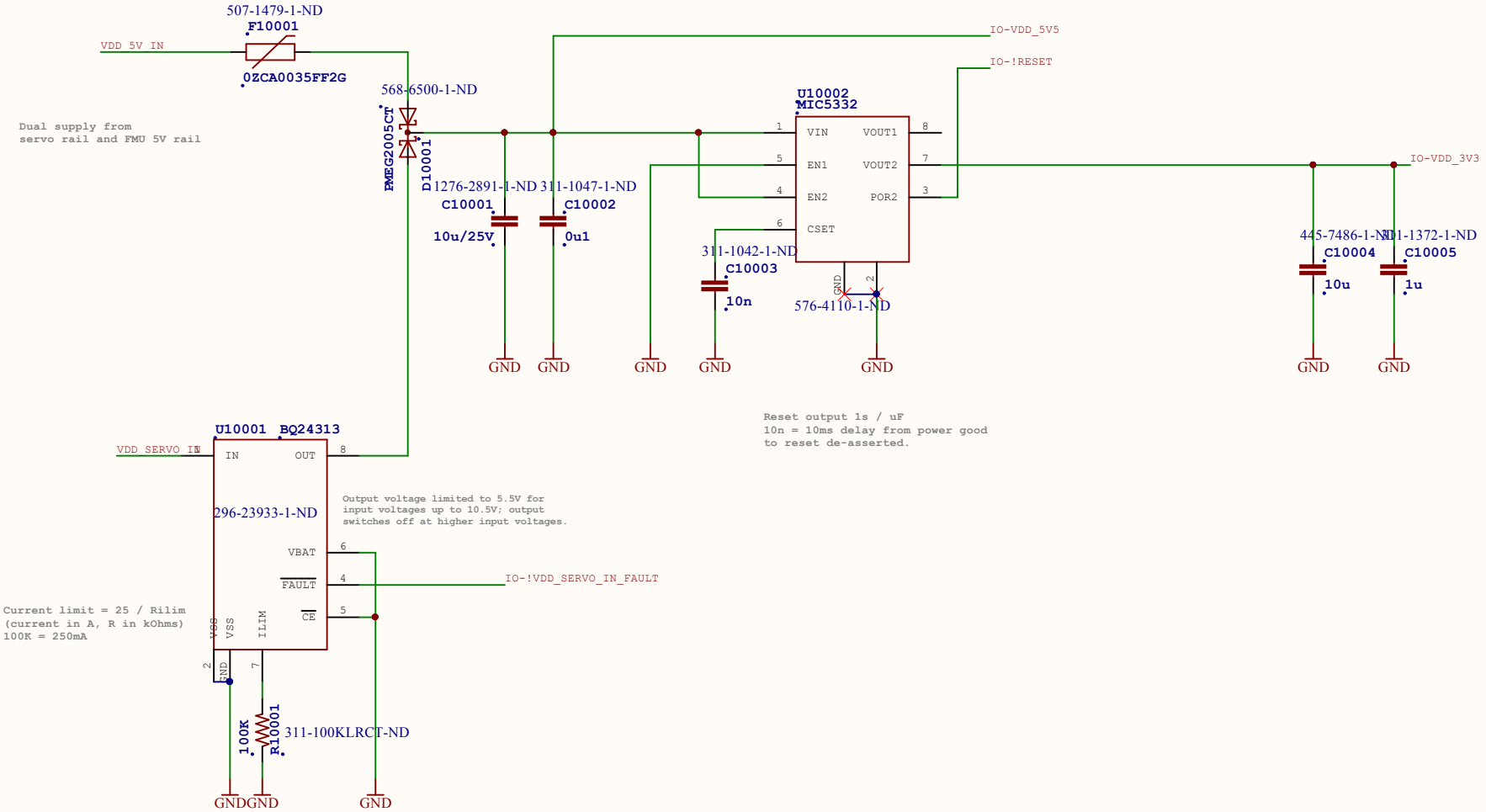






Title: 80PIN_FMU3_REV_G.SchDoc	
Date: 7/09/2015	Time: 1:33:47 PM
Sheet:9 of: 10	Drawn By: Philip Rowse
Approved: *	Checked By: *

3DRobotics



Title: IO_PWR_FMU3_REV_G.SchDoc	
Date: 7/09/2015	Time: 1:33:47 PM
Sheet:10 of: 10	Drawn By: Philip Rowse
Approved: *	Checked By: *

3DRobotics

1. What
   a.new revision of the FMU
2. Why
   a.To increase drive capability of I/O PWM 1-8
3. Who
   a.Production
4. When
   a. URGENT
5. Milestones.
   a.
6. Budget
   a.
7. Testing and programming plan
   a.Testing as per existing FMU
8. Field upgrade plan
   a.Bootloadable, No Change
9. Compliance
   a.No Compliance changes
10. Accountability
    a.Review to be signed off by David. W, and Lorenz

Changes for Rev E

Changed Drive chip on I/O out 1-8 to be SN74LVC8T245
This is to allow the PWM pins to drive up to 10mA each (hard limit is 100 mA for all 8 or aprox 12.5mA each)

Title: CHANGE_FMU3_REV_G.SchDoc	
Date: 7/09/2015	Time: 1:33:47 PM
Sheet:10 of: 10	Drawn By: Philip Rowse
Approved: *	Checked By: *

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