RTL8197D-CG

5-PORT 10/100M ETHERNET ROUTER NETWORK PROCESSOR
PRELIMINARY DATASHEET
(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document provides detailed user guidelines to achieve the best performance when implementing the Realtek 11n AP/Routers.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
0.1	2011/09/09	First draft release.
0.2	2011/09/26	Some errors correction
0.3	2011/11/07	Some errors correction
0.4	2012/01/18	Added interrupt control, Timer, UART, PCIE, USB, IIS and Switch

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1. General Description

The RTL8197D is an integrated System-on-a-Chip (SoC) Application Specific Integrated Circuit (ASIC) that implements a L2 switch. An RLX5281 CPU is embedded and the clock rate can be up to 660MHz. To improve computational performance, a 64-Kbyte I-Cache, 32-Kbyte D-Cache, 16-K I-MEM, and 8-Kbyte D-MEM are provided. A standard 5-signal P1149.1 compliant EJTAG test interface is supported for CPU testing and software development.

The RTL8197D provides five ports (ports 0~4), integrated with five physical layer transceivers for 10Base-T and 100Base-TX. Each port of the RTL8197D may be configured as a LAN or WAN port. Port 5 supports an external MAC interface that could be an GMII/RGMII/MII interface type to work with an external MAC or PHY transceiver.

The RTL8197D supports flexible IEEE 802.3x full-duplex flow control and optional half-duplex backpressure control. For full-duplex, standard IEEE 802.3x flow control will enable pause ability only when both sides of UTP have auto-negotiation ability and have enabled pause ability. The RTL8197D also provides optional forced mode IEEE 802.3x full-duplex flow control. Based on optimized packet memory management, the RTL8197D is capable of Head-Of-Line blocking prevention.

L2 Switch Features: The RTL8197D contains a 1024-entry address look-up table with a 10-bit 4-way XOR hashing algorithm for address searching and learning. Auto-aging of each entry is provided and the aging time is around 200~300 seconds.

The RTL8197D supports port-based, protocol-based, and tagged VLANs. Up to four thousand VLAN groups can be assigned. VLAN tags are inserted or removed based on the VLAN table configuration. The spanning tree protocol is supported and the states are divided into four types: Disabled, Blocking/Listening, Learning, and Forwarding.

For peripheral interfaces, two 16550-compatible UARTs are supported, and a 16-byte FIFO buffer is provided. Both USB 2.0 host and USB OTG controllers are embedded in the RTL8197D to provide EHCI and OHCI 1.1 compliant host and OTG functionality. In addition, two USB PHY have been embedded in the RTL8197D.

An MDI/MDIX auto crossover function is supported. For accessing high-speed devices, the RTL8197D provides two PCI Express host to access a PCI Express interface. Up to two PCI Express devices are supported via this interface on the RTL8197D.

The RTL8197D requires only a single 25MHz crystal or 40MHz clock input for the system PLL. The RTL8197D also has two hardware timers and one watchdog timer to provide accurate timing and watchdog functionality. For extension and flexibility, the RTL8197D has up to 46 GPIO pins.

The RTL8197D is provided in a Thin Profile Plastic Quad Flat Package, 176-Lead (TQFP176) E-pad package. It requires only a 3.3V external power supply. Built-in internal SWR 3.3V to 1.0V can be used on the RTL8197D system core power.

2. Features

- SOC
  - Embedded RISC CPU, RLX5281 with 64K I-Cache, 32K D-Cache, 16K I-MEM, 8K D-MEM
  - Supports MIPS-1 ISA, MIPS16 ISA
  - Clock rate: 500MHz~660MHz
  - Provides a standard 5-signal P1149.1 EJTAG test port
  - Supports RLX5281 CPU suspend mode
- L2 Capabilities
  - Five Ethernet MAC switch with five IEEE 802.3 10/100M physical layer transceivers
  - Supports one GMII/RGMII/MII port to connect to an external MAC or PHY (supports both PHY mode and MAC mode) for HomePlug or HomePNA applications on RTL8197D
  - Non-blocking wire-speed reception and transmission and non-head-of-line-blocking/forwarding
  - Internal 256Kbit SRAM for packet buffering
  - Internal 1024 entry 4-way hash L2 look-up table
  - Supports source and destination MAC address filtering
  - Bi-color LED display mode
- CPU Interface (NIC)
  - Supports BSD mbuf-like packet structure with adjustable cluster size (128-byte to 2Kbyte) to provide optimum memory utilization
  - The NIC DMA support multiple-descriptor-ring architecture for QoS applications (supports 6 RX descriptor rings and 2 TX descriptor rings)
- Peripheral Interfaces
  - Supports PCI Express Host with integrated PHY to connect up to two master devices
  - Two PCI Express PHY embedded
  - Supports two-port USB
    - One is USB 2.0 host
    - Another is USB 2.0 host or device
  - Two USB PHYs are embedded
  - Supports one I2S interface
  - Supports two 16550 UARTs
  - Supports up to 46 GPIO pins
- Memory Interfaces
  - Serial Flash (SPI Type)
    - Supports two banks and dual I/O channels for SPI Flash application
    - Each Flash bank could be configured as 256K/512K/1M/2M/4M/8M/16M Bytes
    - Boot up from SPI flash is supported
  - NAND Flash
    - System supports up to 4 Gbyte Flash memory space
  - SDR DRAM
    - Supports two SDR DRAM banks; each can be configured as 2M/4M/8M/16M/32M/64Mbyte
    - 16bit SDR DRAM data bus supported. System totally supports up to 128Mbyte SDR DRAM memory space
  - DDR1 DRAM
    - Supports one DDR1 DRAM bank that can be configured as 16M/32M/64M/128Mbytes

        - 16-bit DDR1 DRAM data bus supported. System totally supports up to 128Mbyte DDR1 DRAM memory space
    - DDR2 DRAM
        - Supports one DDR2 DRAM bank that can be configured as 32M/64M/128Mbyte
        - 16-bit DDR2 DRAM data bus supported. System totally supports up to 128Mbyte DDR2 DRAM memory space

- Supports Green Ethernet
    - Cable length power saving
    - Link down power saving
- Supports IEEE 802.3az Energy Efficient Ethernet ability for 100Base-TX in full duplex operation and 10Base-T in full/half duplex mode
- Other Add-on-Value Features
    - Supports Link Down Power Saving in Ethernet PHYceivers
    - Supports two hardware timers and one watchdog timer
    - Per-port configurable auto-crossover function
    - Supports Non-Flash Boot Interface (NFBI)
    - Single 25MHz crystal or 40MHz clock input
- Built-in SWR/LDO
    - LDO for DDR1/DDR2
        - DDR1 DRAM to transform 3.3V to 2.5V
        - DDR2 DRAM to transform 3.3V to 1.8V
    - SWR for Core power
        - SWR 3.3V to 1.0V
- TQFP176 E-pad package

3. System Applications

- IEEE 802.11b/g/n AP/Router
- Dualband Concurrent Router
- Network-Attached Storage (NAS)

4. Block Diagram

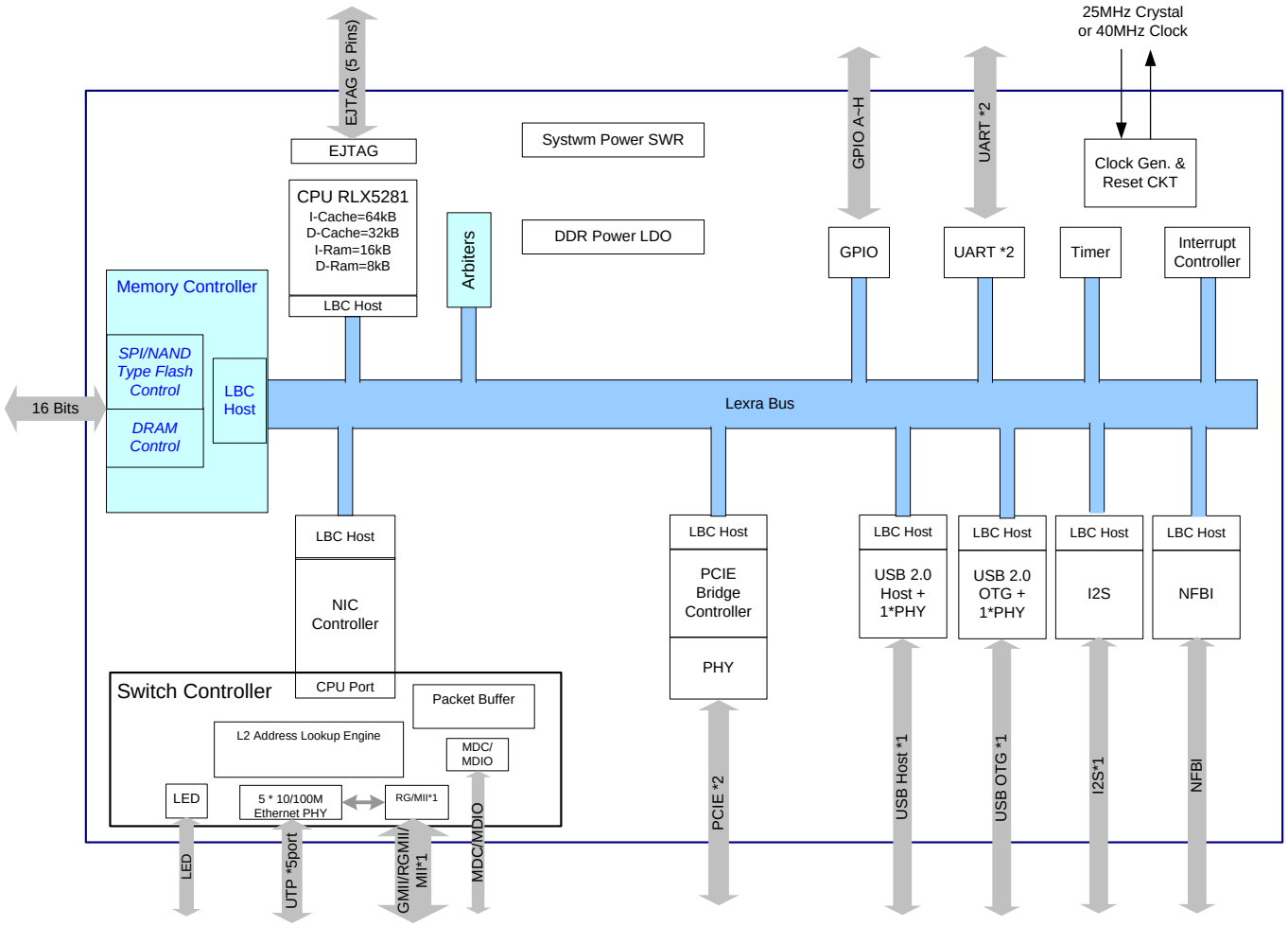


Figure 1. Block Diagram

5. Pin Assignments

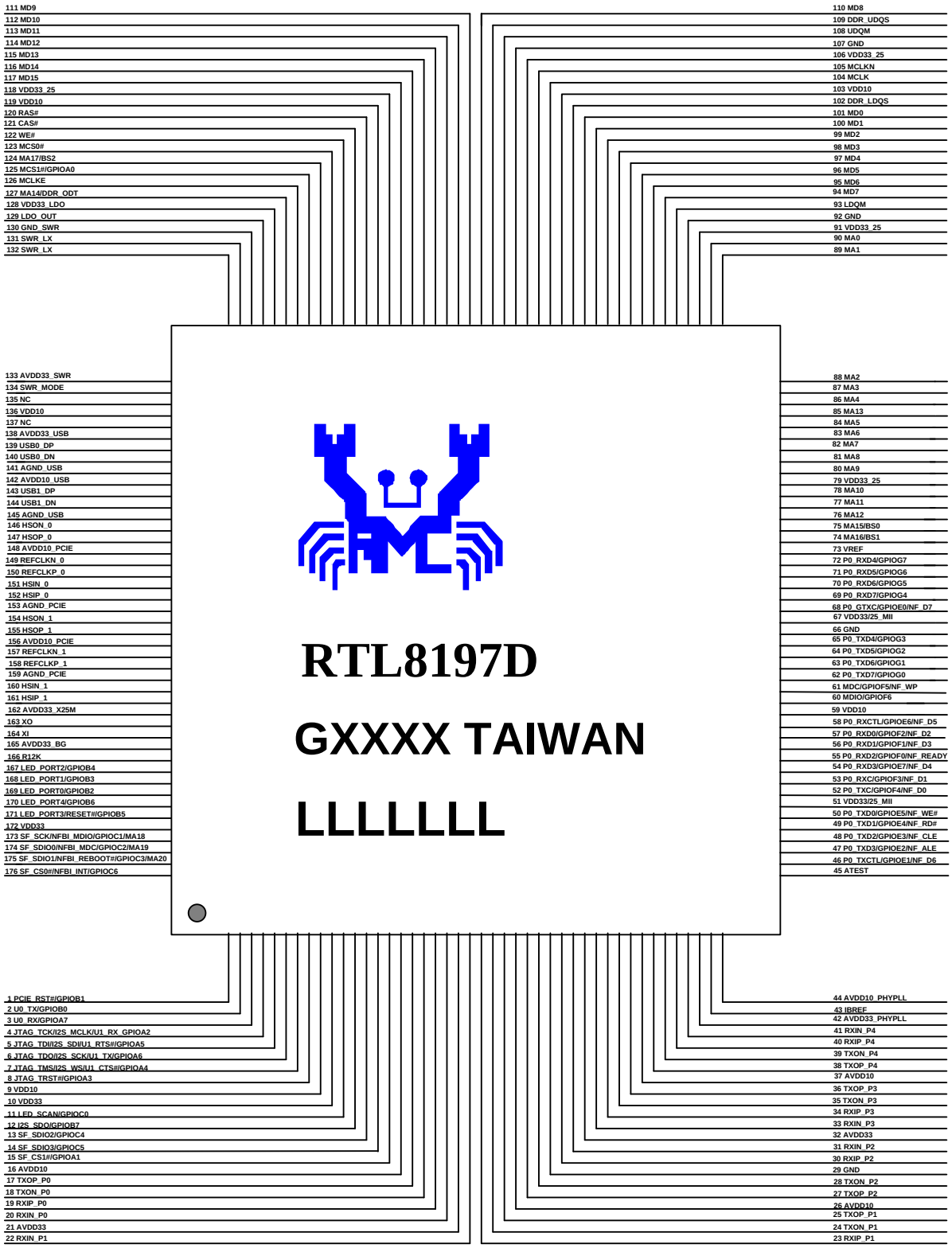


Figure 2. Pin Assignments

5.1. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 2).

6. Pin Descriptions

In this section the following abbreviations are used:

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input

O: Output

I/O: Bi-Directional Input/Output

P: Digital Power

G: Digital Ground

I_{PD}: Input Pin With Pull-Down Resistor

AI: Analog Input

AO: Analog Output

AI/O: Analog Bi-Directional Input/Output

AP: Analog Power

AG: Analog Ground

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

Table 1. Pin Descriptions

Pin Name	Pin No.	Type	Description
Clock & Reset			
XI	164	I	25MHz Crystal Clock or External clock Input Or 40MHz External Clock Input
XO	163	O	25MHz Crystal Clock Output.
RESET#	171	I	External Reset.
10/100M Ethernet Physical Layer			
TXOP_P[4:0] *TXON_P[4:0]*	*38, 36, 27, 25, 17* *39, 35, 28, 24, 18*	*AO*	*10/100M Ethernet Physical Layer Transmit Pair.* *For differential data transmission*
RXIP_P[4:0] *RXIN_P[4:0]*	*40, 34, 30, 23, 19* *41, 33, 31, 22, 20*	*AI*	*10/100M Ethernet Physical Layer Receive Pair.* *For differential data reception*
Ethernet MAC GMII/RGMII/MII Interface			
MDC	61	O	Management Data Clock.
MDIO	60	I_{PU}/O	Management Data I/O.
P0_GTXC	68	O	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 6.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 13.
P0_TXC	52	I	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 6.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 13.

Pin Name	Pin No.	Type	Description
P0_TXCTL	46	O	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 6.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 13.
P0_TXD[7:0]	62, 63, 64, 65, 47, 48, 49, 50	O	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 6.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 13.
P0_RXC	53	I	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 6.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 13.
P0_RXCTL	58	I	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 6.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 13.
P0_RXD[7:0]	69, 70, 71, 72, 54, 55, 56, 57	I	Shared for (1) MII Mode (2) GMII/RGMII Mode (3) MII PHY Mode. For details see section 6.2.1 MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings, page 13.
Memory Interface			
MD[15:0]	117, 116, 115, 114, 113, 112, 111, 110, 94, 95, 96, 97, 98, 99, 100, 101	I/O	Data for DDR DRAM and SDR DRAM.
MA[13:0]	85, 76, 77, 78, 80, 81, 82, 83, 84, 86, 87, 88, 89, 90	O	Address for DDR DRAM and SDR DRAM
SDR DRAM Control			
MCLK	104	O	SDR DRAM Clock.
MCLKE	126	O	SDR DRAM Clock Enable.
MCS0#	123	O	SDR DRAM Chip Select 0.
MCS1#	125	O	SDR DRAM Chip Select 1.
BS[1:0]	74, 75	O	SDR DRAM Chip Bank Select [1:0].
RAS#	120	O	Raw Address Strobe (RAS#) for SDR DRAM.
CAS#	121	O	Column Address Strobe for SDR DRAM.
WE#	122	O	Write Enable for SDR DRAM.
LDQM	93	O	Lower Data Mask Output to SDR DRAM. Corresponds to D[7:0]
UDQM	108	O	Upper Data Mask Output to SDR DRAM. Corresponds to D[15:8]
DDR DRAM Control			
MCLK	104	O	DDR DRAM Differential Clock.
MCLKN	105	O	DDR DRAM Differential Clock.
MCLKE	126	O	DDR DRAM Clock Enable.
MCS0#	123	O	DDR DRAM Chip Select 0.
DDR_BS[2:0]	124, 74, 75	O	DDR DRAM Chip Bank Select [2:0].
RAS#	120	O	Raw Address Strobe (RAS#) for DDR DRAM
CAS#	121	O	Column Address Strobe for DDR DRAM

Pin Name	Pin No.	Type	Description
WE#	122	O	Write Enable for DDR DRAM
LDQM	93	O	Lower Data Mask Output to DDR DRAM. Corresponds to D[7:0]
UDQM	108	O	Upper Data mask output to DDR DRAM. Corresponds to D[15:8]
DDR_LDQS	102	O	Lower Data Strobe to DDR DRAM. Corresponds to D[7:0]
DDR_UDQS	109	O	Upper Data strobe to DDR DRAM. Corresponds to D[15:8]
M_VREF	73	AI	Voltage Reference 1.25V for DDR1. Voltage Reference 0.9V for DDR2.
DDR_ODT	127	O	DDR2 On-Die Termination. ODT (registered HIGH) enables termination resistance internal to the DDR2 DRAM.
Serial SPI Flash Control			
SF_CS0#	176	O	SPI Serial Flash Chip Select 0.
SF_CS1#	15	O	SPI Serial Flash Chip Select 1.
SF_SDIO[1:0]	14, 13, 175, 174	I/O	SPI Serial Flash Serial Data Input/Output.
SF_SCK	173	O	SPI Serial Flash Serial Clock Output. The SF_SDI will be driven on the falling edge. The SF_SDO will be latched on the rising edge.
NAND Flash Control			
NF_D[7:0]	68, 46, 58, 54, 56, 57, 53, 52	I/O	Data for NAND Flash
NF_CLE	48	O	NAND Flash Command Latch Enable
NF_ALE	47	O	NAND Flash Address Latch Enable
NF_CE#	15	O	NAND Flash Chip Enable
NF_RD#	49	O	NAND Flash Read Enable
NF_WE#	50	O	NAND Flash Write Enable
NF_WP#	61	O	NAND Flash Write Portect
NF_READY	55	O	NAND Flash Ready Output
UART			
U0_TX	2	O	Data Transmit Serial Output of UART0.
U0_RX	3	I_{PU}	Data Receive Serial Input of UART0.
U1_TX	6	O	Data Transmit Serial Output of UART1.
U1_RX	4	I_{PU}	Data Receive Serial Input of UART1.
U1_RTS#	5	O	Request to Send of UART1.
U1_CTS#	7	I	Clear to Send of UART1.
JTAG			
JTAG_TCK	4	I_{PU}	JTAG Test Clock.
JTAG_TMS	7	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	6	O	JTAG Test Data Output.
JTAG_TDI	5	I_{PU}	JTAG Test Data In.
JTAG_TRST#	8	I_{PU}	JTAG Test Reset.

Pin Name	Pin No.	Type	Description
LED			
LED_PORT[4:0]	170, 171, 167, 168, 169	O	Scan LED Mode. Link or Link/Speed Status of 5 ports (Low Active).
LEDSCAN	11	O	Scan LED Mode. Scanning control signal for 2-pin bi-color LED in parallel LED mode topology .
I^2S			
I2S_SDO	12	O	Serial Data Output
I2S_SDI	5	I	Serial Data Input
I2S_WS	7	I/O	Word Select
I2S_SCK	6	O	Continuous Serial Clock
I2S_MCLK	4	O	System Clock for Codec
GPIO			
GPIOA[7:0]	3, 6, 5, 7, 8, 4, 15, 125	I/O	GPIO Port A.
GPIOB[7:0]	12, 170, 171,167, 168, 169, 1, 2	I/O	GPIO Port B.
GPIOC[6:0]	176, 14, 13, 175, 174, 173, 11	I/O	GPIO Port C.
GPIOE[7:0]	54, 58, 50, 49, 48, 47, 46, 68	I/O	GPIO Port E.
GPIOF[6:0]	60, 61, 52, 53, 57, 56, 55	I/O	GPIO Port F.
GPIOG[7:0]	72, 71, 70, 69, 65, 64, 63, 62	I/O	GPIO Port G.
USB Host 2.0			
USB0_DP	139	AI/O	USB Host Device Data Plus Pin.
USB0_DN	140	AI/O	USB Host Device Data Minus Pin.
USB OTG			
USB1_DP	143	AI/O	USB OTG Device Data Plus Pin.
USB1_DN	144	AI/O	USB OTG Device Data Minus Pin.
USB_VBUS	137	AI	USB VBUS Voltage
PCI Express Interface			
HSON[1:0] HSOP[1:0]	154, 146 155, 147	AO	Transmitter Differential Pair.
HSIN[1:0] HSIP[1:0]	160, 151 161, 152	AI	Receiver Differential Pair.
REFCLKN[1:0] REFCLKP[1:0]	157, 149 158, 150	AO	Reference Clock Differential Pair.
PCIE_RST#	1	O	PCI Express Reset.

Pin Name	Pin No.	Type	Description
Non-Flash Booting Interface			
NFBI_MDC	174	I	Management Data Clock in NFBI Mode. This pin provides a clock synchronous to MDIO. The clock rate can be from DC to 25MHz.
NFBI_MDIO	173	I/O	Management Data I/O on NFBI Mode. NFBI access data Input/Output and it is synchronous with the rising edge of MDC clock input. The Timing specification and frame format follow IEEE 802.3 SMI (MDC/MDIO) interface specifications.
NFBI_INT	176	O	Interrupt to Host on NFBI Mode. Used by NFBI to interrupt the external host CPU. This pin is Level trigger. Level polarity can be programmed by CMD register.
CHIP_REBOOT#	175	I	Chip Reboot in NFBI Mode. When the external host needs to reboot the RTL8197D CPU, this pin must be asserted to LOW. This pin should be always pulled-up in Non-flash booting mode.
Test			
ATEST	45	O	For Ethernet PHY Internal Test.
Reference Voltage			
IBREF	43	AI	Reference Voltage for Ethernet PHY. 2.5K 1% pull down
R12K	166	AI	Reference Voltage for System. 12K 1% pull down
Power & GND			
VDD33	10, 172	P	Digital I/O Power Supply 3.3V.
VDD33_25	79, 91, 106, 118,	P	Memory I/O Power Supply 3.3V, 2.5V, or 1.8V. SDR DRAM: 3.3V DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
VDD33_25MII	51, 67	P	GMII/RGMII/MII Interface Power Supply 3.3V or 2.5V.
AVDD33	21, 32,	AP	Ethernet Analog Power Supply 3.3V.
AVDD33_PHYPLL	42	AP	Ethernet PHY PLL Power 3.3V.
VDD10	9, 59, 103, 119, 136	P	Digital Core Power Supply 1.0V.
AVDD10	16, 26, 37	AP	Ethernet Analog Power Supply 1.0V.
AVDD33_X25M	162	AP	25M Crystal Power 3.3V.
AVDD33_BG	165	AP	System Band Gap Power Supply 3.3V.
AVDD10_PCIE	148, 156	AP	PCI Express Analog Power Supply 1.0V.
AVDD10_PHYPLL	44	AP	Ethernet PHY PLL Power 1.0V.
AVDD33_USB	138	AP	USB2.0 Analog Power 3.3V.
AVDD10_USB	142	AP	USB2.0 Analog Power 1.0V.
GND	29, 66, 92, 107, E-pad	G	System GND.
GND_SWR	130	AG	Switching Regulator GND.
AGND_PCIE	153, 159	AG	PCI Express GND.
AGND_USB	141, 145	AG	USB GND.

Pin Name	Pin No.	Type	Description
SWR & LDO			
VDD33_LDO	128	AP	LDO Power Supply 3.3V.Input for DDR
LDO_OUT	129	AP	LDO Output Power for DDR DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
AVDD33_SWR	133	AP	SWR Power Supply 3.3V.Input
SWR_LX	131, 132	AP	SWR Power Supply Output
SWR_MODE	134	I	SWR Power Supply Output Voltage Select 0: Output Voltage 1.0V 1: Reserved
Not Connected			
NC	135, 137		Not Connected

6.1. Configuration Upon Power On Strapping

All mode configuration pins are internal pull low. The 1.0V digital core power input pin voltage is up to 0.7V on system power-on. The strap data will be latched after a delay of 300ms.

Table 2. Configuration Upon Power On Strapping

H/W Pin Name	Configuration Name	Pin No	Description
BS1, BS0, U0_TX	ck_cpu_freq_sel[2:0]	74, 75, 2	CPU Clock Configuration. 000: 660MHz 001: Reserved 010: Reserved 011: Reserved 100: 620MHz 101: 580MHz 110: 540MHz 111: 500MHz
MA11, MA10, MA9	ck_freq_sel[2:0]	77, 78, 80	DRAM Clock Rate Configuration. 000: 156.25MHz 001: 193.75MHz 010: 181.25MHz 011: Reserved 100: Reserved 101: 125MHz 110: Reserved 111: 168.75MHz
MA2, MA1, MA0	Bootpinsel[2:0]	88, 89, 90	Boot Pin Selection for RTL8197D Boot Method. 000: SPI 001: Reserved 010: NFBI 011: NAND 100 to 111 : Reserved
MA7	PHYID	82	PHY ID for NFBI 0: PHY ID= 0100 1: PHY ID=1000
MA6, MA5	EnOLTautoTestMode[1:0]	83, 84	Enable OLT Auto Test Mode. 0x: Normal Mode 10: Internal MP Test Mode 11: Internal Debug Mode
MA3	DDR_TYPE	87	DDR DRAM Type. 0: DDR2 1: DDR1
MA4	External_Reset	86	Enable External Reset Pin 0: Disable 1: Enable
MA8	DRAM_TYPE	81	DRAM Type. 0: SDR 1: DDR
MA12	Sel_40M	76	System Clock Source Select. 0: 25MHz 1: 40MHz
MCKE	Strap_Testmode	126	Chip Test Mode Select 0: Normal mode 1: Test mode

H/W Pin Name	Configuration Name	Pin No	Description
P0_TXD2, P0_TXD3	NAFC_AC[1:0]	48, 47	NAND Flash Address Cycle 00: 3 address cycle 01: 4 address cycle 10: 5 address cycle 11: reserved
P0_TXD1	NAFC_RC	49	NAND flash page read command 0: 1 cycle command{00h} (512Byte per page) 1: 2 cycle command{00h, 30h} (2048Byte per page)

6.2. GMAC Pin Mode Description

6.2.1. MAC Interface MII/GMII/RGMII Mode Pin Sharing Mappings

The RTL8197D GMAC port supports four MAC interface modes: (1) MII mode (2) RGMII mode (3) MII PHY mode (4) GMII mode. These four modes I/O pin definition mappings are shown in Table 3.

Table 3. MAC Interface MII/RGMII Mode Pin Sharing Mappings

Pin	MII MAC Mode	RGMII Mode	MII PHY Mode	GMII Mode
GTXC (Output)	-	-	-	GTXC (Output)
TXC (Input)	TXC (Input)	GTXC (Output)	PhyRXC (Output)	-
TXCTL (Output)	TXEN (Output)	TXCTL (Output)	PhyRXDV (Output)	TXCTL (Output)
TXD[7:4] (Output)	-	-	-	TXD[7:4] (Output)
TXD[3:0] (Output)	TXD[3:0] (Output)	TXD[3:0] (Output)	PhyRXD[3:0] (Output)	TXD[3:0] (Output)
RXC (Input)	RXC (Input)	RXC (Input)	PhyTXC (Output)	RXC (Input)
RXCTL (Input)	RXDV (Input)	RXCTL (Input)	PhyTXEN (Input)	RXCTL (Input)
RXD[7:4] (Input)	-	-	-	RXD[7:4] (Input)
RXD[3:0] (Input)	RXD[3:0] (Input)	RXD[3:0] (Input)	PhyTXD[3:0] (Input)	RXD[3:0] (Input)

6.2.2. GMII/RGMII Interface Pin Descriptions

Table 4. GMII/RGMII Interface Pin Descriptions

Pin Name	Type	Description
GTXC	O	GMII/RGMII Transmit Clock. 125MHz, 25MHz, or 2.5MHz transmit clock with ±50ppm tolerance for 100Mbps and 10Mbps respectively.
TXCTL	O	GMII/RGMII Transmit Control Signal. The GTXCTL indicates TXEN at rising of GTXC. TXER XOR TXEN is encoded on the falling edge of GTXC. @ GTXC rising edge: GTXCTL=TXEN. @ GTXC falling edge: GTXCTL=TXEN XOR TXER.

Pin Name	Type	Description
TXD[7:0]	O	GMII/RGMII Transmit Data. Transmits data synchronously to double edge of GTXC, with lower 4 bits (bit[3:0]) present on the rising edge of GTXC and the upper 4 bits (bit[7:4]) present on the falling edge of the GTXC. In GMII/RGMII 10/100Base-T mode, the transmit data nibble is present on GTXD[3:0] on the rising edge of GTXC.
RXC	I	GMII/RGMII Receive Clock. 125MHz, 25MHz, or 2.5MHz transmit clock with ±50ppm tolerance for 100Mbps and 10Mbps respectively.
RXCTL	I	GMII/RGMII Receive Control Signal. The RXCTL indicates RXDV at rising of RXC, and RXER XOR RXDV is encoded on the falling edge of GRXC. @ RXC rising edge: RXCTL=RXEN. @ RXC falling edge: RXCTL=RXDV XOR RXER.
RXD[3:0]	I	GMII/RGMII Receive Data. Transmits data synchronously to double edge of RXC, with lower 4 bits (bit[3:0]) present on the rising edge of RXC and the upper 4 bits (bit[7:4]) present on the falling edge of the RXC. In GMII/RGMII 10/100Base-T mode, the transmit data nibble is present on RXD[3:0] on the rising edge of RXC.
VDD_RGMII	P	GMII/RGMII Interface Power Supply. VDD33/25_RGMII can be supplied with 2.5V COMS or 1.5V HSTL

6.2.3. MII MAC Mode Interface Pin Descriptions

Table 5. MII MAC Mode Interface Pin Descriptions

Pin Name	Type	Description
TXD[3:0]	O	Transmit Data Output (TXD[3:0]). Transmits data synchronously to the rising edge of GTXC.
TXEN	O	Transmit Data Enable. Transmit enable that is sent synchronously at the rising edge of GTXC.
TXC	I	Transmit Clock (25MHz/2.5MHz). 25MHz/2.5MHz clock driven by PHY when MII is operating at 100Mbps/10Mbps. TXD[3:0], TXEN are synchronized by TXC rising edge in this mode.
RXC	I	25MHz/2.5MHz. Receive Clock. RXD[3:0], RXDV, CRS, and COL are synchronized by TXC rising edge in this mode.
RXDV	I	Receive Data Valid Input.
RXD[3:0]	I	Receive Data Input (RXD[3:0]).

6.2.4. MII PHY Mode Interface Pin Descriptions

Table 6. MII PHY Mode Interface Pin Descriptions

Pin Name	Type	Description
phyRXD[3:0]	O	MII PHY Mode Receive Data (phyRXD[3:0]).
phyRXDV	O	MII PHY Mode Receive Data Valid.
phyRXC	O	MII PHY Mode Receive Clock (25MHz/2.5MHz). PhyRXD[3:0], phyRXDV, are synchronized by phyGRXC falling edge in this mode.
phyTXC	O	MII PHY Mode Transmit Clock (25MHz/2.5MHz). phyTXD[3:0], phyTXEN are synchronized by phyTXC falling edge in this mode.
phyTXEN	I	MII PHY Mode Transmit Data Enable.
phyTXD[3:0]	I	MII PHY Mode Transmit Data (phyTXD[3:0]).

6.3. Shared I/O Pin Mapping

Table 7. Shared I/O Pin Mapping

Pin	GPIO	GMII/I2S	Memory	EJTAG	NFBI	LED	UART	Reset
126	GPIOA[0]	-	MCS1#	-	-	-	-	-
15	GPIOA[1]	-	SF_CS1#/ NF_CE#	-	-	-	-	-
4	GPIOA[2]	I2S_MCLK	-	JTAG_TCK	-	-	U1_RX	-
8	GPIOA[3]	-	-	JTAG_TRST#	-	-	-	-
7	GPIOA[4]	I2S_W I2S	-	JTAG_TMS	-	-	U1_CTS	-
5	GPIOA[5]	I2S_SDI	-	JTAG_TDI	-	-	U1_RTS#	-
6	GPIOA[6]	I2S_SCK	-	JTAG_TDO	-	-	U1_TX	-
3	GPIOA[7]	-	-	-	-	-	U0_RX	-
2	GPIOB[0]	-	-	-	-		U0_TX	-
1	GPIOB[1]	-	-	-	-		-	PCIE_RST#
169	GPIOB[2]	I2S_SDO	-	-	-	LED_PORT0	-	-
168	GPIOB[3]	-	-	-	-	LED_PORT1	-	-
167	GPIOB[4]	-	-	-	-	LED_PORT2	-	-
171	GPIOB[5]	-	-	-	-	LED_PORT3	-	-
170	GPIOB[6]	-	-	-	-	LED_PORT4	-	RESET#
12	GPIOB[7]	I2S_SDO	-	-	-	-	-	-
11	GPIOC[0]	-	-	-	-	LED_SCAN	-	-
173	GPIOC[1]	-	SF_SCK	-	NFBI_MDIO	-	-	-
174	GPIOC[2]	-	SF_SDIO0	-	NFBI_MDC	-	-	-
175	GPIOC[3]	-	SF_SDIO1	-	NFBI_ROOT#	-	-	-
13	GPIOC[4]	-	SF_SDIO2	-	-	-	-	-
14	GPIOC[5]	-	SF_SDIO3	-	-	-	-	-
176	GPIOC[6]	-	SF_CS0#	-	NFBI_INT	-	-	-
68	GPIOE[0]	P0_GTXC	NF_D7	-	-	-	-	-
46	GPIOE[1]	P0_TXCTL	NF_D6	-	-	-	-	-

Pin	GPIO	GMII/I2S	Memory	EJTAG	NFBI	LED	UART	Reset
47	GPIOE[2]	P0_TXD3	NF_ALE	-	-	-	-	-
48	GPIOE[3]	P0_TXD2	NF_CLE	-	-	-	-	-
49	GPIOE[4]	P0_TXD1	NF_RD#	-	-	-	-	-
50	GPIOE[5]	P0_TXD0	NF_WE#	-	-	-	-	-
58	GPIOE[6]	P0_RXCTL	NF_D5	-	-	-	-	-
54	GPIOE[7]	P0_RXD3	NF_D4	-	-	-	-	-
55	GPIOF[0]	P0_RXD2	NF_READY	-	-	-	-	-
56	GPIOF[1]	P0_RXD1	NF_D3	-	-	-	-	-
57	GPIOF[2]	P0_RXD0	NF_D2	-	-	-	-	-
53	GPIOF[3]	P0_RXC	NF_D1	-	-	-	-	-
52	GPIOF[4]	P0_TXC	NF_D0	-	-	-	-	-
61	GPIOF[5]	MDC	NF_WP#	-	-	-	-	-
60	GPIOF[6]	MDIO	-	-	-	-	-	-
62	GPIOG[0]	P0_TXD7	-	-	-	-	-	-
63	GPIOG[1]	P0_TXD6	-	-	-	-	-	-
64	GPIOG[2]	P0_TXD5		-	-	-	-	-
65	GPIOG[3]	P0_TXD4	-	-	-	-	-	-
69	GPIOG[4]	P0_RXD7	-	-	-	-	-	-
70	GPIOG[5]	P0_RXD6	-	-	-	-	-	-
71	GPIOG[6]	P0_RXD5	-	-	-	-	-	-
72	GPIOG[7]	P0_RXD4	-	-	-	-		-

7. Memory Controller

The RTL8197D integrates a memory control module to access external DDR DRAM , SDR DRAM, and Flash memory.

The interface is designed for DDR-compliant DDR DRAM, and designed for PC133 or PC166-compliant SDR DRAM, and supports auto-refresh mode, which requires a 4096 refresh cycle within 64ms. The SDR DRAM interface supports two chips (MCS0#, and MCS1#). The DDR DRAM interface supports one chip (MCS0#), and the DRAM size and timing is configurable in registers.

The RTL8197D also supports two flash memory chips (SF_CS0# and SF_CS1#). The interface supports SPI flash memory. When Flash is used, the system will boot from KSEG1 at virtual address 0xBFC0_0000 (physical address: 0x1FC0_0000). Chip1 flash memory will be mapped to the address '0x1FC0_0000 + flash size'. The flash size is configurable from 1M to 32M bytes for each chip. If flash size is set to 4M, 8M, 16M, or 32M byte, 0xBFC0_0000 still maps the first 4M bytes of flash, and there will be a new memory mapping from 0xBD00_0000 (0xBD00_0000 maps to chip 0 byte 0).

7.1. SDR DRAM Control Interface

PC100~PC166-compliant SDR DRAM is supported. The SDR DRAM controller supports Auto Refresh mode, which requires a 4096-cycle refresh each 64ms. The RTL8197D provides a maximum of 512Mbit address space (8Mx16x4Banks) and the SDR DRAM size is configurable.

7.1.1. Features

- Interface (Bus Width): 16-bit
- Targeted SDR Frequency: Up to 168MHz
- Two Chip Selects (CS0# and CS1#)
- Supported SDR DRAM Chip Specification:
  - Bank Counts: 2, 4
  - Row Counts: 2K (A0~A10), 4K (A0~A11), 8K (A0~A12)
  - Column Counts: 256 (A0~A7), 512 (A0~A8), 1K (A0~A9), 2K (A0~A9, A11)
- Programmable Timing Parameters: tRAS, tRP, tRCD, tCL, tREFI…

7.1.2. Bank2 and Bank3

Bank2 (CS0#) and Bank3 (CS1#) are designed for SDR DRAM connections. Bank2 is mapped to either kseg0 or kseg1, with a start address of 0x0000.0000 (virtual address 0x8000.0000 or 0xa000.0000). Bank3 is mapped to 0x0000.0000 + SDR DRAM size. The Bank2 and Bank3 sizes should be exactly the same. If only one SDR DRAM is on-board, the RTL8197D provides 16-bit access mode to handle this.

7.2. DDR DRAM Controller

7.2.1. Features

- Interface (Bus Width): 16-bit
- Targeted DDR Frequency: Up to 193.75MHz
- Supports one Chip Select (MCS0#)
- Supports both DDR1 and DDR2
- Supported DDR DRAM Chip Specification
  - Bank Counts: 8
  - Row Counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column Counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9, A11), 4K (A0~A9, A11, A12)
- Programmable Timing Parameters: tRAS, tRP, tRCD, tCL, tREFI…

7.3. SPI Flash Controller

The SPI flash controller is a new design and incorporates new features.

7.3.1. Features

- Targeted SPI flash frequency: Up to 96.875MHz (when DRAM clock is 193.75MHz)
- Supports two chips
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

7.3.2. Pin Mode and Definition of Serial and Dual I/O

Modes supported on the SPI flash interface:

Serial I/O Mode

- SDI: Flash chip data input pin
- SDO: Flash chip data output pin

Dual I/O Mode

- SDIO0 (SDI): Flash chip data bi-directional pin
- SDIO1 (SDO): Flash chip data bi-directional pin

7.4. Software Register Definitions

7.4.1. Memory Control Register (MCR) (0xB800_1000)

This register does not provide byte access.

Table 8. Memory Control Register (MCR) (0xB800_1000)

Bit	Name	Description	Mode	Default
31	DRAMTYPE	Report the Hardware Strapping Initial Value for DRAM Type. 0: SDR DRAM 1: DDR DRAM	R	0B
30	BOOTSEL	Report the Hardware Strapping Initial Value for Boot Flash Type. 0: Reserved 1:Serial SPI flash	R	0B
29	IPREF	Enable Instruction Prefetch Function. 0: Disable prefetch (also reset buffer status) 1: Enable prefetch (4 words)	RW	0B
28	DPREF	Enable Data Prefetch Function. 0: Disable prefetch (also reset buffer status) 1: Enable prefetch (4 words)	RW	0B
27	IPREF_MODE	Choose Instruction Prefetch Mode. 0: Old prefetch mechanism 1: New prefetch mechanism	RW	0B
26	DPREF_MODE	Choose Data Prefetch Mode. 0: Old prefetch mechanism 1: New prefetch mechanism	RW	0B
25:0	-	Reserved.	-	-

7.4.2. DRAM Configuration Register (DCR) (0xB800_1004)

This register does not provide byte access.

Table 9. DRAM Configuration Register (DCR) (0xB800_1004)

Bit	Name	Description	Mode	Default
31:30	T_CAS	CAS Latency. 00: Latency=2 01: Latency=3 10: Latency=2.5 (only used for DDR) 11: Latency=4 (only used for DDR)	RW	01B
29:28	DBUSWID	DRAM Bus Width. 00: Reserved 01: 16 bit (used for DDR, SDR) 10: Reserved 11: Reserved	RW	01B
27	DCHIPSEL	DRAM Chip Select. 0: CS0# 1: CS0# and CS1#	RW	1B
26:25	ROWCNT	Row Counts. 00: 2K (A0~A10) 01: 4K (A0~A11) 10: 8K (A0~A12) 11: 16K (A0~A13)	RW	00B
24:22	COLCNT	Column Counts. 000: 256 (A0~A7) 001: 512 (A0~A8) 010: 1K (A0~A9) 011: 2K (A0~A9, A11) 100: 4K (A0~A9, A11, A12) 101: Reserved 110: Reserved 111: Reserved	RW	000B
21	BSTREF	Bursted 8 Auto-Refresh Commands (Used for DDR). 0: Disable 1: Enable	RW	0B
20	ARBIT	Enforce Interface Arbitration Take Effect. 0: Reserved 1: Take effect	RW	0B
19	BANKCNT	Bank Counts. 0: 2 banks (used for SDR) 1: 4 banks (used for SDR, DDR)	RW	1B
18	FAST_RX	If RX path turnaround delay is small enough, the memory controller can return read data with reduced latency within 1DRAM clock cycle (used for DDR). 0: Normal path 1: Fast path	RW	0B
17	MR_MODE	Select the Memory Command that Memory Controller Issues (Used for DDR). 0: Mode Register 1: Extended Mode Register	RW	0B
16	DRV_STR	Drive Strength Setting of DRAM Chip (Used for DDR). For this option to be effective, MR_MODE must be first set to 1. 0: Normal 1: Reduced	RW	0B
15:0	-	Reserved.	-	-

7.4.3. DRAM Timing Register (DTR) (0xB800_1008)

This register does not provide byte access.

Table 10. DRAM Timing Register (DTR) (0xB800_1008)

Bit	Name	Description	Mode	Default
31:29	T_RP	tRP Timing Parameter of DRAM Basic unit = 1*DRAM_CLK 000: 1 unit	RW	111B
28:26	T_RCD	tRCD Timing Parameter of DRAM Basic unit = 1*DRAM_CLK 000: 1 unit	RW	111B
25:21	T_RAS	Minimum T_RAS Timing Parameter of DRAM Basic unit = 1*DRAM_CLK 00000: 1 unit	RW	11111B
20:14	T_RFC	tRFC Timing Parameter of DRAM. Refresh row cycle time Basic unit = 1*DRAM_CLK 0000000: 1 unit	RW	1111100B
13:10	T_REFI	tREF Timing Parameter of DRAM. Refresh row interval time Basic unit = T_REFI_UNIT 0000: 1 unit 0001: 2 units … 1111: 16 units	RW	0000B
9:7	T_REFI_UNIT	Basic Unit of T_REFI 000: 32 DRAM_CLK 001: 64 DRAM_CLK 010: 128 DRAM_CLK 011: 256 DRAM_CLK 100: 512 DRAM_CLK 101: 1024 DRAM_CLK 110: 2048 DRAM_CLK 111: 4096 DRAM_CLK	RW	111B
6:4	T_WR	tWR Timing Parameter of DRAM. Write recovery time Basic unit = 1*DRAM_CLK 000: 1 unit	RW	111B
3:0	-	Reserved.	-	-

7.4.4. DDR DRAM Calibration Register (DDCR) (0xB800_1050)

This register does not provide byte access.

Table 11. DDR DRAM Calibration Register (DDCR) (0xB800_1050)

Bit	Name	Description	Mode	Default
31	CAL_MODE	Run-Time Calibration Mode. 0: Use analog DLL calibration 1: Use digital delay line calibration	RW	0B
30	SW_CAL_RDY	Ready for Digital Delay Line Calibration. 0: Not ready 1: Ready	R	0B
29:25	DQS0_TAP[4:0]	Selects 32-Tap Delay Line for LDQS, which is Data Strobe for DQ[7:0] Reception. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap *Note: 32-tap delay is around 2.5 ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
24:20	DQS1_TAP[4:0]	Selection of 32-Tap Delay Line for UDQS, which is Data strobe for DQ[15:8] Reception. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap *Note: 32-tap delay is around 2.5 ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
19:15	DQS0_EN_TAP[4:0]	Selection of 32-Tap Delay Line for the Internal LDQS_EN Window. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap *Note: 32-tap delay is around 2.5 ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
14:10	DQS1_EN_TAP[4:0]	Selection of 32-Tap Delay Line for the Internal UDQS_EN Window. 00000: 1st tap 00001: 2nd tap … 11111: 32nd tap *Note: 32-tap delay is around 2.5 ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
9:0	-	Reserved.	-	-

7.4.5. SPI Flash Configuration Register (SFCR) (0xB800_1200)

This register does not provide byte access.

Table 12. SPI Flash Configuration Register (SFCR) (0xB800_1200)

Bit	Name	Description	Mode	Default
31:29	SPI_CLK_DIV	SPI Operating Clock Rate Selection. The value defines the divisor to generate SPI clock SPI Clock = (DRAM Clock)/(SPI_CLK_DIV). 000: DIV=2 001: DIV=4 010: DIV=6 011: DIV=8 100: DIV=10 101: DIV=12 110: DIV=14 111: DIV=16	RW	111B
28	RBO	Serial Flash Read Byte Ordering. 0: The byte order is from low to high 1: The byte order is from high to low	RW	1B
27	WBO	Serial Flash Write Byte Ordering. 0: The byte order is from low to high 1: The byte order is from high to low	RW	1B
26:23	SPI_TCS	SPI Chip Deselect Time. Basic unit=1*DRAM clock cycle. 0000: 1 unit 0001: 2 units, etc.	RW	1111B
22:0	-	Reserved.	-	-

7.4.6. SPI Flash Configuration Register 2 (SFCR2) (0xB800_1204)

This register does not provide byte access.

Table 13. SPI Flash Configuration Register 2 (SPCR2) (0xB800_1204)

Bit	Name	Description	Mode	Default
31:24	SFCMD	SPI Flash 8-Bit Command Code of a Read Transaction. Example: 'Read Data' is 0x03. 'Fast Read' is 0x0B.	RW	03H
23:21	SFSIZE	SPI Flash Size. 000: 128Kbyte 001: 256Kbyte 010: 512Kbyte 011: 1Mbyte 100: 2Mbyte 101: 4Mbyte 110: 8Mbyte 111: 16Mbyte	RW	111B
20	RD_OPT	SPI Flash Sequential Access Optimization. 0: No optimization 1: Optimization for sequential access	RW	0B
19:18	CMD_IO	SPI Flash I/O Mode Selection for the Command Phase of a Read Transaction. 00: Serial I/O (8 cycles) 01: Dual I/O (4 cycles) 10: Reserved 11: Reserved	RW	00B

Bit	Name	Description	Mode	Default
17:16	ADDR_IO	SPI Flash I/O Mode Selection for the Address Phase of a Read Transaction. 00: Serial I/O (24 cycles) 01: Dual I/O (12 cycles) 10: Reversed 11: Reserved	RW	00B
15:13	DUMMY_CYCLES	SPI Flash Inserted Dummy Cycles for the Dummy Cycle Phase of a Read Transaction. 000: 0 Cycle 001: 2 Cycles 010: 4 Cycles 011: 6 Cycles 100: 8 Cycles 101: 10 Cycles 110: 12 Cycles 111: 14 Cycles	RW	000B
12:11	DATA_IO	SPI Flash I/O Mode Selection for the Data Phase of a Read Transaction (Assume 8*N Cycles). 00: Serial I/O (8*N cycles) 01: Dual I/O (4*N cycles) 10: Reserved 11: Reserved	RW	00B
10	HOLD_TILL_SFDR2	If this bit is '1', it indicates the write operation to this register (SFCR2) will not take effect immediately but will be delayed until another write operation to SFDR2.	RW	0B
9:0	Reserved	Reserved.	-	-

7.4.7. SPI Flash Control & Status Register (SFCSR) (0xB800_1208)

This register does not provide byte access.

Table 14. SPI Flash Control & Status Register (SFCSR) (0xB800_1208)

Bit	Name	Description	Mode	Default
31	SPI_CSB0	SPI Flash Chip Select 0. 0: Active 1: Not active	RW	1B
30	SPI_CSB1	SPI Flash Chip Select 1. 0: Active 1: Not active	RW	1B
29:28	LEN	SPI Read/Write Data Length (Unit=Byte). 00: 1 Byte 01: 2 Bytes 10: 3 Bytes 11: 4 Bytes	RW	11B
27	SPI_RDY	SPI Flash Operation Busy Indication Flag. 0: Busy (operation in progress) 1: Ready (idle or SPI access command is ready)	R	1B
26:25	IO_WIDTH	SPI Flash I/O Mode Selection of a Transaction. 00: Serial I/O 01: Dual I/O 10: Reserved 11: Reserved	RW	00B
24	CHIP_SEL	Chip Selection. 0: CS0# 1: CS1#	RW	0B
23:16	CMD_BYTE	SPI Flash 8-Bit Command Code of a Transaction (This field is only used in MMIO mode). Example: 'Read Data' is 0x03. 'Read ID' is 0x9F.	RW	0B
15:0	-	Reserved.	-	-

7.4.8. SPI Flash Data Register (SFDR) (0xB800_120C)

This register does not provide byte access.

This configuration register is used for the PIO (Programmed I/O) access mode.

Table 15. SPI Flash Data Register (SFDR) (0xB800_120C)

Bit	Name	Description	Mode	Default
31:24	Data3	Read/Write Data Byte 3.	RW	0B
23:16	Data2	Read/Write Data Byte 2.	RW	0B
15:8	Data1	Read/Write Data Byte 1.	RW	0B
7:0	Data0	Read/Write Data Byte 0.	RW	0B

7.4.9. SPI Flash Data Register 2 (SFDR2) (0xB800_1210)

This register does not provide byte access.

This configuration register is intended to be used under MMIO access mode.

Table 16. SPI Flash Data Register 2 (SFDR2) (0xB800_1210)

Bit	Name	Description	Mode	Default
31:24	Data3	Read/Write Data Byte 3.	RW	0B
23:16	Data2	Read/Write Data Byte 2.	RW	0B
15:8	Data1	Read/Write Data Byte 1.	RW	0B
7:0	Data0	Read/Write Data Byte 0.	RW	0B

8. Peripheral and MISC Control

8.1. Interrupt Control

The RTL8197D provides 14 hardware-interrupt inputs, IRQ2 to IRQ15. The Global Interrupt Mask Register (GIMR) enables/disables an interrupt coming from the Timer, USB, UART, PCIE, Switch Core, GPIO, or Timer modules. The Global Interrupt Status Register (GISR) shows the pending interrupt status. The Interrupt Routing Register (IRR) controls the mapping from the interrupt source to IRQ 2~15.

Table 17. Interrupt Control Register Address Mapping (Base = 0xB800_3000)

Offset	Size (byte)	Name	Description
00	4	GIMR	Global interrupt mask register.
04	4	GISR	Global interrupt status register.
08	4	IRR0	Interrupt routing register 0
0C	4	IRR1	Interrupt routing register 1
10	4	IRR2	Interrupt routing register 2
14	4	IRR3	Interrupt routing register 3

8.1.1. Global interrupt mask register (GIMR) (0x B800_3000)

Table 18. Global Interrupt Mask Register (GIMR) (0x B800_3000)

Bit	Bit Name	Description	R/W	Default
31	GISR2_IE	GISR2 interrupt enable	R/W	0
30	Reserved	Reserved	R/W	0
29	Reserved	Reserved	R/W	0
28	USB0_WAKE_IE	USB0 wake up interrupt enable	R/W	0
27	CPU_WAKE_IE	CPU wake up interrupt enable	R/W	0
26	I2S_IE	I2S interrupt enable	R/W	0
25	USB1_WAKE_IE	USB1 wake up interrupt enable	R/W	0
24	Reserved	Reserved	R/W	0
23	MIC_IE	GDMA for MIC	R/W	0
22	PCIE1_IE	PCIE port 1 host interface interrupt enable Or PCIE endpoint interface interrupt enable	R/W	0
21	PCIE0_IE	PCIE port 0 host interface interrupt enable	R/W	0
20	SECURITY_IE	Security Engine interrupt enable	R/W	0
19	PCM_IE	PCM interface interrupt enable	R/W	0
18	NFBI_IE	NFBI interrupt enable	R/W	0
17	GPIO_EFGH_IE	GPIO Port E,F,G,H interrupt enable	R/W	0
16	GPIO_ABCD_IE	GPIO Port A,B,C,D interrupt enable.	R/W	0
15	SW_IE	Switch Core interrupt enable.	R/W	0
14	VOIP_IE	VoIP accelerator interrupt enable	R/W	0
13	UART1_IE	UART 1 interrupt enable.	R/W	0
12	UART0_IE	UART 0 interrupt enable.	R/W	0
11	USB_O_IE	USB 2.0 OTG interrupt enable.	R/W	0

Bit	Bit Name	Description	R/W	Default
10	USB_H_IE	USB 2.0 Host interrupt enable.	R/W	0
9	TC1_IE	Timers/Counters #1 interrupt enable.	R/W	0
8	TC0_IE	Timers/Counters #0 interrupt enable.	R/W	0
7	Reserved	Reserved	R/W	0
6	Reserved	Reserved	R/W	0
5	Reserved	Reserved	R/W	0
4	Reserved	Reserved	R/W	0
3	Reserved	Reserved	R/W	0
2	Reserved	Reserved	R/W	0
1	OTG_CTRL_IE	OTG detect ctrl Interrupt enable	R/W	0
0	NAND_CTRL_IE	NAND flash ctrl Interrupt enable	R/W	0

8.1.2. Global Interrupt Status Register (GISR) (0x B800_3004)

Table 19. Global Interrupt Status Register (GISR) (0x B800_3004)

Bit	Bit Name	Description	R/W	Default
31	GISR2_IP	GISR2 interrupt pending flag	R	0
30	Reserved	Reserved	R	0
39	Reserved	Reserved	R	0
28	USB0_WAKE_IP	USB0 wake up interrupt pending flag	R	0
27	CPU_WAKE_IP	CPU wake up interrupt pending flag	R	0
26	I2S_IP	I2S interrupt pending flag	R	0
25	USB1_WAKE_IP	USB1 wake up interrupt pending flag.	R	0
24	Reserved	Reserved	R	0
23	MIC_IP	MIC	R	0
22	PCIE1_IP	PCIE port 1host interface interrupt pending flag Or PCIE Endpoint interface interrupt pending flag	R	0
21	PCIE0_IP	PCIE port 0 host interface interrupt pending flag	R	0
20	SECURITY_IP	Security Engine interrupt pending flag	R	0
19	PCM_IP	PCM interface interrupt pending flag	R	0
18	NFBI_IP	NFBI interrupt pending flag.	R	0
17	GPIO_EFGH_IP	GPIO Port E,F,G,H interrupt pending flag	R	0
16	GPIO_ABCD_IP	GPIO Port A,B,C,D interrupt pending flag.	R	0
15	SW_IP	Switch Core interrupt pending flag.	R	0
14	VOIP_IP	VoIP accelerator interrupt pending flag	R	0
13	UART1_IP	UART 1 interrupt pending flag.	R	0
12	UART0_IP	UART 0 interrupt pending flag.	R	0
11	USB_O_IP	USB 2.0 OTG interrupt pending flag.	R	0
10	USB_H_IP	USB 2.0 Host interrupt pending flag.	R	0
9	TC1_IP	Timers/Counters #1 interrupt pending flag.	R	0
8	TC0_IP	Timers/Counters #0 interrupt pending flag.	R	0
7	Reserved	Reserved	R	0
6	Reserved	Reserved	R/WC	0
5	Reserved	Reserved	R/WC	0
4	Reserved	Reserved	R/WC	0
3	Reserved	Reserved	R/WC	0
2	Reserved	Reserved	R/WC	0
1	OTG_CTRL_IP	OTG detect ctrl Interrupt pending flag.	R/WC	0
0	NAND_CTRL_IP	NAND flash ctrl Interrupt pending flag.	R/WC	0

8.1.3. Interrupt Routing Register 0 (IRR0) (0xB800_3008)

Table 20. Interrupt Routing Register 0 (IRR0) (0xB800_3008)

Bit	Bit Name	Description	R/W	Default
n.31-n.28	Reserved	Reserved	R/W	0
n.27-n.24	Reserved	Reserved	R/W	0
n.23-n.20	Reserved	Reserved	R/W	0
n.19-n.16	Reserved	Reserved	R/W	0
n.15-n.12	Reserved	Reserved	R/W	0
n.11-n.8	Reserved	Reserved	R/W	0
n.7-n.4	OTG_CTRL_RS[3:0]	OTG detect ctrl Interrupt route select	R/W	0
n.3-n.0	NAND_CTRL_RS[3:0]	NAND flash ctrl Interrupt route select	R/W	0

8.1.4. Interrupt Routing Register 1 (IRR1) (0xB800_300C)

Table 21. Interrupt Routing Register 1 (IRR1) (0xB800_300C)

Bit	Bit Name	Description	R/W	Default
n.31-n.28	SW_RS[3:0]	Switch Core interrupt route select.	R/W	0
n.27-n.24	VOIP_RS[3:0]	VoIP Accelerator interrupt route select	R/W	0
n.23-n.20	UART1_RS[3:0]	UART1 interrupt route select.	R/W	0
n.19-n.16	UART0_RS[3:0]	UART 0 interrupt route select.	R/W	0
n.15-n.12	USB_O_RS[3:0]	USB 2.0 OTG interrupt route select.	R/W	0
n.11-n.8	USB_H_RS[3:0]	USB 2.0 Host interrupt route select.	R/W	0
n.7-n.4	TC1_RS[3:0]	Timers/Counters #1 interrupt route select.	R/W	0
n.3-n.0	TC0_RS[3:0]	Timers/Counters #0 interrupt route select.	R/W	0

8.1.5. Interrupt Routing Register 2 (IRR2) (0xB800_3010)

Table 22. Interrupt Routing Register 2 (IRR2) (0xB800_3010)

Bit	Bit Name	Description	R/W	Default
n.31-n.28	MIC_RS[3:0]	Generic DMA MIC interrupt route select	R/W	0
n.27-n.24	PCIE1_RS[3:0]	PCIE port 1 Interface interrupt route select Or PCIE Interface endpoint interrupt route select	R/W	0
n.23-n.20	PCIE0_RS[3:0]	PCIE port 0 Interface interrupt route select	R/W	0
n.19-n.16	SECURITY_RS[3:0]	Security Engine interrupt route select	R/W	0
n.15-n.12	PCM_RS[3:0]	PCM interface interrupt route select	R/W	0
n.11-n.8	NFBI_RS[3:0]	NFBI interrupt route select	R/W	0
n.7-n.4	GPIO_EFGH_RS[3:0]	GPIO Port E,F,G,H interrupt route select	R/W	0
n.3-n.0	GPIO_ABCD_RS[3:0]	GPIO Port A,B,C,D interrupt route select.	R/W	0

8.1.6. Interrupt Routing Register 3 (IRR3) (0xB800-3014)

Table 23. Interrupt Routing Register 3 (IRR3) (0xB800-3014)

Bit	Bit Name	Description	R/W	InitVal
n.31-n.28	GISR2_RS[3:0]	GISR2 interrupt route select	R/W	0
n.27-n.24	Reserved	Reserved	R/W	0
n.23-n.20	Reserved	Reserved	R/W	0
n.19-n.16	USB0_WAKE_RS[3:0]	USB0 wake up interrupt route select	R/W	0
n.15-n.12	CPU_WAKE_RS[3:0]	CPU wake up interrupt route select	R/W	0
n.11-n.8	I2S_RS[3:0]	I2S interrupt route select	R/W	0
n.7-n.4	USB1_WAKE_RS[3:0]	USB1 wake up interrupt route select	R/W	0
n.3-n.0	Reserved	Reserved	R/W	0

8.2. Timer

The RTL8197D provides four sets of hardware timers and one watchdog timer. Each timer can be configured to timer mode or counter mode. Counter mode means the timer only times-out once. The initial time-out values are configured via TC0DATA and TC1DATA. The current count values are shown in TC0CNT, TC1CNT, TC2CNT and TC3CNT. CDBR defines the base clock for counting, and is based on a multiple of the system clock. TCIR controls the interrupt resulting from timer time-out. The Watchdog timer is controlled by WDTCNR.

8.2.1. Timer Control (0xB800-3100)

Table 24. Timer Control (0xB800-3100)

Offset	Size (byte)	Name	Description
0x00	4	TC0DATA	Timer/Counter 0 data register. It specifies the time-out duration.
0x04	4	TC1DATA	Timer/Counter 1 data register. It specifies the time-out duration.
0x08	4	TC0CNT	Timer/Counter 0 count register.
0x0C	4	TC1CNT	Timer/Counter 1 count register.
0x10	4	TCCNR	Timer/Counter control register.
0x14	4	TCIR	Timer/Counter interrupt register.
0x18	4	CDBR	Clock division base register.
0x1C	4	WDTCNR	Watchdog timer control register.

8.2.2. Timer/Counter 0 Data Register (0xB800_3100)

Table 25. Timer/Counter 0 Data Register (0xB800-3100)

Bit	Name	Description	RW	Default
31:4	TC0Data[27:0]	The Timer or Counter Initial Value. 0 and 1 not allowed.	RW	0H

8.2.3. Timer/Counter 1 Data Register (0xB800_3104)

Table 26. Timer/Counter 1 Data Register (0xB800-3104)

Bit	Name	Description	RW	Default
31:4	TC1Data[27:0]	The Timer or Counter Initial Value. 0 and 1 not allowed.	RW	0H

8.2.4. Timer/Counter 0 Counter Register (0xB800_3108)

Table 27. Timer/Counter 0 Counter Register (0xB800_3108)

Bit	Name	Description	RW	Default
31:4	TC0Value[27:0]	The Timer or Counter Value. Count incremental by 1 from 0.	R	-

8.2.5. Timer/Counter 1 Counter Register (0xB800_310C)

Table 28. Timer/Counter 1 Counter Register (0xB800_310C)

Bit	Name	Description	RW	Default
31:4	TC1Value[27:0]	The Timer or Counter Value. Count incremental by 1 from 0.	R	-

8.2.6. Timer/Counter Control Register (0xB800_3110)

Table 29. Timer/Counter Control Register (0xB800_3110)

Bit	Bit Name	Description	R/W	Default
31	TC0En	Timer/Counter 0 enable	R/W	0
30	TC0Mode	Timer/Counter 0 mode 0=Counter mode 1=Timer mode	R/W	0
29	TC1En	Timer/Counter 1 enable	R/W	0
28	TC1Mode	Timer/Counter 1 mode 0=counter mode 1=timer mode (When Mitigation&Timer1 is asserted, this bit should be set as 1 to assure normal processing)	R/W	0
27: 0	Reserved		R/W	0

8.2.7. Timer/Counter Interrupt Register (0xB800_3114)

Table 30. Timer/Counter Interrupt Register (0xB800_3114)

Bit	Bit Name	Description	R/W	Default
31	TC0IE	Timer/Counter 0 interrupt enable.	R/W	0
30	TC1IE	Timer/Counter 1 interrupt enable (When Mitigation&Timer1 is asserted, this bit should be set as 0 to assure normal processing)	R/W	0

29	TC0IP	Timer/Counter 0 interrupt pending. Write '1' to clear the interrupt.	R/W	0
28	TC1IP	Timer/Counter 1 interrupt pending. Write '1' to clear the interrupt.	R/W	0
27:0	Reserved		R/W	0

8.2.8. Clock Division Base Register (0xB800_3118)

Table 31. Clock Division Base Register (0xB800_3118)

Bit	Name	Description	RW	Default
31:16	DivFactor[16:0]	Clock Source Division Factor. Assume DivFactor = N, then Base clock = System_clock (Peripheral Lexra Bus)/N. Both values 0x0000 and 0x0001 disable the clock.	RW	0x0000

8.2.9. Watchdog Control Register (0xB800_311C)

Table 32. Watchdog Control Register (0xB800-311C)

Bit	Name	Description	RW	Default
31:24	WDTE[7:0]	Watchdog Enable. When these bits are set to 0xA5, the watchdog timer stops. Other values will enable the watchdog timer and cause a system reset when an overflow signal occurs.	W	0xA5
23	WDTCLR	Watchdog Clear. Write a 1 to clear the up-count watchdog counter.	W	0
22:21	OVSEL[1:0]	Lower Overflow Select bits. These bits specify the overflow condition when the watchdog timer counts to the value. The watch dog timer is based on the base clock defined by CDBR. 00: 2^{15} 01: 2^{16} 10: 2^{17} 11: 2^{18}	RW	00
20	WatchDogIND	Watchdog Event Indicator. 0: A Watchdog RESET did not occur (POWER-ON or PIN RESET) 1: A Watchdog RESET occurred Write '1' to clear.	RW	0

Bit	Name	Description	RW	Default
19	NRFRstType	NOR Flash Reset Command Type selection. When the watchdog event is active and WatchDogIND =1, It will cause the memory controller reboot and issue a Flash reset command. the command type should be pre-defined by this control bit. 0: AMD NOR Flash reset command Type 1: Intel NOR Flash reset command Type *Note: This bit should not be reset by watchdog reset.* PS. This bit has taken over by System_Register hw_strap (Offset: 0xB800-0008h~B800-000bh, R/W) initial value: 0xff00_1410 Reg.bit[19] Strap register without PAD: Indicate NOR flash reset type	RW	0
18:17	OVSEL[3:2]	Higher Overflow Select bits. These bits specify the overflow condition when the watchdog timer counts to the value. The watch dog timer is based on the base clock defined by CDBR. 00: 2^0 x (the counter value of the Lower overflow select bits). 01: 2^4 x (the counter value of the Lower overflow select bits). 10: 2^8 x (the counter value of the Lower overflow select bits). Partial There have 24 bits for watchdog totally. The all condition value list:[bit18, bit17, bit22, bit21] 0000: 2^{15} 0001: 2^{16} 0010: 2^{17} 0011: 2^{18} 0100: 2^{19} 0101: 2^{20} 0110: 2^{21} 0111: 2^{22} 1000: 2^{23} 1001: 2^{24}	RW	0

8.3. GPIO Control

The RTL8197D provides 8 sets of General Purpose Input/Output (GPIO) pins (GPIO A, B, C, D, E, F, G, H). Each GPIO pin may be configured as an input or output pin. The GPIO DATA register may be used to control GPIO pin signals. The GPIO pins are shared with some peripheral pins, and the type of peripheral can affect the attributes of the shared pins. All GPIO sets can be used to generate interrupts, and an interrupt mask and status register are provided. The GPIO control registers are defined in the following table.

8.3.1. GPIO Register Set (0xB800_3500)

Table 33. GPIO Register Set (0xB800_3500)

Offset	Size (Byte)	Name	Description
0x00	4	PABCD_CNR	Port A, B, C, D Control Register
0x08	4	PABCD_DIR	Port A, B, C, D Direction Register
0x0C	4	PABCD_DAT	Port A, B, C, D Data Register
0x10	4	PABCD_ISR	Port A, B, C, D Interrupt Status Register
0x14	4	PAB_IMR	Port A, B Interrupt Mask Register
0x18	4	PCD_IMR	Port C, D Interrupt Mask Register
0x1C	4	PEFGH_CNR	Port E, F, G, H Control Register
0x24	4	PEFGH_DIR	Port E, F, G, H Direction Register
0x28	4	PEFGH_DAT	Port E, F, G, H Data Register
0x2C	4	PEFGH_ISR	Port E, F, G, H Interrupt Status Register
0x30	4	PEF_IMR	Port E, F Interrupt Mask Register
0x34	4	PGH_IMR	Port G, H Interrupt Mask Register

8.3.2. GPIO Port A, B, C, D Control Register (PABCD_CNR) (0xB800_3500)

Table 34. GPIO Port A, B, C, D Control Register (PABCD_CNR) (0xB800_3500)

Bit	Name	Description	Mode	Default
31:24	PFC_D[7:0]	Pin Function Configuration of Port D	RW	FFH
23:16	PFC_C[7:0]	Pin Function Configuration of Port C	RW	FFH
15:8	PFC_B[7:0]	Pin Function Configuration of Port B	RW	FFH
7:0	PFC_A[7:0]	Pin Function Configuration of Port A Bit Value: 0: Configured as GPIO pin 1: Configured as dedicated peripheral pin	RW	FFH

8.3.3. GPIO Port A, B, C, D Direction Register (PABCD_DIR) (0xB800_3508)

Table 35. GPIO Port A, B, C, D Direction Register (PABCD_DIR) (0xB800_3508)

Bit	Name	Description	Mode	Default
31:24	DRC_D[7:0]	Pin Direction Configuration of Port D 0: Configured as input pin 1: Configured as output pin	RW	00H
23:16	DRC_C[7:0]	Pin Direction Configuration of Port C 0: Configured as input pin 1: Configured as output pin	RW	00H
15:8	DRC_B[7:0]	Pin Direction Configuration of Port B 0: Configured as input pin 1: Configured as output pin	RW	00H
7:0	DRC_A[7:0]	Pin Direction Configuration of Port A 0: Configured as input pin 1: Configured as output pin	RW	00H

8.3.4. Port A, B, C, D Data Register (PABCD_DAT) (0xB800_350C)

Table 36. Port A, B, C, D Data Register (PABCD_DAT) (0xB800_350C)

Bit	Name	Description	Mode	Default
31:24	PD_D[7:0]	Pin Data of Port D 0: Data=0 1: Data=1	RW	00H
23:16	PD_C[7:0]	Pin Data of Port C 0: Data=0 1: Data=1	RW	00H
15:8	PD_B[7:0]	Pin Data of Port B 0: Data=0 1: Data=1	RW	00H
7:0	PD_A[7:0]	Pin Data of Port A 0: Data=0 1: Data=1	RW	00H

8.3.5. Port A, B, C, D Interrupt Status Register (PABCD_ISR) (0xB800_3510)

Table 37. Port A, B, C, D Interrupt Status Register (PABCD_ISR) (0xB800_3510)

Bit	Name	Description	Mode	Default
31:24	IPS_D[7:0]	Interrupt Pending Status of Port D Write '1' to clear the interrupt	RW	00H
23:16	IPS_C[7:0]	Interrupt Pending Status of Port C Write '1' to clear the interrupt	RW	00H
15:8	IPS_B[7:0]	Interrupt Pending Status of Port B Write '1' to clear the interrupt	RW	00H
7:0	IPS_A[7:0]	Interrupt Pending Status of Port A Write '1' to clear the interrupt	RW	00H

8.3.6. Port A, B Interrupt Mask Register (PAB_IMR) (0xB800_3514)

Table 38. Port A, B Interrupt Mask Register (PAB_IMR) (0xB800_3514)

Bit	Name	Description	Mode	Default
31:30	PB7_IM[1:0]	PortB.7 Interrupt Mode	RW	00B
29:28	PB6_IM[1:0]	PortB.6 Interrupt Mode	RW	00B
27:26	PB5_IM[1:0]	PortB.5 Interrupt Mode	RW	00B
25:24	PB4_IM[1:0]	PortB.4 Interrupt Mode	RW	00B
23:22	PB3_IM[1:0]	PortB.3 Interrupt Mode	RW	00B
21:20	PB2_IM[1:0]	PortB.2 Interrupt Mode	RW	00B
19:18	PB1_IM[1:0]	PortB.1 Interrupt Mode	RW	00B
17:16	PB0_IM[1:0]	PortB.0 Interrupt Mode	RW	00B
15:14	PA7_IM[1:0]	PortA.7 Interrupt Mode	RW	00B
13:12	PA6_IM[1:0]	PortA.6 Interrupt Mode	RW	00B
11:10	PA5_IM[1:0]	PortA.5 Interrupt Mode	RW	00B
9:8	PA4_IM[1:0]	PortA.4 Interrupt Mode	RW	00B
7:6	PA3_IM[1:0]	PortA.3 Interrupt Mode	RW	00B
5:4	PA2_IM[1:0]	PortA.2 Interrupt Mode	RW	00B
3:2	PA1_IM[1:0]	PortA.1 Interrupt Mode	RW	00B
1:0	PA0_IM[1:0]	PortA.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

8.3.7. Port C, D Interrupt Mask Register (PCD_IMR) (0xB800_3518)

Table 39. Port C, D Interrupt Mask Register (PCD_IMR) (0xB800_3518)

Bit	Name	Description	Mode	Default
31:30	PD7_IM[1:0]	PortD.7 Interrupt Mode	RW	00B
29:28	PD6_IM[1:0]	PortD.6 Interrupt Mode	RW	00B
27:26	PD5_IM[1:0]	PortD.5 Interrupt Mode	RW	00B
25:24	PD4_IM[1:0]	PortD.4 Interrupt Mode	RW	00B
23:22	PD3_IM[1:0]	PortD.3 Interrupt Mode	RW	00B
21:20	PD2_IM[1:0]	PortD.2 Interrupt Mode	RW	00B
19:18	PD1_IM[1:0]	PortD.1 Interrupt Mode	RW	00B
17:16	PD0_IM[1:0]	PortC.0 Interrupt Mode	RW	00B
15:14	PC7_IM[1:0]	PortC.7 Interrupt Mode	RW	00B
13:12	PC6_IM[1:0]	PortC.6 Interrupt Mode	RW	00B
11:10	PC5_IM[1:0]	PortC.5 Interrupt Mode	RW	00B
9:8	PC4_IM[1:0]	PortC.4 Interrupt Mode	RW	00B
7:6	PC3_IM[1:0]	PortC.3 Interrupt Mode	RW	00B
5:4	PC2_IM[1:0]	PortC.2 Interrupt Mode	RW	00B
3:2	PC1_IM[1:0]	PortC.1 Interrupt Mode	RW	00B

Bit	Name	Description	Mode	Default
1:0	PC0_IM[1:0]	PortC.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

8.3.8. GPIO Port E, F, G, H Control Register (PEFGH_CNR) (0xB800_351C)

Table 40. GPIO Port E, F, G, H Control Register (PEFGH_CNR) (0xB800_351C)

Bit	Name	Description	Mode	Default
31:24	PFC_H[7:0]	Pin Function Configuration of Port H	RW	FFH
23:16	PFC_G[7:0]	Pin Function Configuration of Port G	RW	FFH
15:8	PFC_F[7:0]	Pin Function Configuration of Port F	RW	FFH
7:0	PFC_E[7:0]	Pin Function Configuration of Port E Bit Value: 0: Configured as GPIO pin 1: Configured as dedicated peripheral pin	RW	FFH

8.3.9. GPIO Port E, F, G, H Direction Register (PEFGH_DIR) (0xB800_3524)

Table 41. GPIO Port E, F, G, H Direction Register (PEFGH_DIR) (0xB800_3524)

Bit	Name	Description	Mode	Default
31:24	DRC_H[7:0]	Pin Direction Configuration of Port H 0: Configured as input pin 1: Configured as output pin	RW	00H
23:16	DRC_G[7:0]	Pin Direction Configuration of Port G 0: Configured as input pin 1: Configured as output pin	RW	00H
15:8	DRC_F[7:0]	Pin Direction Configuration of Port F 0: Configured as input pin 1: Configured as output pin	RW	00H
7:0	DRC_E[7:0]	Pin Direction Configuration of Port E 0: Configured as input pin 1: Configured as output pin	RW	00H

8.3.10. Port E, F, G, H Data Register (PEFGH_DAT) (0xB800_3528)

Table 42. Port E, F, G, H Data Register (PEFGH_DAT) (0xB800_3528)

Bit	Name	Description	Mode	Default
31:24	PD_H[7:0]	Pin Data of Port H 0: Data=0 1: Data=1	RW	00H
23:16	PD_G[7:0]	Pin Data of Port G 0: Data=0 1: Data=1	RW	00H
15:8	PD_F[7:0]	Pin Data of Port F 0: Data=0 1: Data=1	RW	00H
7:0	PD_E[7:0]	Pin Data of Port E 0: Data=0 1: Data=1	RW	00H

8.3.11. Port E, F, G, H Interrupt Status Register (PEFGH_ISR) (0xB800_352C)

Table 43. Port E, F, G, H Interrupt Status Register (PEFGH_ISR) (0xB800_352C)

Bit	Name	Description	Mode	Default
31:24	IPS_H[7:0]	Interrupt Pending Status of Port H Write '1' to clear the interrupt	RW	00H
23:16	IPS_G[7:0]	Interrupt Pending Status of Port G Write '1' to clear the interrupt	RW	00H
15:8	IPS_F[7:0]	Interrupt Pending Status of Port F Write '1' to clear the interrupt	RW	00H
7:0	IPS_E[7:0]	Interrupt Pending Status of Port E Write '1' to clear the interrupt	RW	00H

8.3.12. Port E, F Interrupt Mask Register (PEF_IMR) (0xB800_3530)

Table 44. Port E, F Interrupt Mask Register (PEF_IMR) (0xB800_3530)

Bit	Name	Description	Mode	Default
31:30	PF7_IM[1:0]	PortF.7 Interrupt Mode	RW	00B
29:28	PF6_IM[1:0]	PortF.6 Interrupt Mode	RW	00B
27:26	PF5_IM[1:0]	PortF.5 Interrupt Mode	RW	00B
25:24	PF4_IM[1:0]	PortF.4 Interrupt Mode	RW	00B
23:22	PF3_IM[1:0]	PortF.3 Interrupt Mode	RW	00B
21:20	PF2_IM[1:0]	PortF.2 Interrupt Mode	RW	00B
19:18	PF1_IM[1:0]	PortF.1 Interrupt Mode	RW	00B
17:16	PF0_IM[1:0]	PortF.0 Interrupt Mode	RW	00B
15:14	PE7_IM[1:0]	PortE.7 Interrupt Mode	RW	00B
13:12	PE6_IM[1:0]	PortE.6 Interrupt Mode	RW	00B
11:10	PE5_IM[1:0]	PortE.5 Interrupt Mode	RW	00B
9:8	PE4_IM[1:0]	PortE.4 Interrupt Mode	RW	00B
7:6	PE3_IM[1:0]	PortE.3 Interrupt Mode	RW	00B

Bit	Name	Description	Mode	Default
5:4	PE2_IM[1:0]	PortE.2 Interrupt Mode	RW	00B
3:2	PE1_IM[1:0]	PortE.1 Interrupt Mode	RW	00B
1:0	PE0_IM[1:0]	PortE.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

8.3.13. Port G, H Interrupt Mask Register (PGH_IMR) (0xB800_3534)

Table 45. Port G, H Interrupt Mask Register (PGH_IMR) (0xB800_3534)

Bit	Name	Description	Mode	Default
31:30	PH7_IM[1:0]	PortH.7 Interrupt Mode	RW	00B
29:28	PH6_IM[1:0]	PortH.6 Interrupt Mode	RW	00B
27:26	PH5_IM[1:0]	PortH.5 Interrupt Mode	RW	00B
25:24	PH4_IM[1:0]	PortH.4 Interrupt Mode	RW	00B
23:22	PH3_IM[1:0]	PortH.3 Interrupt Mode	RW	00B
21:20	PH2_IM[1:0]	PortH.2 Interrupt Mode	RW	00B
19:18	PH1_IM[1:0]	PortH.1 Interrupt Mode	RW	00B
17:16	PH0_IM[1:0]	PortH.0 Interrupt Mode	RW	00B
15:14	PG7_IM[1:0]	PortG.7 Interrupt Mode	RW	00B
13:12	PG6_IM[1:0]	PortG.6 Interrupt Mode	RW	00B
11:10	PG5_IM[1:0]	PortG.5 Interrupt Mode	RW	00B
9:8	PG4_IM[1:0]	PortG.4 Interrupt Mode	RW	00B
7:6	PG3_IM[1:0]	PortG.3 Interrupt Mode	RW	00B
5:4	PG2_IM[1:0]	PortG.2 Interrupt Mode	RW	00B
3:2	PG1_IM[1:0]	PortG.1 Interrupt Mode	RW	00B
1:0	PG0_IM[1:0]	PortG.0 Interrupt Mode 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

8.4. GPIO Shared Pin Configured Mapping List

The RTL8197D GPIO pins are shared with the other functions.

8.4.1. Shared Pin Register (PIN_MUX_SEL) (0xB800_0040~0xB800_0043h)

Table 46. Shared Pin Register (PIN_MUX_SEL) (0xB800_0040~0xB800_0043h)

Bit	Bit Name	Description	Mode	Default
31:30	Reserved	Reserved	-	-
29:28	reg_iocfg_sdio3	Configure SF_SDIO3 PAD as SF_SDIO3 or GPIOC5 00: SF_SDIO3 01: Reserved 10: Reserved 11: GPIOC5	RW	00B
27:26	reg_iocfg_sdio2	Configure SF_SDIO2 PAD as SF_SDIO2 or GPIOC4 00: SF_SDIO2 01: Reserved 10: Reserved 11: GPIOC4	RW	00B
25:24	reg_iocfg_sdio1	Configure SF_SDIO1 PAD as SF_SDIO1 or GPIOC3 00: SF_SDIO1 01: Reserved 10: Reserved 11: GPIOC3	RW	00B
23:22	reg_iocfg_sdio0	Configure SF_SDIO0 PAD as SF_SDIO0 or GPIOC2 00: SF_SDIO0 01: Reserved 10: Reserved 11: GPIOC2	RW	00B
21:20	reg_iocfg_sck	Configure SF_SCK PAD as SF_SCK or GPIOC1 00: SF_SCK 01: Reserved 10: Reserved 11: GPIOC1	RW	00B
19:18	reg_iocfg_fcs0n	Configure SF_CS0# PAD as SF_CS0# or GPIOC6 00: SF_CS0# 01: Reserved 10: Reserved 11: GPIOC6	RW	00B
17:16	reg_iocfg_mcs1n	Configure MCS1# PAD as SF_MCS1# or GPIOA0 00: MCS1# 01: Reserved 10: Reserved 11: GPIOA0	RW	00B
15	reg_iocfg_p0_crs_col	Configure P0_RXD4 as P0_CRS and P0_RXD5 as P0_COL, default: 1'b0(disable) 0: P0_RXD4, P0_RXD5 01: P0_CRS, P0_COL	RW	00B
14	Reserved	Reserved	-	-
13:12	reg_iocfg_fcs1n	Configure SF_CS1# Pin as flash or GPIO Mode 00: SF_CS1# 01: NAND_CE# 10: Reserved 11: GPIOA1	RW	00B
11:10	reg_iocfg_p0mii_2	Configure P0_TXD[7:4], P0_RXD[7:4] Pins as GMII, UART1, or GPIO Mode 00: P5_TXD[7:4], P5_RXD[7:4] 01: UART1 10: Reserved 11: GPIO	RW	00B

Bit	Bit Name	Description	Mode	Default
9:8	reg_iocfg_p0mii	Configure GMII except P5_TXD[7:4], P5_RXD[7:4] Pins as GMII/RGMII/MII, flash, or GPIO Mode 00: GMII/RGMII/MII 01: NAND flash 10: Reserved 11: GPIO	RW	00B
7	Reserved	Reserved	-	-
6	reg_iocfg_pcie	Configure PCIE_RST# Pin as PCIE or GPIO Mode 0: PCIE_RST# 11: GPIOB1	RW	00B
5	reg_iocfg_uart	Configure UART0_TX, UART0_RX Pins as UART or GPIO Mode 0: UART 1: GPIO	RW	0B
4:3	reg_iocfg_p0mdio	Configure MDC/MDIO PAD as P0-MDIO or GPIO Mode 00: MDC/MDIO 01: Reserved 10: Reserved 11: GPIOF5, GPIOF6	RW	00B
2:0	reg_iocfg_jtag	Configure JTAG Pins as JTAG, DBG, or GPIO Mode 000: Reserved 001: JTAG 010: UART1 011: I2S 100: Reserved 101: Reserved 110: GPIO 111: Reserved	RW	000B

8.4.2. Shared Pin Register (PIN_MUX_SEL_2) (0xB800_0044~0xB800_0047h)

Table 47. Shared Pin Register (PIN_MUX_SEL_2) (0xB800_0044~0xB800_0047h)

Bit	Bit Name	Description	Mode	Default
31:21	Reserved	Reserved	-	-
20:18	reg_iocfg_led_scan	Configure LED_P2 Pin as LED-SW, or GPIO Mode 000: Reserved 001: LED_SCAN 010: Reserved 011: Reserved 100: GPIOC0 101: Reserved 110: Reserved 111: Reserved	RW	000B
17:15	reg_iocfg_led_p1	Configure GPIO Pin as I2S or GPIO Mode 000: Reserved 001: Reserved 010: I2S 011: Reserved 100: GPIOB7 101: Reserved 110: Reserved 111: Reserved	RW	000B
14	Reserved	Reserved	-	-
13:12	reg_iocfg_led_port4	Configure LED_PORT4 Pin as LED-SW or GPIO Mode 00: LED_PORT4 01: Reserved 10: Reserved 11: GPIOB6	RW	10B
11	Reserved	Reserved	-	-
10:9	reg_iocfg_led_port3	Configure LED_PORT3 Pin as LED-SW or GPIO Mode 00: LED_PORT3 01: Reserved 10: Reserved 11: GPIOB5	RW	10B
8	Reserved	Reserved	-	-

Bit	Bit Name	Description	Mode	Default
7:6	reg_iocfg_led_port2	Configure LED_PORT2 Pin as LED-SW or GPIO Mode 00: LED_PORT2 01: Reserved 10: Reserved 11: GPIOB4	RW	10B
5	Reserved	Reserved	-	-
4:3	reg_iocfg_led_port1	Configure LED_PORT1 Pin as LED-SW or GPIO Mode 00: LED_PORT1 01: Reserved 10: Reserved 11: GPIOB3	RW	10B
2	Reserved	Reserved	-	-
1:0	reg_iocfg_led_port0	Configure LED_PORT0 Pin as LED-SW or GPIO Mode 00: LED_PORT0 01: Reserved 10: Reserved 11: GPIOB2	RW	10B

9. UART

9.1. Features

The RTL8197D products provide two 16550 compatible UARTs, which contains a 16-byte First In First Out (FIFO) buffer and Auto Flow Control to control transmissions on port 1. The baud rate can be up to 1Mbps and a programmable baud rate generator allows division of any input reference clock by 1 to (2^16-1) and generates an internal 16x clock.

9.2. Interface Pins

The UART interface pins are shown in Table 48.

Table 48. UART Control Interface Pins

Signal Name	Type	Function
TXD#	O	Transmit Data For Port 0 and port 1
RXD#	I	Receive Data For Port 0 and port 1
RTS#	O	Request To Send For port 1
CTS#	I	Clear To Send For Port 1

9.3. UART Control Register

9.3.1. UART Control Register Address Mapping

Table 49. UART Control Register Address Mapping (Base: 0xB800_2000)

Offset	Size (byte)	Name	Description
000	1	UART0_RBR	Receiver Buffer Register (DLAB=0)
000	1	UART0_THR	Transmitter Holding Register (DLAB=0)
000	1	UART0_DLL	Divisor Latch LSB (DLAB=1)
004	1	UART0_IER	Interrupt Enable Register (DLAB=0)
004	1	UART0_DLM	Divisor Latch MSB (DLAB=1)
008	1	UART0_IIR	Interrupt Identification Register
008	1	UART0_FCR	FIFO Control Register
00c	1	UART0_LCR	Line Control Register
010	1	UART0_MCR	Modem Control Register
014	1	UART0_LSR	Line Status Register
018	1	UART0_MSR	Modem Status Register
01c	1	UART0_SCR	Scratch Register
100	1	UART1_RBR	Receiver Buffer Register (DLAB=0)
100	1	UART1_THR	Transmitter Holding Register (DLAB=0)
100	1	UART1_DLL	Divisor Latch LSB (DLAB=1)
104	1	UART1_IER	Interrupt Enable Register (DLAB=0

Offset	Size (byte)	Name	Description
104	1	UART1_DLM	Divisor Latch MSB (DLAB=1)
108	1	UART1_IIR	Interrupt Identification Register
108	1	UART1_FCR	FIFO Control Register
10c	1	UART1_LCR	Line Control Register
110	1	UART1_MCR	Modem Control Register
114	1	UART1_LSR	Line Status Register
118	1	UART1_MSR	Modem Status Register
11c	1	UART1_SCR	Scratch Register

9.3.2. UART Receiver Buffer Register (DLAB=0)

Table 50. UART Receiver Buffer Register (DLAB=0) (0xB800_2100, 0xB800_2000)

Reg.bit	Name	Description	Mode	Default
31:24	RBR[7:0]	Receiver Buffer Data.	R	00H

9.3.3. UART Transmitter Holding Register (DLAB=0)

Table 51. UART Transmitter Holding Register (DLAB=0) (0xB800_2100,0xB800_2000)

Reg.bit	Name	Description	Mode	Default
31:24	THR[7:0]	Transmitter Holding Data	W	00H

9.3.4. UART Divisor Latch LSB (DLAB=1)

Table 52. UART Divisor Latch LSB (DLAB=1) (0xB800_2100, ,0xB800_2000)

Reg.bit	Name	Description	Mode	Default
31:24	DLL[7:0]	Divisor Latch LSB	RW	00H

9.3.5. UART Divisor Latch MSB (DLAB=1)

Table 53. UART Divisor Latch MSB (DLAB=1) (0xB800_2104,0xB800_2004)

Reg.bit	Name	Description	Mode	Default
31:24	DLM[7:0]	Divisor Latch MSB	RW	00H

9.3.6. UART Interrupt Enable Register (DLAB=0)

Table 54. UART Interrupt Enable Register (DLAB=0) (0xB800_2104,0xB800_2004)

Reg.bit	Name	Description	Mode	Default
24	ERBI	Enable Received Data Available Interrupt	RW	0B
25	ETBEI	Enable Transmitter Holding Register Empty Interrupt	RW	0B
26	ELSI	Enable Receiver Line Status Interrupt	RW	0B
27	EDSSI	Enable Modem Status Register Interrupt	RW	0B
28	ESLP	Sleep Mode Enable	RW	0B
29	ELP	Low Power Mode Enable	RW	0B
31:30	-	Reserved	-	-

9.3.7. UART Interrupt Identification Register

Table 55. UART Interrupt Identification Register (0xB800_2108,0xB800_2008)

Reg.bit	Name	Description	Mode	Default
24	IPND	Interrupt Pending. 0: Interrupt pending	R	1B
27:25	IID[2:0]	Interrupt ID. IID[1:0] indicates the interrupt priority.	R	000B
29:28	-	Reserved	-	-
31:30	FIFO16[1:0]	00: No FIFO 11: 16-byte FIFO	R	11B

9.3.8. UART FIFO Control Register

Table 56. UART FIFO Control Register (0xB800_2108,0xB800_2008)

Reg.bit	Name	Description	Mode	Default
24	EFIFO	Enable FIFO. When this bit is set, enables the transmitter and receiver FIFOs. Changing this bit clears the FIFOs.	W	0B
25	RFRST	Receiver FIFO Reset. Writes 1 to clear the receiver FIFO.	W	0B
26	TFRST	Transmitter FIFO Reset. Writes 1 to clear the transmitter FIFO.	W	0B
29:27	-	Reserved.	-	-
31:30	RTRG[1:0]	Receiver Trigger Level. Trigger level: 16-byte. 00: 01 01: 04 10: 08 11: 14	W	11B

9.3.9. UART Line Control Register

Table 57. UART Line Control Register (0xB800_210C, ,0xB800_200C)

Reg.bit	Name	Description	Mode	Default
25:24	WLS[1:0]	Word Length Select. 00: Reserved (NA.) 01: 6 bits (NA.) 10: 7 bits 11: 8 bits	RW	11B
26	STB	Number of Stop Bits. 0: 1 bit 1: 2 bits	RW	0B
27	PEN	Parity Enable.	RW	0B
29:28	EPS[1:0]	Even Parity Select. 00: Odd parity 01: Even parity 10: Mark parity 11: Space parity	RW	00B
30	BRK	Break Control. Set this bit force TXD to the spacing (low) state (break). Clear this bit to disable break condition.	RW	0B
31	DLAB	Divisor Latch Access Bit.	RW	0B

9.3.10. UART Modem Control Register

Table 58. UART Modem Control Register (0xB800_2110,0xB800_2010)

Reg.bit	Bit Name	Description	Mode	Default
24	DTR	Data Terminal Ready. 0: Set DTR# high 1: Set DTR# low	RW	0B
25	RTS	Request To Send. 0: Set RTS# high 1: Set RTS# low	RW	0B
26	OUT1	Out 1	RW	0B
27	OUT2	Out 2	RW	0B
28	LOOP	Loopback	RW	0B
29	AFE	Auto Flow Control Enable	RW	0B

9.3.11. UART Line Status Register

Table 59. UART Line Status Register (0xB800_2114,0xB800_2014)

Reg.bit	Name	Description	Mode	Default
24	DR	Data Ready. Character mode: Data ready in RBR FIFO mode: Receiver FIFO is not empty	R	0B
25	OE	Overrun Error. An overrun occurs when the receiver FIFO is full and the next character is completely received in the receiver shift register. An OE is indicated. The character in the shift register will be overwritten.	R	0B
26	PE	Parity Error	R	0B
27	FE	Framing Error	R	0B
28	BI	Break Interrupt Indicator	R	0B

Reg.bit	Name	Description	Mode	Default
29	THRE	Transmitter Holding Register Empty. Character mode: THR is empty FIFO mode: Transmitter FIFO is empty	R	1B
30	TEMT	Transmitter Empty. Character mode: Both THR and TSR are empty. FIFO mode: Both transmitter FIFO and TSR are empty.	R	1B
31	RFE	Receiver FIFO Error. Either a parity, framing, or break error in the FIFO.	R	0B

9.3.12. UART Modem Status Register

Table 60. UART Modem Status Register (0xB800_2110,0xB800_2018)

Reg.bit	Name	Description	Mode	Default
31	ΔCTS	Delta Clear to Send. CTS# signal transmits.	R	1B
30	ΔDSR	Delta Data Set Ready. DSR# signal transmits. Returns 0.	R	0B
29	TERI	Trailing edge ring indicator. RI# signal changes from low to high. Returns 0.	R	0B
28	ΔDCD	Delta Data Carrier Detect. DCD# signal transmits. Returns 0.	R	0B
27	CTS	Clear to Send. 0: CTS# detected high 1: CTS# detected low	R	0B
26	DSR	Data Set Ready. 0: DSR # detected high 1: DSR# detected low In loopback mode, returns bit 0 of MCR In normal mode, returns 1.	R	1B
25	RI	Ring Indicator. 0: RI# detected high 1: RI# detected low In loopback mode, returns bit 3 of MCR. In normal mode, returns 0.	R	0B
24	DCD	Data Carrier Detect. 0: DCD# detected high 1: DCD# detected low In loopback mode, returns bit 2 of MCR. In normal mode, returns 1.	R	1B

9.4. Baud Rate

Value of divisor latch = [Base clock/(16*baud rate)]–1. The Base clock is 200MHz.

Table 61. Divisor Latch Value Examples

System CLK Base Clock	300bps	1200bps	2400bps	9600bps	19200bps	38400bps	57600bps	115200bps
200MHz	41665	10415	5207	1301	650	324	216	107

10. IIS

10.1. I²S Description

10.1.1. I²S Interface

I²S (Inter-IC Sound) is a standard communication structure used in new digital audio systems. Previously digital audio signals in the consumer audio market were processed by a number of VLSI ICs. The I²S standardized communication structure increases system flexibility.

10.1.2. I²S Voice Standard

Figure 3 shows a sample I²S Mono-Out/Audio-Out Interface Configuration in the RTL8197D.

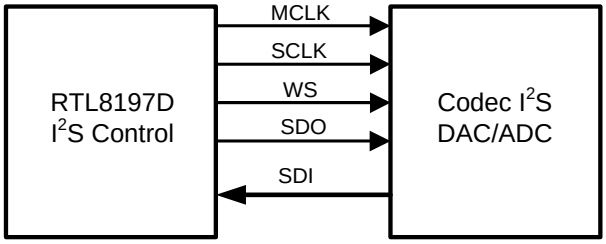


Figure 3. I²S Mono-Out/Audio-Out Interface Configuration in the RTL8197D

Figure 4 shows the basic timing of an I²S transfer. Note that the first bit after the WS line change is the LSB of the previous sample data.

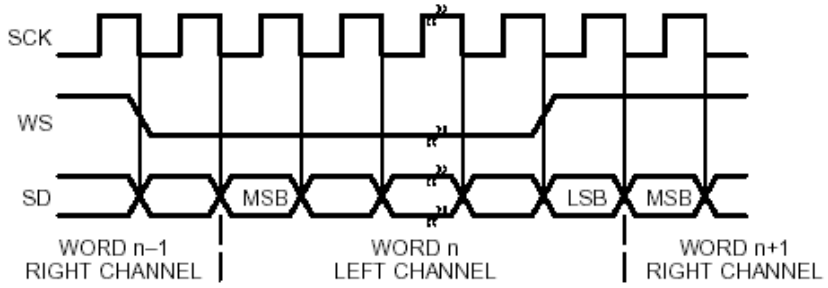


Figure 4. I²S Basic Transfer Timing

- WS clock is the defined sampling rate frequency
- SCLK is 32x the sampling rate frequency, which means maximum 16-bit channel sampling is supported
- For MCLK, typically a 256x sampling rate frequency is supported. Table 62, page 50 shows a sample clock configuration

Table 62. I²S Sample Clock Configuration

Signal Line	Description	
	Frequency	Sampling Rate
SCLK (16-bit)	3.072MHz	96.0kHz
	1.536MHz	48.0kHz
	1.024MHz	32.0kHz
	0.768MHz	24.0kHz
	0.512MHz	16.0kHz
	0.256MHz	8.0kHz
MCLK (16-bit)	24.576MHz	96.0kHz
	12.288MHz	48.0kHz
	8.192MHz	32.0kHz
	6.144MHz	24.0kHz
	4.096MHz	16.0kHz
	2.048MHz	8.0kHz
WS (16-bit)	WS=0 to Left Channel (Mono). WS=1 to Right Channel	
SDO	Transmits Voice/Audio Data Channel. Serial data is transmitted in 2's complement, with MSB first, and synchronized with the trailing (HIGH to LOW) edge of the clock signal.	
SDI	Receives Voice/Audio Data Channel. Serial data is transmitted in 2's complement, with MSB first, and synchronized with the trailing (HIGH to LOW) edge of the clock signal.	

10.2. Clock Type

- SCLK: 3.072MHz, 2.048MHz, 1.536MHz, 1.024MHz, 0.512MHz, 0.256MHz
- MCLK: 24.576MHz, 12.288MHz, 8.192MHz, 6.144MHz, 4.096MHz, 2.048MHz
- WS (Sample Rate): 96K, 48K, 32K, 24K, 16K, 8K
- MCLK=8SCLK=256WS (16-bit)

10.3. Features

- Sample Bit: 16-bit
- Sample Rate: 8K, 16K, 24K, 32K, 48K, 96K
- IIS Throughput: 0.128Mbps (8K*16bit) ~ 1.536Mbps (96K*16bit)
- IIS Channel Num: Mono

- Maximum Page Number: 4
- Maximum Page Size: 16K-byte
- Supports Mono TX or RX, and TX&RX mode
-

10.4. FIFO Allocation

10.4.1. Mono Channel (FIFO)

Table 63. Mono Channel (FIFO)

Sample Size = 16 Bits	
(MSB)Bit 31 to 16	**Bit 15 to 0 (LSB)**
Mono Channel (1)	Mono Channel (2)
Mono Channel (3)	Mono Channel (4)
Mono Channel (5)	Mono Channel (6)
Mono Channel (7)	Mono Channel (8)
Mono Channel (9)	Mono Channel (10)
Mono Channel (11)	Mono Channel (12)
Mono Channel (13)	Mono Channel (14)
Mono Channel (15)	Mono Channel (16)

10.4.2. Stereo channel (FIFO)

Table 64. Stereo Channel (FIFO)

Sample Size = 16 Bits	
(MSB)Bit 31 to 16	**Bit 23 to 0 (LSB)**
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel
Left Channel	Right Channel

10.4.3. IIS Register Address Mapping

Table 65. IIS Register Address Mapping (Base: 0xB800_9000)

Offset	Size (Byte)	Mode	Tag	Description
0x00	4	RW	IIS_CR	IIS Control Register.
0x04	4	RW	PAGE_PTR_TX	TX Page Pointer Register.

Offset	Size (Byte)	Mode	Tag	Description
0x08	4	RW	PAGE_PTR_RX	RX Page Pointer Register.
0x0C	4	RW	PAGE_SIZE PAGE_NUM_SR	Page Size and Sample Rate Setting Register. The used page number can be configured from 1 to 4 (default is 2).
0x10	4	RW	P0OKIE_TX P1OKIE_TX P2OKIE_TX P3OKIE_TX BUFUNAVA_IE_TX	TX Interrupt Enable Register.
0x14	4	R	P0OKIP_TX P1OKIP_TX P2OKIP_TX P3OKIP_TX BUFUNAVA_IP_TX	TX Interrupt Status Register.
0x18	4	RW	P0OKIE_RX P1OKIE_RX P2OKIE_RX P3OKIE_RX BUFUNAVA_IE_RX	RX Interrupt Enable Register.
0x1C	4	R	P0OKIP_RX P1OKIP_RX P2OKIP_RX P3OKIP_RX BUFUNAVA_IP_RX	RX Interrupt Status Register.
0x20	4	RW	POWN_TX	TX Page 0 Own Bit.
0x24	4	RW	P1WN_TX	TX Page 1 Own Bit.
0x28	4	RW	P2WN_TX	TX Page 2 Own Bit.
0x2C	4	RW	P3WN_TX	TX Page 3 Own Bit.
0x30	4	RW	POWN_RX	RX Page 0 Own Bit.
0x34	4	RW	P1WN_RX	RX Page 1 Own Bit.
0x38	4	RW	P2WN_RX	RX Page 2 Own Bit.
0x3C	4	RW	P3WN_RX	RX Page 3 Own Bit.

10.4.4. IIS Control Register

Table 66. IIS Control Register (0xB800_9000)

Reg.bit	Name	Description	Mode	Default
31	SW_RSTN	0: SW reset (This reset will clear FIFO, reset to memory 1st address, but not clear ISR. The last pending interrupt must be cleared before re-enabling IIS) 1: No SW reset	RW	0x1B
30:11	-	Reserved	-	-

Reg.bit	Name	Description	Mode	Default
10	DACLRSWAP	Controls whether the DAC Appears on the 'Right' or 'Left' Phase of the WS Clock. 0: Left phase 1: Right phase	RW	0B
9:8	FORMAT	Digital Interface Format. 0 (00): I^2S 1 (01): Left justified 2 (10): Right justified	RW	0B
7	LOOP_BACK	Internal Testing.	RW	0B
6	WL	Word Length. 0: 16 bits 1: Reserved	RW	0B
5	EDGE_SW	Edge Switch. 0: Negative edge 1: Positive edge	RW	0B
4:3	Audio_Mono	Stereo or Mono Mode select 0 (00): Stereo Audio 1 (01): Reserved 2 (10): Mono 3 (11): Reserved	RW	0B
2:1	TX_RX_ACT	TX/RX Active 00: RX path 01: TX path 10: TX_RX path (Bi-directional applications)	RW	0B
0	IIS_EN	IIS Enable 0: Disable 1: Enable	R/W	0B

10.4.5. TX Page Pointer Register

Table 67. TX Page Pointer Register (0xB800_9004)

Reg.bit	Name	Description	Mode	Default
31:2	PAGE_PTR_TX	TX Page Pointer. This is a physical address with word-align limitation.	RW	0H

10.4.6. RX Page Pointer Register

Table 68. RX Page Pointer Register (0xB800_9008)

Reg.bit	Name	Description	Mode	Default
31:2	PAGE_PTR_RX	RX Page Pointer. This is a physical address with word-align limitation.	RW	0H

10.4.7. Page Size and Sample Rate Setting Register

Table 69. Page Size and Sample Rate Setting Register (0xB800_900C)

Reg.bit	Name	Description	Mode	Default
11:0	PAGE_SIZE	Page Size in Unit of 4(n+1) Bytes.	RW	0H
13:12	PAGE_NUM	Page Number. 00: One page 01: Two pages 10: Three pages 11: Four pages	RW	0H
16:14	SR	Sample Rate. 000: 8kHz 001: 16kHz 010: 24kHz 011: 32kHz 101: 48kHz 110: 96kHz 111: Reserved	RW	101B

10.4.8. TX Interrupt Enable Register

Table 70. TX Interrupt Enable Register (0xB800_9010)

Reg.bit	Name	Description	Mode	Default
0	P0OKIE_TX	TX Page 0 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
1	P1OKIE_TX	TX Page 1 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
2	P2OKIE_TX	TX Page 2 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
3	P3OKIE_TX	TX Page 3 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
4	PAGEUNAVA_IE_TX	TX Page Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
5	FIFO_EMPTY_IE_TX	TX FIFO Empty Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B

10.4.9. TX Interrupt Status Register

Table 71. TX Interrupt Status Register (0xB800_9014)

Reg.bit	Name	Description	Mode	Default
0	P0OKIP_TX	TX Page 0 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
1	P1OKIP_TX	TX Page 1 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
2	P2OKIP_TX	TX Page 2 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
3	P3OKIP_TX	TX Page 3 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B

Reg.bit	Name	Description	Mode	Default
4	PAGEUNAVA_IP_TX	TX Page Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
5	FIFO_EMPTY_IP_TX	TX FIFO Empty Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B

10.4.10. RX Interrupt Enable Register

Table 72. RX Interrupt Enable Register (0xB800_9018)

Reg.bit	Name	Description	Mode	Default
0	P0OKIE_RX	RX Page 0 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
1	P1OKIE_RX	RX Page 1 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
2	P2OKIE_RX	RX Page 2 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
3	P3OKIE_RX	RX Page 3 OK Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
4	PAGEUNAVA_IE_RX	RX Page Unavailable Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B
5	FIFO_FULL_IE_RX	RX FIFO Full Interrupt Enable. 0: Disable interrupt 1: Enable interrupt	RW	0B

10.4.11. RX Interrupt Status Register

Table 73. RX Interrupt Status Register (0xB800_901C)

Reg.bit	Name	Description	Mode	Default
0	P0OKIP_RX	RX Page 0 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
1	P1OKIP_RX	RX Page 1 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
2	P2OKIP_RX	RX Page 2 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
3	P3OKIP_RX	RX Page 3 OK Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
4	PAGEUNAVA_IP_RX	RX Page Unavailable Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B
5	FIFO_FULL_IP_RX	RX FIFO Full Interrupt Pending. 0: No interrupt 1: Interrupt pending; write 1 to clear	RW	0B

10.4.12. TX Page 0 Own Bit

Table 74. TX Page 0 Own Bit (0xB800_9020)

Reg.bit	Name	Description	Mode	Default
31	P0OWN_TX	TX Page 0 Own Bit. 0: Page 0 owned by CPU 1: Page 0 owned by IIS controller	RW	0B

10.4.13. TX Page 1 Own Bit

Table 75. TX Page 1 Own Bit (0xB800_9024)

Reg.bit	Name	Description	Mode	Default
31	P1OWN_TX	TX Page 1 Own Bit. 0: Page 1 owned by CPU 1: Page 1 owned by IIS controller	RW	0B

10.4.14. TX Page 2 Own Bit

Table 76. TX Page 2 Own Bit (0xB800_9028)

Reg.bit	Name	Description	Mode	Default
31	P2OWN_TX	TX Page 2 Own Bit. 0: Page 2 owned by CPU 1: Page 2 owned by IIS controller	RW	0B

10.4.15. TX Page 3 Own Bit

Table 77. TX Page 3 Own Bit (0xB800_902C)

Reg.bit	Name	Description	Mode	Default
31	P3OWN_TX	TX Page 3 Own Bit. 0: Page 3 owned by CPU 1: Page 3 owned by IIS controller	RW	0B

10.4.16. RX Page 0 Own Bit

Table 78. RX Page 0 Own Bit (0xB800_9030)

Reg.bit	Name	Description	Mode	Default
31	P0OWN_RX	RX Page 0 Own Bit. 0: Page 0 owned by CPU 1: Page 0 owned by IIS controller	RW	0B

10.4.17. RX Page 1 Own Bit

Table 79. RX Page 1 Own Bit (0xB800_9034)

Reg,bit	Name	Description	Mode	Default
31	P1OWN_RX	RX Page 1 Own Bit. 0: Page 1 owned by CPU 1: Page 1 owned by IIS controller	RW	0B

10.4.18. RX Page 2 Own Bit

Table 80. RX Page 2 Own Bit (0xB800_9038)

Reg.bit	Name	Description	Mode	Default
31	P2OWN_RX	RX Page 2 Own Bit. 0: Page 2 owned by CPU 1: Page 2 owned by IIS controller	RW	0B

10.4.19. RX Page 3 Own Bit

Table 81. RX Page 3 Own Bit (0xB800_903C)

Reg.bit	Name	Description	Mode	Default
31	P3OWN_RX	RX Page 3 Own Bit. 0: Page 3 owned by CPU 1: Page 3 owned by IIS controller	RW	0B

11. PCI Express Bus Interface

The RTL8197D is compliant with PCI Express Base Specification Revision 1.1, and run at a 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8197D supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal and link reversal are also supported. The RTL8197D provides two ports on the PCI Express Host interface.

11.1. PCI Express Transmitter

The RTL8197D PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of two extra bits. The data code groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

11.2. PCI Express Receiver

The RTL8197D PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL8197D internal Ethernet MAC to be transmitted onto the Ethernet media.

11.3. PCI Express Host Mode

11.3.1. PCI-E Port 0 Host Mode Extended Register Address Mapping

Table 82. PCI-E Host Mode Extended Register Address Mapping (Base: 0xB8B0_1000)

Offset	Size (byte)	Name	Description
0x00	4	MDIO	PCI-E Port 0 MDIO Control Register.
0x04	4	INTSTR	PCI-E Port 0 Interrupt Status Register.
0x08	4	PWRCR	PCI-E Port 0 Power Control Register.
0x0C	4	IPCFG	PCI-E Port 0 IP Configuration Register.
0x10	4	BISTFAIL	PCI-E Port 0 BIST Fail Check Register.

Table 83. PCI-E Port 1Host Mode Extended Register Address Mapping (Base: 0xB8B2_1000)

Offset	Size (byte)	Name	Description
0x00	4	MDIO	PCI-E Port 1 MDIO Control Register.
0x04	4	INTSTR	PCI-E Port 1 Interrupt Status Register.
0x08	4	PWRCR	PCI-E Port 1 Power Control Register.
0x0C	4	IPCFG	PCI-E Port 1 IP Configuration Register.
0x10	4	BISTFAIL	PCI-E Port 1 BIST Fail Check Register.

11.3.2. PCI-E MDIO Register

Table 84. PCI-E MDIO Register (0xB8B0_1000/0xB8B2_1000)

Reg.bit	Name	Description	Mode	Default
31:16	Mdio_data	MDIO Read Data or Write Data.	RW	0H
15:13	Mdip_phyaddr	MDIO PHY Page Addr[2:0].	RW	-
12:8	Mdio_regaddr	MDIO Register Address[4:0].	RW	0H
7	-	Reversed.	-	-
6:5	Mdio_st	MDIO Status[1:0] for Debug Checking.	R	00B
4	Mdio rdy	MDIO Ready for Debug Checking.	R	0
3:2	Mdio_rate	MDIO Clock Rate. 2'b00: lx clock/32 2'b01: lx clock/16 2'b10: lx clock/8 2'b11: lx clock/4	RW	00B
1	Mdio_srst	MDIO Soft Reset. 1: Active 0: No active	RW	0B
0	Mdio_rdwr	MDIO Read/Write Command. 1: Write 0: Read	RW	0B

11.3.3. PCI-E Interrupt Status Register

Table 85. PCI-E Interrupt Status Register (0xB8B0_1004/0xB8B2_1004)

Reg.bit	Name	Description	Mode	Default
3	INTD	Interrupt D Status Register (Level Active).	R	0B
2	INTC	Interrupt C Status Register (Level Active).	R	0B
1	INTB	Interrupt A Status Register (Level Active).	R	0B
0	INTA	Interrupt A Status Register (Level Active).	R	0B

11.3.4. PCI-E Power Control Register

Table 86. PCI-E Power Control Register (0xB8B0_1008/0xB8B2_1008)

Reg.bit	Name	Description	Mode	Default
10	App_unlock_msg	Generate Unlock Message (One Pulse).	RW	0B
9	Apps_pm_xmt_turnoff	Generate PME Turn Off Message.	RW	0B
8	App_init_rst	Application User Trigger Hot Reset (Must Keep Asserted for 2ms Minimum).	RW	0B
7	Phy_srst_n	PCI-E PHY Software Reset. 0: Active 1: Not active *Note: This bit is for internal PCI-E PHY reset and its default value is 'high'. Software must set this bit to 'low' for longer than 100ms to generate a REFCLK for the RTL8197D and any external device.*	RW	1B
6	P1_clk_req_en	Auxiliary State Enable. 1: Enable 0: Disable	RW	0B
5	Low_power enable	Enter Lower Power State Enable. 1: Enable 0: Disable	RW	0B
4	Sys_aux_pwr_det	System Detect Auxiliary Power Stable. 1: Stable 0: Unstable	RW	0B
3	App_ready_enter_l23	Application User Ready Enter L23 when Device in D3 Hot/Cold.	RW	0B
2	App_req_exit_l1	Application Request Exit L1 State.	RW	0B
1	App_req_enter_l1	Application Request Enter L1 State.	RW	0B
0	App_ltssm_en	Application User LTSSM Enable. 1: Enable LTSSM 0: Hold LTSSM in initial state	RW	1B

11.3.5. PCI-E IP Configuration Register

Table 87. PCI-E IP Configuration Register (0xB8B0_100C/0xB8B2_100C)

Reg.bit	Name	Description	Mode	Default
15:8	Bus_num	Target Bus Number (265 Types).	RW	0H
7:3	Dev_num	Target Device Number (32 Types).	RW	0H

Reg.bit	Name	Description	Mode	Default
2:0	Fun_num	Target Function Number (8 Types).	RW	0H

11.3.6. PCI-E SRAM BIST Check Register

Table 88. PCI-E SRAM BIST Check Register (0xB8B0_1010/0xB8B2_1010)

Reg.bit	Name	Description	Mode	Default
31:0	Bist_fail_chk	SRAM BIST Fail Check.	R	0H

12. USB 2.0 Host Interface

The RTL8197D provides a USB host controller that complies with the USB 2.0 Enhanced Host Controller Interface (EHCI) and the USB 1.x Open Host Controller Interface (OHCI) specifications.

12.1. Open Host Controller Interface (OHCI) Operational Registers

12.1.1. Open Host Controller Interface (OHCI) Operational Registers

Table 89. OHCI Operational Register Set (0xB802_0000)

Offset	Size (byte)	Name	Description
0x00	4	HcRevision	Host Controller Revision.
0x04	4	HcControl	Host Controller Register.
0x08	4	HcCommandStatus	Host Controller Command Status.
0x0C	4	HcInterruptStatus	Host Controller Interrupt Status.
0x10	4	HcInterruptEnable	Host Controller Interrupt Enable.
0x14	4	HcInterruptDisable	Host Controller Interrupt Disable.
0x18	4	HcHCCA	Host Controller Communication Area.
0x1C	4	HcPeriodCurrentED	Current Isochronous or Interrupt Endpoint Descriptor.
0x20	4	HcControlHeadED	First Endpoint Descriptor of the Control List.
0x24	4	HcControlCurrentED	Current Endpoint Descriptor of the Control List.
0x28	4	HcBulkHeadED	First Endpoint Descriptor of the Bulk List.
0x2C	4	HcBulkCurrentED	Current Endpoint of the Bulk List.
0x30	4	HcDoneHead	Last Completed Transfer Descriptor.
0x34	4	HcFmInterval	Time Interval in a Frame.
0x38	4	HcFmRemaining	Time Remaining in the Current Frame.
0x3C	4	HcFmNumber	Current Frame Number.
0x40	4	HcPeriodicStart	This Determines the Earliest Time HC Should Start Processing the Periodic List.
0x44	4	HcLSThreshold	This Determines whether to Commit to the Transfer of a Maximum 8-Byte LS Packet before EOF.
0x48	4	HcRhDescriptorA	The First Register of Two Describing the Characteristics of the Root Hub.
0x4C	4	HcRhDescriptorB	The Second Register of Two Describing the Characteristics of the Root Hub.
0x50	4	HcRhStatus	The Hub Status and Hub Status Change Register.
0x54	4	HcRhPortStatus[1]	This Controls and Reports Port Events on a Per-Port Basis.
0x58	4	HcRhPortStatus[2]	This Controls and Reports Port Events on a Per-Port Basis.

12.1.2. Control and Status Partition

12.1.2.1 HcRevision Register

Table 90. HcRevision Register (0xB802_0000)

Reg.bit	Name	Description	Mode	Default
31:8	-	Reserved.	-	-
7:0	REV	Complies with OpenHCI Release: 1.0a.	R	00010000B

12.1.2.2 HcControl Register

Table 91. HcControl Register (0xB802_0004)

Reg.bit	Name	Description	Mode	Default
31:11	-	Reserved.	-	-
10	RWE	RemoteWakeupEnable. This bit is used by HCD to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupts.	RW	0B
9	RWC	RemoteWakeupConnected. This bit indicates whether HC supports remote wakeup signaling. If remote wakeup is supported and used by the system it is the responsibility of system firmware to set this bit during the POST. HC clears the bit upon a hardware reset but does not alter it upon a software reset. Remote wakeup signaling of the host system is host-bus-specific and is not described in this datasheet.	RW	0B
8	IR	InterruptRouting. This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If clear, all interrupts are routed to the normal host bus interrupt mechanism. If set, interrupts are routed to the System Management Interrupt. HCD clears this bit upon a hardware reset, but it does not alter this bit upon a software reset. HCD uses this bit as a tag to indicate the ownership of HC.	RW	0B
7:6	HCFS	HostControllerFunctionalState for USB. 00b: UsbReset 01b: UsbResume 10b: UsbOperational 11b: UsbSuspend A transition to UsbOperational from another state causes SOF generation to begin 1ms later. HCD may determine whether HC has begun sending SOFs by reading the StartofFrame field of HcInterruptStatus. This field may be changed by HC only when in the UsbSuspend state. HC may move from the UsbSuspend state to the UsbResume state after detecting the resume signaling from a downstream port. HC enters UsbSuspend after a software reset, whereas it enters UsbReset after a hardware reset. The latter also resets the Root Hub and asserts subsequent reset signaling to downstream ports.	RW	00B

Reg.bit	Name	Description	Mode	Default
5	BLE	BulkListEnable. This bit is set to enable the processing of the Bulk list in the next Frame. If cleared by HCD, processing of the Bulk list does not occur after the next SOF. HC checks this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcBulkCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcBulkCurrentED before re-enabling processing of the list.	RW	0B
4	CLE	ControlListEnable. This bit is set to enable the processing of the Control list in the next Frame. If cleared by HCD, processing of the Control list does not occur after the next SOF. HC must check this bit whenever it determines to process the list. When disabled, HCD may modify the list. If HcControlCurrentED is pointing to an ED to be removed, HCD must advance the pointer by updating HcControlCurrentED before re-enabling processing of the list.	RW	0B
3	IE	IsochronousEnable. This bit is used by HCD to enable/disable processing of isochronous EDs. While processing the periodic list in a Frame, HC checks the status of this bit when it finds an Isochronous ED (F=1). If set (enabled), HC continues processing the EDs. If cleared (disabled), HC halts processing of the periodic list (which now contains only isochronous EDs) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame).	RW	0B
2	PLE	PeriodicListEnable. This bit is set to enable the processing of the periodic list in the next Frame. If cleared by HCD, processing of the periodic list does not occur after the next SOF. HC must check this bit before it starts processing the list.	RW	0B
1:0	CBSR	ControlBulkServiceRatio. This specifies the service ratio between Control and Bulk EDs. Before processing any of the non-periodic lists, HC must compare the ratio specified with its internal count on how many nonempty Control EDs have been processed, in determining whether to continue serving another Control ED or switching to Bulk EDs. The internal count will be retained when crossing the frame boundary. In case of reset, HCD is responsible for restoring this value.	RW	00B

CBSR	No. of Control EDs Over Bulk EDs Served
0	1:1
1	2:1
2	3:1
3	4:1

12.1.2.3 HcCommandStatus Register

Table 92. HcCommandStatus Register (0xB802_0008)

Reg.bit	Name	Description	Mode	Default
31:18	-	Reserved.	-	-
17:16	SOC	SchedulingOverrunCount. These bits are incremented on each scheduling overrun error. It is initialized to 00b and wraps around at 11b. This will be incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus has already been set. This is used by HCD to monitor any persistent scheduling problems.	R	00B
15:4	-	Reserved.	-	-
3	OCR	OwnershipChangeRequest. This bit is set by an OS HCD to request a change of control of the HC. When set HC will set the OwnershipChange field in HcInterruptStatus. After the changeover, this bit is cleared and remains so until the next request from OS HCD.	RW	0B
2	BLF	BulkListFilled. This bit is used to indicate whether there are any TDs on the Bulk list. It is set by HCD whenever it adds a TD to an ED in the Bulk list. When HC begins to process the head of the Bulk list, it checks BF. As long as BulkListFilled is 0, HC will not start processing the Bulk list. If BulkListFilled is 1, HC will start processing the Bulk list and will set BF to 0. If HC finds a TD on the list, then HC will set BulkListFilled to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if HCD does not set BulkListFilled, then BulkListFilled will still be 0 when HC completes processing the Bulk list and Bulk list processing will stop.	RW	0B
1	CLF	ControlListFilled. This bit is used to indicate whether there are any TDs on the Control list. It is set by HCD whenever it adds a TD to an ED in the Control list. When HC begins to process the head of the Control list, it checks CLF. As long as ControlListFilled is 0, HC will not start processing the Control list. If CF is 1, HC will start processing the Control list and will set ControlListFilled to 0. If HC finds a TD on the list, then HC will set ControlListFilled to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if the HCD does not set ControlListFilled, then ControlListFilled will still be 0 when HC completes processing the Control list and Control list processing will stop.	RW	0B
0	HCR	HostControllerReset. This bit is set by HCD to initiate a software reset of HC. Regardless of the functional state of HC, it moves to the UsbSuspend state in which most of the operational registers are reset except those stated otherwise; e.g., the InterruptRouting field of HcControl, and no Host bus accesses are allowed. This bit is cleared by HC upon the completion of the reset operation. The reset operation must be completed within 10µs. This bit, when set, should not cause a reset to the Root Hub and no subsequent reset signaling should be asserted to its downstream ports.	RW	0B

12.1.2.4 HcInterruptStatus Register

Table 93. HcInterruptStatus Register (0xB802_000C)

Reg.bit	Name	Description	Mode	Default
31	-	Reserved.	-	-
30	OC	OwnershipChange. This bit is set by HC when HCD sets the OwnershipChangeRequest field in HcCommandStatus. This event, when unmasked, will always generate an System Management Interrupt (SMI) immediately. This bit is tied to 0b when the SMI pin is not implemented.	RW	0B
29:7	-	Reserved.	-	-
6	RHSC	RootHubStatusChange. This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus[NumberofDownstreamPort] has changed.	RW	0B
5	FNO	FrameNumberOverflow. This bit is set when the MSb of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated.	RW	0B
4	UE	UnrecoverableError. This bit is set when HC detects a system error not related to USB. HC should not proceed with any processing nor signaling before the system error has been corrected. HCD clears this bit after HC has been reset.	RW	0B
3	RD	ResumeDetected. This bit is set when HC detects that a device on the USB is asserting resume signaling. It is the transition from no resume signaling to resume signaling causing this bit to be set. This bit is not set when HCD sets the UsbResume state.	RW	0B
2	SF	StartofFrame. This bit is set by HC at each start of a frame and after the update of HccaFrameNumber. HC also generates a SOF token at the same time.	RW	0B
1	WDH	WritebackDoneHead. This bit is set immediately after HC has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. HCD should only clear this bit after it has saved the content of HccaDoneHead.	RW	0B
0	SO	SchedulingOverrun. This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun will also cause the SchedulingOverrunCount of HcCommandStatus to be incremented.	RW	0B

12.1.2.5 HcInterruptEnable Register

Table 94. HcInterruptEnable Register (0xB802_0010)

Reg.bit	Name	Description	Mode	Default
31	MIE	Master Interrupt Enable A '0' written to this field is ignored by HC. A '1' written to this field enables interrupt generation due to events specified in the other bits of this register. This is used by HCD as a Master Interrupt Enable.	RW	0B
30	OC	Ownership Change. 0: Ignore 1: Enable interrupt generation due to Ownership Change	RW	0B
29:7	-	Reserved.	-	-
6	RHSC	RootHubStatusChange. 0: Ignore 1: Enable interrupt generation due to Root Hub Status Change	RW	0B
5	FNO	FrameNumberOverflow. 0: Ignore 1: Enable interrupt generation due to Frame Number Overflow	RW	0B
4	UE	UnrecoverableError. 0: Ignore 1: Enable interrupt generation due to Unrecoverable Error	RW	0B
3	RD	ResumeDetect. 0: Ignore 1: Enable interrupt generation due to Resume Detect	RW	0B
2	SF	StartofFrame. 0: Ignore 1: Enable interrupt generation due to Start of Frame	RW	0B
1	WDH	WritebackDoneHead. 0: Ignore 1: Enable interrupt generation due to WritebackDoneHead	RW	0B
0	SO	SchedulingOverrun. 0: Ignore 1: Enable interrupt generation due to Scheduling Overrun	RW	0B

12.1.2.6 HcInterruptDisable Register

Table 95. HcInterruptDisable Register (0xB802_0014)

Reg.bit	Name	Description	Mode	Default
31	MIE	Master Interrupt Enable A '0' written to this field is ignored by HC. A '1' written to this field disables interrupt generation due to events specified in the other bits of this register. This field is set after a hardware or software reset.	RW	0B
30	OC	OwnershipChange. 0: Ignore 1: Disable interrupt generation due to Ownership Change	RW	0B
29:7	-	Reserved.	-	-
6	RHS	RootHubStatusChange. 0: Ignore 1: Disable interrupt generation due to Root Hub Status Change	RW	0B
5	FNO	FrameNumberOverflow. 0: Ignore 1: Disable interrupt generation due to Frame Number Overflow	RW	0B
4	UE	UnrecoverableError. 0: Ignore 1: Disable interrupt generation due to Unrecoverable Error	RW	0B
3	RD	ResumeDetect. 0: Ignore 1: Disable interrupt generation due to Resume Detect	RW	0B
2	SF	StartofFrame. 0: Ignore 1: Disable interrupt generation due to Start of Frame	RW	0B
1	WDH	WritebackDoneHead. 0: Ignore 1: Disable interrupt generation due to WritebackDoneHead	RW	0B
0	SO	SchedulingOverrun. 0: Ignore 1: Disable interrupt generation due to Scheduling Overrun	RW	0B

12.1.3. Memory Pointer Partition

12.1.3.1 HcHCCA Register

Table 96. HcHCCA Register (0xB802_0018)

Reg.bit	Name	Description	Mode	Default
31:8	HCCA	This is the Base Address of the Host Controller Communication Area.	RW	0B
7:0	0	For 256-Byte Boundary.	R	0B

12.1.3.2 HcPeriodCurrentED Register

Table 97. HcPeriodCurrentED Register (0xB802_001C)

Reg.bit	Name	Description	Mode	Default
31:4	PCED	PeriodCurrentED. This is used by HC to point to the head of one of the Periodic lists which will be processed in the current Frame. The content of this register is updated by HC after a periodic ED has been processed. HCD may read the content in determining which ED is currently being processed at the time of reading.	R	0B
3:0	0	For 16-Byte Boundary.	R	0B

12.1.3.3 HcControlHeadED Register

Table 98. HcControlHeadED Register (0xB802_0020)

Reg.bit	Name	Description	Mode	Default
31:4	CHED	ControlHeadED. HC traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of HC.	RW	0B
3:0	0	For 16-Byte Boundary.	R	0B

12.1.3.4 HcControlCurrentED Register

Table 99. HcControlCurrentED Register (0xB802_0024)

Reg.bit	Name	Description	Mode	Default
31:4	CCED	ControlCurrentED. This pointer is advanced to the next ED after serving the present one. HC will continue processing the list from where it left off in the last frame. When it reaches the end of the Control list, HC checks the ControlListFilled in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. HCD is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, HCD only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.	RW	0B
3:0	0	For 16-Byte Boundary.	R	0B

12.1.3.5 HcBulkHeadED Register

Table 100. HcBulkHeadED Register (0xB802_0028)

Reg.bit	Name	Description	Mode	Default
31:4	BHED	BulkHeadED. HC traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of HC.	RW	0B
3:0	0	For 16-Byte Boundary.	R	0B

12.1.3.6 HcBulkCurrentED Register

Table 101. HcBulkCurrentED Register (0xB802_002C)

Reg.bit	Name	Description	Mode	Default
31:4	BCED	BulkCurrentED. This is advanced to the next ED after the HC has served the present one. HC continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, HC checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. HCD is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.	RW	0B
3:0	0	For 16-Byte Boundary.	R	0B

12.1.3.7 HcDoneHead Register

Table 102. HcDoneHead Register (0xB802_0030)

Reg.bit	Name	Description	Mode	Default
31:4	DH	DoneHead. When a TD is completed, HC writes the content of HcDoneHead to the NextTD field of the TD. HC then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever HC writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.cleared. When set, the HCD only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.	R	0B
3:0	0	For 16-Byte Boundary.	R	0B

12.1.4. Frame Counter Partition

12.1.4.1 HcFmInterval Register

Table 103. HcFmInterval Register (0xB802_0034)

Reg.bit	Name	Description	Mode	Default
31	FIT	FrameIntervalToggle. HCD toggles this bit whenever it loads a new value to FrameInterval.	RW	0B
30:16	FSMPS	FSLargestDataPacket. This field specifies a value which is loaded into the Largest Data Packet Counter at the beginning of each frame. The counter value represents the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The field value is calculated by the HCD.	RW	0B
15:14	-	Reserved.	-	-
13:0	FI	FrameInterval. This specifies the interval between two consecutive SOFs in bit times. The nominal value is set to 11,999. HCD should store the current value of this field before resetting HC. By setting the HostControllerReset field of HcCommandStatus as this will cause the HC to reset this field to its nominal value. HCD may choose to restore the stored value upon the completion of the Reset sequence.	RW	2EDFH

12.1.4.2 HcFmRemaining Register

Table 104. HcFmRemaining Register (0xB802_0038)

Reg.bit	Name	Description	Mode	Default
31	FRT	FrameRemainingToggle. This bit is loaded from the FrameIntervalToggle field of HcFmInterval whenever FrameRemaining reaches 0. This bit is used by HCD for the synchronization between FrameInterval and FrameRemaining.	R	0B
30:14	-	Reserved.	-	-
13:0	FR	FrameRemaining. This counter is decremented at each bit time. When it reaches zero, it is reset by loading the FrameInterval value specified in HcFmInterval at the next bit time boundary. When entering the UsbOperational state, HC re-loads the content with the FrameInterval of HcFmInterval and uses the updated value from the next SOF.	R	0B

12.1.4.3 HcFmNumber Register

Table 105. HcFmNumber Register (0xB802_003C)

Reg.bit	Name	Description	Mode	Default
31:16	-	Reserved.	-	-
15:0	FN	FrameNumber. This is incremented when HcFmRemaining is re-loaded. It will be rolled over to 0h after ffffh. When entering the UsbOperational state, this will be incremented automatically. The content will be written to HCCA after HC has incremented the FrameNumber at each frame boundary and sent a SOF but before HC reads the first ED in that Frame. After writing to HCCA, HC will set the StartofFrame in HcInterruptStatus.	R	0B

12.1.4.4 HcPeriodicStart Register

Table 106. HcPeriodicStart Register (0xB802_0040)

Reg.bit	Name	Description	Mode	Default
31:14	-	Reserved.	-	-
13:0	PS	PeriodicStart. After a hardware reset, this field is cleared. This is then set by HCD during the HC initialization. The value is calculated roughly as 10% off from HcFmInterval. A typical value will be 3E67h. When HcFmRemaining reaches the value specified, processing of the periodic lists will have priority over Control/Bulk processing. HC will therefore start processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.	RW	0B

12.1.4.5 HcLSThreshold Register

Table 107. HcLSThreshold Register (0xB802_0044)

Reg.bit	Name	Description	Mode	Default
31:12	-	Reserved.	-	-
11:0	LST	LSThreshold. This field contains a value that is compared to the FrameRemaining field prior to initiating a Low Speed transaction. The transaction is started only if FrameRemaining ≥ this field. The value is calculated by HCD with consideration for transmission and setup overhead.	RW	0628H

12.1.5. Root Hub Partition

12.1.5.1 HcRhDescriptorA Register

Table 108. HcRhDescriptorA Register (0xB802_0048)

Reg.bit	Name	Description	Mode	Default
31:24	POTPGT	PowerOnToPowerGoodTime. This byte specifies the duration HCD has to wait before accessing a powered-on port of the Root Hub. It is implementation-specific. The unit of time is 2ms. The duration is calculated as POTPGT*2ms.	RW	02H
23:11	-	Reserved.	-	-
10	DT	DeviceType. This bit specifies that the Root Hub is not a compound device. The Root Hub is not permitted to be a compound device. This field should always read/write to 0.	R	0B
9	PSM	PowerSwitchingMode. This bit is used to specify how the power switching of the Root Hub ports is controlled. It is implementation-specific. This field is only valid if the NoPowerSwitching field is cleared. 0: All ports are powered at the same time 1: Each port is powered individually This mode allows port power to be controlled by either the global switch or per-port switching. If the PortPowerControlMask bit is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).	RW	1B

Reg.bit	Name	Description	Mode	Default
8	NPS	NoPowerSwitching. These bits are used to specify whether power switching is supported or ports are always powered. It is implementation-specific. When this bit is cleared, the PowerSwitchingMode specifies global or per-port switching. 0: Ports are power switched 1: Ports are always powered on when the HC is powered on	RW	0B
7:0	NDP	NumberDownstreamPorts. These bits specify the number of downstream ports supported by the Root Hub. It is implementation-specific. The minimum number of ports is 1. The maximum number of ports supported by OpenHCI is 15.	R	01H

12.1.5.2 HcRhDescriptorB Register

Table 109. HcRhDescriptorB Register (0xB802_004C)

Reg.bit	Name	Description	Mode	Default
31:16	PPCM	PortPowerControlMask. Each bit indicates if a port is affected by a global power control command when PowerSwitchingMode is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PowerSwitchingMode=0), this field is not valid. Bit 0: Reserved Bit 1: Ganged-power mask on Port #1 Bit 2: Ganged-power mask on Port #2 ... Bit15: Ganged-power mask on Port #15	RW	0H
15:0	DR	DeviceRemovable. Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. Bit 0: Reserved Bit 1: Device attached to Port #1 Bit 2: Device attached to Port #2 ... Bit15: Device attached to Port #15	RW	0H

12.1.5.3 HcRhStatus Register

Table 110. HcRhStatus Register (0xB802_0050)

Reg.bit	Name	Description	Mode	Default
31	CRWE	(Write) ClearRemoteWakeupEnable. Writing a '1' clears DeviceRemoveWakeupEnable. Writing a '0' has no effect.	W	-
30:17	-	Reserved.	-	-
16	LPSC	(Read) LocalPowerStatusChange. The Root Hub does not support the local power status feature thus, this bit is always read as '0'. (Write) SetGlobalPower. In global power mode (PowerSwitchingMode=0). This bit is written to '1' to turn on power to all ports (clear PortPowerStatus). In per-port power mode, it sets PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.	RW	0B
15	DRWE	(Read) DeviceRemoteWakeupEnable. This bit enables a ConnectStatusChange bit as a resume event, causing a UsbSuspend to UsbResume state transition and setting the ResumeDetected interrupt. 0: ConnectStatusChange is not a remote wakeup event 1: ConnectStatusChange is a remote wakeup event (Write) SetRemoteWakeupEnable. Writing a '1' sets DeviceRemoveWakeupEnable. Writing a '0' has no effect.	RW	0B
14:1	-	Reserved.	-	-
0	LPS	(Read) LocalPowerStatus. The Root Hub does not support the local power status feature; thus, this bit is always read as '0'. (Write) ClearGlobalPower. In global power mode (PowerSwitchingMode=0), this bit is written to '1' to turn off power to all ports (clear PortPowerStatus). In per-port power mode, it clears PortPowerStatus only on ports whose PortPowerControlMask bit is not set. Writing a '0' has no effect.	RW	0B

12.1.5.4 HcRhPortStatus[1:NDP] Register

Table 111. HcRhStatus Register (0xB802_0054, 0058)

Reg.bit	Name	Description	Mode	Default
31:21	-	Reserved.	-	-
20	PRSC	PortResetStatusChange. This bit is set at the end of the 10-ms port reset signal. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: Port reset is not complete 1: Port reset is complete	RW	0B
19	-	Reserved.	-	-
18	PSSC	PortSuspendStatusChange. This bit is set when the full resume sequence has been completed. This sequence includes the 20 seconds resume pulse, LS EOP, and 3-ms resychronization delay. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. This bit is also cleared when ResetStatusChange is set. 0: Resume is not completed 1: Resume completed	RW	0B
17	PESC	PortEnableStatusChange. This bit is set when hardware events cause the PortEnableStatus bit to be cleared. Changes from HCD writes do not set this bit. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. 0: No change in PortEnableStatus 1: Change in PortEnableStatus	RW	0B
16	CSC	ConnectStatusChange. This bit is set whenever a connect or disconnect event occurs. The HCD writes a '1' to clear this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared when a SetPortReset, SetPortEnable, or SetPortSuspend write occurs, this bit is set to force the driver to re-evaluate the connection status since these writes should not occur if the port is disconnected. 0: No change in CurrentConnectStatus 1: Change in CurrentConnectStatus *Note: If the DeviceRemovable[NDP] bit is set, this bit is set only after a Root Hub reset to inform the system that the device is attached.*	RW	0B
15:10	-	Reserved.	-	-
9	LSDA	(Read) LowSpeedDeviceAttached. This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When clear, a Full Speed device is attached to this port. This field is valid only when the CurrentConnectStatus is set. 0: Full speed device attached 1: Low speed device attached (Write) ClearPortPower. The HCD clears the PortPowerStatus bit by writing a '1' to this bit. Writing a '0' has no effect.	RW	-

Reg.bit	Name	Description	Mode	Default
8	PPS	(Read) PortPowerStatus. This bit reflects the port's power status, regardless of the type of power switching implemented. HCD sets this bit by writing SetPortPower or SetGlobalPower. HCD clears this bit by writing ClearPortPower or ClearGlobalPower. Which power control switches are enabled is determined by PowerSwitchingMode and PortPortControlMask[NDP]. In global switching mode (PowerSwitchingMode=0), only Set/ClearGlobalPower controls this bit. In per-port power switching (PowerSwitchingMode=1), if the PortPowerControlMask[NDP] bit for the port is set, only Set/ClearPortPower commands are enabled. If the mask is not set, only Set/ClearGlobalPower commands are enabled. When port power is disabled, CurrentConnectStatus, PortEnableStatus, PortSuspendStatus, and PortResetStatus should be reset. 0: Port power is off 1: Port power is on (Write) SetPortPower. The HCD writes a '1' to set the PortPowerStatus bit. Writing a '0' has no effect. *Note: This bit is always reads '1b' if power switching is not supported.*	RW	0B
7:5	-	Reserved.	-	-
4	PRS	(Read) PortResetStatus. When this bit is set by a write to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PortResetStatusChange is set. This bit cannot be set if CurrentConnectStatus is cleared. 0: Port reset signal is not active 1: Port reset signal is active (Write) SetPortReset. The HCD sets the port reset signaling by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortResetStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to reset a disconnected port.	RW	0B
3	-	Reserved.	-	-
2	PSS	(Read) PortSuspendStatus. This bit indicates the port is suspended or in the resume sequence. It is set by a SetSuspendState write and cleared when PortSuspendStatusChange is set at the end of the resume interval. This bit cannot be set if CurrentConnectStatus is cleared. This bit is also cleared when PortResetStatusChange is set at the end of the port reset or when the HC is placed in the UsbResume state. If an upstream resume is in progress, it should propagate to the HC. 0: Port is not suspended 1: Port is suspended (Write) SetPortSuspend. The HCD sets the PortSuspendStatus bit by writing a '1' to this bit. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortSuspendStatus; instead it sets ConnectStatusChange. This informs the driver that it attempted to suspend a disconnected port.	RW	0B

Reg.bit	Name	Description	Mode	Default
1	PES	(Read) PortEnableStatus. This bit indicates whether the port is enabled or disabled. The Root Hub may clear this bit when a disconnect event, switched-off power, or operational bus error such as babble is detected. This change also causes PortEnabledStatusChange to be set. HCD sets this bit by writing SetPortEnable and clears it by writing ClearPortEnable. This bit cannot be set when CurrentConnectStatus is cleared. This bit is also set, if not already, at the completion of a port reset when ResetStatusChange is set or port suspend when SuspendStatusChange is set. 0: Port is disabled 1: Port is enabled (Write) SetPortEnable. The HCD sets PortEnableStatus by writing a '1'. Writing a '0' has no effect. If CurrentConnectStatus is cleared, this write does not set PortEnableStatus, but instead sets ConnectStatusChange. This informs the driver that it attempted to enable a disconnected port.	RW	0B
0	CCS	(Read) CurrentConnectStatus. This bit reflects the current state of the downstream port. 0: No device connected 1: Device connected (Write) ClearPortEnable. The HCD writes a '1' to this bit to clear the PortEnableStatus bit. Writing a '0' has no effect. The CurrentConnectStatus is not affected by a write. *Note: This bit is always read '1b' when the attached device is not removable (DeviceRemoveable[NDP]).*	RW	0B

12.2. EHCI Capability and Operational Registers

12.2.1. Capability Registers

12.2.1.1 EHCI Capability Register Set

Table 112. EHCI Capability Register Set (0xB802_1000)

Offset	Size (byte)	Name	Description
0x00	1	CAPLENGTH	Capability Register Length.
0x01	1	-	Reserved.
0x02	2	HCIVERSION	Interface Version Number.
0x04	4	HCSPARAMS	Structural Parameters.
0x08	4	HCCPARAMS	Capability Parameters.
0x0C	8	HCSP-PORTROUTE	Companion Port Route Description.

12.2.1.2 Capability Register Length

Table 113. CAPLENGTH Register (0xB802_1000)

Reg.bit	Name	Description	Mode	Default
7:0	CAPLENGTH	This Register is Used to Find the Beginning of the Operational Registers by Adding to the Capability Registers Address.	R	10H

12.2.1.3 Host Controller Interface Version Number

Table 114. HCIVERSION Register (0xB802_1002)

Reg.bit	Name	Description	Mode	Default
15:0	HCIVERSION	The EHCI Revision Number Supported by This Host Controller.	R	100H

12.2.1.4 Host Controller Structural Parameters

Table 115. HCSPARAMS Register (0xB802_1004)

Reg.bit	Name	Description	Mode	Default
31:16	-	Reserved.	-	-
15:12	Number of Companion Controllers (N_CC)	This field indicates the number of companion USB 1.1 HC (OHCI) associated with USB 2.0 HC (EHCI).	R	1H
11:8	Number of Port per Companion Controller (N_PCC)	This field indicates the number of ports supported by a companion USB 1.1 HC (OHCI).	R	1H
7	Port Routing Rules	This field indicates the routing rules implementation for how all ports are mapped to companion USB 1.1 HC (OHCI).	R	0B
6:5	-	Reserved.	-	-
4	Port Power Control (PPC)	This field indicates whether the HC implementation supports Port Power Control.	R	1B
3:0	N_PORTS	This field indicates the number of physical downstream ports implemented on this host controller.	R	1H

12.2.1.5 Host Controller Capability Parameters

Table 116. HCCPARAMS Register (0xB802_1008)

Reg.bit	Name	Description	Mode	Default
31:16	-	Reserved.	-	-
15:8	EHCI Extended Capabilities Pointer (EECP)	This Field Indicates the Existence of a Capabilities List.	R	A0H
7:4	Isochronous Scheduling Threshold	This field indicates the current position of the executing host controller, where software can reliably update the isochronous schedule.	R	1H
3	-	Reserved.	-	-
2	Asynchronous Schedule Park Capability	When this bit is set to 1, the host controller supports the park feature for high-speed queue heads in Asynchronous Schedule.	R	0B
1	Programmable Frame List Flag	0b: The system software must use a frame list length of 1024 elements with this HC 1b: The system software can specify a smaller frame list via USBCMD register FrameList Size field	R	0B
0	64-bit Addressing Capability	This Field Indicates the Addressing Range Capability. 0b: Data structures using 32-bit address memory pointers 1b: Data structures using 64-bit address memory pointers	R	0B

12.2.1.6 Companion Port Route

Table 117. HCSP-PORTROUTE Register (0xB802_100C)

Reg.bit	Name	Description	Mode	Default
63:0	HCSP-PORTROUTE	This Field is a 15-Element Array (Each Element 4 Bits). Each array location corresponds one-to-one with a physical port. The value of each element indicates to which of the companion host controllers this port is routed.	R	-

12.2.2. Operational Registers

Table 118. EHCI Operational Register Set (Base: 0xB802_1010)

Offset	Size (byte)	Name	Description
0x00	4	USBCMD	USB Command.
0x04	4	USBSTS	USB Status.
0x08	4	USBINTR	USB Interrupt Enable.
0x0c	4	FRINDEX	USB Frame Index.
0x10	4	CTRLDSSEGMENT	4G Segment Selector.
0x14	4	PERIODICLISTBASE	Frame List Base Address.
0x18	4	ASYNCLISTADDR	Next Asynchronous List Address.
0x1C~0x3F	36	-	Reserved.
0x40	4	CONFIGFLAG	Configures Flag Register.
0x44	4	PORTSC (1-N_PORTS)	Port Status/Control.

12.2.2.1 USB Command

Table 119. USBCMD Register (0xB802_1010)

Reg.bit	Name	Description	Mode	Default
31:24	-	Reserved.	-	-
23:16	Interrupt Threshold Control	This field is used by software to select the maximum rate at which the host controller will issue interrupts. **Value** / **Maximum Interrupt Interval** 00h: Reserved. 01h: 1 Micro-Frame. 02h: 2 Micro-Frames. 04h: 4 Micro-Frames. 08h: 8 Micro-Frames (Default, 1ms). 10h: 16 Micro-Frames. 20h: 32 Micro-Frames. 40h: 64 Micro-Frames.	RW	08H
15:12	-	Reserved.	-	-
11	Asynchronous Schedule Park Mode Enable	When This Bit is One, Park Mode is Enabled.	-	1B
10	-	Reserved.	-	-
9:8	Asynchronous Schedule Park Mode Count	A Counter of the Number of Successive Transactions.	RW	11B
7	Light Host Controller Reset	This bit allows the driver to reset the EHCI controller without affecting the state of the ports or the relationship to the companion host controller.	RW	0B
6	Interrupt on Async Advance Doorbell	This bit is used as a doorbell by software to tell the HC to issue an interrupt the next time it advances the asynchronous schedule.	RW	0B
5	Asynchronous Schedule Enable	0b: Do not process the Asynchronous Schedule 1b: Use the ASYNCLISTADDR register to access the Asynchronous Schedule	RW	0B
4	Periodic Schedule Enable	0b: Do not process the Periodic Schedule 1b: Use the PERIODICLISTBASE register to access the Periodic Schedule	RW	0B
3:2	Frame List Size	This Field Specifies the Size of the Frame List. 00b: 1024 elements (4096 bytes) 01b: 512 elements (2048 bytes) 10b: 256 element (1024 bytes) 11b: Reserved	-	0B

Reg.bit	Name	Description	Mode	Default
1	Host Controller Reset	This Control Bit is Used by SW to Reset the Host Controller. The effects of this on Root Hub registers are similar to a Chip Hardware Reset. When software writes a one to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. This bit is set to zero by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing a zero to this register. Software should not set this bit to a 1 when the HCHalted bit in the USBSTS register is a zero. Attempting to reset an actively running host controller will result in undefined behavior.	RW	0B
0	Run/Stop	This Bit is Set to a 1 when the Host Controller Continues Execution. When this bit is set to 0, the Host Controller completes the current and any actively pipelined transactions on the USB and then halts.	RW	0B

12.2.2.2 USB Status Register

Table 120. USBSTS Register (0xB802_1014)

Reg.bit	Name	Description	Mode	Default
31:16	-	Reserved.	-	-
15	Asynchronous Schedule Status	If this bit is a zero then the status of Asynchronous Schedule is disabled. If this bit is a one then the status of Asynchronous Schedule is enabled.	R	0B
14	Periodic Schedule Status	If this bit is a zero then the status of Periodic Schedule is disabled. If this bit is a one then the status of Periodic Schedule is enabled.	R	0B
13	Reclamation	If this bit is a one, indicates an empty asynchronous schedule is able to reclaim.	R	0B
12	HCHalted	When the Run/Stop bit is a one, this bit is set to zero; else set this bit to one.	R	1B
11:6	-	Reserved.	-	-
5	Interrupt on Async Advance	System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing a one to the Interrupt on the Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source.	RW	0B
4	Host System Error	The Host Controller sets this bit to 1 when a serious error occurs during a host system access involving the Host Controller module. When this error occurs, the Host Controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs.	RW	0B

Reg.bit	Name	Description	Mode	Default
3	Frame List Rollover	The Host Controller sets this bit to a 1 when the Frame List Index rolls over from its maximum value to zero. The exact value at which the rollover occurs depends on the frame list size. For example, if the frame list size (as programmed in the Frame List Size field of the USBCMD register) is 1024, the Frame Index Register rolls over every time FRINDEX[13] toggles. Similarly, if the size is 512, the Host Controller sets this bit to a 1 every time FRINDEX[12] toggles.	RW	0B
2	Port Change Detect	The Host Controller sets this bit to a 1 when any port for which the Port Owner bit is set to 0 has a change bit transition from a 0 to a 1 or a Force Port Resume bit transition from a zero to a 1 as a result of a J-K transition detected on a suspended port. This bit will also be set as a result of the Connect Status Change being set to a 1 after the system software has relinquished ownership of a connected port by writing a 1 to a port's Port Owner bit. This bit is allowed to be maintained in Auxiliary power. Alternatively, it is also acceptable that on a D3 to D0 transition of the EHCI HC device, this bit is loaded with the OR of all of the PORTSC change bits (including: Force port resume, enable/disable change and connect status change).	RW	0B
1	USB Error Interrupt (USBERRINT)	The Host Controller sets this bit to 1 when completion of a USB transaction results in an error condition (e.g., error counter underflow). If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and USBINT bit are set.	RW	0B
0	USB Interrupt (USBINT)	The Host Controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The Host Controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes).	RW	0B

12.2.2.3 USB Interrupt Enable Register

Table 121. USBINTR Register (0xB802_1018)

Reg.bit	Name	Description	Mode	Default
31:6	-	Reserved.	-	-
5	Interrupt on Async Advance Enable	When this bit is a one, and the Interrupt on Async Advance bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.	RW	0B
4	Host System Error Enable	When this bit is a one, and the Host System Error Status bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.	RW	0B
3	Frame List Rollover Enable	When this bit is a one, and the Frame List Rollover bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.	RW	0B
2	Port Change Interrupt Enable	When this bit is a one, and the Port Change Detect bit in the USBSTS register is a one, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.	RW	0B
1	USB Error Interrupt Enable	When this bit is a one, and the USBERRINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.	RW	0B
0	USB Interrupt Enable	When this bit is a one, and the USBINT bit in the USBSTS register is a one, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.	RW	0B

12.2.2.4 Frame Index Register

Table 122. FRINDEX Register (0xB802_101C)

Reg.bit	Name	Description	Mode	Default
31:14	-	Reserved.	-	-
13:0	Frame Index	The value in this register increments at the end of each time frame (e.g., micro-frame). Bits [N:3] are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following illustrates values of N based on the value of the Frame List Size field in the USBCMD register.	RW	0H

USBCMD[Frame List Size]	Elements	N
00b	(1024)	12
01b	(512)	11
10b	(256)	10
11b	Reserved	-

12.2.2.5 Control Data Structure Segment Register

Table 123. CTRLDSSEGMENT Register (0xB802_1020)

Reg.bit	Name	Description	Mode	Default
31:0	CTRLDSSEGMENT	This 32-bit register corresponds to the most significant address bits [63:32] for all EHCI data structures. If the 64-bit Addressing Capability field in HCCPARAMS is a zero, then this register is not used. This register is concatenated with the link pointer from either the PERIODICLISTBASE, ASYNCLISTADDR, or any control data structure link field to construct a 64-bit address.	RW	0H

12.2.2.6 Periodic Frame List Base Address Register

Table 124. PERIODICLISTBASE Register (0xB802_1024)

Reg.bit	Name	Description	Mode	Default
31:12	Base Address (Low)	This 32-bit register contains the beginning address of the Periodic Frame List in the system memory.	RW	-
11:0	-	Reserved.	-	-

12.2.2.7 Current Asynchronous List Address Register

Table 125. ASYNCLISTBASE Register (0xB802_1024)

Reg.bit	Name	Description	Mode	Default
31:5	Link Pointer Low (LPL)	This 32-bit register contains the address of the next asynchronous queue head to be executed.	RW	-
4:0	-	Reserved.	-	-

12.2.2.8 Configure Flag Register

Table 126. CONFIGFLAG Register (0xB802_1050)

Reg.bit	Name	Description	Mode	Default
31:1	-	Reserved.	-	-
0	Configure Flag (CF)	Host software sets this bit as the last action in its process of configuring the Host Controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below. 0b Port routing control logic default-routes each port to an implementation dependent classic host controller. 1b Port routing control logic default-routes all ports to this host controller.	RW	0B

12.2.2.9 Port Status and Control Register

Table 127. PORTSC Register (0xB802_1054)

Reg.bit	Name	Description	Mode	Default
31:22	-	Reserved.	-	-
21	Wake on Disconnect Enable (WKDSCNNT_E)	Writing this bit to a 1 enables the port to be sensitive to device disconnects as wake-up events. This field is zero if Port Power is zero.	RW	0B
20	Wake on Connect Enable (WKCNNT_E)	Writing this bit to a 1 enables the port to be sensitive to device connects as wake-up events. This field is zero if Port Power is zero.	RW	0B
19:16	Port Test Control	When this field is zero, the port is NOT operating in a test mode. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. The encoding of the test mode bits are (0110b~1111b are reserved): **Bits** / **Test Mode** 0000b: Test Mode Not Enabled. 0001b: Test J_STATE. 0010b: Test K_STATE. 0011b: Test SE0_NAK. 0100b: Test Packet. 0101b: Test FORCE_ENABLE.	RW	0H
15:14	Port Indicator Control	Writing to these bits has no effect if the P_INDICATOR bit in the HCSPARAMS register is a zero. If the P_INDICATOR bit is a one, then the bit encodings are: **Bit Value** / **Meaning** 00b: Port Indicators are Off. 01b: Amber. 10b: Green. 11b: Undefined.	RW	0H
13	Port Owner	This bit unconditionally goes to a 0b when the Configured bit in the CONFIGFLAG register makes a 0b to 1b transition. This bit unconditionally goes to 1b whenever the Configured bit is zero. System software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes a one to this bit when the attached device is not a high-speed device. A one in this bit means that a companion host controller owns and controls the port.	RW	1B

<table>
<tr><th>Reg.bit</th><th>Name</th><th>Description</th><th>Mode</th><th>Default</th></tr>
<tr><td>12</td><td>Port Power (PP)</td><td>The function of this bit depends on the value of the Port Power Control (PPC) field in the HCSPARAMS register.
The behavior is as follows:
<table>
<tr><th>PPC</th><th>PP</th><th>Operation</th></tr>
<tr><td>0b</td><td>1b</td><td>RO-Host controller does not have port power control switches. Each port is hard-wired to power.</td></tr>
<tr><td>1b</td><td>1b/0b</td><td>RW-Host controller has port power control switches. This bit represents the current setting of the switch (0: OFF; 1: ON). When power is not available on a port (i.e., PP equals a 0), the port is nonfunctional and will not report attaches, detaches, etc.</td></tr>
</table></td><td>-</td><td>-</td></tr>
<tr><td>11:10</td><td>Line Status</td><td>These bits reflect the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. These bits are used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when the port enable bit is zero and the current connect status bit is set to a 1.
The encoding of the bits are:
<table>
<tr><th>Bits[11:10]</th><th>USB State</th><th>Interpretation</th></tr>
<tr><td>00b</td><td>SE0</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>10b</td><td>J-state</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
<tr><td>01b</td><td>K-state</td><td>Low-speed device, release ownership of port.</td></tr>
<tr><td>11b</td><td>Undefined</td><td>Not Low-speed device, perform EHCI reset.</td></tr>
</table>
This value of this field is undefined if Port Power is zero.</td><td>R</td><td>0B</td></tr>
<tr><td>9</td><td>-</td><td>Reserved.</td><td>-</td><td>-</td></tr>
</table>

<table>
<tr><th>Reg.bit</th><th>Name</th><th>Description</th><th>Mode</th><th>Default</th></tr>
<tr><td>8</td><td>Port Reset</td><td>1: Port is in Reset
0: Port is not in Reset
When software writes a one to this bit (from a zero), the bus reset sequence as defined in the USB Specification Revision 2.0 is started. Software writes a zero to this bit to terminate the bus reset sequence. Software must keep this bit at ‘1’ long enough to ensure the reset sequence, as specified in the USB Specification Revision 2.0, completes.
Note 1: When software writes this bit to a 1, it must also write a zero to the Port Enable bit.
Note 2: When software writes a zero to this bit there may be a delay before the bit status changes to a zero. The bit status will not read as a zero until after the reset has completed. If the port is in high-speed mode after reset is complete, the host controller will automatically enable this port (e.g., set the Port Enable bit to a 1). A host controller must terminate the reset and stabilize the state of the port within 2 milliseconds of software transitioning this bit from a one to a zero.
For example: If the port detects that the attached device is high-speed during reset, then the host controller must have the port in the enabled state within 2ms of software writing this bit to a zero.
The HCHalted bit in the USBSTS register should be a zero before software attempts to use this bit. The host controller may hold Port Reset asserted to a 1 when the HCHalted bit is a one. This field is zero if Port Power is zero.</td><td>RW</td><td>0B</td></tr>
<tr><td>7</td><td>Suspend</td><td>1: Port in suspend state
0: Port not in suspend state Port Enabled Bit and Suspend bit of this register define the port states as follows
<table>
<tr><th>Bits [Port Enabled, Suspend]</th><th>Port State</th></tr>
<tr><td>0X</td><td>Disable</td></tr>
<tr><td>10</td><td>Enable</td></tr>
<tr><td>11</td><td>Suspend</td></tr>
</table>
When in suspend state, downstream propagation of data is blocked on this port, except for port reset. The blocking occurs at the end of the current transaction, if a transaction was in progress when this bit was written to 1. In the suspend state, the port is sensitive to resume detection. Note that the bit status does not change until the port is suspended and that there may be a delay in suspending a port if there is a transaction currently in progress on the USB.
A write of zero to this bit is ignored by the host controller. The host controller will unconditionally set this bit to a zero when:
• Software sets the Force Port Resume bit to a zero (from a one)
• Software sets the Port Reset bit to a 1 (from a zero)
If host software sets this bit to a 1 when the port is not enabled (i.e., Port enabled bit is a zero) the results are undefined. This field is zero if Port Power is zero.</td><td>RW</td><td>0B</td></tr>
</table>

Reg.bit	Name	Description	Mode	Default
6	Force Port Resume	1: Resume detected/driven on port 0: No resume (K-state) detected/driven on port This functionality defined for manipulating this bit depends on the value of the Suspend bit. For example, if the port is not suspended (Suspend and Enabled bits are a 1) and software transitions this bit to a 1, then the effects on the bus are undefined. Software sets this bit to a 1 to drive resume signaling. The Host Controller sets this bit to a 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to a 1 because a J-to-K transition is detected, the Port Change Detect bit in the USBSTS register is also set to a 1. If software sets this bit to a 1, the host controller must not set the Port Change Detect bit. Note that when the EHCI controller owns the port, the resume sequence follows the defined sequence documented in the USB Specification Revision 2.0. The resume signaling (full-speed 'K') is driven on the port as long as this bit remains a 1. Software must appropriately time the Resume and set this bit to a zero when the appropriate amount of time has elapsed. Writing a zero (from 1) causes the port to return to high-speed mode (forcing the bus below the port into a high-speed idle). This bit will remain a 1 until the port has switched to high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to a zero. This field is zero if Port Power is zero.	RW	0B
5:4	-	Reserved.	-	-
3	Port Enable/Disable Change	1: Port enabled/disabled status has changed 0: No change For the root hub, this bit gets set to a 1 only when a port is disabled due to the appropriate conditions existing at the EOF2 point (for the definition of a Port Error, see Chapter 11 of the USB Specification). Software clears this bit by writing a 1 to it. This field is zero if Port Power is zero.	RW	0B
2	Port Enabled/Disabled	1: Enable 0: Disable Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing a one to this field. The host controller will only set this bit to a 1 when the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by host software. Note that the bit status does not change until the port state actually changes. There may be a delay in disabling or enabling a port due to other host controller and bus events. When the port is disabled (0b) downstream propagation of data is blocked on this port, except for reset. This field is zero if Port Power is zero.	RW	0B

Reg.bit	Name	Description	Mode	Default
1	Connect Status Change	1: Change in Current Connect Status 0: No change Indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if system software has not cleared an existing connect status change. For example, the insertion status changes twice before system software has cleared the changed condition, hub hardware will be 'setting' an already-set bit (i.e., the bit will remain set). Software sets this bit to 0 by writing a 1 to it. This field is zero if Port Power is zero.	RW	0B
0	Current Connect Status	1: Device is present on port 0: No device is present This value reflects the current state of the port, and may not correspond directly to the event that caused the Connect Status Change bit (Bit 1) to be set. This field is zero if Port Power is zero.	R	0B

13. Switch Core Control

13.1. Global Port Control Register

13.1.1. Global Port Control Register Address Mapping (0xBB80-4000)

The RTL8197D provides an MDC/MDIO (Management Data Clock/Management Data Input/Output) interface to access external PHYs. As the MDC/MDIO interface is relatively slow, the access is divided into command and status registers.

Table 128. Global Port Control Register Address Mapping (0xBB80-4000)

Offset	Size (byte)	Name	Description
04	4	MDCIOCR	MDC/MDIO Command Register.
08	4	MDCIOSR	MDC/MDIO Status Register.

13.1.2. Global MDC/MDIO Command Register (0xBB80-4004)

Table 129. MDC/MDIO Command Register (0xBB80-4004)

Reg.bit	Name	Description	Mode	Default
31	COMMAND	MDC/MDIO Command Type. 0: Read Access 1: Write Access *Note: The procedure to access the external PHY via the MDC/MDIO interface is as follows:* *1. Define the PHY address (PHYADD), register address (REGADD)* *2. Define the write data content for write command (WRDATA)* *3. Identify the command type (COMMAND)* *4. Get the command execution status (STATUS) and read data content (RDATA)*	RW	0B
30:29	-	Reserved.	-	-
28:24	PHYADD[4:0]	PHY Address of MDC/MDIO Command.	RW	00000B
23:21	-	Reserved.	-	-
20:16	REGADD[4:0]	Register Address of MDC/MDIO Command.	RW	00000B
15:0	WRDATA[15:0]	Write Data of MDC/MDIO Command.	RW	0000H

13.1.3. Global MDC/MDIO Status Register (0xBB80-4008)

Table 130. MDC/MDIO Status Register (0xBB80-4008)

Reg.bit	Name	Description	Mode	Default
31	STATUS	MDC/MDIO Command in Process Status. 0: Process done 1: In progress	R	0000B
30:16	-	Reserved.	-	-
15:0	RDATA	Read Data Result of MDC/MDIO Command.	R	0B

13.1.4. Global Frame Filtering Control Register Address Mapping (0xBB80-4000)

Table 131. Frame Filtering Control Register Address Mapping (0xBB80-4000)

Offset	Size (byte)	Name	Description
44	4	BSCR	Broadcast Storm Control Register.

13.1.5. Global Broadcast Storm Control Register (0xBB80-4044)

Per-port broadcast storm traffic utilization is a global parameter that is defined by BCSC_CNT[14:0] in the Broadcast Storm Control Register (0xBB80-4044). Broadcast storm control can be enabled/disabled on a per-port basis, and the broadcast traffic definition is user configurable.

Table 132. Broadcast Storm Control Register (0xBB80-4044)

Reg.bit	Name	Description	Mode	Default
31:15	-	Reserved.	-	-
14:0	BCSC_CNT[14:0]	Broadcast Storm Control Rate Configuration. Defines the per-port-based broadcast storm control valid accumulated byte count in each default time interval 25ms/2.5ms/0.25ms for 10M/100M/1000M (the time interval will auto update for different port link speeds). For BCSC_BCNT[14:0] value = N The % max rate = N/30360*100%.	RW	0

Note: When Broadcast Storm Control is enabled, every 25ms, each port will limit the max incoming byte counts of broadcast, multicast, or unknown-unicast packets to 3 counts maximum. Other excessive packets within the duration time will be dropped.

13.2. Per-Port Configuration Register

All five switch port interfaces of the RTL8197D can be individually configured as either 10/100Mbps UTP or RGMII/GMII/MII via Port Interface Control registers.

The port ability properties, e.g., auto negotiation, port speed, duplex, flow control, can be configured via the Per-Port Configuration Register.

Table 133. Per-Port Configuration Register Address Mapping (Base: 0xBB80_4100)

Offset	Size (byte)	Name	Description
00	4	PITCR	Port Interface Type Control Register
04	4	PCRP0	Port Configuration Register of Port 0
08	4	PCRP1	Port Configuration Register of Port 1
0C	4	PCRP2	Port Configuration Register of Port 2
10	4	PCRP3	Port Configuration Register of Port 3
14	4	PCRP4	Port Configuration Register of Port 4
18	4	PCRP5	Port Configuration Register of Port 5 (GMII)
1C	4	PCRP6	Port Configuration Register of Port 6 (Ext. P0)
20	4	PCRP7	Port Configuration Register of Port 7 (Ext. P1)
24	4	PCRP8	Port Configuration Register of Port 8 (Ext. P2)
28	4	PSRP0	Port Status Register of Port 0
2C	4	PSRP1	Port Status Register of Port 1
30	4	PSRP2	Port Status Register of Port 2
34	4	PSRP3	Port Status Register of Port 3
38	4	PSRP4	Port Status Register of Port 4
3C	4	PSRP5	Port Status Register of Port 5
40	4	PSRP6	Port Status Register of Port 6
44	4	PSRP7	Port Status Register of Port 7
48	4	PSRP8	Port Status Register of Port 8
4C	4	-	Reserved
50	4	P5GMIICR	Port-5 GMII Configuration Register

13.2.1. Port Interface Type Control Register

Table 134. Port Interface Type Control Register (0xBB80_4100)

Reg.bit	Name	Description	Mode	Default
31:12	-	Reserved.	-	-
11:10	Port5_TypeCfg[1:0]	Port 5 Interface Type Configuration. 00: GMII/RGMII/MII interface 01: Reserved 1x: Reserved	RW	00B
9:8	Port4_TypeCfg[1:0]	Port 4 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
7:6	Port3_TypeCfg[1:0]	Port 3 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
5:4	Port2_TypeCfg[1:0]	Port 2 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
3:2	Port1_TypeCfg[1:0]	Port 1 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
1:0	Port0_TypeCfg[1:0]	Port 0 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B

13.2.2. Port Configuration Register of Port N [N= 0~4] (0x)

Table 135. Port Configuration Register of Port N [N= 0~8] (0x)

Reg.bit	Name	Description	Mode	Default
31	ByPassTCRC	1: Do not recalculate CRC for CRC error frame 0: Recalculate CRC for CRC error frame	RW	0B
30:26	ExtPHYID[4:0]	External PHY ID Assign for PHY MII Register Polling Addressing. Identifies the external PHY ID for MDC/MDIO polling addressing. Only valid for ports 0~5.	RW	Port0~5=0x0~5 Port6=0x6
25	EnForceMode	Enable Port Property (Link/Speed/Duplex/Flow Control) to be Set by Force Mode. 0: Disable (enable Auto-Negotiation) In this mode, the port link/speed/duplex /flow control setting is based on the MDC/MDIO polling result. 1: Enable (Force Mode) (Disable Auto-Negotiation) In this mode, the port speed/duplex /flow control setting is set by the force mode control bits in this register. Note that the method of determining the link status depends on the PollinkStatus setting. In this mode MDC/MDIO polling of the external PHY access for this Gigabit port will be disabled.	RW	0
24	PollinkStatus	Polling PHY Link Status {EnForceMode, PollinkStatus}. 00, 01: Enable Auto-Negotiation 10: ForceMode. Disables Auto-Negotiation (this mode should be set for MAC-to-MAC connection) 11: ForceMode with polling link status. Disables Auto-Negotiation but polls the PHY's link status	RW	0
23	ForceLink	Force Link-Up or Link-Down Setting. Available Only If {EnForceMode, PollinkStatus}=10. 0: Force link down 1: Force link up *Note: If {EnForceMode, PollinkStatus}=11, the link status information is derived from PHY register 1 via the ASIC's auto-polling mechanism.*	RW	0

Reg.bit	Name	Description	Mode	Default
22:18	FrcAbi_AnAbi_sel	If EnForceMode=1, FrcAbi_AnAbi_sel is used to indicate the force mode operation for MAC or PHY mode operations. FrcAbi_AnAbi_sel[0]: ForceDuplex 1: Force FULL duplex 0: Force HALF duplex FrcAbi_AnAbi_sel[2:1]: ForceSpeed 00: Force 10Mbps 01: Force 100Mbps (default setting for port#5 NFBI-PHY-mode specification) 10: Reserved 11: Reserved FrcAbi_AnAbi_sel[4:3]: Reserved. If EnForceMode=0, FrcAbi_AnAbi_sel is used to indicate Auto-Negotiation advertising ability. FrcAbi_AnAbi_sel[0]: 10Mbps Half-duplex FrcAbi_AnAbi_sel[1]: 10Mbps Full-duplex FrcAbi_AnAbi_sel[2]: 100Mbps Half-duplex FrcAbi_AnAbi_sel[3]: 100Mbps Full-duplex FrcAbi_AnAbi_sel[4]: Reserved	RW	5'b11111 for port#0~4 5'b11011 only for port#5
17:16	PauseFlowControl[1:0] (ADVERTISE_ PAUSEABY)	If EnForceMode=1, this register controls PAUSE flow control. 0: Enable TX pause ability 1: Enable RX pause ability If EnForceMode=0, the PHY advertises PAUSE flow control. 0: PAUSE operation for full duplex links 1: Asymmetric PAUSE operation for full duplex links	RW	2'b11
15:12	-	Reserved	-	-
11:9	BCSC_Types[2:0]	Broadcast Storm Control Packet Types Selection. When Broadcast storm control is enabled, the control packet types can be selected. Bit[0]: Enable control for broadcast packets Bit[1]: Enable control for multicast packet Bit[2]: Reserved 0: Disable 1: Enable When Bit[3:0] are set as '000', the port's broadcast storm function is disabled.	RW	0B
8	EnBCSC	Enable Broadcast Storm Control. 0: Disable 1: Enable When enabled, the broadcast storm control rate and control packet type should be defined in the broadcast storm control register.	RW	0B

<table>
<tr><th>Reg.bit</th><th>Name</th><th>Description</th><th>Mode</th><th>Default</th></tr>
<tr><td>7</td><td>EnLoopBack</td><td>Enable MAC – PHY Interface for MII Loopback.
Enable internal and external loopback. Sets the MAC as an internal loopback, and sets the PHY side as an external loopback.
0: Disable 1: Enable</td><td>RW</td><td>0B</td></tr>
<tr><td>6</td><td>DisBKP</td><td>Per-Port Disable Backpressure Function for Half Duplex Mode.
1: Disable 0: Enable</td><td>RW</td><td>0B</td></tr>
<tr><td>5:4</td><td>STP_PortST[1:0]</td><td>Spanning Tree Protocol Port State Control.
00: Disable State 01: Blocking/Listen State
10: Learning State 11: Forwarding State
<table>
<tr><th>802.1d Port State</th><th>Pass Received Non-BPDU Frames</th><th>Pass Received BPDU Frames</th><th>Learning Station Location Into Address Database</th></tr>
<tr><td>Disabled</td><td>No</td><td>No</td><td>No</td></tr>
<tr><td>Blocking</td><td>No</td><td>Yes</td><td>No</td></tr>
<tr><td>Listening</td><td>No</td><td>Yes</td><td>No</td></tr>
<tr><td>Learning</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>Forwarding</td><td>Yes</td><td>Yes</td><td>Yes</td></tr>
</table></td><td>RW</td><td>11</td></tr>
<tr><td>3</td><td>MAC S/W Reset</td><td>MAC S/W Reset supports a method to reset the MAC by software. It can reset the circuit in the RXC and TXC domain via an active-low signal. To reset the MAC, software should write a 1 following the writing of a 0 .
0: Reset state
1: Normal state</td><td>RW</td><td>1</td></tr>
<tr><td>2:1</td><td>AcptMaxLen[1:0]</td><td>Configures the Maximum Acceptable Packet Length Supported.
This control is valid only when jumbo packet accept is disabled on a port.
00: 1536 bytes
01: 1552 bytes
10: 9k bytes (jumbo packet: 9216 bytes)
11: 16k~14 bytes (jumbo packet: 16370 bytes)</td><td>RW</td><td>00B</td></tr>
<tr><td>0</td><td>EnablePHYIf</td><td>Enable PHY Interface.
The bit controls the MAC vs. PHY interface, irrelevant as to whether the port interface is UTP or GMII/RGMII/MII modes.
0: Disable
When disabled, the PHY interface will be isolated from the MAC. Packets will not be transmitted or received to/from the PHY to/from the MAC interface (internal GMII/MII interface).
1: Enable</td><td>RW</td><td>0B</td></tr>
</table>

13.2.3. Port Status Register of Port N (N=0~4) (0x)

Table 136. Port Status Register of Port N (N=0~8) (0x)

Reg.bit	Name	Description	Mode	Default
31:14	-	Reserved.	-	-
13:12	EEE Status[1:0]	Port Link Status. In NWay Mode, the status is the compare result of PHY local and remote ability. In Force mode, the status is the configuration result of the force mode configuration registers. Bit 1: Reserved Bit 0: 100M EEE ability	R	0
11:9	-	Reserved.	-	-
8	LinkDownEventFlag	Port Link Down Event Detection Monitor Flag 0: Idle 1: Link Down event detected When the Port link status changes from link-up to link-down, the flag bit will be latched as '1' until read to clear and updated to the new status.	Latch, RW	0
7:0	PortStatus[7:0]	Port Link Status In an NWay Mode port, the status is the compared result of local and remote PHY abilities. In Force mode, the status is the configuration result of the force mode configuration registers. This report is valid for UTP or GMII/RGMII Interface mode. Bit 7: NWay Enable (link by auto-negotiation) Bit 6: RX PAUSE ability Bit 5: TX PAUSE ability Bit 4: LinkUp Bit 3: Duplex Bit 2: Reserved Bit [1:0] LinkSpeed[1:0] LinkSpeed[1:0]: 00: 10M 01: 100M 10: Reserved 11: Reserved	R	0

13.2.4. Port0 GMII/RGMII Configuration Register (0x BB80414C)

Table 137. Port0 GMII/RGMII Configuration Register (0x BB80414C)

Reg.bit	Name	Description	Mode	Default
31:25	-	Reserved.	-	-
24:23	CFG_GMAC[1:0]	GMII Port MAC Interface Mode Configuration. The register default reflects the HW power on strapping value of H/W pin 'CFG_GMAC[1:0]'. The register can be updated by the host. CFG_GMAC[1:0]= 00: RGMII mode 01: GMII/MII MAC mode 10: GMII/MII PHY mode 11: Reserved	RW	0
22:18	-	Reserved.	-	-
17:8	MediaTypeAddr[9:0]	MediaTypeStatus Register Bit Location Address. MediaTypeAddr[9:5]=RegA[4:0] (REG address) MediaTypeAddr[4:0]=BitLA[4:0] (Bit location address) *Note: This bit is valid and be used only when the Gigabit PHY MII Register 15 report both 1000Base-T and 1000Base-X capability. This configuration bits direct RTL865xC to identify the correct link media type. The value is depend on the Gigabit PHY chip.*	RW	0x1B1D
7	FiberMTB_polarity	Fiber Media Type Defined Bit Polarity. To define the MediaTypeStatus Register bit definition. To tell the system whether 0=Fiber mode or 1=Fiber mode are defined in the register that MediaTypeAddr[9:0] addressed. If write 0, it means that 0=Fiber mode. If write 1, it means that 1=Fiber mode.	RW	0
6	Conf_done	Port5 Configuration is Done to Enable the Frame Reception and Transmission.	RW	0
5	-	Reserved.	-	-
4	GMII/RGMII TXC _PHASE	GMII/RGMII Output Timing Compensation Control. GMII Interface: 1: Invert the TXC 0: Same phase of GTXC RGMII Interface: 1: Delay TXC 2ns compared to TXD 0: TXC is the same phase as TXD	RW	0
3	-	Reserved.	-	-
2:0	GMII/RGMII _Rcomp[2:0]	GMII/RGMII Input Timing Compensation Control. Add internal input delay to RXC to implement the RXD setup time and hold time required spec at the input side. GMII Interface: GMII_Rcomp[2] ([1:0] are irrelevant) 0: 0ns 2: 4ns (use RXC negative edge) RGMII Interface: RGMII_Rcomp[2:0] 000: 0.0ns 001: 0.5ns 010: 1.0ns ….. 111: 3.5ns	RW	000

13.3. LED Control Register

13.3.1. LED Topology Operation

The RTL8197D support single and Bi-Color LED display. Table 138 illustrates all combinations of LED topologies.

Mixed mode LED display is supported. For example, developers might design some ports in single-color/type#0 and some in Bi-color/type# mode. Note that the topology (LedTopology) field should be the same in all six ports.

Table 138. Display Arrangement of Each SCAN LED Mode

Location	LED Mode=SCAN 0	LED Mode=SCAN 1	LED Mode=SCAN 2
LED#0	OFF=Link Down ON/Blink=Link/Act	OFF=Link Down Y=10/100M Link/Act *Note: Y=Yellow color (when signal LINKN[0:5] active low).*	OFF=Link Down Y=10M Link/Act *Note: Y=Yellow color (when signal LINKN[0:5] active low).*
LED#1	N/A	*N/A*	OFF=Link Down G=100M Link Act *Note: G=Green color (when signal LINKN[0:5] active high).*
USBLED	Link/Active	Link/Active	Link/Active
Topology Description	SCAN Mode Signal LED#0: Single-Color LED	SCAN Mode Signal LED#[0:1]: 2-Pin Dual-Color LED	SCAN Mode Signal LED#[0:1]: 2-Pin Dual-Color LED

Note: 'Y' indicates yellow color LED, and 'G' indicates green color LED (depends on the external LED component). 'ON' means this LED is turned on. 'OFF' means this LED is turned off. 'N/A' means this LED is not applicable. The CPU can still control this LED using the CPUCtrlPort/CPUCtrlMask register.

13.3.2. Scan Mode LED

The 2-pin dual-color LEDs are also supported in scan mode. The dual-color LEDs are controlled by the polarity of LINKN[n] and LEDSCAN. The LEDSCAN signal should change polarity to turn on the target LED, and turn off other LEDs in the target port's scan phase. When the port is IDLE, the LINKN[n] is driven low in its scan phase.

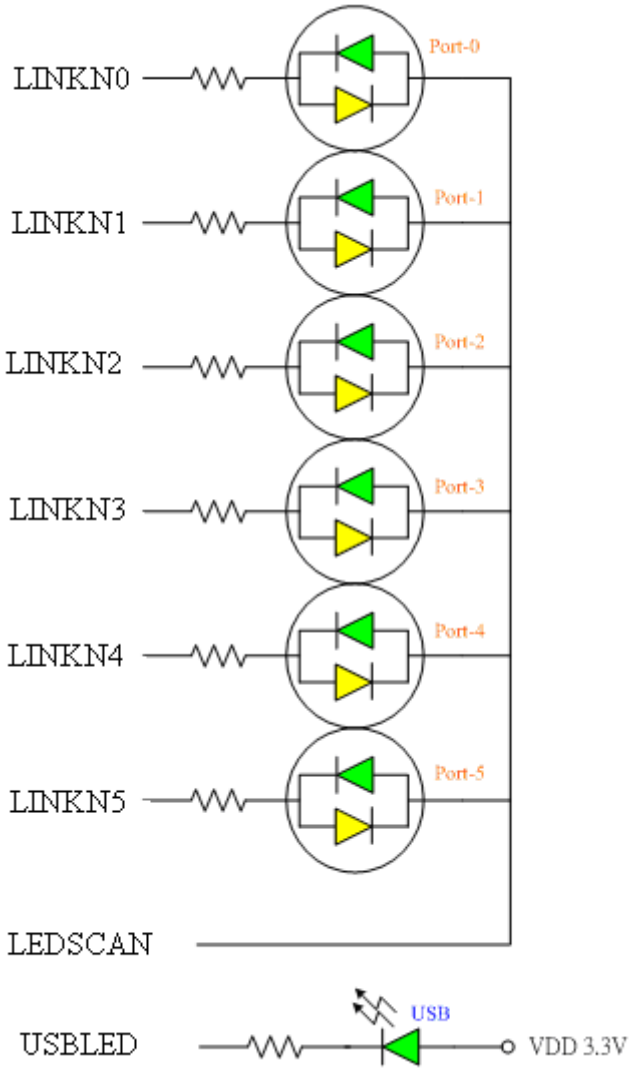


Figure 5. Dual-Color LED Interconnections

13.3.3. Bi-Color LED Timing Waveform

Figure 6 shows Port0 in 100M, Port1 in 10M, and Port2 in 10M. Other ports are link-down.

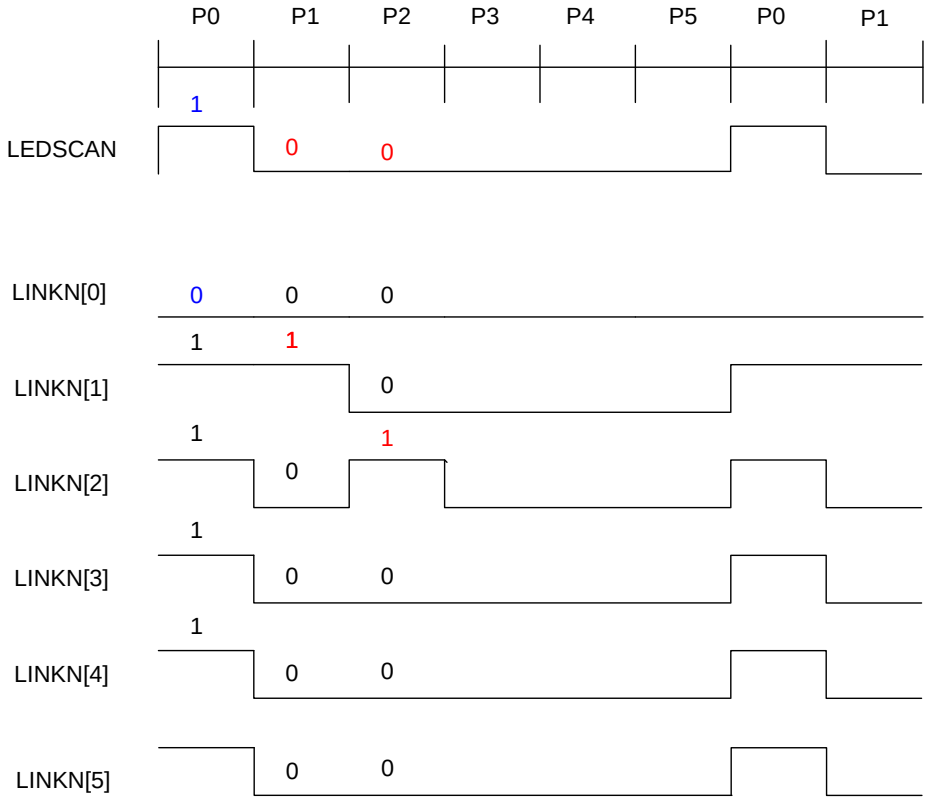


Figure 6. Bi-Color LED Timing Waveform

13.3.4. LED Control Register Address Mapping

Table 139. LED Control Register Address Mapping (Base: 0xBB80_4300)

Offset	Size (byte)	Name	Description
00	4	LEDCR0	LED Control Register 0.
04	4	LEDCR1	LED Control Register 1.
08	4	PSIR	Port State Information Register.
0C	4	LEDBCR	LED Blinking Control Register.
10	4	EEELCR	EEE LED Configuration Register.

13.3.5. LED Control Register#0

Table 140. LED Control Register#0 (0xBB80_4300)

Reg.bit	Name	Description	Mode	Default
31:21	-	Reserved.	-	-
20	LedTopology	LED Topology Selection. Selects the Scan mode of LED topology. 0: Scan mode Topology 1: Reserved	RW	0B
19:18	P0_LedDefSel[1:0]	Select P0 LED Display Mode Definition. Selects LED bit display definition. 00: Mode Scan 0 01: Mode Scan 1 10: Mode Scan 2 11: Reserved	RW	00B
17:16	P1_LedDefSel[1:0]	Select P1 LED Display Mode Definition.	RW	00B
15:14	P2_LedDefSel[1:0]	Select P2 LED Display Demo Definition.	RW	00B
13:12	P3_LedDefSel[1:0]	Select P3 LED Display Mode Definition.	RW	00B
11:10	P4_LedDefSel[1:0]	Select P4 LED Display Mode Definition.	RW	00B
9:8	P5_LedDefSel[1:0]	Select P5 LED Display Mode Definition.	RW	00B
7	DisLEDBlinking	Disable LED Initial Blinking. 0: Enable LED blinking 1: Disable LED blinking	RW	0B
6	BlinkTime	0: LED blink time: 40ms 1: LED blink time: 120ms	RW	0B
5	-	Reserved.	-	-
4:2	CPUCtrlMask[2:0]	CPU Control LED Masking. When any bit of CPUCtrlMask[2:0] is 0b, it means the corresponding LED is controlled by internal circuit. Conversely, when any bit of CPUCtrlMask[2:0] is 1b, the corresponding LED is controlled by CPU and the indication is controlled by CPUCtrlPort. 0: LED is controlled by internal circuit 1: LED is controlled by CPU CPUCtrlMask[2:0] are mapped to LED[2:0] respectively. The developer could make a specific LED display a designated mode through CPUCtrlPort without influencing other LEDs. The other LEDs will still operate with the LedTopology, EnBiColor, and LedType settings. This setting effects all six ports.	RW	000B
1	-	Reserved	-	-
0	CPUCtrlUSBMask	CPU Controls USBLED Masking. CPUCtrlUSBMask are mapped to USBLED respectively. 0: USBLED is controlled by internal circuit 1: USBLED is controlled by CPU	RW	0B

13.3.6. LED Control Register#1

Table 141. LED Control Register#1 (0xBB80_4304)

Reg.bit	Name	Description	Mode	Default
31:21	-	Reserved.	-	-
20:18	CPUCtrlPort0[2:0]	CPU Control Manner for Port0. CPUCtrlPort0[2:0] are mapped to LED[2:0] respectively. Only valid when CPUCtorlMask bit is 1b. 0: LED off 1: LED on	RW	000B
17:15	CPUCtrlPort1[2:0]	CPU Control Mode for Port1.	RW	000B
14:12	CPUCtrlPort2[2:0]	CPU Control Mode for Port2.	RW	000B
11:9	CPUCtrlPort3[2:0]	CPU Control Mode for Port3.	RW	000B
8:6	CPUCtrlPort4[2:0]	CPU Control Mode for Port4.	RW	000B
5:3	CPUCtrlPort5[2:0]	CPU Control Mode for Port5.	RW	000B
2	-	Reserved	-	-
1	CPUCtrlUSB0	USB Link/Active Indication. 0: LED Off 1: LED On	RW	0B
0	-	Reserved.	-	-

13.3.7. Port State Information Register#1

Table 142. Port State Information Register#1 (0xBB80_4308)

Reg.bit	Name	Description	Mode	Default
31:1	-	Reserved.	-	-
0	USBState	USB Port Link State Information. 0: Link Down 1: Link Up	R	0B

13.3.8. LED Blinking Control Register #1

Table 143. LED Blinking Control Register 1 (0xBB80_430C)

Reg.bit	Name	Description	Mode	Default
31:20	-	Reserved.	-	-
19:17	LEDBlinkP0[2:0]	CPU Controls the LED to Blink for Port0. LEDBlinkP0[2:0] are mapped to LED[2:0] respectively. Only valid when CPUCtorlMask bit is 1b. 0: Disable LED blinking 1: Enable LED blinking When LED blinking is enabled, no matter whether the designated LED is on or off, the designated LED will be forced to start blinking until the CPU disables it.	RW	000B
16:14	LEDBlinkP1[2:0]	CPU Controls the LED to Blink for Port1.	RW	000B
13:11	LEDBlinkP2[2:0]	CPU Controls the LED to Blink for Port2.	RW	000B

Reg.bit	Name	Description	Mode	Default
10:8	LEDBlinkP3[2:0]	CPU Controls the LED to Blink for Port3.	RW	000B
7:5	LEDBlinkP4[2:0]	CPU Controls the LED to Blink for Port4.	RW	000B
4:2	LEDBlinkP5[2:0]	CPU Controls the LED to Blink for Port5.	RW	000B
1	LEDBlinkUSB	CPU Controls the USBLED to Blink for USB. 0: Disable USBLED blinking 1: Enable USBLED blinking When enable LED blinking is active, and the current LED is ON or OFF, the LED will be forced to start blinking active until the user disables it.	RW	0B
0	-	Reserved.	-	-

13.3.9. EEE LED Configuration Register

Table 144. EEE LED Configuration Register (0xBB80_4310)

Reg.bit	Name	Description	Mode	Default
31:22	-	Reserved.	-	-
21:16	EEE-LPI-LED_test[5:0]	Emulate PHY Entering LPI States for LED Test (Only in FPGA). Each bit maps to an individual port (from port#0~5). In normal operation this field must be kept to the default value (0).	RW	0x0
15:11	LPI_SBTOFF[4:0]	LPI Slow Blink Timer OFF-Period Time (Unit=100ms). Default=2000ms	RW	0x14
10:6	LPI_SBTON[4:0]	LPI Slow Blink Timer ON-Period Time (Unit=100ms). Default=400ms.	RW	0x4
5:2	LPI_MT[3:0]	LPI Mask Off Time (Unit=100ms). To define the LED mask off time in a LPI LED state. Default=600ms.	RW	0x6
1	En10MLP	Enable 10Mbps port to show low power driving indication on LPI LED (same as the 10/100M port). 0: Disable 1: Enable	RW	0
0	enLPILED	Enable EEE LED Display Ability. 1: Enable 0: Disable *Note: When set to 1, the LPI LED display feature will remain disabled until after detecting a port has been 'link-up' for longer than 5 seconds.*	RW	0

14. Green Ethernet

14.1. Cable Length Power Saving

The RTL8197D provides link-on and dynamic detection of cable length, and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

14.2. Link-Down Power Saving

The RTL8197D implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. A port automatically enters link-down power saving mode ten seconds after the cable is disconnected from it. Once a port enters link-down power saving mode, it transmits normal link pulses on its TXOP/TXON pins and continues to monitor the RXIP/RXIN pins to detect incoming signals, which might be 100Base-TX MLT-3 idle pattern, 10Base-T link pulses, or Auto-Negotiation's FLP (Fast Link Pulse). After it detects an incoming signal, it wakes up from link-down power saving mode and operates in normal mode according to the result of the connection's auto-negotiation.

14.3. Energy Efficient Ethernet (EEE)

The RTL8197D supports IEEE 802.3az, also known as Energy Efficient Ethernet (EEE) in 100Base-TX in full duplex operation, and 10Base-T in full/half duplex mode. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

- For 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle.
- For 10Base-T, EEE defines a 10Mbps PHY (10Base-Te) with reduced transmit amplitude requirements. 10Base-Te is fully interoperable with 10Base-T PHYs over 100m of class-D (Cat-5) cable.

The RTL8197D MAC uses Low Power Idle signaling to indicate to the PHY and to the link partner that a break in the data stream is expected. Components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

15. Non-Flash Booting Interface (NFBI)

The RTL8197D total system acts in a PHY chip slave role for external host CPU master use.

- Designed with standard MDC/MDIO frame format
- PHY ID parser provided
- Supports forced RTL8197D CPU reset and enter into holding mode
- For burst read/write data; provides automatic increment of adjacent RAM address register

15.1. Block Diagram

The RTL8197D total system simulates a pure PHY function, and uses a standard MDC/MDIO interface to communicate with an external host CPU. The transfer data protocol is standard MDC/MDIO frame format.

On power up, the external host CPU needs to reset the RTL8197D, and then read the PHYID register to check that the MDC/MDIO bus is operating correctly. Next it checks that the 'NeedBootCode' bit=1, which means the NFBI (Non-Flash Booting Interface) module is ready.

If transferring the kernel into DRAM, first the DRAM configuration and timing register must be set to suitable values. After transferring all software code, the external host CPU uses the 'StartRunBootcode' bit to allow the RTL8197D to begin booting. After the 'kernel code' boot is completed, software will respond with the 'All Software Ready' bit to notify the external host CPU that the software is ready.

The following block shows the hardware pins between the external host CPU and RTL8197D system.

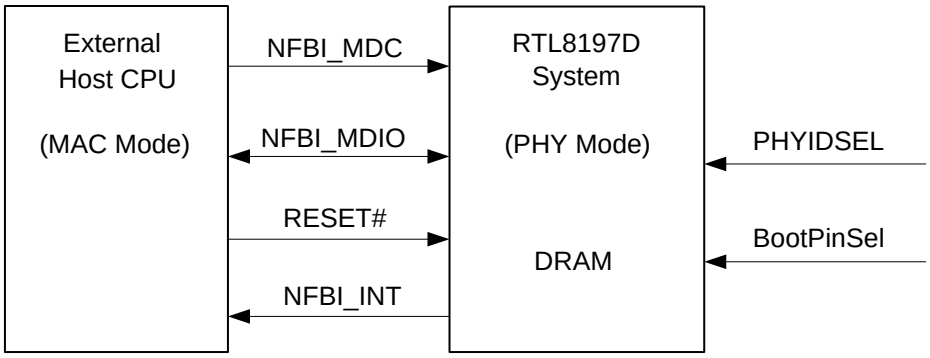


Figure 7. NFBI (Non-Flash Booting Interface)

15.2. NFBI Frame Format

The RTL8197D NFBI unit follows the same serial frame format as the IEEE 802.3 MDC/MDIO Interface. It acts in a slave role and will only respond to a command with a valid PHYID. The frame format is show in Table 145.

Table 145. NFBI Frame Format

	Preamble (8~32 bits)	Start (2 bits)	OP Code (2 bits)	PHYID (5 bits)	REGAD (5 bits)	Turn Around (2 bits)	Data (16 bits)	Idle
Read	1……..1	01	10	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	Z0	D_{15}…….D_0	Z*
Write	1……..1	01	01	$A_4A_3A_2A_1A_0$	$R_4R_3R_2R_1R_0$	10	D_{15}…….D_0	Z*

Note: PHYID[4:0]: Each PHY will be configured with a unique PHYID (default value is by hardware strapping pin).

15.3. NFBI Register Address Mapping

The RTL8197D supports the following register set for NFBI control functions.

Table 146. NFBI Register Address Mapping

REGAD[4:0]	Name	Size (Byte)	Register Name
0x02	PHYID1	2	PHY Identifier Register 1
0x03	PHYID2	2	PHY Identifier Register 2
0x10	CMD	2	Command Register
0x11	ADDH	2	Address High Register
0x12	ADDL	2	Address Low Register
0x13	DH	2	Data High Register
0x14	DL	2	Data Low Register
0x15	SCR	2	Send Command Register
0x16	RSR	2	Receive Status Register
0x17	SYSSR	2	System Status Register
0x19	IMR	2	Interrupt Mask Register
0x1A	ISR	2	Interrupt Status Register

15.4. PHY Identifier Registers

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY section of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number and the model revision number.

Table 147. PHY Identifier Register 1 (REGAD 0x02)

Bit	Name	Description	Mode	Default
15:0	OUI_MSB	Composed of the 3rd to 18th Bits of the Organizationally Unique Identifier (OUI)	RO	001CH

Table 148. PHY Identifier Register 2 (REGAD 0x03)

Bit	Name	Description	Mode	Default
15:10	OUI_LSB	Assigned to the 19th through 24th Bits of the OUI	RO	110010B
9:4	Model Number	Manufacturer's Model Number	RO	111000B
3:0	Revision Number	Manufacturer's Revision Number	RO	0001B

15.5. Command Register

Table 149. Command Register (REGAD 0x10)

Bit	Name	Description	Mode	Default
15	CMDType	Command Type. 0: Bus Write Access command. The external host CPU writes data to the RTL8197D CPU 1: Bus Read Access command. The external host CPU reads data from the RTL8197D *Note: Writing 1 causes hardware to pre-fetch a memory word. If CMDType changes from Write to Read mode, be sure that ADDR is set correctly before changing the set CMDType to read mode.*	RW	0B
14	Busy	1: Busy. When the busy bit is high, the external CPU cannot read/write any Address or Data. 0: Done. When busy is low, NFBI can read/write address and data. Hardware will automatically clear this bit. Software can query this bit to check NFBI hardware status.	RO	0B
13:3	-	Reserved	-	-
2	IntLevel	Select Interrupt Level. 1: In normal operation with no interrupt having occurred, the signal NFBI_INT bit is low. When an interrupt occurs, NFBI_INT is high 0: In normal operation with no interrupt having occurred, the signal NFBI_INT bit is high. When an interrupt occurs, NFBI_INT is low	RW	0
1	SystemRst	The External Host CPU can write 1 to force a RTL8197D whole system reset at any time. After the hardware reset is completed, this bit automatically returns to zero.	RW	0B

Bit	Name	Description	Mode	Default
0	StartRunBootCode	After all transfer code is ready in RAM, the external host CPU will write 1 to let the RTL8197D CPU release pending mode and start to run the boot code. 1: Leave holding mode and start to run boot code 0: Ignore Read back is CPU status. 0: Pending mode 1: Running mode	RW	0

15.6. Address Registers

The External host CPU can read/write any address of the RTL8197D SDRAM and built-in SRAM. The RTL8197D CPU address and data bus width are all 32 bits, but the MDC/MDIO bus width is 16 bits. The read/write Address and Data register width is divided into the higher and lower register, and the minimal transfer data length is 4 bytes (one word, 32 bits).
When transferring boot code, the access address register is sequential by order. To save bandwidth, only a contiguous read/write data request is required, and the contiguous read/write address value is ignored. This is because the NFBI unit automatically increases the address value when accessing RAM.

Table 150. Address Register (High) (REGAD 0x11)

Bit	Name	Description	Mode	Default
15:0	ADDH[31:16]	Address Bus Higher 16 Bits.	RW	1FC0H

Table 151. Address Register (Low) (REGAD 0x12)

Reg.bit	Name	Description	Mode	Default
15:0	ADDL[15:0]	Address Bus Lower 16 Bits.	RW	0000H

15.7. Data Register

When writing the 'Data Register', be sure the write sequence is 'write high data (MSB) first' and then low data (LSB) later. This is because writing the low data register will trigger a hardware latch circuit and start a read/write procedure.

Table 152. Data Register (High) (REGAD 0x13)

Bit	Name	Description	Mode	Default
15:0	DATAH[31:16]	Read/Write Access Physical Data Bus.	RW	0000H

Table 153. Data Register (Low) (REGAD 0x14)

Bit	Name	Description	Mode	Default
15:0	DATAL[15:0]	Read/Write Access Physical Data Bus Lower 16 Bits. When this register is written, it will trigger a write procedure. It will write DATA[31:0] values to SRAM at ADD[31:0]. The built-in Address Counter will automatically increase.	RW	0000H

15.7.1. Command and Status Register

There are two communication channels between the external host CPU and the RTL8197D CPU. From the external host CPU view, one line sends commands to the RTL8197D CPU; another line is read-only and receives the status from RTL8197D CPU writes. The transfer command and status message communication is defined in Table 154 and Table 155.

Table 154. Send Command Register (REGAD 0x15)

Bit	Name	Description	Mode	Default
15:0	MsgID	External host CPU sends Message ID to RTL8197D CPU	RW	0

Table 155. Receive Status Register (REGAD 0x16)

Bit	Name	Description	Mode	Default
15:0	MsgID	External host CPU receives Message ID from RTL8197D CPU write in. This register value is the same as the 'RTL8197D CPU Send Booting Status Register'.	R	0

15.8. System Status Register

The RTL8197D CPU reports the whole system status to an external host CPU to monitor device status.

Table 156. System Status Register (REGAD 0x17)

Bit	Name	Description	Mode	Default
15	CheckSumDone	1: Boot code kernel checksum done 0: Boot code has not done a checksum, or a checksum is in progress	R	0B
14	CheckSumOK	1: Checksum OK 0: Checksum fail This bit value is valid when the 'CheckSumDone' bit=1.	R	0B
13:11	-	Reserved	-	-
10	AllSoftwareReady	0: Software is not ready (possibly still booting) 1: All software has booted OK and is ready	R	0B
9:6	-	Reserved	-	-
5	Bootcode Ready	Bootcode Ready Status. Each time the boot loader boots up successfully, this bit will be modified from 1 to 0 or from 0 to 1 to indicate the boot loader is ready for service.	R	0
4:0	-	Reserved	-	-

15.8.1. Interrupt Mask Register

Table 157. Interrupt Mask Register (REGAD 0x19)

Bit	Name	Description	Mode	Default
15	CheckSumDoneMask	CheckSumDone Mask. 0: Disable 1: Enable	RW	0
14	CheckSumOKMask	CheckSumOK Mask. 0: Disable 1: Enable	RW	0
13:11	-	Reserved	RW	0
10	AllSoftwareReadyMask	All Software Ready Mask. 0: Disable 1: Enable	RW	0
9:6	-	Reserved.	RW	0
5	BootcodeReadyMask	Bootcode Ready Mask. 0: Disable 1: Enable	RW	0
4:3	-	Reserved	RW	0
2	PrevMsgFetchMask	Previous Message was Fetch Mask. 0: Disable 1: Enable	RW	0
1	NewMsgComingMask	New Message has Coming Mask. 0: Disable 1: Enable	RW	0
0	NeedBootCodeMask	Need Boot Code Mask. 0: Disable 1: Enable	RW	1

15.8.2. Interrupt Status Register

Table 158. Interrupt Status Register (REGAD 0x1A)

Bit	Name	Description	Mode	Default
15	CheckSumDoneIP	CheckSumDone Interrupt Pending. Write 1 to clear.	RW	0
14	CheckSumOKIP	CheckSumOK Interrupt Pending. Write 1 to clear.	RW	0
13:11	-	Reserved	RW	0
10	AllSoftwareReadyIP	All Software Ready Interrupt Pending. Write 1 to clear.	RW	0
9:6	-	Reserved	RW	0
5	BootcodeReadyIP	Bootcode Ready Interrupt Pending. Write 1 to clear.	RW	0
4:3	-	Reserved.	RW	0
2	PrevMsgFetchIP	Previous Message Fetch Interrupt Pending. When a message has been sent from the external host CPU to the RTL8197D CPU, and the RTL8197D has fetched the message and performed the interrupt service, this bit=1. This function is used to inform the external host CPU that Send Command Register (SCR) data was already fetched by the RTL8197D CPU. Write 1 to clear.	RW	0
1	NewMsgComingIP	New Message Coming Interrupt Pending. When a New Message is ready to be sent from the RTL8197D CPU to the external host CPU, this bit=1. The external host CPU then reads the Receive Status Register (RSR) for more information. Write 1 to clear.	RW	0
0	NeedBootCodeIP	Need Boot Code Interrupt Pending. After power on and the RTL8197D CPU is ready and waiting for boot code, this bit=1. When the external host CPU has finished transfering boot code, write 1 to clear.	RW	0

15.9. RTL8197D Internal CPU NFBI Control Register

The RTL8197D internal CPU uses these registers to control the NFBI (Non-Flash Booting Interface) block.

Table 159. CPU Internal Register Table (0xB801_9000)

Offset	Name	Size (byte)	Register Name
0x00	RCR	4	Receive Command Register
0x04	SSR	4	Send Status Register
0x10	IMR	4	Interrupt Mask Register
0x14	ISR	4	Interrupt Status Register

15.9.1. Receive Command and Send Status Register

There are two communication channels between the external host CPU and the RTL8197D CPU.

From the RTL8197D CPU's view, one line is read-only and receives commands from the external host CPU; another line sends the status to the external host CPU.

From the external host CPU view, one line sends commands to the RTL8197D CPU; another line is read-only and receives the status from RTL8197D CPU writes. The receive command and status message communication is defined in Table 160 and Table 161.

Table 160. RTL8197D CPU Receive Command Register (0xB801_9000)

Bit	Name	Description	Mode	Default
31:16	-	Reserved	-	-
15:0	MsgID	The RTL8197D CPU received a Message ID after an external host CPU write. This register value is the same as the 'External Host CPU Send Booting Status Register'.	R	0

Table 161. RTL8197D CPU Send Status Register (0xb801_9004)

Bit	Name	Description	Mode	Default
31:16	-	Reserved	-	-
15:0	MsgID	The RTL8197D CPU sent a Message ID to the external host CPU.	RW	0

15.9.2. Interrupt Mask and Interrupt Status Register On NFBI

Table 162. RTL8197D NFBI Interrupt Mask Register (0xB801_9010)

Bit	Name	Description	Mode	Default
31:3	-	Reserved	RW	0
2	PrevMsgFetchMask	Previous Message Fetch Interrupt Enable. 0: Disable 1: Enable	RW	0
1	NewMsgComingMask	New Message Coming Interrupt Enable. 0: Disable 1: Enable	RW	0
0	-	Reserved	RW	0

Table 163. RTL8197D NFBI Interrupt Status Register (0xB801_9014)

Bit	Name	Description	Mode	Default
31:3	-	Reserved	RW	0
2	PrevMsgFetchByHostIP	Previous Message Fetch By Host Pending. When a message has been sent from the RTL8197D CPU to the external host CPU, and the external host CPU has fetched the message and performed the interrupt service, this bit=1. This function is used to inform the RTL8197D CPU that Send Status Register (SSR) data was already fetched by the external host CPU. Write 1 to clear.	RW	0
1	NewMsgFromHosIP	New Message From Host Interrupt Pending. When a New Message is ready to be sent from the external host CPU to the RTL8197D CPU, this bit=1. The RTL8197D CPU then reads the Receive Command Register (RCR) for more information. Write 1 to clear.	RW	0
0	-	Reserved	RW	0

16. DC Specifications

16.1. Operating Conditions

Table 164. Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD33	Digital I/O Power Supply 3.3V	3.135	3.3	3.465	V
AVDD33	Analog Power Supply 3.3V	3.135	3.3	3.465	V
VDD10	Core Power Supply 1.0V	1.00	1.05	1.10	V
AVDD10	Analog Power Supply 1.0V	1.00	1.05	1.10	V
AVDD33_X25M	25M Crystal Power 3.3V	3.135	3.3	3.465	V
AVDD33_BG	System Bandgap Power Supply 3.3V	3.135	3.3	3.465	V
AVDD10_PCIE	PCI Express Analog Power 1.0V	1.00	1.05	1.10	V
AVDD10_PHYPLL	Ethernet PHY PLL Power 1.0V	1.00	1.05	1.10	V
AVDD33_PHYPLL	Ethernet PHY PLL Power 3.3V	3.135	3.3	3.465	V
AVDD33_USB	USB2.0 Analog Power 3.3V	3.135	3.3	3.465	V
AVDD10_USB	USB2.0 Analog Power 1.0V	1.00	1.05	1.10	V
VDD33_25	SDR DRAM I/O Power Supply 3.3V DDR1 DRAM I/O Power Supply 2.5V DDR2 DRAM I/O Power Supply 1.8V	3.135 2.4 1.7	3.3 2.5 1.8	3.465 2.7 1.9	V
VREF	DDR1/DDR2 Reference Voltage	0.49*VDD33_25	0.5*VDD33_25	0.51*VDD33_25	V
VDD33_25MII	GMII/RGMII/MII Interface For Power Supply 3.3V For Power Supply 2.5V.	 3.135 2.4	 3.3 2.5	 3.465 2.7	V

16.2. Total Power Consumption

Table 165. Total Power Consumption

SYM	Conditions	Min	Typ.	Max	Units
PS	All LAN Ports Idle	-	0.47	-	Watt
	LAN Full Load Active for Link at 100Base-TX	-	1.15	-	

Note: Power consumption is measured at full load of the chip system.

16.3. SDR DRAM Bus DC Parameters

Table 166. SDR DRAM Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	-
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshot: $V_{IH\ (MAX)}$=V_{DDH} + 2V for a pulse width ≤3ns, and the pulse width not greater than one third of the cycle rate.

Note 2: V_{IL} undershot: $V_{IL\ (MIN)}$=-2V for a pulse width ≤3ns cannot be exceeded.

Note 3: The output current buffer is 16mA for SDR DRAM clock, address, and data bus.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

16.4. DDR DRAM Bus DC Parameters

Table 167. DDR DRAM Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	SSTL_2	VREF+0.15	-	VREF+0.3	V
V_{IL}	Input-Low Voltage	SSTL_2	-0.3	-	VREF-0.15	V
V_{TT}	I/O Termination Voltage	-	VREF-0.04	-	VREF+0.04	V
I_{IL}	Input-Leakage Current	V_{IN}=VREF or 0	-10	±1	10	µA
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA

16.5. Flash Bus DC Parameters

Table 168. Flash Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	-
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshot: VIH (MAX)=VDDH + 2V for a pulse width ≤3ns.

Note 2: V_{IL} undershot: $V_{IL\ (MIN)}$=-2V for a pulse width ≤3ns.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

16.6. USB v1.1 DC Parameters

Table 169. USB v1.1 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	2.0	-	-	V	2
V_{IL}	Input-Low Voltage	-	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	2
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	2
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-	-	-	µA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.
Note 2: For additional information, see the USB v1.1 Specification.

16.7. USB v2.0 DC Parameters

Table 170. USB v2.0 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	200	-	-	mV	2
V_{IL}	Input-Low Voltage	-	-	-	10	mV	2
V_{OH}	Output-High Voltage	-	300	-	500	mV	2
V_{OL}	Output-Low Voltage	-	-10	-	10	mV	2
I_{IL}	Input-Leakage Current	-	-	-	-	µA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.
Note 2: For additional information, see the USB v2.0 Specification.

16.8. UART DC Parameters

Table 171. UART DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for UART related signals.
Note 2: These values are typical values checked in the manufacturing process and are not tested.

16.9. GPIO DC Parameters

Table 172. GPIO DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	μA	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for GPIO related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

16.10. JTAG DC Parameters

Table 173. JTAG DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	$\lvert I_{OH} \rvert$ =2~16mA	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	$\lvert I_{OL} \rvert$ =2~16mA	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	μA	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 4mA for JTAG related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

16.11. MII DC Parameters

Table 174. MII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	μA	2
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	μA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for MII related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

16.12. GMII DC Parameters

Table 175. GMII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	-	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	µA	2
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for GMII related signals.
Note 2: These values are typical values checked in the manufacturing process and are not tested.

16.13. RGMII DC Parameters

Table 176. RGMII DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	3.3V/2.5V	2.0/1.7	-	-	V	-
V_{IL}	Input-Low Voltage	3.3V/2.5V	-	-	0.8/0.7	V	-
V_{OH}	Output-High Voltage	3.3V/2.5V	2.4/2.0	-	-	V	1
V_{OL}	Output-Low Voltage	3.3V/2.5V	-	-	0.4/0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	µA	2
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for RGMII related signals.
Note 2: These values are typical values checked in the manufacturing process and are not tested.

16.14. Reset DC Parameters

Table 177. Reset DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V

16.15. LED DC Parameters

Table 178. LED DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OHED}	Output-High Voltage	-	2.4	-	-	V
V_{OLLED}	Output-Low Voltage	-	-	-	0.4	V

Note: The output current buffer for LED signals is 8mA.

17. AC Specifications

17.1. Clock Signal Timing

17.1.1. 25MHz System Clock Timing

Table 179. 25MHz System Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	-	-	0.8	V	-
$T_{FREQUENCY}$	Clock Frequency for RTL8197D Crystal or Oscillator	-	25	-	MHz	1
$\Delta_{FREQUENCY}$	Clock Tolerance Over 0℃ to 50℃	-50	-	50	ppm	-
C_{SHUNT}	Crystal Parameter (Sometimes Referred to as the Holder Capacitance)	-	-	7	pF	2
C_1	Load Capacitance	-	-	30	pF	3
C_2	Load Capacitance	-	-	30	pF	3
T_{DC}	Duty Cycle	-	50	-	%	-

Note 1: This value could be an oscillator input or a series resonant frequency from a crystal. If used as an oscillator input, tie to the crystal input pin and leave the crystal output pin disconnected.

Note 2: The 25MHz Crystal CL=16pF is used on the RTL8197D.

Note 3: The RTL8197D PLL circuit requires an external 25MHz crystal with shunt capacitors. These shunt capacitors cannot be over 30pF due to chip design requirements.

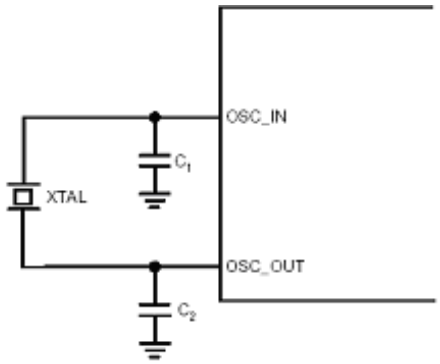


Figure 8. Typical Connection to a Crystal

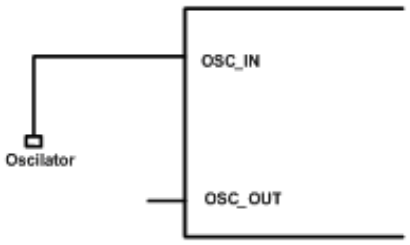


Figure 9. Typical Connection to an Oscillator

17.1.2. 40MHz System Clock Timing

Table 180. 40MHz System Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	1.2	1.4	2.0	V
V_{IL}	Input-Low Voltage	-	-	0.2	V
$T_{FREQUENCY}$	Clock Frequency	-	40	-	MHz
$\Delta_{FREQUENCY}$	Clock Tolerance (between 0℃~70℃)	-50	-	50	ppm
T_{DC}	Duty Cycle	-	50	-	%

17.1.3. SDR DRAM Clock Timing

Table 181. SDR DRAM Clock Timing

Symbol	Parameter	Min. (130MHz)	Typ. (160MHz)	Max. (180MHz)	Units	Notes
$T_{PERIOD\_SDRAMCLK}$	Clock Period for SDR DRAM Clock	7.7	6.25	5.5	ns	-
$T_{CLKHIGH}$	SDR DRAM Clock High Time	3.57	3.57	3.57	ns	-
T_{CLKLOW}	SDR DRAM Clock Low Time	3.57	3.57	3.57	ns	-
$T_{RISE/FALL}$	Rise and Fall Time Requirements for SDR DRAM Clock	-	-	2	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	NA	-	ns	1

Note 1: For detailed information, contact Realtek for the IBIS model.

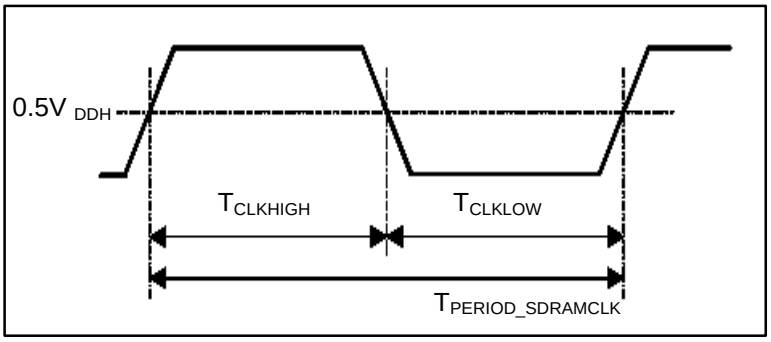


Figure 10. SDR DRAM Clock Specifications-1

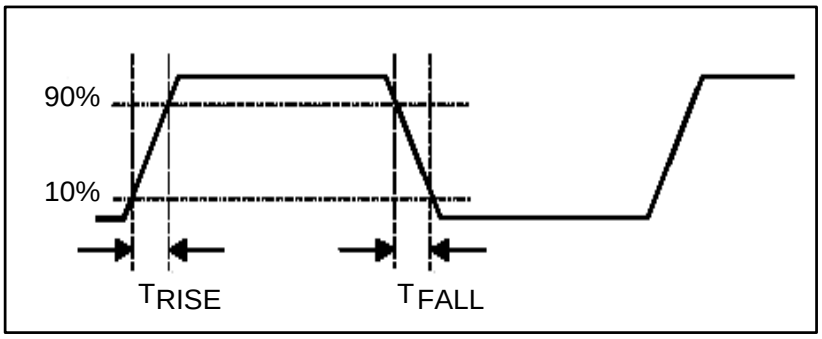


Figure 11. SDR DRAM Clock Specifications-2

17.1.4. MII Clock Timing

Table 182. MII Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{PERIOD100Mbit}$	Clock Period for Tx and Rx Ethernet Clocks	-	25	25	-	-
$T_{PERIOD10Mbit}$	Clock Period for Tx and Rx Ethernet Clocks	-	2.5	2.5	MHz	-
T_{DUTY}	Duty Cycle for Tx and Rx Ethernet Clocks	35	50	65	%	-
$T_{RISE/FALL}$	Rise And Fall Time Requirement for Tx and Rx Ethernet Clocks	-	-	2	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	NA	-	ns	1

Note 1: For detailed contact Realtek for the IBIS model.

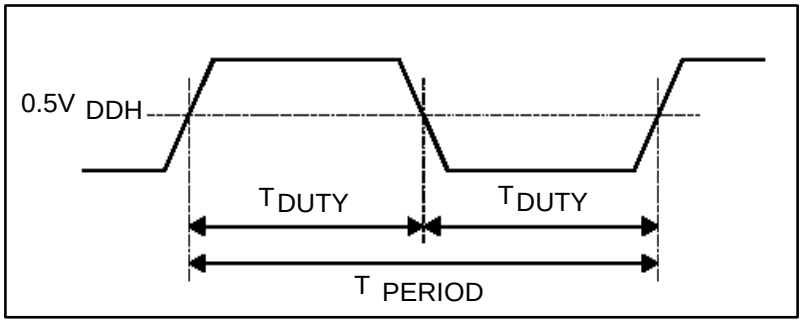


Figure 12. MII Clock Specifications-1

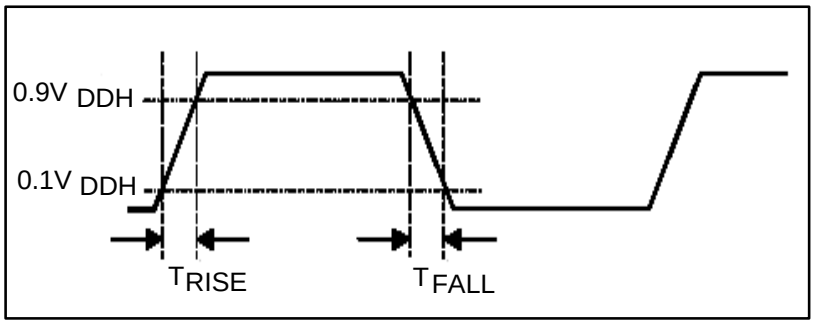


Figure 13. MII Clock Specifications-2

17.1.5. GMII Clock Timing

Table 183. GMII Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{PERIOD1000Mbit}$	Clock Period for Tx and Rx Ethernet Clocks	-	8	-	-	-
T_{DUTY}	Duty Cycle for Tx and Rx Ethernet Clocks	35	50	65	%	-
$T_{RISE/FALL}$	Rise and Fall Time Requirement for Tx and Rx Ethernet Clocks	-	-	1	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	N.A.	-	ns	1

Note 1: For detailed information contact Realtek for the IBIS model.

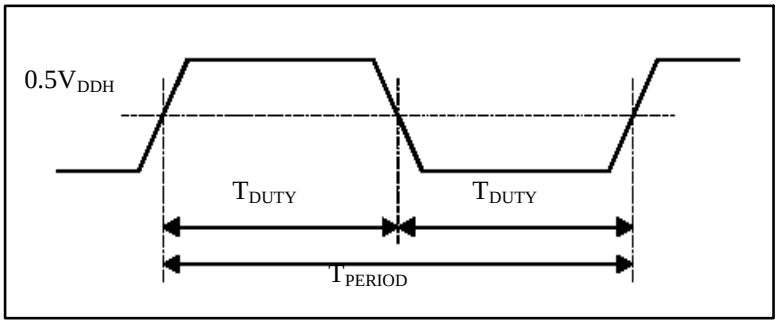


Figure 14. GMII Clock Specifications-1

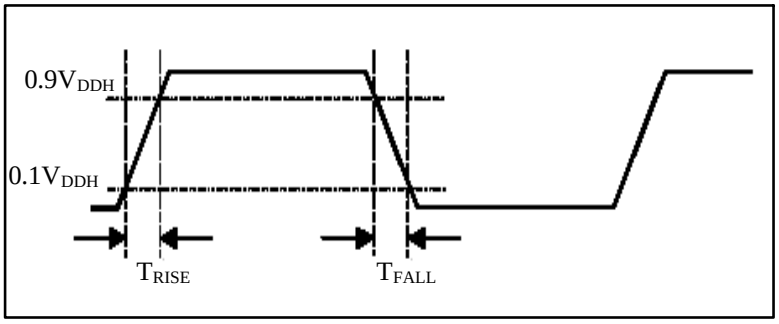


Figure 15. GMII Clock Specifications-2

17.1.6. RGMII Clock Timing

Table 184. RGMII Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
$T_{PERIOD1000Mbit}$	Clock Period for Tx and Rx Ethernet Clocks	7.2	8	8.8	-	-
T_{DUTY}	Duty Cycle for Tx and Rx Ethernet Clocks	45	50	55	%	-
$T_{RISE/FALL}$	Rise And Fall Time Requirement for Tx and Rx Ethernet Clocks (20~80%)	-	-	0.75	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	-	-	ns	1

Note 1: For detailed information contact Realtek for the IBIS model.

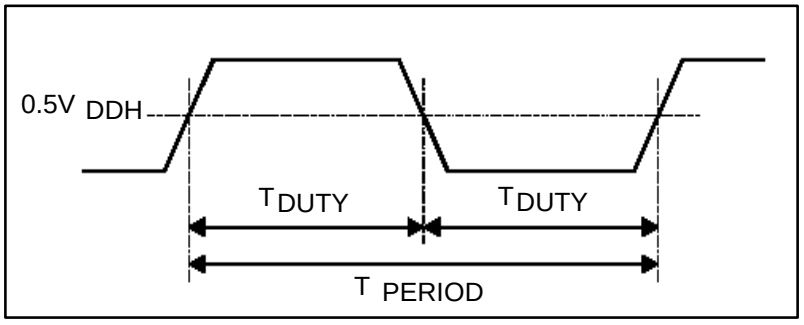


Figure 16. RGMII Clock Specifications-1

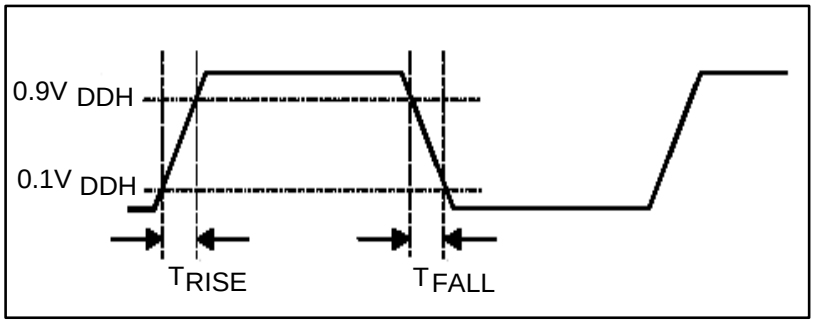


Figure 17. RGMII Clock Specifications-2

17.2. Bus Signal Timing

17.2.1. SDR DRAM Bus

17.2.1.1 SDR DRAM Input Timing

Table 185. SDR DRAM Input Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{SETUP}	Input Setup Prior to Rising Edge of Clock. Inputs included in this timing are MD[15: 0] (during a read operation)	-	1.13	-	ns
T_{HOLD}	Input Hold Time after the Rising Edge of Clock. Inputs included in this timing are MD[15:0] (during a read operation)	-	0	-	ns

Note: The RTL8197D integrates some timing controls on the interface. Here the timing parameters listed in the table are extracted in the default situation (without specific controls).

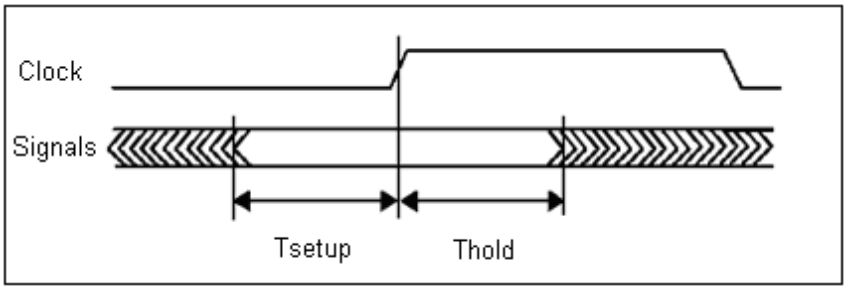


Figure 18. SDR DRAM Input Timing

17.2.1.2 SDR DRAM Output Timing

Table 186. SDR DRAM Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$T_{CLK2OUT}$	Rising Edge of Clock-to-Signal Output. Outputs include this timing are MD[15: 0], MCS0#, MCS1#, RAS#, CAS#, LDQM, UDQM, WE# (during a write operation)	-	-	2.3	ns
$T_{HOLDOUT}$	Signal Output Hold Time after the Rising Edge of the Clock. Outputs included in this timing are MD[15: 0] (during a write operation)	0.8	-	-	ns

Note: Timing was tested with 75-pF capacitor to ground.

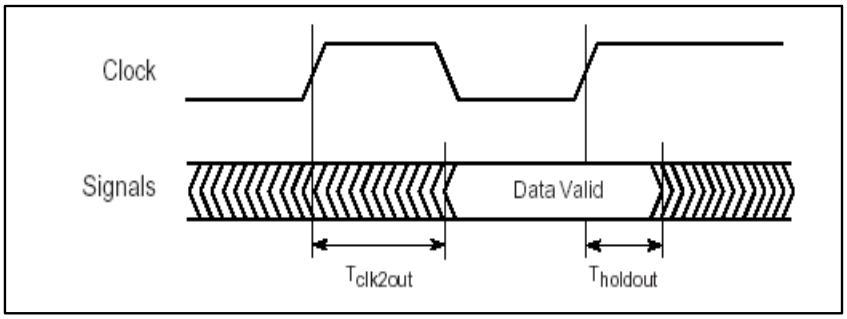


Figure 19. SDR DRAM Output Timing

17.2.1.3 SDR DRAM Access Control Timing

Table 187. SDR DRAM Access Control Timing

Symbol	Parameter	Units	Notes
$T_{REFRESH}$	Auto-Refresh Timing. Controlled by Reg. 0xB8001008 (DTR)	µs	-
T_{RCD}	The Time Interval between RAS# Active and CAS# Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RP}	The Time Interval between Pre-Charge and the Next Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RAS}	The Time Interval between Active and Pre-Charge. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RC}	The Time Interval between Active and the Next Active. Controlled by Reg. 0xB8001008 (DTR)	ns	1
T_{RFC}	The Time Interval between Auto-Refresh and Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
$T_{CAS\_LATENCY}$	The Data Output Delay after CAS# Active. Controlled by Reg. 0xB8001004 (DCR)	ns	-

Note 1: TRC=TRAS+TRP.

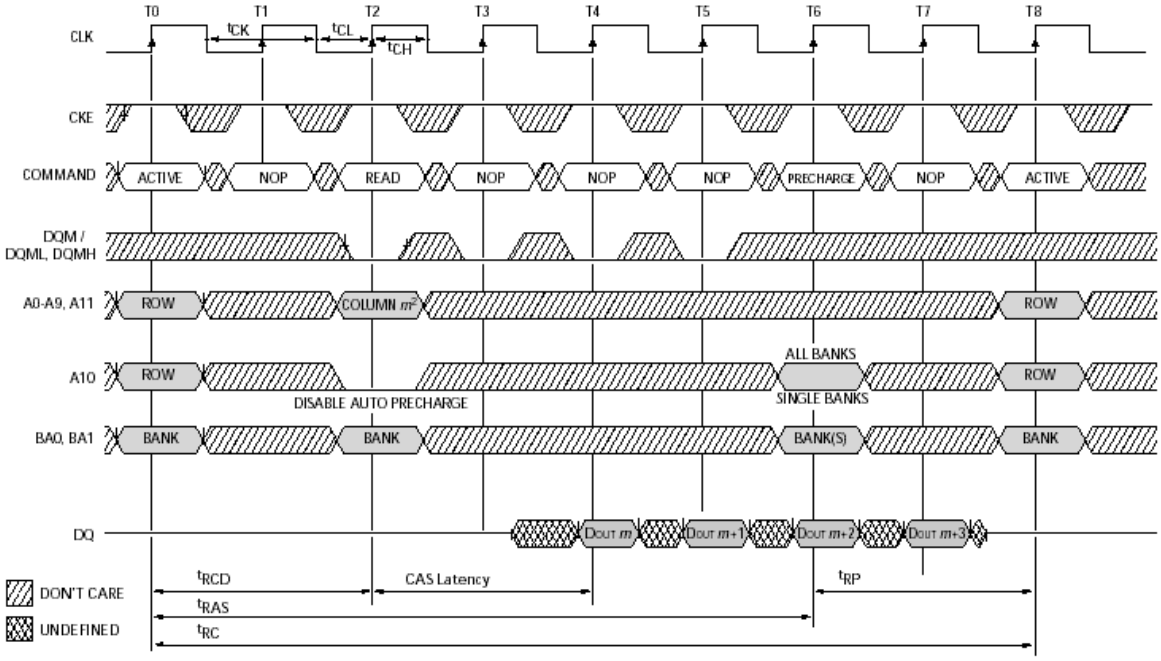


Figure 20. SDR DRAM Access Control Timing

17.2.2. DDR DRAM Bus

17.2.2.1 DDR DRAM Input Timing

Table 188. DDR DRAM Input Timing

Symbol	Parameter	Units	Notes
T_{SETUP}	Input Setup Prior to Rising Edge of Clock. Inputs included in this timing are D[31: 0] (during a read operation)	ns	1
T_{HOLD}	Input Hold Time after the Rising Edge of Clock. Inputs included in this timing are D[31:0] (during a read operation)	ns	1

Note1: The RTL8197D integrates some timing control registers on the interface.

17.2.2.2 DDR DRAM Output Timing

Table 189. DDR DRAM Output Timing

Symbol	Parameter	Units	Notes
$T_{CLK2OUT}$	Rising Edge of Clock-to-Signal Output. Outputs include this timing are D[31: 0], CS0#, CS1#, RAS#, CAS#, LDQM, UDQM, WE#, LDQS, UDQS (during a write operation)	ns	1
$T_{HOLDOUT}$	Signal Output Hold Time after the Rising Edge of the Clock. Outputs included in this timing are D[31: 0] (during a write operation)	ns	1

Note1: The RTL8197D integrates some timing control registers on the interface.

17.2.2.3 DDR DRAM Access Control Timing

Table 190. DDR DRAM Access Control Timing

Symbol	Parameter	Units	Notes
$T_{REFRESH}$	Auto-Refresh Timing. Controlled by Reg. 0xB8001008 (DTR)	µs	-
T_{RCD}	The Time Interval between RAS# Active and CAS# Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RP}	The Time Interval between Pre-Charge and the Next Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RAS}	The Time Interval between Active and Pre-Charge. Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RC}	The Time Interval between Active and the Next Active. Controlled by Reg. 0xB8001008 (DTR)	ns	1
T_{RFC}	The Time Interval between Auto-Refresh and Active. Controlled by Reg. 0xB8001008 (DTR)	ns	-
$T_{CAS\_LATENCY}$	The Data Output Delay after CAS# Active. Controlled by Reg. 0xB8001004 (DCR)	ns	-

Note 1: TRC=TRAS+TRP.

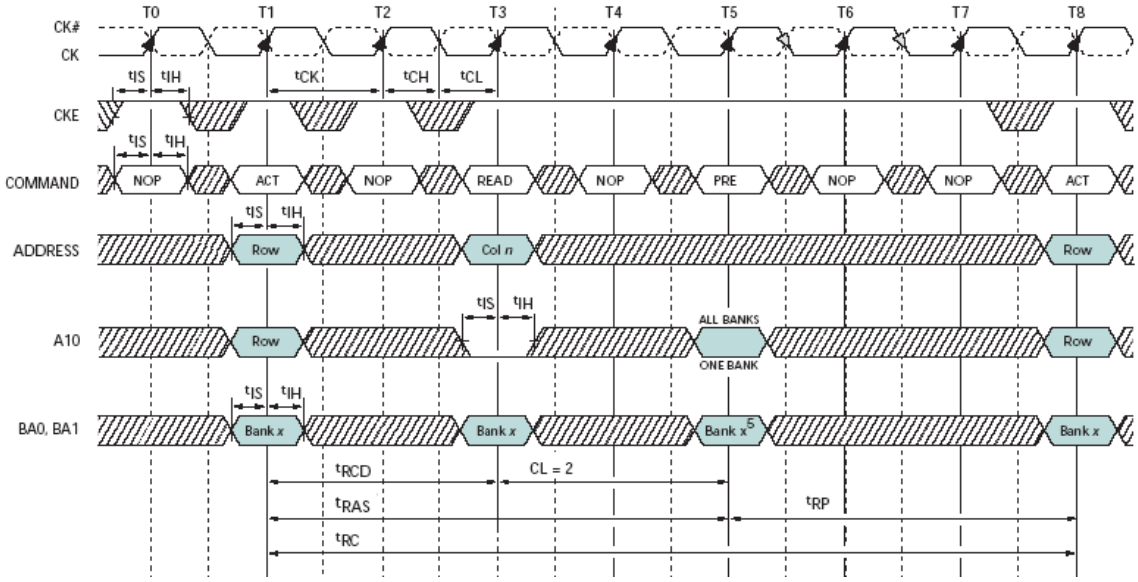


Figure 21. DDR DRAM Access Control Timing

17.2.3. Serial Flash Interface

17.2.3.1 Serial Flash Interface Output Timing

Table 191. Serial Flash Interface Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{SLCH}	The Timing Interval from Chip-Select Activated to the First Clock Rising Edge	2	-	-	ns
T_{CHSH}	The Timing Interval from the Last Clock Rising Edge to Chip-Select De-Activated	5	-	-	ns
T_{CLQV}	The Timing Interval from the Last Clock Falling Edge to Data-Out Validated	-	-	10	ns
T_{CLQX}	The Timing Interval from the Next Clock Falling Edge to Data-Out Invalidated	0	-	-	ns

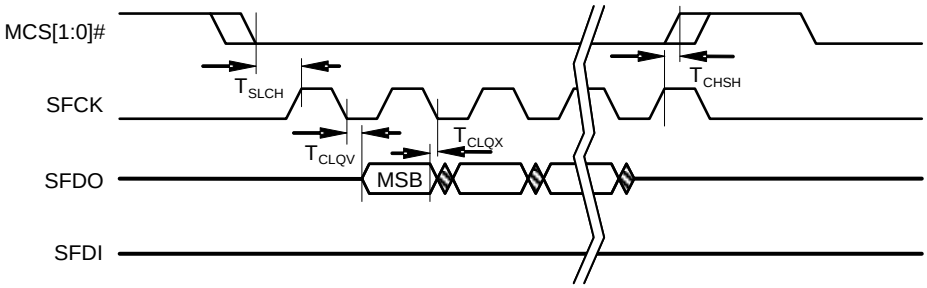


Figure 22. Serial Flash Interface Output Timing

17.2.3.2 Serial Flash Interface Intput Timing

Table 192. Serial Flash Interface Intput Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{DVCH}	The Timing Interval from Data-Input Ready to the Clock Rising Edge	2	-	-	ns
T_{CHDX}	The Timing Interval from the Clock Rising Edge to Data-Input Invalidated	5	-	-	ns

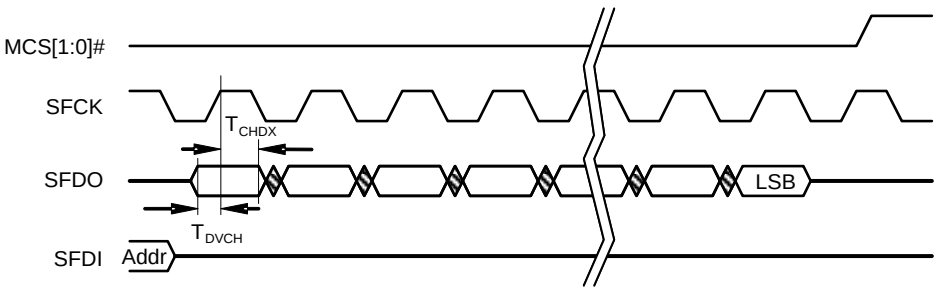


Figure 23. Serial Flash Interface Intput Timing

17.2.4. MII Interface

17.2.4.1 MII MAC Mode Output Timing

Table 193. MII MAC Mode Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_1	Clock Rising Edge to Output Delay for TXD[3:0] and TXEN	-	-	6	ns
T_2	Signal Output Hold Time after the Rising Edge of the TXCLK. Outputs included in this timing are TXD[3:0] and TXEN	3	-	-	ns

17.2.4.2 MII PHY Mode Output Timing

Table 194. MII PHY Mode Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_1	Clock Rising Edge to Output Delay for TXD[3:0] and TXEN	-	-	19	ns
T_2	Signal Output Hold Time after the Rising Edge of the TXCLK. Outputs included in this timing are TXD[3:0] and TXEN	21	-	-	ns

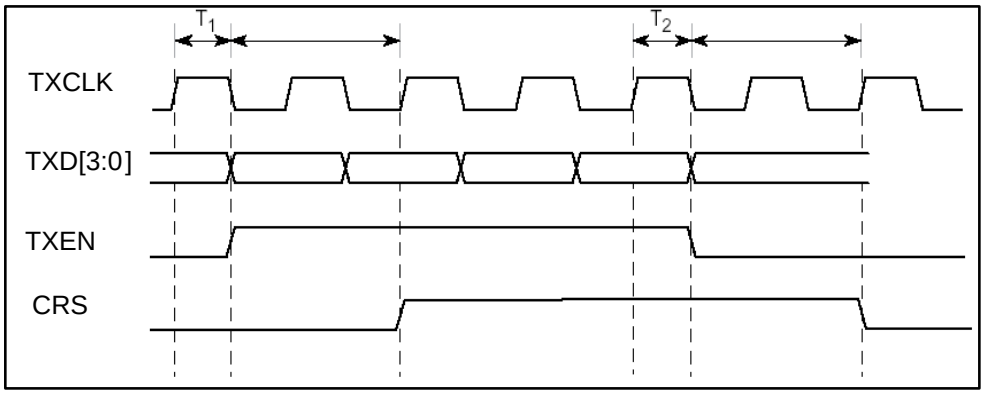


Figure 24. MII Output Timing

17.2.4.3 MII MAC Mode Input Timing Values

Table 195. MII MAC Mode Input Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units
T_3	RXD[3:0] and RXDV Setup Time Prior to Rising Edge of RXCLK	1	-	-	ns
T_4	RXD[3:0] and RXDV Hold Time after the Rising Edge of RXCLK	1	-	-	ns

17.2.4.4 MII PHY Mode Input Timing Values

Table 196. MII PHY Mode Input Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units
T_3	RXD[3:0] and RXDV Setup Time Prior to Rising Edge of RXCLK	7	-	-	ns
T_4	RXD[3:0] and RXDV Hold Time after the Rising Edge of RXCLK	0	-	-	ns

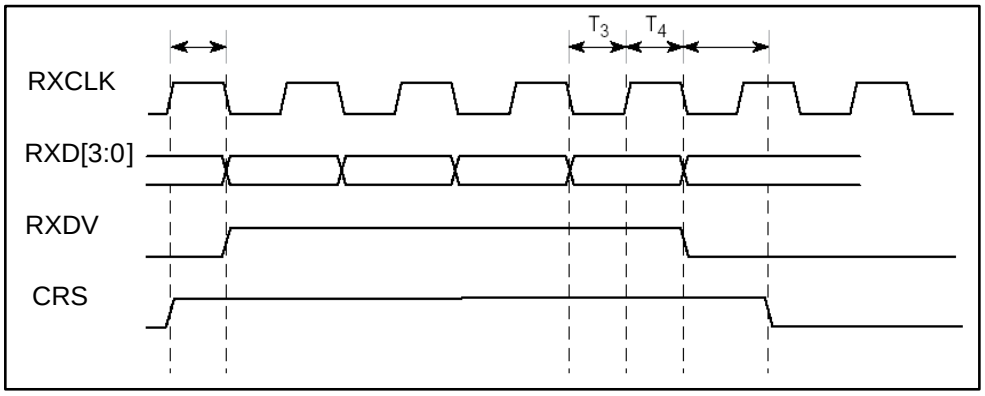


Figure 25. MII Input Timing

17.2.5. GMII Timing Characteristics

Table 197. GMII Timing Characteristics

Symbol	Description	Min	Typ.	Max	Units
T_{TX_SU}	Data to Clock Output Setup Time. Enable TXC delay	3	4	-	ns
T_{TX_HO}	Data to Clock Output Hold Time. Enable TXC delay	1	4	-	ns
T_{RX_SU}	Data to Clock Input Setup Time.	1.3	-	-	ns
T_{RX_HO}	Data to Clock Input Hold Time.	1	-	-	ns

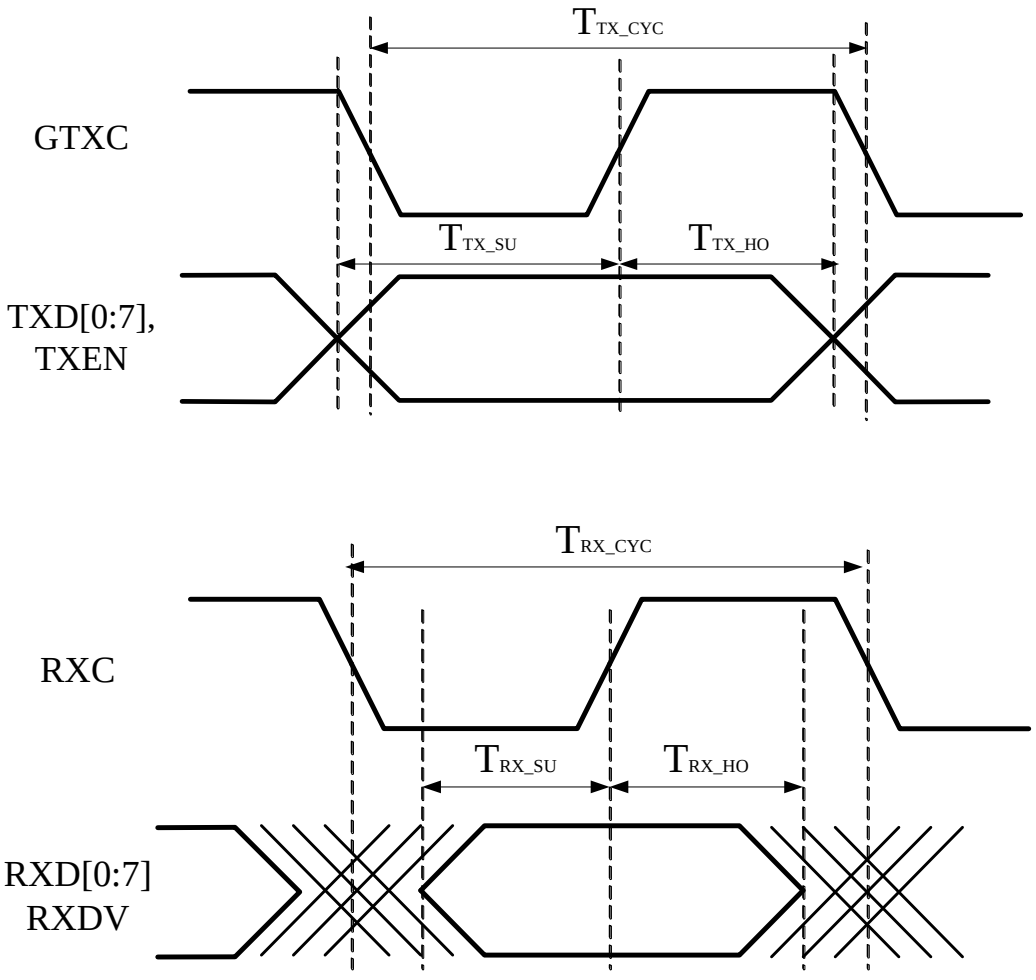


Figure 26. GMII Timing Characteristics

17.2.6. RGMII Timing Characteristics

Table 198. RGMII Timing Characteristics

SYM	Description/Condition	Min	Typ.	Max.	Units
T_{skewT}	Disable TXC Delay	-500	0	500	ps
T_{TX_SU}	Data to Clock Output Setup Time. Disable TXC Delay	-	400	-	ps
T_{TX_HO}	Data to Clock Output Hold Time. Disable TXC Delay	-	3.6	-	ns
T_{TX_SU}	Data to Clock Output Setup Time. Enable TXC Delay	-	1.6	-	ns
T_{TX_HO}	Data to Clock Output Hold Time. Enable TXC Delay	-	2.2	-	ns
T_{RX_SU}	Data to Clock Input Setup Time. Disable RXC Delay	1.0	-	-	ns
T_{RX_HO}	Data to Clock Input Hold Time. Disable RXC Delay	1.0	-	-	ns

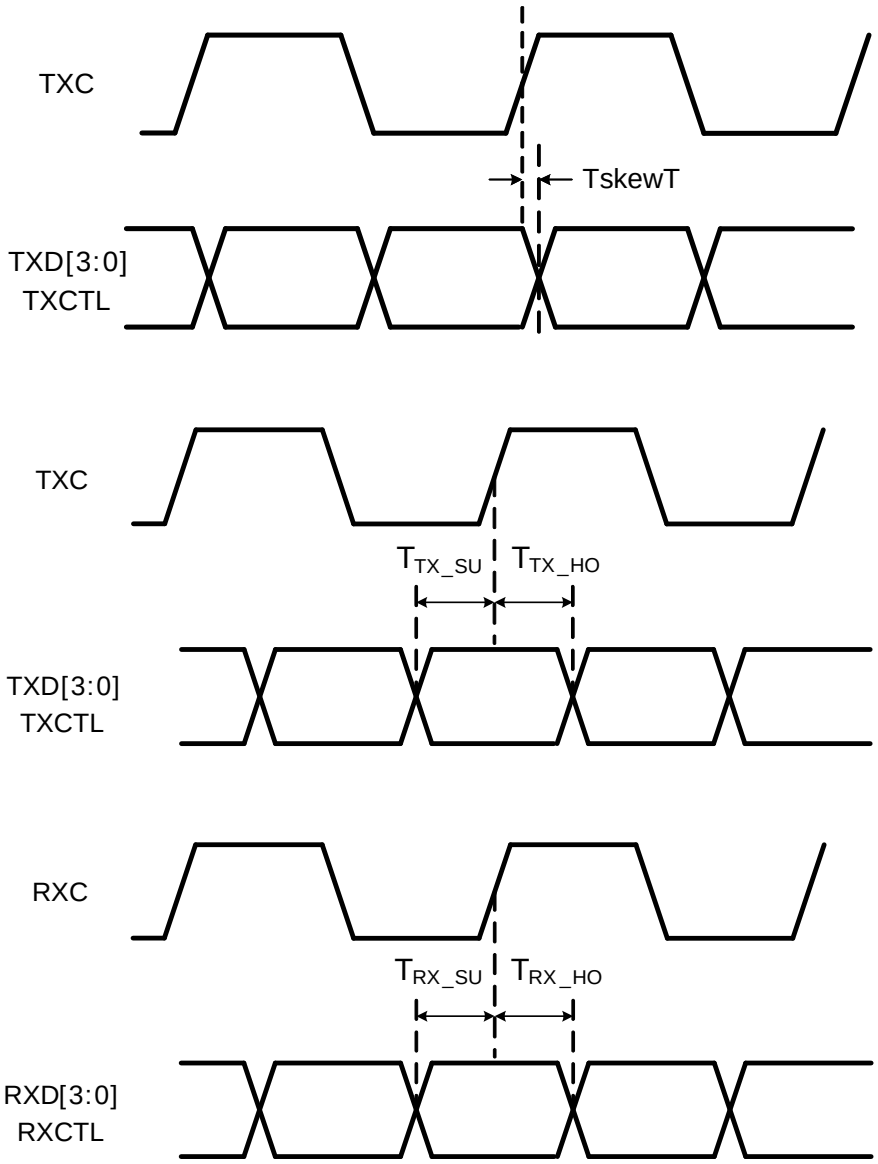


Figure 27. RGMII Timing Characteristics

17.2.7. JTAG Boundary Scan

Table 199. JTAG Boundary Scan Interface Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{bscl}	JTAG Clock Low Time	50	-	-	ns	1
T_{bsch}	JTAG Clock High Time	50	-	-	ns	1
T_{bsis}	TDI, TMS Setup Time to Rising Edge of TCK	10	-	-	ns	-
T_{bsih}	TDI, TMS Hold Time from Rising Edge of TCK	10	-	-	ns	-
T_{bsoh}	TDO Hold Time after Falling Edge of TCK	1.5	-	-	ns	-
T_{bsod}	TDO Output from Falling Edge of TCK	-	-	40	ns	-
T_{bsr}	JTAG Reset Period	30	-	-	ns	-
T_{bsrs}	TMS Setup Time to Rising Edge of JTAG Reset	10	-	-	ns	-
T_{bsrh}	TMS Hold Time from Rising Edge of JTAG Reset	10	-	-	ns	-

Note 1: JTAG clock TCK may be stopped indefinitely in either the low or high phase.

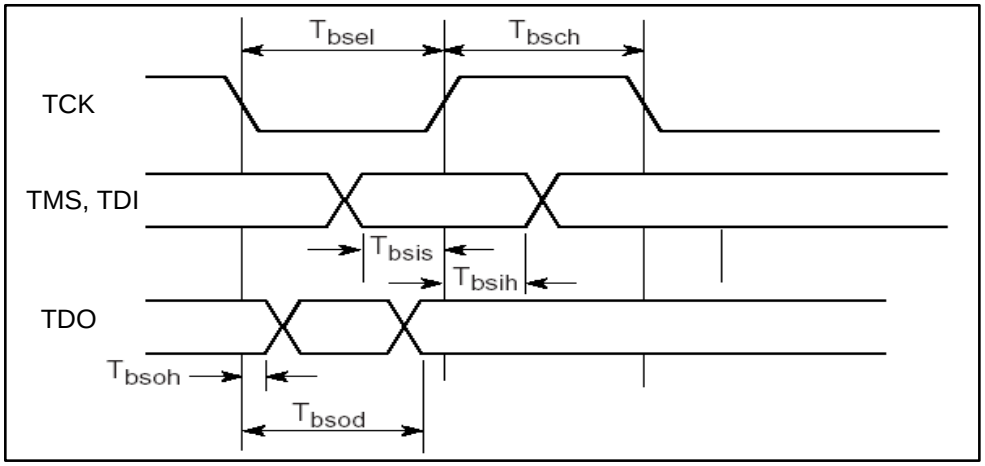


Figure 28. Boundary-Scan General Timing

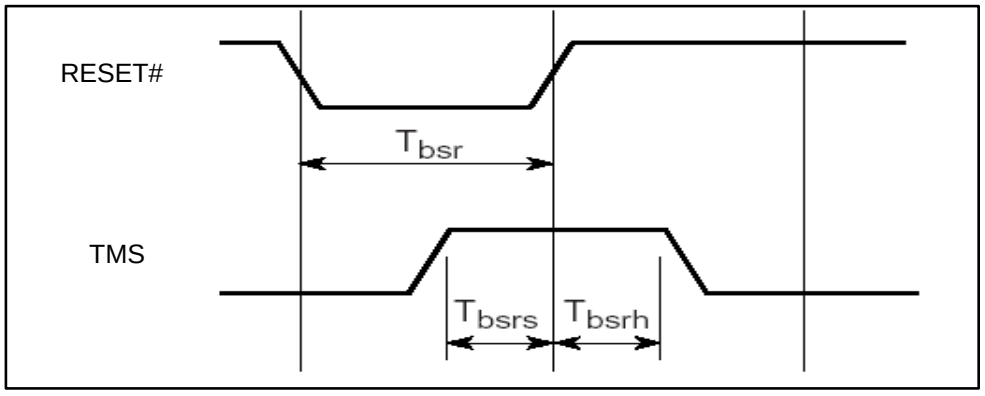


Figure 29. Boundary-Scan Reset Timing

17.2.8. Power Configuration Timing

Power up configuration only relates to internal timing. The external hardware pin reset is unconcerned with power up configuration. The Hardware reset pin is valid when an internal reset ends the active state.

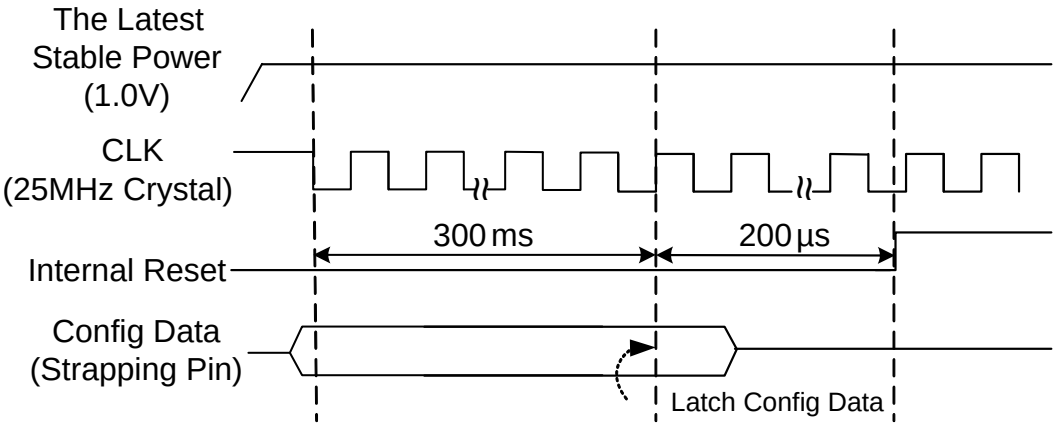


Figure 30. Power Up Configuration Timing

17.3. PCI Express Bus Parameters

17.3.1. Differential Transmitter Parameters

Table 200. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX\text{-}DIFFp\text{-}p}$	Differential Peak to Peak Output Voltage	0.800	-	1.2	V
$V_{TX\text{-}DE\text{-}RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
$T_{TX\text{-}EYE}$	Minimum Tx Eye Width	0.75	-	-	UI
$T_{TX\text{-}EYE\text{-}MEDIAN\text{-}to\text{-}MAX\text{-}JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	-	-	0.125	UI
$T_{TX\text{-}RISE}$, $T_{TX\text{-}FALL}$	D+/D- Tx Output Rise/Fall Time	0.125	-	-	UI
$V_{TX\text{-}CM\text{-}ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX\text{-}CM\text{-}DCACTIVE\text{-}IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX\text{-}CM\text{-}DCLINE\text{-}DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX\text{-}IDLE\text{-}DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX\text{-}RCV\text{-}DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX\text{-}DC\text{-}CM}$	Tx DC Common Mode Voltage	0	-	3.6	V
$I_{TX\text{-}SHORT}$	Tx Short Circuit Current Limit	-	-	90	mA
$T_{TX\text{-}IDLE\text{-}MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI

Symbol	Parameter	Min	Typical	Max	Units
$T_{TX-IDLE- SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO- DIFF-DATA}$	Maximum Time to Transition to Valid Tx Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential Tx Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

Note2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The ±300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

17.3.2. Differential Receiver Parameters

Table 201. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak to Peak Voltage	0.175	-	1.200	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to- MAX-JITTER}$	Maximum Time Between the Jitter Median and Maximum Deviation from the Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX--DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET- DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

17.3.3. REFCLK Parameters

Table 202. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-	-0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
Z_{C-DC}	Clock Source DC Impedance	40	60	Ω	1, 11

Note1: Measurement taken from single-ended waveform.

Note2: Measurement taken from differential waveform.

Note3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 34, page 140.

Note4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 31, page 139.

Note5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 31, page 139.

Note6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 33, page 139.

Note7: Defined as the maximum instantaneous voltage including overshoot. See Figure 31, page 139.

Note8: Defined as the minimum instantaneous voltage including undershoot. See Figure 31, page 139.

Note9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 31, page 139.

Note10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note11: System board compliance measurements must use the test load card described in Figure 37, page 141. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note12: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100mV differential range. See Figure 36, page 141.

*Note13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*

Note14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 32, page 139.

Note15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

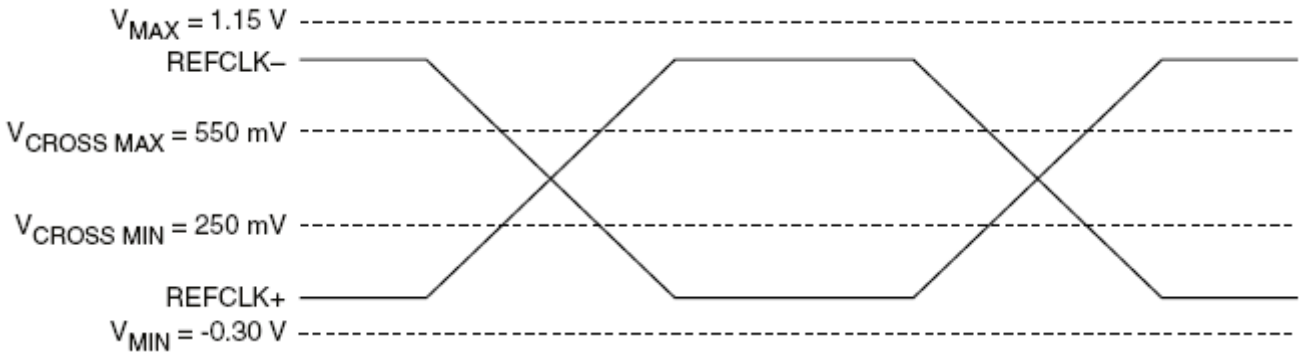


Figure 31. Single-Ended Measurement Points for Absolute Cross Point and Swing

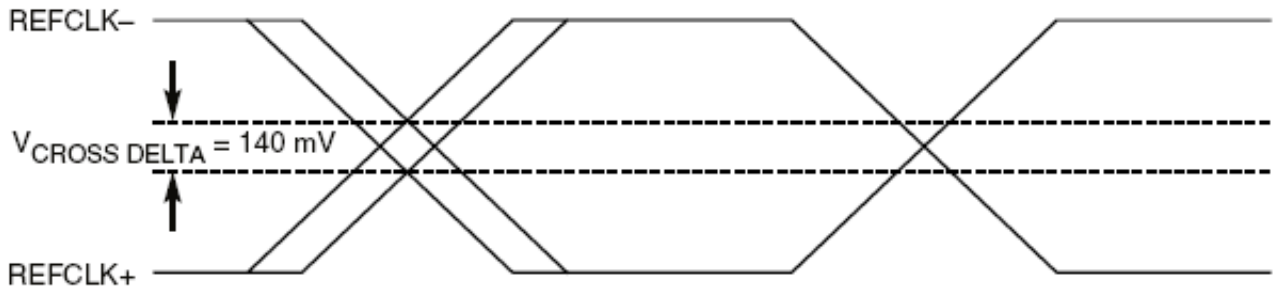


Figure 32. Single-Ended Measurement Points for Delta Cross Point

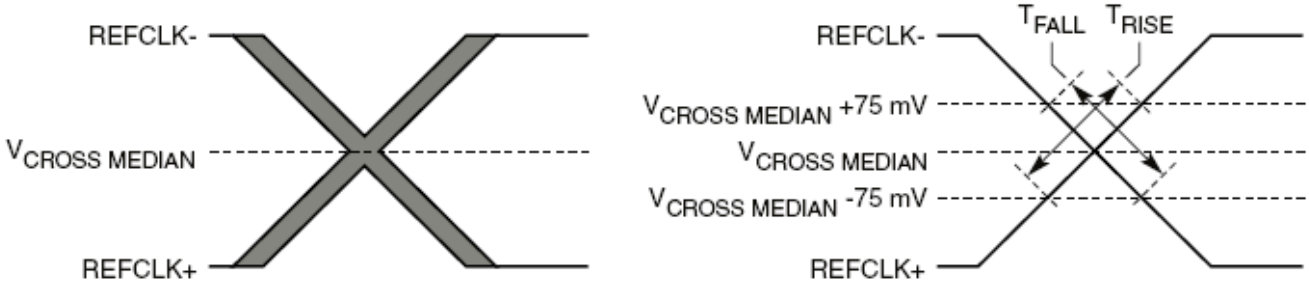


Figure 33. Single-Ended Measurement Points for Rise and Fall Time Matching

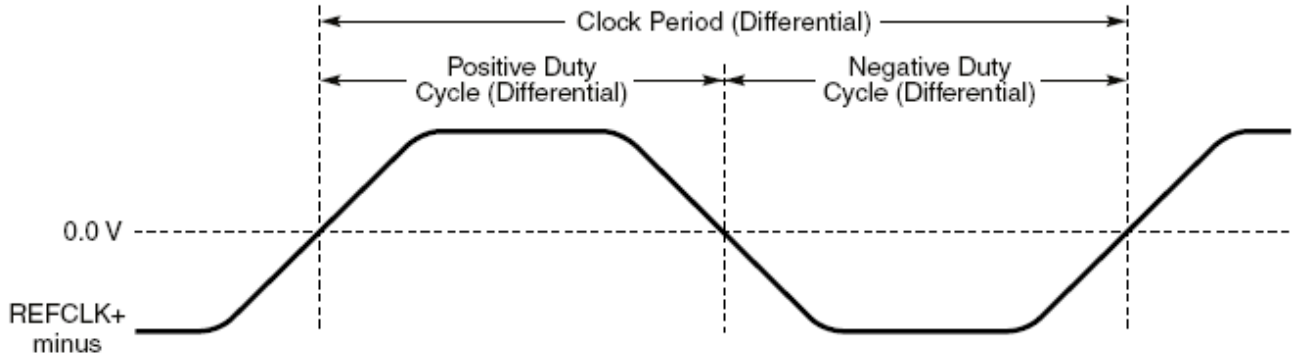


Figure 34. Differential Measurement Points for Duty Cycle and Period

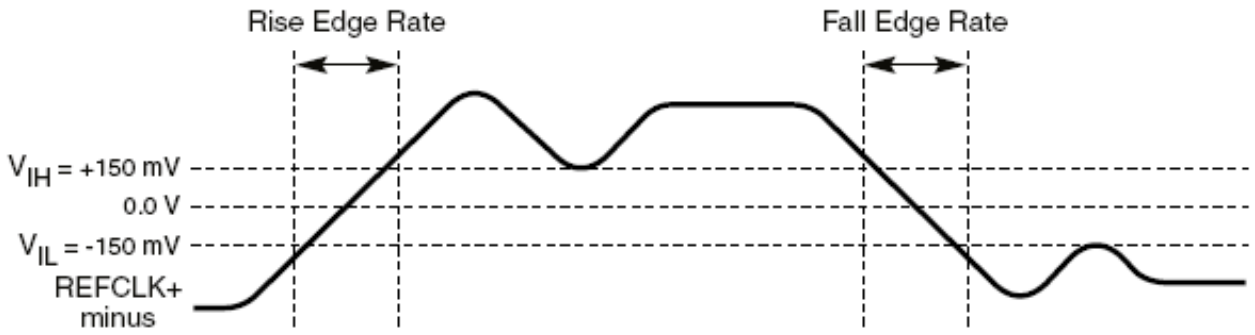


Figure 35. Differential Measurement Points for Rise and Fall Time

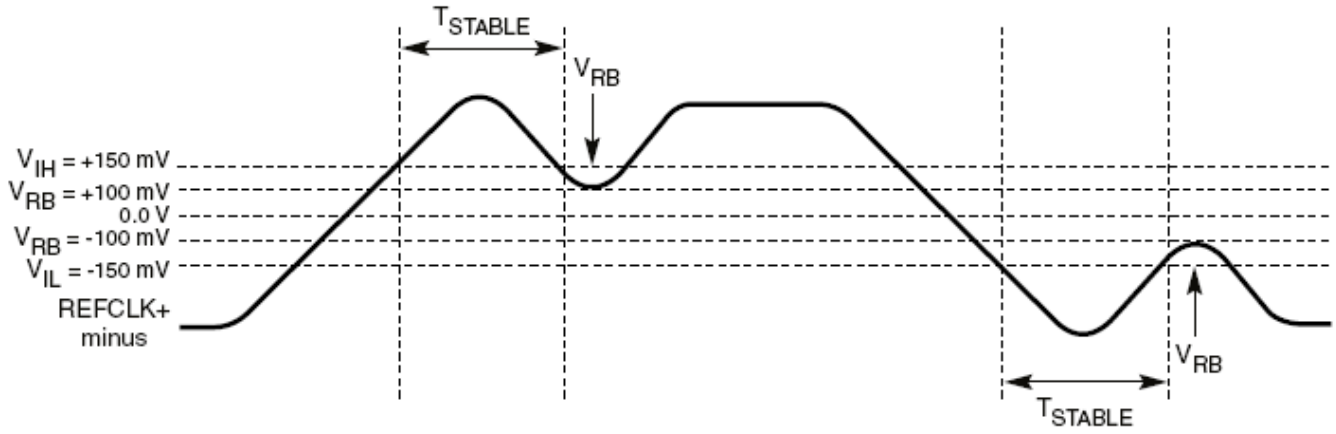


Figure 36. Differential Measurement Points for Ringback

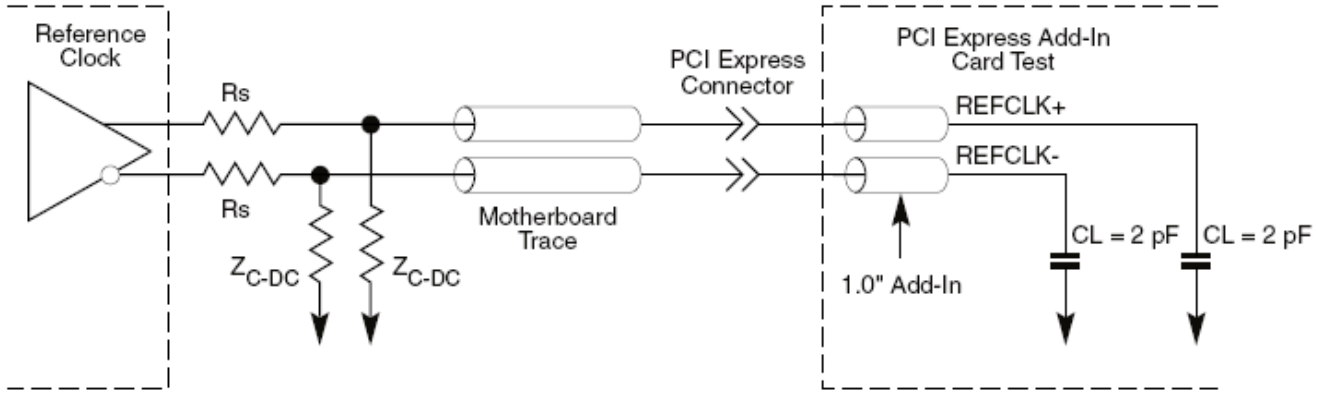


Figure 37. Reference Clock System Measurement Point and Loading

18. Thermal Characteristics

Heat generated by the chip causes a temperature rise of the package. If the temperature of the chip (Tj, junction temperature) is beyond the design limits, there will be negative effects on operation and the life of the IC package. Heat dissipation, either through a heat sink or electrical fan, is necessary to provide a reasonable environment (Ta, ambient temperature) in a closed case. As power density increases, thermal management becomes more critical. A method to estimate the possible Ta is outlined below.

Thermal parameters are defined as below according to JEDEC standard JESD 51-2, 51-6:

(1) θja (Thermal resistance from junction to ambient), represents resistance to heat flow from the chip to ambient air. This is an index of heat dissipation capability. A lower θja means better thermal performance.

θja=(Tj-Ta)/P

Where Tj is the die junction temperature, Ta is the ambient air temperature,

P is the power dissipation by device (Watts)

(2) θjc (Thermal Resistance Junction-to-Case, ℃/W), measures the heat flow resistance between the die surface and the surface of the package (case). This data is relevant for packages used with external heatsinks.

θjc=(Tj-Tc)/P

Where Tj is the die junction temperature, Tc is the package case temperature.

P is the power dissipation by device (Watts)

(3) Ψjt (Thermal Characterization Parameter: Junction to package top), represents the correlation between the temperature of the chip and the package top.

Ψjt=(Tj-Tt)/P

Where Tj is the die junction temperature, Tt is the top of package temperature.

P is the power dissipation by the device (Watts)

Thermal Terminology

The major thermal dissipation paths can be illustrated as following:

Tj: The maximum junction temperature

Ta: The ambient or environment temperature

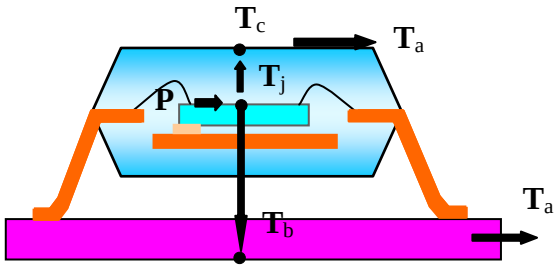
Tc: The maximum compound surface temperature

Tb: The maximum surface temperature of PCB bottom

P: Total input power

PQFP Junction to ambient thermal resistance, θja, defined as:

$$\theta JA = \frac{TJ - TA}{P}$$



Thermal Dissipation of PQFP Package

18.1. Thermal Operating Range

Table 203. Thermal Operating Range

Parameter	SYM	Condition	Min	Typ.	Max	Units
Junction Operating Temperature	Tj	-	0	-	125	°C
Ambient Operating Temperature	Ta	4-layer FR4 PCB (without heat sink)	0	25	65	°C

Note: PCB conditions (JEDEC JESD51-7). Dimensions: 120mm x 90mm. Thickness: 1.6mm.

18.2. Thermal Parameters

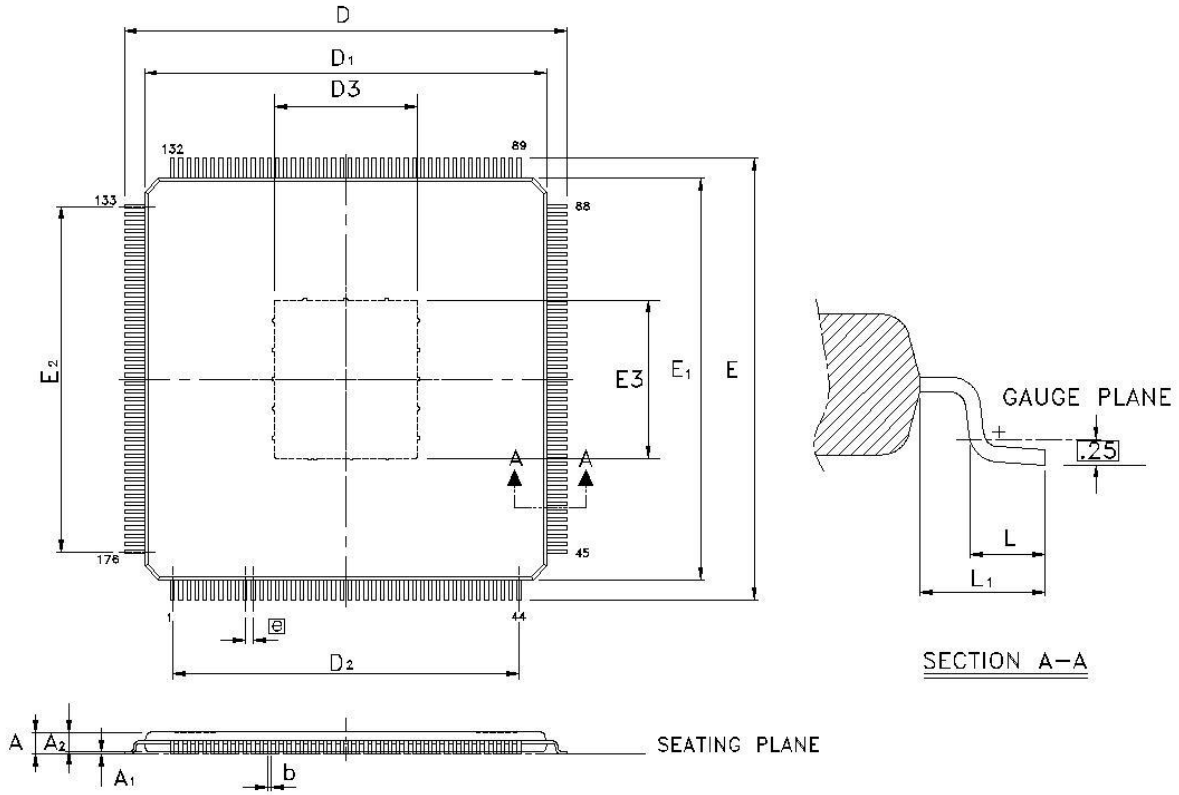
Table 204. Thermal Parameters

Parameter	SYM	Condition	Air Flow 0 m/s	Air Flow 1 m/s	Air Flow 2 m/s	Air Flow 3 m/s	Units
Thermal Resistance: Junction to Ambient	θja	4-layer FR4 PCB	15.8	12.3	11.2	10.6	°C/W
Thermal Characterization: Junction to Package Top	Ψjt	4-layer FR4 PCB	1.8	-	-	-	°C/W
Thermal Resistance: Junction to Case	θjc	4-layer FR4 PCB	8.2	-	-	-	°C/W

Note: PCB conditions (JEDEC JESD51-7). Dimensions: 120mm x 90mm. Thickness: 1.6mm.

19. Mechanical Dimensions

Thermal Enhance Thin Profile Plastic Quad Flat Package 176 Leads 20x20mm² Outline



19.1. Mechanical Dimensions Notes

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.20	—	—	0.047
A_1	0.05	—	0.15	0.002	—	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.13	0.18	0.23	0.005	0.007	0.009
D	22.00BSC			0.866BSC		
D_1	20.00BSC			0.787BSC		
D_2	17.20BSC			0.677BSC		
D_3	5.95	6.20	6.45	0.234	0.244	0.254
E	22.00BSC			0.866BSC		
E_1	20.00BSC			0.787BSC		
E_2	17.20BSC			0.677BSC		
E_3	5.75	6.00	6.25	0.226	0.236	0.246
e	0.40BSC			0.016BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00 REF			0.039 REF		

Notes：

1. CONTROLLING DIMENSION：MILLIMETER(mm).
2. REFERENCE DOCUMENTL：JEDEC MS-26.

20. Ordering Information

Table 205. Ordering Information

Part Number	Package	Status
RTL8197D-CG	Thermal Enhance Thin Profile Plastic Quad Flat Package 176 'Green' Package	Mass production

Note: See page 5 for 'Green' package identification information.

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