RTL8196E-VE1-CG
RTL8196E-VE2-CG
RTL8196E-VE3-CG

5-PORT 10/100M ETHERNET ROUTER NETWORK PROCESSOR

Draft DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the software engineer's reference and provides detailed programming information.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
D1.0	2013/04/19	First release.
D1.1	2013/07/17	Update AC/DC data

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1. General Description

The RTL8196E-VE1/2/3-CG is an integrated System-on-a-Chip (SoC) Application Specific Integrated Circuit (ASIC) L2 5-Port Ethernet switch. An RLX4181 CPU is embedded and the clock rate can be up to 400MHz. To improve computational performance, a 16Kbyte I-Cache, 8Kbyte D-Cache, 16Kbyte I-MEM, and 8Kbyte D-MEM are provided. A standard 5-signal P1149.1 compliant EJTAG test interface is supported for CPU testing and software development.

The RTL8196E-VE1/2/3 provide embedded DRAM by MCM technology. The DRAM size could be 8M, 16M or 32M byte for different mode type. Please refer to the ordering Information.

The RTL8196E-VE1/2/3 provides five ports (ports 0~4), integrated with five physical layer transceivers for 10Base-T and 100Base-TX. Each port of the RTL8196E-VE1/2/3 may be configured as a LAN or WAN port.

The RTL8196E-VE1/2/3 supports flexible IEEE 802.3x full-duplex flow control and optional half-duplex backpressure control. For full-duplex, standard IEEE 803.3x flow control will enable pause ability only when both sides of UTP have auto-negotiation ability and have enabled pause ability. The RTL8196E-VE1/2/3 also provides optional forced mode IEEE 802.3x full-duplex flow control. Based on optimized packet memory management, the RTL8196E-VE1/2/3 is capable of Head-Of-Line blocking prevention.

L2 Switch Features: The RTL8196E-VE1/2/3 contains a 1024-entry address look-up table with a 10-bit 4-way XOR hashing algorithm for address searching and learning. Auto-aging of each entry is provided and the aging time is around 300~450 seconds.

The RTL8196E-VE1/2/3 supports IEEE 802.3az, also known as Energy Efficient Ethernet (EEE). IEEE 802.3az operates with the IEEE 802.3 Media Access Control (MAC) Sublayer to support operation in Low Power Idle mode. When the Ethernet network is in low link utilization, EEE allows systems on both sides of the link to save power. Green Ethernet power saving provides: link-on and dynamic detection of cable length, and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption. The RTL8196E-VE1/2/3 also implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected.

For peripheral interfaces, two 16550-compatible UARTs are supported, and a 16-byte FIFO buffer is provided. USB OTG (On-The-Go) controllers are embedded in the RTL8196E-VE1/2/3 to provide OTG functionality. In addition, one USB PHY is embedded in the RTL8196E-VE1/2/3.

An MDI/MDIX auto crossover function is supported. For accessing high-speed devices, the RTL8196E-VE1/2/3 provides one PCI Express host to access a PCI Express interface.

The RTL8196E-VE1/2/3 requires only a single 25MHz crystal or 40MHz clock input for the system PLL. The RTL8196E-VE1/2/3 also has two hardware timers and one watchdog timer to provide accurate timing and watchdog functionality. For extension and flexibility, the RTL8196E-VE1/2/3 supports up to 16 GPIO pins.

The RTL8196E-VE1/2/3 is provided in a Low Profile Plastic Quad Flat Package, 128-Lead (LQFP128) package and requires only a 3.3V external power supply. The built-in SWR or LDO 3.3V to 1.0V can be used for the RTL8196E-VE1/2/3 system core power.

2. Features

- SOC
  - Embedded RISC CPU, RLX4181 with 16Kbyte I-Cache, 8Kbyte D-Cache, 16Kbyte I-MEM, 8Kbyte D-MEM
  - Supports MIPS-1 ISA, MIPS16 ISA
  - Clock Rate: 400MHz
  - Provides a standard P1149.1 EJTAG test port
  - Supports RLX4181 CPU suspend mode
- L2 Capabilities
  - Five Ethernet MAC switch with five IEEE 802.3 10/100M physical layer transceivers
  - Non-blocking wire-speed reception and transmission and non-head-of-line-blocking/forwarding
  - Internal 256Kbit SRAM for packet buffering
  - Internal 1024 entry 4-way hash L2 look-up table
  - Supports source and destination MAC address filtering
- CPU Interface (NIC)
  - Supports BSD mbuf-like packet structure with adjustable cluster size (128-byte to 2Kbyte) to provide optimum memory utilization
  - The NIC DMA supports multiple-descriptor-ring architecture for QoS applications
- Peripheral Interfaces
  - Supports PCI Express Host with integrated PHY
  - One PCI Express PHY embedded
  - Supports one-port USB
    - USB 2.0 Host or Device
  - One USB PHY embedded
  - Supports two 16550 UARTs
  - Supports up to 16 GPIO pins
- Memory Interfaces
  - Serial Flash (SPI Type)
    - Supports one bank and dual I/O channels for SPI Flash application
    - Each Flash bank could be configured as 256K/512K/1M/2M/4M/8M/16M Bytes
    - Boot up from SPI flash is supported
  - Provide embedded MCM DRAM
    - Data bus : 16 bits
    - Provide different DRAM size model:
      RTL8196E-VE1: 8Mbyte SDR DRAM
      RTL8196E-VE2: 16Mbyte SDR DRAM
      RTL8196E-VE3: 32Mbyte DDR1 DRAM
- Supports Green Ethernet
  - Cable length power saving
  - Link down power saving
- Supports IEEE 802.3az Energy Efficient Ethernet ability for 100Base-TX in full duplex operation and 10Base-T in full/half duplex mode

- Other Added-Value Features
  - Supports Link Down Power Saving in Ethernet PHYceivers
  - Supports two hardware timers and one watchdog timer
  - Per-port configurable auto-crossover function
  - Built-in internal ROM booting
  - Single 25MHz crystal or 40MHz clock input
- Built-in SWR/LDO
  - LDO for DDR1/DDR2
    - DDR1 DRAM: 3.3V to 2.5V
    - DDR2 DRAM: 3.3V to 1.8V
  - SWR or LDO for Core Power
    - SWR or LDO 3.3V to 1.0V
- LQFP128 package

3. System Applications

- IEEE 802.11b/g/n AP/Router
- Wired Router

4. Block Diagram

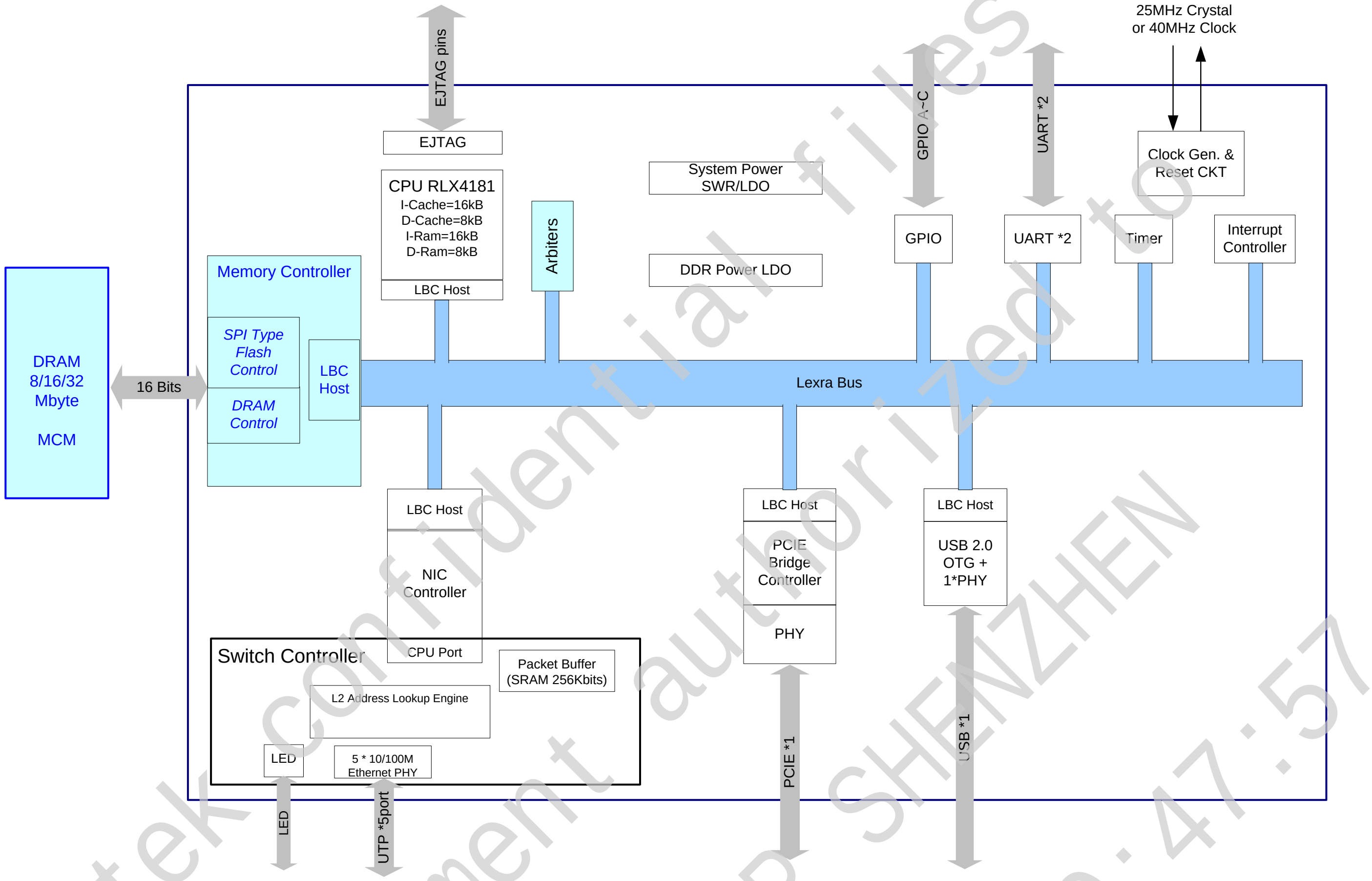


Figure 1. Block Diagram

5. Pin Assignments

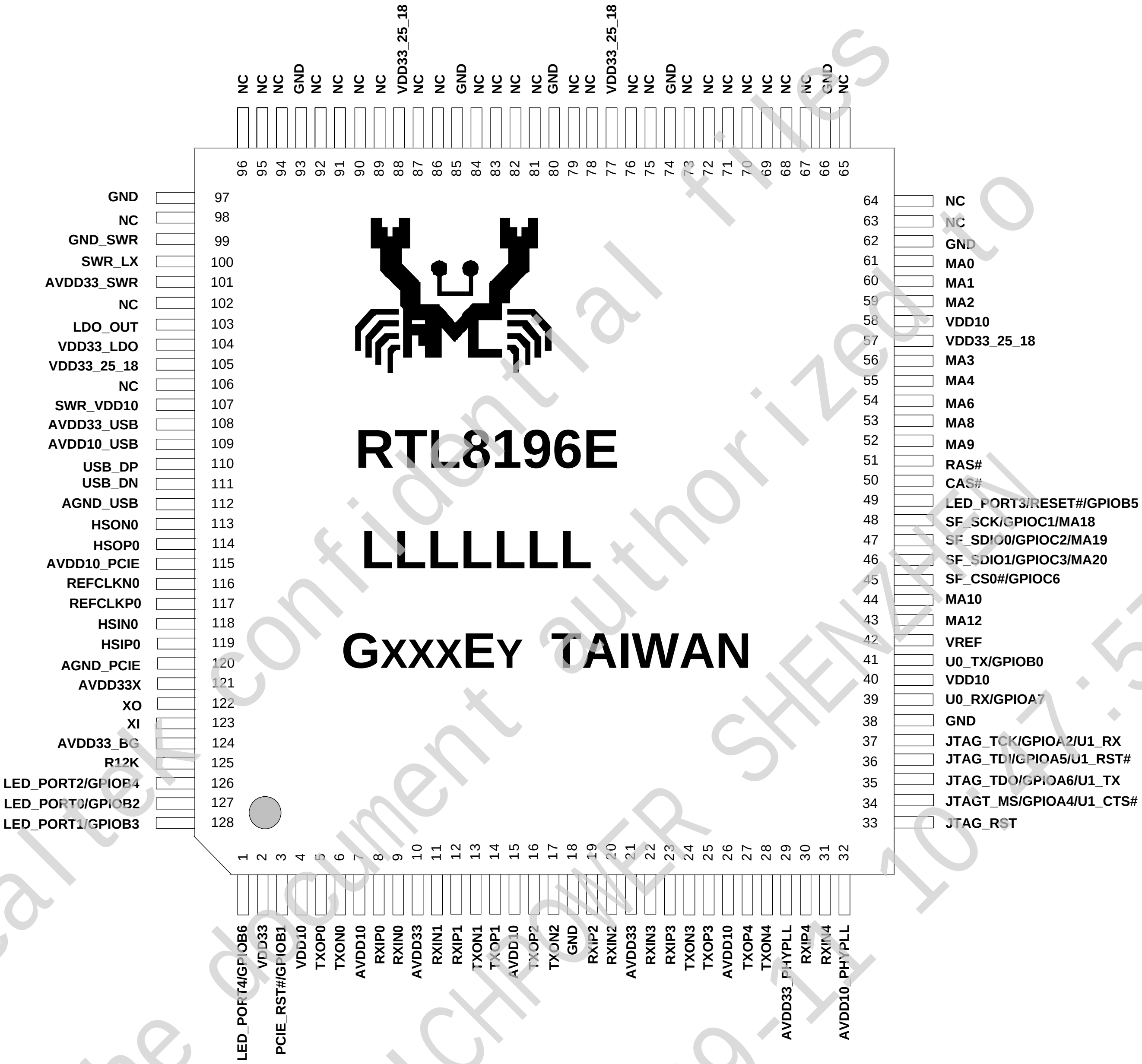


Figure 2. Pin Assignments

5.1. Package Identification

Green package is indicated by the 'G' in GxxxEY (Figure 2).
Embedded memory size indicate by Y in GxxxEY (Figure 2).

Y=1 : 8M byte SDR DRAM embedded
Y=2 : 16M byte SDR DRAM embedded
Y=3 : 32M byte DDR1 DRAM embedded

6. Pin Descriptions

In this section the following abbreviations are used:

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified ‘Upon Reset’ time.

I: Input	AI: Analog Input
O: Output	AO: Analog Output
I/O: Bi-Directional Input/Output	AI/O: Analog Bi-Directional Input/Output
P: Digital Power	AP: Analog Power
G: Digital Ground	AG: Analog Ground
I_{PD}: Input Pin With Pull-Down Resistor	I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

Table 1. Pin Descriptions

Pin Name	Pin No.	Type	Description
Clock & Reset			
XI	123	I	25MHz Crystal Clock, 25MHz External Clock Input, or 40MHz External Clock Input.
XO	122	O	25MHz Crystal Clock Output.
RESET#	49	I	System External Reset.
10/100M Ethernet Physical Layer			
TXOP_P[4:0] TXON_P[4:0]	27, 25, 16, 14, 5 28, 24, 17, 13, 6	AO	10/100M Ethernet Physical Layer Transmit Pair. For differential data transmission.
RXIP_P[4:0] RXIN_P[4:0]	30, 23, 19, 12, 8 31, 22, 20, 11, 9	AI	10/100M Ethernet Physical Layer Receive Pair. For differential data reception.
Memory Interface			
MA12 MA[10:8] MA6 MA[4:0]	43, 44, 52, 53, 54, 55, 56, 5, 60	O	Address of embedded DRAM., Only provided for power on strapping setting purpose.
DDR DRAM Control			
RAS#	51	O	Raw Address Strobe (RAS#) for SDR/DDR DRAM.. Only provided for power on strapping setting purpose.
CAS#	51	O	Column Address Strobe for SDR/DDR DRAM. Only provided for power on strapping setting purpose.
VREF	42	AI	Voltage Reference 1.25V for DDR1. Voltage Reference 0.9V for DDR2.
Serial SPI Flash Control			
SF_CS0#	45	O	SPI Serial Flash Chip Select 0.

Pin Name	Pin No.	Type	Description
SF_SDIO[1:0]	46, 47	I/O	SPI Serial Flash Serial Data Input/Output.
SF_SCK	48	O	SPI Serial Flash Serial Clock Output. SF_SDI will be driven on the falling edge. SF_SDO will be latched on the rising edge.
UART			
U0_TX	41	O	Data Transmit Serial Output of UART0.
U0_RX	39	I_{PU}	Data Receive Serial Input of UART0.
U1_TX	35	O	Data Transmit Serial Output of UART1.
U1_RX	37	I_{PU}	Data Receive Serial Input of UART1.
U1_RTS#	36	O	Request to Send of UART1.
U1_CTS#	34	I	Clear to Send of UART1.
JTAG			
JTAG_TCK	37	I_{PU}	JTAG Test Clock.
JTAG_TMS	34	I_{PU}	JTAG Test Mode Select.
JTAG_TDO	35	O	JTAG Test Data Output.
JTAG_TDI	36	I_{PU}	JTAG Test Data In.
JATG_RST	33	I_{PU}	JTAG Test Reset
LED			
LED_PORT[4:0]	1, 49, 126, 128, 127	O	Ethernet LED. Link/Activity Status of 5 Ports (Low Active).
GPIO			
GPIOA[7:4] GPIOA2	39, 35, 36, 34, 37	I/O	GPIO Port A.
GPIOB[6:0]	1, 49, 126, 128, 127, 3, 41	I/O	GPIO Port B.
GPIOC6 GPIOC[3:1]	46, 46, 47, 48	I/O	GPIO Port C.
USB Host 2.0			
USB_DP	110	AI/O	USB Host/OTG Device Data Plus Pin.
USB_DN	111	AI/O	USB Host/OTG Device Data Minus Pin.
PCI Express Interface			
HSON0 HSOP0	113 114	AO	Transmitter Differential Pair.
HSIN0 HSIP0	118 119	AI	Receiver Differential Pair.
REFCLKN0 REFCLKP0	116 117	AO	Reference Clock Differential Pair.
PCIE_RST#	3	O	PCI Express Reset.
Reference Voltage			
R12K	125	AI	Reference Voltage for System. 12K 1% resistance pull down.
Power & GND			
VDD33	2	P	Digital I/O Power Supply 3.3V.

Pin Name	Pin No.	Type	Description
VDD33_25_18	57, 77, 88, 105	P	Memory I/O Power Supply 3.3V, 2.5V, or 1.8V. SDR DRAM: 3.3V DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
AVDD33	10, 21	AP	Ethernet Analog Power Supply 3.3V.
AVDD33_PHYPLL	29	AP	Ethernet PHY PLL Power 3.3V.
VDD10	4, 40, 58	P	Digital Core Power Supply 1.0V.
AVDD10	7, 15, 26	AP	Ethernet Analog Power Supply 1.0V.
AVDD33X	121	AP	25M Crystal Power 3.3V.
AVDD33_BG	124	AP	System Bandgap Power Supply 3.3V.
AVDD10_PCIE	115	AP	PCI Express Analog Power Supply 1.0V.
AVDD10_PHYPLL	32	AP	Ethernet PHY PLL Power 1.0V.
AVDD33_USB	108	AP	USB 2.0 Analog Power 3.3V.
AVDD10_USB	109	AP	USB 2.0 Analog Power 1.0V.
GND	18, 38, 62, 66, 74, 80, 85, 93, 97	G	System GND.
GND_SWR	99	AG	Switching Regulator GND.
AGND_PCIE	120	AG	PCI Express GND.
AGND_USB	112	AG	USB GND.
SWR & LDO			
VDD33_LDO	104	AP	LDO Power Supply 3.3V Input for DDR.
LDO_OUT	103	AP	LDO Output Power for DDR. DDR1 DRAM: 2.5V DDR2 DRAM: 1.8V
AVDD33_SWR	101	AP	SWR Power Supply 3.3V Input.
SWR_LX	100	AP	SWR Power Supply Output.
SWR_VDD10	107	AP	SWR Power supply 1.0V input
Not Connected Pin			
NC	63, 64, 65, 67, 68, 69, 70, 71, 72, 73, 75, 76, 78, 79, 81, 82, 83, 84, 86, 87, 89, 90, 91, 92, 94, 95, 96, 98, 102, 106	-	Not Connected.

6.1. Configuration Upon Power On Strapping

All mode configuration pins are internal pull low. The 1.0V digital core power input pin voltage is up to 0.7V on system power-on. The strap data will be latched after a delay of 300ms.

Table 2. Configuration Upon Power On Strapping

H/W Pin Name	Configuration Name	Pin No	Description
U0_TX	ck_cpu_freq_sel[0]	41	CPU Clock Configuration. 0: 400MHz 1: 380MHz
MA10, MA9	ck_freq_sel[1:0]	44, 52	DRAM Clock Rate Configuration. 00: 156.25MHz 01: Reserved 10: Reserved 11: Reserved
MA2, MA1, MA0	Bootpinsel[2:0]	59, 60, 61	Boot Pin Selection for the RTL8196E-VE1/2/3Boot Method. 000: SPI 001: Reserved 010: Reserved 011: Reserved 100: ROM booting Mode for SDR/DDR 16MB 101: ROM booting Mode for SDR/DDR 32MB 110: ROM booting Mode for SDR 8MB or DDR 64MB 111: ROM booting Mode for SDR 2MB or DDR 128MB
MA3	DDR_TYPE	56	DDR DRAM Type. 0: DDR2 1: DDR1
MA4	External_Reset	55	Enable External Reset Pin. 0: Disable 1: Enable
MA8	DRAM_TYPE	53	DRAM Type. 0: SDR 1: DDR
MA12	Sel_40M	43	System Clock Source Select. 0: 25MHz 1: 40MHz

6.2. Shared I/O Pin Mapping

Table 3. Shared I/O Pin Mapping

Pin	GPIO	Memory	EJTAG	LED	UART	Reset
37	GPIOA[2]	-	JTAG_TCK	-	U1_RX	-
34	GPIOA[4]	-	JTAG_TMS	-	U1_CTS#	-
36	GPIOA[5]	-	JTAG_TDI	-	U1_RTS#	-
35	GPIOA[6]	-	JTAG_TDO	-	U1_TX	-
39	GPIOA[7]	-	-	-	U0_RX	-
41	GPIOB[0]	-	-	-	U0_TX	-
3	GPIOB[1]	-	-	-	-	PCIE_RST#
127	GPIOB[2]	-	-	LED_PORT0	-	-

Pin	GPIO	Memory	EJTAG	LED	UART	Reset
128	GPIOB[3]	-	-	LED_PORT1	-	-
126	GPIOB[4]	-	-	LED_PORT2	-	-
49	GPIOB[5]	-	-	LED_PORT3	-	RESET#
1	GPIOB[6]	-	-	LED_PORT4	-	-
48	GPIOC[1]	SF_SCK	-	-	-	-
47	GPIOC[2]	SF_SDIO0	-	-	-	-
46	GPIOC[3]	SF_SDIO1	-	-	-	-
45	GPIOC[6]	SF_CS0#	-	-	-	-

7. Memory Controller

The RTL8196E-VE1/2/3integrates a memory control module to access external DDR DRAM, SDR DRAM, and Flash memory.

The interface is designed for DDR-compliant DDR DRAM, and designed for PC133 or PC166-compliant SDR DRAM, and supports auto-refresh mode, which requires a 4096 refresh cycle within 64ms. The DRAM interface supports one chip (MCS0#), and the DRAM size and timing is configurable in registers.

The RTL8196E-VE1/2/3supports one flash memory chip (SF_CS0#). The interface supports SPI flash memory. When Flash is used, the system will boot from KSEG1 at virtual address 0xBFC0_0000 (physical address: 0x1FC0_0000).

7.1. SDR DRAM Control Interface

PC100~PC166-compliant SDR DRAM is supported. The SDR DRAM controller supports Auto Refresh mode, which requires a 4096-cycle refresh each 64ms. The RTL8196E-VE1/2/3provides a maximum of 512Mbit address space (8Mx16x4Banks) and the SDR DRAM size is configurable.

7.1.1. Features

- Interface (Bus Width): 16-bit
- Targeted SDR Frequency: Up to 168MHz
- Supports one Chip Select (MCS0#)
- Supported SDR DRAM Chip Specification
  - Bank Counts: 2, 4
  - Row Counts: 2K (A0~A10), 4K (A0~A11), 8K (A0~A12)
  - Column Counts: 256 (A0~A7), 512 (A0~A8), 1K (A0~A9), 2K (A0~A9, A11)
- Programmable Timing Parameters: tRAS, tRP, tRCD, tCL, tREFI…

7.2. DDR DRAM Controller

7.2.1. Features

- Interface (Bus Width): 16-bit
- Targeted DDR Frequency: Up to 193.75MHz
- Supports one Chip Select (MCS0#)
- Supports both DDR1 and DDR2
- Supported DDR DRAM Chip Specification
  - Bank Counts: 8
  - Row Counts: 4K (A0~A11), 8K (A0~A12), 16K (A0~A13)
  - Column Counts: 512 (A0~A8), 1K (A0~A9), 2K (A0~A9, A11), 4K (A0~A9, A11, A12)
- Programmable Timing Parameters: tRAS, tRP, tRCD, tCL, tREFI…

7.3. SPI Flash Controller

The SPI flash controller is a new design and incorporates new features.

7.3.1. Features

- Targeted SPI flash frequency: Up to 96.875MHz (when DRAM clock is 193.75MHz)
- Supports one chip
- In addition to a programmed I/O interface, also supports a memory-mapped I/O interface for read operation
- Supports Read and Fast Read in memory-mapped I/O mode

7.3.2. Pin Mode and Definition of Serial and Dual I/O

Modes supported on the SPI flash interface:

Serial I/O Mode

- SDI: Flash chip data input pin
- SDO: Flash chip data output pin

Dual I/O Mode

- SDIO0 (SDI): Flash chip data bi-directional pin
- SDIO1 (SDO): Flash chip data bi-directional pin

7.4. Software Register Definitions

7.4.1. Memory Control Register (MCR) (0xB800_1000)

This register does not provide byte access.

Table 4. Memory Control Register (MCR) (0xB800_1000)

Bit	Name	Description	Mode	Default
31	DRAMTYPE	Report the Hardware Strapping Initial Value for DRAM Type. 0: SDR DRAM 1: DDR DRAM	R	0B
30	BOOTSEL	Report the Hardware Strapping Initial Value for Boot Flash Type. 0: Reserved 1: Serial SPI flash	R	0B
29	IPREF	Enable Instruction Prefetch Function. 0: Disable prefetch (also reset buffer status) 1: Enable prefetch (4 words)	RW	0B
28	DPREF	Enable Data Prefetch Function. 0: Disable prefetch (also reset buffer status) 1: Enable prefetch (4 words)	RW	0B
27	IPREF_MODE	Choose Instruction Prefetch Mode. 0: Old prefetch mechanism 1: New prefetch mechanism	RW	0B
26	DPREF_MODE	Choose Data Prefetch Mode. 0: Old prefetch mechanism 1: New prefetch mechanism	RW	0B
25:0	-	Reserved.	-	-

7.4.2. DRAM Configuration Register (DCR) (0xB800_1004)

This register does not provide byte access.

Table 5. DRAM Configuration Register (DCR) (0xB800_1004)

Bit	Name	Description	Mode	Default
31:30	T_CAS	CAS Latency. 00: Latency=2 01: Latency=3 10: Latency=2.5 (only used for DDR) 11: Latency=4 (only used for DDR)	RW	01B
29:28	DBUSWID	DRAM Bus Width. 00: Reserved 01: 16 bit (used for DDR and SDR) 10: Reserved 11: Reserved	RW	01B
27	DCHIPSEL	DRAM Chip Select. 0: CS0# 1: CS0# and CS1#	RW	1B
26:25	ROWCNT	Row Counts. 00: 2K (A0~A10) 01: 4K (A0~A11) 10: 8K (A0~A12) 11: 16K (A0~A13)	RW	00B
24:22	COLCNT	Column Counts. 000: 256 (A0~A7) 001: 512 (A0~A8) 010: 1K (A0~A9) 011: 2K (A0~A9, A11) 100: 4K (A0~A9, A11, A12) 101: Reserved 110: Reserved 111: Reserved	RW	000B
21	BSTREF	Bursted 8 Auto-Refresh Commands (Used for DDR). 0: Disable 1: Enable	RW	0B
20	ARBIT	Enforce Interface Arbitration Take Effect. 0: Reserved 1: Take effect	RW	0B
19	BANKCNT	Bank Counts. 0: 2 banks (used for SDR) 1: 4 banks (used for SDR and DDR)	RW	1B
18	FAST_RX	If RX path turnaround delay is small enough, the memory controller can return read data with reduced latency within 1DRAM clock cycle (used for DDR). 0: Normal path 1: Fast path	RW	0B
17	MR_MODE	Select the Memory Command that Memory Controller Issues (Used for DDR). 0: Mode Register 1: Extended Mode Register	RW	0B
16	DRV_STR	Drive Strength Setting of DRAM Chip (Used for DDR). For this option to be effective, MR_MODE must be first set to 1. 0: Normal 1: Reduced	RW	0B
15:0	-	Reserved.	-	-

7.4.3. DRAM Timing Register (DTR) (0xB800_1008)

This register does not provide byte access.

Table 6. DRAM Timing Register (DTR) (0xB800_1008)

Bit	Name	Description	Mode	Default
31:29	T_RP	tRP Timing Parameter of DRAM. Basic Unit = 1*DRAM_CLK. 000: 1 unit	RW	111B
28:26	T_RCD	tRCD Timing Parameter of DRAM. Basic Unit = 1*DRAM_CLK. 000: 1 unit	RW	111B
25:21	T_RAS	Minimum T_RAS Timing Parameter of DRAM. Basic Unit = 1*DRAM_CLK. 00000: 1 unit	RW	11111B
20:14	T_RFC	tRFC Timing Parameter of DRAM (Refresh Row Cycle Time). Basic Unit = 1*DRAM_CLK. 0000000: 1 unit	RW	1111100B
13:10	T_REFI	tREF Timing Parameter of DRAM (Refresh Row Interval Time). Basic unit = T_REFI_UNIT. 0000: 1 unit 0001: 2 units … 1111: 16 units	RW	0000B
9:7	T_REFI_UNIT	Basic Unit of T_REFI. 000: 32 DRAM_CLK 001: 64 DRAM_CLK 010: 128 DRAM_CLK 011: 256 DRAM_CLK 100: 512 DRAM_CLK 101: 1024 DRAM_CLK 110: 2048 DRAM_CLK 111: 4096 DRAM_CLK	RW	111B
6:4	T_WR	tWR Timing Parameter of DRAM (Write Recovery Time). Basic Unit = 1*DRAM_CLK. 000: 1 unit	RW	111B
3:0	-	Reserved.	-	-

7.4.4. DDR DRAM Calibration Register (DDCR) (0xB800_1050)

This register does not provide byte access.

Table 7. DDR DRAM Calibration Register (DDCR) (0xB800_1050)

Bit	Name	Description	Mode	Default
31	CAL_MODE	Run-Time Calibration Mode. 0: Use analog DLL calibration 1: Use digital delay line calibration	RW	0B
30	SW_CAL_RDY	Ready for Digital Delay Line Calibration. 0: Not ready 1: Ready	R	0B
29:25	DQS0_TAP[4:0]	Selects 32-Tap Delay Line for LDQS, which is Data Strobe for DQ[7:0] Reception. 00000: 1^{st} tap 00001: 2^{nd} tap … 11111: 32^{nd} tap *Note: 32-tap delay is around 2.5ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
24:20	DQS1_TAP[4:0]	Selects 32-Tap Delay Line for UDQS, which is Data strobe for DQ[15:8] Reception. 00000: 1^{st} tap 00001: 2^{nd} tap … 11111: 32^{nd} tap *Note: 32-tap delay is around 2.5ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
19:15	DQS0_EN_TAP[4:0]	Selects 32-Tap Delay Line for the Internal LDQS_EN Window. 00000: 1^{st} tap 00001: 2^{nd} tap … 11111: 32^{nd} tap *Note: 32-tap delay is around 2.5ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
14:10	DQS1_EN_TAP[4:0]	Selects 32-Tap Delay Line for the Internal UDQS_EN Window. 00000: 1^{st} tap 00001: 2^{nd} tap … 11111: 32^{nd} tap *Note: 32-tap delay is around 2.5ns, which is chosen as it is around 1/2 the DDR cycle (1 tap is around 78.125ps).*	RW	00000B
9:0	-	Reserved.	-	-

7.4.5. SPI Flash Configuration Register (SFCR) (0xB800_1200)

This register does not provide byte access.

Table 8. SPI Flash Configuration Register (SFCR) (0xB800_1200)

Bit	Name	Description	Mode	Default
31:29	SPI_CLK_DIV	SPI Operating Clock Rate Selection. The value defines the divisor to generate the SPI clock. SPI Clock = (DRAM Clock)/(SPI_CLK_DIV). 000: DIV=2 001: DIV=4 010: DIV=6 011: DIV=8 100: DIV=10 101: DIV=12 110: DIV=14 111: DIV=16	RW	111B
28	RBO	Serial Flash Read Byte Ordering. 0: The byte order is from low to high 1: The byte order is from high to low	RW	1B
27	WBO	Serial Flash Write Byte Ordering. 0: The byte order is from low to high 1: The byte order is from high to low	RW	1B
26:22	SPI_TCS	SPI Chip Deselect Time. Basic Unit = 1*DRAM Clock Cycle. 00000: 1 unit 00001: 2 units, etc.	RW	11111B
21:0	-	Reserved.	-	-

7.4.6. SPI Flash Configuration Register 2 (SFCR2) (0xB800_1204)

This register does not provide byte access.

Table 9. SPI Flash Configuration Register 2 (SPCR2) (0xB800_1204)

Bit	Name	Description	Mode	Default
31:24	SFCMD	SPI Flash 8-Bit Command Code of a Read Transaction. Example: 'Read Data' is 0x03. 'Fast Read' is 0x0B.	RW	03H
23:21	SFSIZE	SPI Flash Size. 000: 128Kbyte 001: 256Kbyte 010: 512Kbyte 011: 1Mbyte 100: 2Mbyte 101: 4Mbyte 110: 8Mbyte 111: 16Mbyte	RW	111B
20	RD_OPT	SPI Flash Sequential Access Optimization. 0: No optimization 1: Optimization for sequential access	RW	0B
19:18	CMD_IO	SPI Flash I/O Mode Selection for the Command Phase of a Read Transaction. 00: Serial I/O (8 cycles) 01: Dual I/O (4 cycles) 10: Reserved 11: Reserved	RW	00B

Bit	Name	Description	Mode	Default
17:16	ADDR_IO	SPI Flash I/O Mode Selection for the Address Phase of a Read Transaction. 00: Serial I/O (24 cycles) 01: Dual I/O (12 cycles) 10: Reserved 11: Reserved	RW	00B
15:13	DUMMY_CYCLES	SPI Flash Inserted Dummy Cycles for the Dummy Cycle Phase of a Read Transaction. 000: 0 cycle 001: 2 cycles 010: 4 cycles 011: 6 cycles 100: 8 cycles 101: 10 cycles 110: 12 cycles 111: 14 cycles	RW	000B
12:11	DATA_IO	SPI Flash I/O Mode Selection for the Data Phase of a Read Transaction (Assume 8*N Cycles). 00: Serial I/O (8*N cycles) 01: Dual I/O (4*N cycles) 10: Reserved 11: Reserved	RW	00B
10	HOLD_TILL_SFDR2	If this bit is '1', it indicates the write operation to this register (SFCR2) will not take effect immediately but will be delayed until another write operation to SFDR2.	RW	0B
9:0	-	Reserved.	-	-

7.4.7. SPI Flash Control & Status Register (SFCSR) (0xB800_1208)

This register does not provide byte access.

Table 10. SPI Flash Control & Status Register (SFCSR) (0xB800_1208)

Bit	Name	Description	Mode	Default
31	SPI_CSB0	SPI Flash Chip Select 0. 0: Active 1: Not active	RW	1B
30	SPI_CSB1	SPI Flash Chip Select 1. 0: Active 1: Not active	RW	1B
29:28	LEN	SPI Read/Write Data Length (Unit=Byte). 00: 1 byte 01: 2 bytes 10: 3 bytes 11: 4 bytes	RW	11B
27	SPI_RDY	SPI Flash Operation Busy Indication Flag. 0: Busy (operation in progress) 1: Ready (idle or SPI access command is ready)	R	1B
26:25	IO_WIDTH	SPI Flash I/O Mode Selection of a Transaction. 00: Serial I/O 01: Dual I/O 10: Reserved 11: Reserved	RW	00B
24	CHIP_SEL	Chip Selection. 0: CS0# 1: Reserved	RW	0B
23:16	CMD_BYTE	SPI Flash 8-Bit Command Code of a Transaction (This Field is Only Used in MMIO Mode). Example: 'Read Data' is 0x03. 'Read ID' is 0x9F.	RW	0B
15:0	-	Reserved.	-	-

7.4.8. SPI Flash Data Register (SFDR) (0xB800_120C)

This register does not provide byte access.

This configuration register is used for the PIO (Programmed I/O) access mode.

Table 11. SPI Flash Data Register (SFDR) (0xB800_120C)

Bit	Name	Description	Mode	Default
31:24	Data3	Read/Write Data Byte 3.	RW	0B
23:16	Data2	Read/Write Data Byte 2.	RW	0B
15:8	Data1	Read/Write Data Byte 1.	RW	0B
7:0	Data0	Read/Write Data Byte 0.	RW	0B

7.4.9. SPI Flash Data Register 2 (SFDR2) (0xB800_1210)

This register does not provide byte access.

This configuration register is intended to be used under MMIO access mode.

Table 12. SPI Flash Data Register 2 (SFDR2) (0xB800_1210)

Bit	Name	Description	Mode	Default
31:24	Data3	Read/Write Data Byte 3.	RW	0B
23:16	Data2	Read/Write Data Byte 2.	RW	0B
15:8	Data1	Read/Write Data Byte 1.	RW	0B
7:0	Data0	Read/Write Data Byte 0.	RW	0B

8. Peripheral and MISC Controls

8.1. Interrupt Control Registers

The RTL8196E-VE1/2/3provides fourteen hardware-interrupt inputs, IRQ2 to IRQ15. The Global Interrupt Mask Register (GIMR) enables/disables an interrupt feature from the Timer, USB, UART, PCIe, Switch Core, or GPIO modules. The Global Interrupt Status Register (GISR) shows the pending interrupt status. The Interrupt Routing Register (IRR) controls the mappings of the IRQ2 to IRQ15 interrupt sources.

Table 13. Interrupt Control Register Address Mapping (Base: 0xB800_3000)

Offset	Size (byte)	Name	Description
00	4	GIMR	Global Interrupt Mask Register.
04	4	GISR	Global Interrupt Status Register.
0C	4	IRR1	Interrupt Routing Register 1.
10	4	IRR2	Interrupt Routing Register 2.
14	4	IRR3	Interrupt Routing Register 3.

8.1.1. Global Interrupt Mask Register (GIMR) (0x B800_3000)

Table 14. Global Interrupt Mask Register (GIMR) (0x B800_3000)

Bit	Bit Name	Description	RW	Default
31:28	-	Reserved.	RW	0
27	CPU_WAKE_IE	CPU Wake-Up Interrupt Enable.	RW	0
26	-	Reserved.	RW	0
25	USB1_WAKE_IE	USB Port 1 OTG (On-The-Go) Wake-Up Interrupt Enable.	RW	0
24:22	-	Reserved.	RW	0
21	PCIE0_IE	PCIe Port 0 Host Interface Interrupt Enable.	RW	0
20:17	-	Reserved.	RW	0
16	GPIO_ABCD_IE	GPIO Port A, B, C, D Interrupt Enable.	RW	0
15	SW_IE	Switch Core Interrupt Enable.	RW	0
14	-	Reserved.	RW	0
13	UART1_IE	UART 1 Interrupt Enable.	RW	0
12	UART0_IE	UART 0 Interrupt Enable.	RW	0
11	USB_O_IE	USB 2.0 OTG Interrupt Enable.	RW	0
10	-	Reserved.	RW	0
9	TC1_IE	Timers/Counters #1 Interrupt Enable.	RW	0
8	TC0_IE	Timers/Counters #0 Interrupt Enable.	RW	0
7:0	-	Reserved.	RW	0

8.1.2. Global Interrupt Status Register (GISR) (0x B800_3004)

Table 15. Global Interrupt Status Register (GISR) (0x B800_3004)

Bit	Bit Name	Description	RW	Default
31:28	-	Reserved.	R	0
27	CPU_WAKE_IP	CPU Wake-Up Interrupt Pending Flag.	R	0
26	-	Reserved.	R	0
25	USB1_WAKE_IP	USB Port 1 OTG (On-The-Go) Wake-Up Interrupt Pending Flag.	R	0
24:22	-	Reserved.	R	0
21	PCIE0_IP	PCIe Port 0 Host Interface Interrupt Pending Flag.	R	0
20:17	-	Reserved.	R	0
16	GPIO_ABCD_IP	GPIO Port A, B, C, D Interrupt Pending Flag.	R	0
15	SW_IP	Switch Core Interrupt Pending Flag.	R	0
14	-	Reserved.	R	0
13	UART1_IP	UART 1 Interrupt Pending Flag.	R	0
12	UART0_IP	UART 0 Interrupt Pending Flag.	R	0
11	USB_O_IP	USB 2.0 OTG Interrupt Pending Flag.	R	0
10	-	Reserved.	R	0
9	TC1_IP	Timers/Counters #1 Interrupt Pending Flag.	R	0
8	TC0_IP	Timers/Counters #0 Interrupt Pending Flag.	R	0
7:0	-	Reserved.	R	0

8.1.3. Interrupt Routing Register 1 (IRR1) (0xB800_300C)

Table 16. Interrupt Routing Register 1 (IRR1) (0xB800_300C)

Bit	Bit Name	Description	RW	Default
31:28	SW_RS[3:0]	Switch Core Interrupt Route Select.	RW	0
27:24	-	Reserved.	RW	0
23:20	UART1_RS[3:0]	UART 1 Interrupt Route Select.	RW	0
19:16	UART0_RS[3:0]	UART 0 Interrupt Route Select.	RW	0
15:12	USB_O_RS[3:0]	USB 2.0 OTG Interrupt Route Select.	RW	0
11:8	-	Reserved.	RW	0
7:4	TC1_RS[3:0]	Timers/Counters #1 Interrupt Route Select.	RW	0
3:0	TC0_RS[3:0]	Timers/Counters #0 Interrupt Route Select.	RW	0

8.1.4. Interrupt Routing Register 2 (IRR2) (0xB800_3010)

Table 17. Interrupt Routing Register 2 (IRR2) (0xB800_3010)

Bit	Bit Name	Description	RW	Default
31:28	-	Reserved.	RW	0
27:24	-	Reserved.	RW	0
23:20	PCIE0_RS[3:0]	PCIe Port 0 Interface Interrupt Route Select.	RW	0
19:8	-	Reserved.	RW	0
7:4	-	Reserved.	RW	0
3:0	GPIO_ABCD_RS[3:0]	GPIO Port A, B, C, D Interrupt Route Select.	RW	0

8.1.5. Interrupt Routing Register 3 (IRR3) (0xB800_3014)

Table 18. Interrupt Routing Register 3 (IRR3) (0xB800_3014)

Bit	Bit Name	Description	RW	InitVal
31:20	-	Reserved.	RW	0
19:16	-	Reserved.	RW	0
15:12	CPU_WAKE_RS[3:0]	CPU Wake-Up Interrupt Route Select.	RW	0
11:8	-	Reserved.	RW	0
7:4	USB1_WAKE_RS[3:0]	USB Port 1 OTG (On-The-Go) Wake-Up Interrupt Route Select.	RW	0
3:0	-	Reserved.	RW	0

8.2. Timer

The RTL8196E-VE1/2/3provides two sets of hardware timers and one watchdog timer. Each timer can be configured to timer mode or counter mode. Counter mode means the timer only times-out once. The initial time-out values are configured via TC0DATA and TC1DATA. The current count values are shown in TC0CNT and TC1CNT. The Clock Division Base Register (CDBR) defines the base clock for counting, and is based on a multiple of the system clock. The Timer/Counter Interrupt Register (TCIR) controls the interrupt resulting from a timer time-out. The Watchdog timer is controlled by the Watchdog Timer Control Register (WDTCNR).

8.2.1. Timer Control Address Mapping (Base: 0xB800_3100)

Table 19. Timer Control Address Mapping (Base: 0xB800_3100)

Offset	Size (byte)	Name	Description
0x00	4	TC0DATA	Timer/Counter 0 Data Register. It specifies the time-out duration.
0x04	4	TC1DATA	Timer/Counter 1 Data Register. It specifies the time-out duration.
0x08	4	TC0CNT	Timer/Counter 0 Count Register.
0x0C	4	TC1CNT	Timer/Counter 1 Count Register.
0x10	4	TCCNR	Timer/Counter Control Register.

Offset	Size (byte)	Name	Description
0x14	4	TCIR	Timer/Counter Interrupt Register.
0x18	4	CDBR	Clock Division Base Register.
0x1C	4	WDTCNR	Watchdog Timer Control Register.

8.2.2. Timer/Counter 0 Data Register (0xB800_3100)

Table 20. Timer/Counter 0 Data Register (0xB800_3100)

Bit	Name	Description	RW	Default
31:4	TC0Data[27:0]	The Timer or Counter Initial Value. Counter values of 0 and 1 are not allowed.	RW	0H
3:0	-	Reserved.	-	-

8.2.3. Timer/Counter 1 Data Register (0xB800_3104)

Table 21. Timer/Counter 1 Data Register (0xB800_3104)

Bit	Name	Description	RW	Default
31:4	TC1Data[27:0]	The Timer or Counter Initial Value. Counter values of 0 and 1 are not allowed.	RW	0H
3:0	-	Reserved.	-	-

8.2.4. Timer/Counter 0 Counter Register (0xB800_3108)

Table 22. Timer/Counter 0 Counter Register (0xB800_3108)

Bit	Name	Description	RW	Default
31:4	TC0Value[27:0]	The Timer or Counter Value. Count incremented by 1 from 0.	R	-
3:0	-	Reserved.	-	-

8.2.5. Timer/Counter 1 Counter Register (0xB800_310C)

Table 23. Timer/Counter 1 Counter Register (0xB800_310C)

Bit	Name	Description	RW	Default
31:4	TC1Value[27:0]	The Timer or Counter Value. Count incremented by 1 from 0.	R	-
3:0	-	Reserved.	-	-

8.2.6. Timer/Counter Control Register (0xB800_3110)

Table 24. Timer/Counter Control Register (0xB800_3110)

Bit	Bit Name	Description	RW	Default
31	TC0En	Timer/Counter 0 Enable.	RW	0
30	TC0Mode	Timer/Counter 0 Mode. 0: Counter mode 1: Timer mode	RW	0
29	TC1En	Timer/Counter 1 Enable.	RW	0
28	TC1Mode	Timer/Counter 1 Mode. 0: Counter mode 1: Timer mode When Mitigation&Timer1 is asserted, this bit should be set to 1 to ensure normal processing.	RW	0
27: 0	-	Reserved.	RW	0

8.2.7. Timer/Counter Interrupt Register (0xB800_3114)

Table 25. Timer/Counter Interrupt Register (0xB800_3114)

Bit	Bit Name	Description	RW	Default
31	TC0IE	Timer/Counter 0 Interrupt Enable.	RW	0
30	TC1IE	Timer/Counter 1 Interrupt Enable. When Mitigation&Timer1 is asserted, this bit should be set as 0 to assure normal processing.	RW	0
29	TC0IP	Timer/Counter 0 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
28	TC1IP	Timer/Counter 1 Interrupt Pending. Write '1' to clear the interrupt.	RW	0
27:0	-	Reserved.	RW	0

8.2.8. Clock Division Base Register (0xB800_3118)

Table 26. Clock Division Base Register (0xB800_3118)

Bit	Name	Description	RW	Default
31:16	DivFactor[16:0]	Clock Source Division Factor. Assume DivFactor=N, Base clock=System_clock (Peripheral Lexra Bus)/N. Both values 0x0000 and 0x0001 disable the clock.	RW	0x0000
15:0	-	Reserved.	-	-

8.2.9. Watchdog Timer Control Register (0xB800_311C)

Table 27. Watchdog Timer Control Register (0xB800_311C)

Bit	Name	Description	RW	Default
31:24	WDTE[7:0]	Watchdog Enable. When these bits are set to 0xA5, the watchdog timer stops. Other values will enable the watchdog timer and cause a system reset when an overflow signal occurs.	W	0xA5
23	WDTCLR	Watchdog Clear. Write a 1 to clear the up-count watchdog counter.	W	0
22:21	OVSEL[1:0]	Lower Overflow Select Bits. These bits specify the overflow condition when the watchdog timer counts to the value. The watchdog timer is based on the base clock defined by CDBR. 00: 2^{15} 01: 2^{16} 10: 2^{17} 11: 2^{18}	RW	00
20	WatchDogIND	Watchdog Event Indicator. 0: A Watchdog RESET did not occur (POWER-ON or PIN RESET) 1: A Watchdog RESET occurred Write '1' to clear.	RW	0
19	NRFRstType	NOR Flash Reset Command Type Selection. When the watchdog event is active and WatchDogIND=1, It will cause the memory controller to reboot and issue a Flash reset command. The command type should be pre-defined by this control bit. 0: AMD NOR Flash reset command Type 1: Intel NOR Flash reset command Type *Note: This bit should not be reset by watchdog reset.* This bit has been taken over by System_Register hw_strap. Offset: 0xB800_0008h~B800_000bh, RW Initial value: 0xff00_1410 Reg.bit[19] Strap register without PAD: Indicates NOR flash reset type	RW	0
18:17	OVSEL[3:2]	Higher Overflow Select Bits. These bits specify the overflow condition when the watchdog timer counts to the value. The watchdog timer is based on the base clock defined by CDBR. There are a total of 24 watchdog bits. Condition values are the OVSEL[3:0]. 0000: 2^{15} 0001: 2^{16} 0010: 2^{17} 0011: 2^{18} 0100: 2^{19} 0101: 2^{20} 0110: 2^{21} 0111: 2^{22} 1000: 2^{23} 1001: 2^{24}	RW	0
16:0	-	Reserved.	-	-

8.3. GPIO Control

The RTL8196E-VE1/2/3provides eight sets of General Purpose Input/Output (GPIO) pins (GPIO A, B, C, D). Each GPIO pin may be configured as an input or output pin. The GPIO DATA register may be used to control GPIO pin signals. The GPIO pins are shared with some peripheral pins, and the type of peripheral can affect the attributes of the shared pins. All GPIO sets can be used to generate interrupts, and an interrupt mask and status register are provided. The GPIO control registers are defined in the following table.

8.3.1. GPIO Register Set (0xB800_3500)

Table 28. GPIO Register Set (0xB800_3500)

Offset	Size (Byte)	Name	Description
0x00	4	PABCD_CNR	Port A, B, C, D Control Register.
0x08	4	PABCD_DIR	Port A, B, C, D Direction Register.
0x0C	4	PABCD_DAT	Port A, B, C, D Data Register.
0x10	4	PABCD_ISR	Port A, B, C, D Interrupt Status Register.
0x14	4	PAB_IMR	Port A, B Interrupt Mask Register.
0x18	4	PCD_IMR	Port C, D Interrupt Mask Register.

8.3.2. GPIO Port A, B, C, D Control Register (PABCD_CNR) (0xB800_3500)

Table 29. GPIO Port A, B, C, D Control Register (PABCD_CNR) (0xB800_3500)

Bit	Name	Description	Mode	Default
31:24	PFC_D[7:0]	Pin Function Configuration of Port D.	RW	FFH
23:16	PFC_C[7:0]	Pin Function Configuration of Port C.	RW	FFH
15:8	PFC_B[7:0]	Pin Function Configuration of Port B.	RW	FFH
7:0	PFC_A[7:0]	Pin Function Configuration of Port A. Bit Value: 0: Configured as GPIO pin 1: Configured as dedicated peripheral pin	RW	FFH

8.3.3. GPIO Port A, B, C, D Direction Register (PABCD_DIR) (0xB800_3508)

Table 30. GPIO Port A, B, C, D Direction Register (PABCD_DIR) (0xB800_3508)

Bit	Name	Description	Mode	Default
31:24	DRC_D[7:0]	Pin Direction Configuration of Port D. 0: Configured as input pin 1: Configured as output pin	RW	00H
23:16	DRC_C[7:0]	Pin Direction Configuration of Port C. 0: Configured as input pin 1: Configured as output pin	RW	00H
15:8	DRC_B[7:0]	Pin Direction Configuration of Port B. 0: Configured as input pin 1: Configured as output pin	RW	00H
7:0	DRC_A[7:0]	Pin Direction Configuration of Port A. 0: Configured as input pin 1: Configured as output pin	RW	00H

8.3.4. Port A, B, C, D Data Register (PABCD_DAT) (0xB800_350C)

Table 31. Port A, B, C, D Data Register (PABCD_DAT) (0xB800_350C)

Bit	Name	Description	Mode	Default
31:24	PD_D[7:0]	Pin Data of Port D. 0: Data=0 1: Data=1	RW	00H
23:16	PD_C[7:0]	Pin Data of Port C. 0: Data=0 1: Data=1	RW	00H
15:8	PD_B[7:0]	Pin Data of Port B. 0: Data=0 1: Data=1	RW	00H
7:0	PD_A[7:0]	Pin Data of Port A. 0: Data=0 1: Data=1	RW	00H

8.3.5. Port A, B, C, D Interrupt Status Register (PABCD_ISR) (0xB800_3510)

Table 32. Port A, B, C, D Interrupt Status Register (PABCD_ISR) (0xB800_3510)

Bit	Name	Description	Mode	Default
31:24	IPS_D[7:0]	Interrupt Pending Status of Port D. Write '1' to clear the interrupt.	RW	00H
23:16	IPS_C[7:0]	Interrupt Pending Status of Port C. Write '1' to clear the interrupt.	RW	00H
15:8	IPS_B[7:0]	Interrupt Pending Status of Port B. Write '1' to clear the interrupt.	RW	00H
7:0	IPS_A[7:0]	Interrupt Pending Status of Port A. Write '1' to clear the interrupt.	RW	00H

8.3.6. Port A, B Interrupt Mask Register (PAB_IMR) (0xB800_3514)

Table 33. Port A, B Interrupt Mask Register (PAB_IMR) (0xB800_3514)

Bit	Name	Description	Mode	Default
31:30	PB7_IM[1:0]	PortB.7 Interrupt Mode.	RW	00B
29:28	PB6_IM[1:0]	PortB.6 Interrupt Mode.	RW	00B
27:26	PB5_IM[1:0]	PortB.5 Interrupt Mode.	RW	00B
25:24	PB4_IM[1:0]	PortB.4 Interrupt Mode.	RW	00B
23:22	PB3_IM[1:0]	PortB.3 Interrupt Mode.	RW	00B
21:20	PB2_IM[1:0]	PortB.2 Interrupt Mode.	RW	00B
19:18	PB1_IM[1:0]	PortB.1 Interrupt Mode.	RW	00B
17:16	PB0_IM[1:0]	PortB.0 Interrupt Mode.	RW	00B
15:14	PA7_IM[1:0]	PortA.7 Interrupt Mode.	RW	00B
13:12	PA6_IM[1:0]	PortA.6 Interrupt Mode.	RW	00B
11:10	PA5_IM[1:0]	PortA.5 Interrupt Mode.	RW	00B
9:8	PA4_IM[1:0]	PortA.4 Interrupt Mode.	RW	00B
7:6	PA3_IM[1:0]	PortA.3 Interrupt Mode.	RW	00B
5:4	PA2_IM[1:0]	PortA.2 Interrupt Mode.	RW	00B
3:2	PA1_IM[1:0]	PortA.1 Interrupt Mode.	RW	00B
1:0	PA0_IM[1:0]	PortA.0 Interrupt Mode. 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

8.3.7. Port C, D Interrupt Mask Register (PCD_IMR) (0xB800_3518)

Table 34. Port C, D Interrupt Mask Register (PCD_IMR) (0xB800_3518)

Bit	Name	Description	Mode	Default
31:30	PD7_IM[1:0]	PortD.7 Interrupt Mode.	RW	00B
29:28	PD6_IM[1:0]	PortD.6 Interrupt Mode.	RW	00B
27:26	PD5_IM[1:0]	PortD.5 Interrupt Mode.	RW	00B
25:24	PD4_IM[1:0]	PortD.4 Interrupt Mode.	RW	00B
23:22	PD3_IM[1:0]	PortD.3 Interrupt Mode.	RW	00B
21:20	PD2_IM[1:0]	PortD.2 Interrupt Mode.	RW	00B
19:18	PD1_IM[1:0]	PortD.1 Interrupt Mode.	RW	00B
17:16	PD0_IM[1:0]	PortC.0 Interrupt Mode.	RW	00B
15:14	PC7_IM[1:0]	PortC.7 Interrupt Mode.	RW	00B
13:12	PC6_IM[1:0]	PortC.6 Interrupt Mode.	RW	00B
11:10	PC5_IM[1:0]	PortC.5 Interrupt Mode.	RW	00B
9:8	PC4_IM[1:0]	PortC.4 Interrupt Mode.	RW	00B
7:6	PC3_IM[1:0]	PortC.3 Interrupt Mode.	RW	00B
5:4	PC2_IM[1:0]	PortC.2 Interrupt Mode.	RW	00B
3:2	PC1_IM[1:0]	PortC.1 Interrupt Mode.	RW	00B
1:0	PC0_IM[1:0]	PortC.0 Interrupt Mode. 00: Disable interrupt 01: Enable falling edge interrupt 10: Enable rising edge interrupt 11: Enable both falling or rising edge interrupt	RW	00B

8.4. GPIO Shared Pin Configured Mapping List

The RTL8196E-VE1/2/3GPIO pins are shared with the other functions.

8.4.1. Shared Pin Register (PIN_MUX_SEL) (0xB800_0040)

Table 35. Shared Pin Register (PIN_MUX_SEL) (0xB800_0040)

Bit	Bit Name	Description	Mode	Default
31:26	-	Reserved.	-	-
25:24	reg_iocfg_sdio1	Configure SF_SDIO1 Pin as SF_SDIO1 or GPIOC3. 00: SF_SDIO1 01: Reserved 10: Reserved 11: GPIOC3	RW	00B
23:22	reg_iocfg_sdio0	Configure SF_SDIO0 Pin as SF_SDIO0 or GPIOC2. 00: SF_SDIO0 01: Reserved 10: Reserved 11: GPIOC2	RW	00B
21:20	reg_iocfg_sck	Configure SF_SCK Pin as SF_SCK or GPIOC1. 00: SF_SCK 01: Reserved 10: Reserved 11: GPIOC1	RW	00B
19:18	reg_iocfg_fcs0n	Configure SF_CS0# Pin as SF_CS0# or GPIOC6. 00: SF_CS0# 01: Reserved 10: Reserved 11: GPIOC6	RW	00B
17:7	-	Reserved.	-	-
6	reg_iocfg_pcie	Configure PCIE_RST# Pin as PCIe or GPIO Mode. 0: PCIE_RST# 1: GPIOB1	RW	00B
5	reg_iocfg_uart	Configure UART0_TX and UART0_RX Pins as UART or GPIO Mode. 0: UART 1: GPIO	RW	0B
4:3	-	Reserved.		
2:0	reg_iocfg_jtag	Configure JTAG Pins as JTAG, UART1, or GPIO Mode. 000: Reserved 001: JTAG 010: UART1 011: Reserved 100: Reserved 101: Reserved 110: GPIO 111: Reserved	RW	000B

8.4.2. Shared Pin Register (PIN_MUX_SEL_2) (0xB800_0044)

Table 36. Shared Pin Register (PIN_MUX_SEL_2) (0xB800_0044)

Bit	Bit Name	Description	Mode	Default
31:14	-	Reserved.	-	-
13:12	reg_iocfg_led_port4	Configure LED_PORT4 Pin as LED_PORT4 or GPIO Mode. 00: LED_PORT4 01: Reserved 10: Reserved 11: GPIOB6	RW	10B
11	-	Reserved.	-	-
10:9	reg_iocfg_led_port3	Configure LED_PORT3 Pin as LED_PORT3 or GPIO Mode. 00: LED_PORT3 01: Reserved 10: Reserved 11: GPIOB5	RW	10B
8	-	Reserved.	-	-
7:6	reg_iocfg_led_port2	Configure LED_PORT2 Pin as LED_PORT2 or GPIO Mode. 00: LED_PORT2 01: Reserved 10: Reserved 11: GPIOB4	RW	10B
5	-	Reserved.	-	-
4:3	reg_iocfg_led_port1	Configure LED_PORT1 Pin as LED_PORT1 or GPIO Mode. 00: LED_PORT1 01: Reserved 10: Reserved 11: GPIOB3	RW	10B
2	-	Reserved.	-	-
1:0	reg_iocfg_led_port0	Configure LED_PORT0 Pin as LED_PORT0 or GPIO Mode. 00: LED_PORT0 01: Reserved 10: Reserved 11: GPIOB2	RW	10B

9. UART

9.1. Features

The RTL8196E-VE1/2/3provides two 16550 compatible UARTs. These contain a 16-byte First In First Out (FIFO) buffer and Auto Flow Control to control transmissions on port 1. The baud rate can be up to 1Mbps and a programmable baud rate generator allows division of any input reference clock by 1 to (2^16-1) and generates an internal 16x clock.

9.2. Interface Pins

The UART interface pins are shown in Table 37.

Table 37. UART Control Interface Pins

Signal Name	Type	Function
TXD#	O	Transmit Data for Port 0 and Port 1.
RXD#	I	Receive Data for Port 0 and Port 1.
RTS#	O	Request to Send for Port 1.
CTS#	I	Clear to Send for Port 1.

9.3. UART Control Register

9.3.1. UART Control Register Address Mapping (Base: 0xB800_2000)

Table 38. UART Control Register Address Mapping (Base: 0xB800_2000)

Offset	Size (byte)	Name	Description
000	1	UART0_RBR	Receiver Buffer Register (DLAB=0).
000	1	UART0_THR	Transmitter Holding Register (DLAB=0).
000	1	UART0_DLL	Divisor Latch LSB (DLAB=1).
004	1	UART0_IER	Interrupt Enable Register (DLAB=0).
004	1	UART0_DLM	Divisor Latch MSB (DLAB=1).
008	1	UART0_IIR	Interrupt Identification Register.
008	1	UART0_FCR	FIFO Control Register.
00c	1	UART0_LCR	Line Control Register.
010	1	UART0_MCR	Modem Control Register.
014	1	UART0_LSR	Line Status Register.
018	1	UART0_MSR	Modem Status Register.
01c	1	UART0_SCR	Scratch Register.
100	1	UART1_RBR	Receiver Buffer Register (DLAB=0).
100	1	UART1_THR	Transmitter Holding Register (DLAB=0).
100	1	UART1_DLL	Divisor Latch LSB (DLAB=1).
104	1	UART1_IER	Interrupt Enable Register (DLAB=0).

Offset	Size (byte)	Name	Description
104	1	UART1_DLM	Divisor Latch MSB (DLAB=1).
108	1	UART1_IIR	Interrupt Identification Register.
108	1	UART1_FCR	FIFO Control Register.
10c	1	UART1_LCR	Line Control Register.
110	1	UART1_MCR	Modem Control Register.
114	1	UART1_LSR	Line Status Register.
118	1	UART1_MSR	Modem Status Register.
11c	1	UART1_SCR	Scratch Register.

9.3.2. UART Receiver Buffer Register (DLAB=0) (0xB800_2100, 0xB800_2000)

Table 39. UART Receiver Buffer Register (DLAB=0) (0xB800_2100, 0xB800_2000)

Reg.bit	Name	Description	Mode	Default
31:24	RBR[7:0]	Receiver Buffer Data.	R	00H

9.3.3. UART Transmitter Holding Register (DLAB=0) (0xB800_2100, 0xB800_2000)

Table 40. UART Transmitter Holding Register (DLAB=0) (0xB800_2100, 0xB800_2000)

Reg.bit	Name	Description	Mode	Default
31:24	THR[7:0]	Transmitter Holding Data.	W	00H

9.3.4. UART Divisor Latch LSB (DLAB=1) (0xB800_2100, 0xB800_2000)

Table 41. UART Divisor Latch LSB (DLAB=1) (0xB800_2100, 0xB800_2000)

Reg.bit	Name	Description	Mode	Default
31:24	DLL[7:0]	Divisor Latch LSB.	RW	00H

9.3.5. UART Divisor Latch MSB (DLAB=1) (0xB800_2104, 0xB800_2004)

Table 42. UART Divisor Latch MSB (DLAB=1) (0xB800_2104, 0xB800_2004)

Reg.bit	Name	Description	Mode	Default
31:24	DLM[7:0]	Divisor Latch MSB.	RW	00H

9.3.6. UART Interrupt Enable Register (DLAB=0) (0xB800_2104, 0xB800_2004)

Table 43. UART Interrupt Enable Register (DLAB=0) (0xB800_2104, 0xB800_2004)

Reg.bit	Name	Description	Mode	Default
24	ERBI	Enable Received Data Available Interrupt.	RW	0B
25	ETBEI	Enable Transmitter Holding Register Empty Interrupt.	RW	0B
26	ELSI	Enable Receiver Line Status Interrupt.	RW	0B
27	EDSSI	Enable Modem Status Register Interrupt.	RW	0B
28	ESLP	Sleep Mode Enable.	RW	0B
29	ELP	Low Power Mode Enable.	RW	0B
31:30	-	Reserved.	-	-

9.3.7. UART Interrupt Identification Register (0xB800_2108, 0xB800_2008)

Table 44. UART Interrupt Identification Register (0xB800_2108, 0xB800_2008)

Reg.bit	Name	Description	Mode	Default
24	IPND	Interrupt Pending. 0: Interrupt pending	R	1B
27:25	IID[2:0]	Interrupt ID. IID[1:0] indicates the interrupt priority.	R	000B
29:28	-	Reserved.	-	-
31:30	FIFO16[1:0]	00: No FIFO 11: 16-byte FIFO	R	11B

9.3.8. UART FIFO Control Register (0xB800_2108, 0xB800_2008)

Table 45. UART FIFO Control Register (0xB800_2108, 0xB800_2008)

Reg.bit	Name	Description	Mode	Default
24	EFIFO	Enable FIFO. When this bit is set, enables the transmitter and receiver FIFOs. Changing this bit clears the FIFOs.	W	0B
25	RFRST	Receiver FIFO Reset. Writes 1 to clear the receiver FIFO.	W	0B
26	TFRST	Transmitter FIFO Reset. Writes 1 to clear the transmitter FIFO.	W	0B
29:27	-	Reserved.	-	-
31:30	RTRG[1:0]	Receiver Trigger Level (Trigger Level: 16-byte). 00: 01 01: 04 10: 08 11: 14	W	11B

9.3.9. UART Line Control Register (0xB800_210C, 0xB800_200C)

Table 46. UART Line Control Register (0xB800_210C, 0xB800_200C)

Reg.bit	Name	Description	Mode	Default
25:24	WLS[1:0]	Word Length Select. 00: Reserved (NA) 01: 6 bits (NA) 10: 7 bits 11: 8 bits	RW	11B
26	STB	Number of Stop Bits. 0: 1 bit 1: 2 bits	RW	0B
27	PEN	Parity Enable.	RW	0B
29:28	EPS[1:0]	Even Parity Select. 00: Odd parity 01: Even parity 10: Mark parity 11: Space parity	RW	00B
30	BRK	Break Control. Set this bit force TXD to the spacing (low) state (break). Clear this bit to disable break condition.	RW	0B
31	DLAB	Divisor Latch Access Bit.	RW	0B

9.3.10. UART Modem Control Register (0xB800_2110, 0xB800_2010)

Table 47. UART Modem Control Register (0xB800_2110, 0xB800_2010)

Reg.bit	Bit Name	Description	Mode	Default
24	DTR	Data Terminal Ready. 0: Set DTR# high 1: Set DTR# low	RW	0B
25	RTS	Request to Send. 0: Set RTS# high 1: Set RTS# low	RW	0B
27:26	-	Reserved.	-	-
28	LOOP	Loopback.	RW	0B
29	AFE	Auto Flow Control Enable.	RW	0B

9.3.11. UART Line Status Register (0xB800_2114, 0xB800_2014)

Table 48. UART Line Status Register (0xB800_2114, 0xB800_2014)

Reg.bit	Name	Description	Mode	Default
24	DR	Data Ready. Character Mode: Data ready in RBR FIFO Mode: Receiver FIFO is not empty	R	0B
25	OE	Overrun Error. An overrun occurs when the receiver FIFO is full and the next character is completely received in the shift register. An OE is indicated. The character in the shift register will be overwritten.	R	0B
26	PE	Parity Error.	R	0B
27	FE	Framing Error.	R	0B
28	BI	Break Interrupt Indicator.	R	0B

Reg.bit	Name	Description	Mode	Default
29	THRE	Transmitter Holding Register Empty. Character Mode: THR is empty FIFO Mode: Transmitter FIFO is empty	R	1B
30	TEMT	Transmitter Empty. Character Mode: Both THR and TSR are empty FIFO Mode: Both transmitter FIFO and TSR are empty	R	1B
31	RFE	Receiver FIFO Error. Either a parity, framing, or break error in the FIFO.	R	0B

9.3.12. UART Modem Status Register (0xB800_2110, 0xB800_2018)

Table 49. UART Modem Status Register (0xB800_2110, 0xB800_2018)

Reg.bit	Name	Description	Mode	Default
31	ΔCTS	Delta Clear to Send (CTS# Signal Transmits).	R	1B
30	ΔDSR	Delta Data Set Ready (DSR# Signal Transmits; Returns 0).	R	0B
29	TERI	Trailing Edge Ring Indicator. RI# signal changes from low to high (Returns 0).	R	0B
28	ΔDCD	Delta Data Carrier Detect (DCD# Signal Transmits; Returns 0).	R	0B
27	CTS	Clear to Send. 0: CTS# detected high 1: CTS# detected low	R	0B
26	DSR	Data Set Ready. 0: DSR# detected high 1: DSR# detected low Loopback mode: Returns bit 0 of MCR Normal mode: Returns 1	R	1B
25	RI	Ring Indicator. 0: RI# detected high 1: RI# detected low Loopback mode: Returns bit 3 of MCR Normal mode: Returns 0	R	0B
24	DCD	Data Carrier Detect. 0: DCD# detected high 1: DCD# detected low Loopback mode: Returns bit 2 of MCR Normal mode: Returns 1	R	1B

9.4. Baud Rate

Value of divisor latch=[base clock/(16×baud rate)]–1. The base clock is 200MHz.

Table 50. Divisor Latch Value Examples

System CLK Base Clock	300bps	1200bps	2400bps	9600bps	19200bps	38400bps	57600bps	115200bps
200MHz	41665	10415	5207	1301	650	324	216	107

10. PCI Express Bus Interface

The RTL8196E-VE1/2/3complies with PCI Express Base Specification Revision 1.1, and runs at a 2.5GHz signaling rate with X1 link width, i.e., one transmit and one receive differential pair. The RTL8196E-VE1/2/3supports four types of PCI Express messages: interrupt messages, error messages, power management messages, and hot-plug messages. To ease PCB layout constraints, PCI Express lane polarity reversal and link reversal are also supported. The RTL8196E-VE1/2/3provides one port on the PCI Express Host interface.

10.1. PCI Express Transmitter

The RTL8196E-VE1/2/3PCI Express block receives digital data from the Ethernet interface and performs data scrambling with Linear Feedback Shift Register (LFSR) and 8B/10B coding technology into 10-bit code groups. Data scrambling is used to reduce the possibility of electrical resonance on the link, and 8B/10B coding technology is used to benefit embedded clocking, error detection, and DC balance by adding an overhead to the system through the addition of two extra bits. The data code groups are passed through its serializer for packet framing. The generated 2.5Gbps serial data is transmitted onto the PCB trace to its upstream device via a differential driver.

10.2. PCI Express Receiver

The RTL8196E-VE1/2/3PCI Express block receives 2.5Gbps serial data from its upstream device to generate parallel data. The receiver's PLL circuits are re-synchronized to maintain bit and symbol lock. Through 8B/10B decoding technology and data de-scrambling, the original digital data is recovered and passed to the RTL8196E-VE1/2/3internal Ethernet MAC to be transmitted onto the Ethernet media.

10.3. *PCI Express Host Mode*

10.3.1. PCIe Port 0 Host Mode Extended Register Address Mapping (Base: 0xB8B0_1000)

Table 51. PCIe Port 0 Host Mode Extended Register Address Mapping (Base: 0xB8B0_1000)

Offset	Size (byte)	Name	Description
0x00	4	MDIO	PCIe Port 0 MDIO Control Register.
0x04	4	INTSTR	PCIe Port 0 Interrupt Status Register.
0x08	4	PWRCR	PCIe Port 0 Power Control Register.
0x0C	4	IPCFG	PCIe Port 0 IP Configuration Register.
0x10	4	BISTFAIL	PCIe Port 0 BIST Fail Check Register.

10.3.2. PCIe MDIO Register (0xB8B0_1000)

Table 52. PCIe MDIO Register (0xB8B0_1000)

Reg.bit	Name	Description	Mode	Default
31:16	Mdio_data	MDIO Read Data or Write Data.	RW	0H
15:13	Mdip_phyaddr	MDIO PHY Page Addr[2:0].	RW	-
12:8	Mdio_regaddr	MDIO Register Address[4:0].	RW	0H
7	-	Reserved.	-	-
6:5	Mdio_st	MDIO Status[1:0] for Debug Checking.	R	00B
4	Mdio rdy	MDIO Ready for Debug Checking.	R	0
3:2	Mdio_rate	MDIO Clock Rate. 2’b00: lx clock/32 2’b01: lx clock/16 2’b10: lx clock/8 2’b11: lx clock/4	RW	00B
1	Mdio_srst	MDIO Soft Reset. 1: Active 0: Not active	RW	0B
0	Mdio_rdwr	MDIO Read/Write Command. 1: Write 0: Read	RW	0B

10.3.3. PCIe Interrupt Status Register (0xB8B0_1004)

Table 53. PCIe Interrupt Status Register (0xB8B0_1004)

Reg.bit	Name	Description	Mode	Default
3	INTD	Interrupt D Status Register (Level Active).	R	0B
2	INTC	Interrupt C Status Register (Level Active).	R	0B
1	INTB	Interrupt B Status Register (Level Active).	R	0B
0	INTA	Interrupt A Status Register (Level Active).	R	0B

10.3.4. PCIe Power Control Register (0xB8B0_1008)

Table 54. PCIe Power Control Register (0xB8B0_1008)

Reg.bit	Name	Description	Mode	Default
10	App_unlock_msg	Generate Unlock Message (One Pulse).	RW	0B
9	Apps_pm_xmt_turnoff	Generate PME Turn Off Message.	RW	0B
8	App_init_rst	Application User Trigger Hot Reset (Must Keep Asserted for 2ms Minimum).	RW	0B
7	Phy_srst_n	PCIe PHY Software Reset. 0: Active 1: Not active *Note: This bit is for internal PCIe PHY reset and its default value is 'high'. Software must set this bit to 'low' for longer than 100ms to generate a REFCLK for the RTL8196E-VE1/2/3and any external device.*	RW	1B
6	P1_clk_req_en	Auxiliary State Enable. 1: Enable 0: Disable	RW	0B
5	Low_power enable	Enter Lower Power State Enable. 1: Enable 0: Disable	RW	0B
4	Sys_aux_pwr_det	System Detect Auxiliary Power Stable. 1: Stable 0: Unstable	RW	0B
3	App_ready_enter_l23	Application User Ready Enter L23 when Device in D3 Hot/Cold.	RW	0B
2	App_req_exit_l1	Application Request Exit L1 State.	RW	0B
1	App_req_enter_l1	Application Request Enter L1 State.	RW	0B
0	App_ltssm_en	Application User LTSSM Enable. 1: Enable LTSSM 0: Hold LTSSM in initial state	RW	1B

10.3.5. PCIe IP Configuration Register (0xB8B0_100C)

Table 55. PCIe IP Configuration Register (0xB8B0_100C)

Reg.bit	Name	Description	Mode	Default
15:8	Bus_num	Target Bus Number (265 Types).	RW	0H
7:3	Dev_num	Target Device Number (32 Types).	RW	0H
2:0	Fun_num	Target Function Number (8 Types).	RW	0H

10.3.6. PCIe SRAM BIST Check Register (0xB8B0_1010)

Table 56. PCIe SRAM BIST Check Register (0xB8B0_1010)

Reg.bit	Name	Description	Mode	Default
31:0	Bist_fail_chk	SRAM BIST Fail Check.	R	0H

11. Switch Core Control

11.1. Global Port Control Register

11.1.1. Global Port Control Register Address Mapping (Base: 0xBB80_4000)

The RTL8196E-VE1/2/3provides an MDC/MDIO (Management Data Clock/Management Data Input/Output) interface to access embedded PHYs. As the MDC/MDIO interface is relatively slow, the access is divided into command and status registers.

Table 57. Global Port Control Register Address Mapping (Base: 0xBB80_4000)

Offset	Size (byte)	Name	Description
04	4	MDCIOCR	MDC/MDIO Command Register.
08	4	MDCIOSR	MDC/MDIO Status Register.

11.1.2. Global MDC/MDIO Command Register (0xBB80_4004)

Table 58. Global MDC/MDIO Command Register (0xBB80-4004)

Reg.bit	Name	Description	Mode	Default
31	COMMAND	MDC/MDIO Command Type. 0: Read Access 1: Write Access *Note: The procedure to access the external PHY via the MDC/MDIO interface is as follows:* *1. Define the PHY address (PHYADD), register address (REGADD).* *2. Define the write data content for write command (WRDATA).* *3. Identify the command type (COMMAND).* *4. Get the command execution status (STATUS) and read data content (RDATA).*	RW	0B
30:29	-	Reserved.	-	-
28:24	PHYADD[4:0]	PHY Address of MDC/MDIO Command.	RW	00000B
23:21	-	Reserved.	-	-
20:16	REGADD[4:0]	Register Address of MDC/MDIO Command.	RW	00000B
15:0	WRDATA[15:0]	Write Data of MDC/MDIO Command.	RW	0000H

11.1.3. Global MDC/MDIO Status Register (0xBB80_4008)

Table 59. Global MDC/MDIO Status Register (0xBB80_4008)

Reg.bit	Name	Description	Mode	Default
31	STATUS	MDC/MDIO Command in Process Status. 0: Process done 1: In progress	R	0000B
30:16	-	Reserved.	-	-
15:0	RDATA	Read Data Result of MDC/MDIO Command.	R	0B

11.1.4. Global Frame Filtering Control Register Address Mapping (Base: 0xBB80_4000)

Table 60. Global Frame Filtering Control Register Address Mapping (Base: 0xBB80_4000)

Offset	Size (byte)	Name	Description
44	4	BSCR	Broadcast Storm Control Register.

11.1.5. Global Broadcast Storm Control Register (0xBB80_4044)

Per-port broadcast storm traffic utilization is a global parameter that is defined by BCSC_CNT[14:0] in the Broadcast Storm Control Register (0xBB80_4044). Broadcast storm control can be enabled/disabled on a per-port basis, and the broadcast traffic definition is user configurable.

Table 61. Global Broadcast Storm Control Register (0xBB80_4044)

Reg.bit	Name	Description	Mode	Default
31:15	-	Reserved.	-	-
14:0	BCSC_CNT[14:0]	Broadcast Storm Control Rate Configuration. Defines the per-port-based broadcast storm control valid accumulated byte count in each default time interval 25ms/2.5ms/0.25ms for 10M/100M/1000M (the time interval will auto update for different port link speeds). For BCSC_BCNT[14:0] value=N, The % max rate=N/30360*100%.	RW	0

Note: When Broadcast Storm Control is enabled, every 25ms, each port will limit the max incoming byte counts of broadcast, multicast, or unknown-unicast packets to 3 counts maximum. Other excessive packets within the duration time will be dropped.

11.2. Per-Port Configuration Register

The port ability properties, e.g., auto negotiation, port speed, duplex, flow control, can be configured via the Per-Port Configuration Register.

Table 62. Per-Port Configuration Register Address Mapping (Base: 0xBB80_4100)

Offset	Size (byte)	Name	Description
00	4	PITCR	Port Interface Type Control Register.
04	4	PCRP0	Port Configuration Register of Port 0.
08	4	PCRP1	Port Configuration Register of Port 1.
0C	4	PCRP2	Port Configuration Register of Port 2.
10	4	PCRP3	Port Configuration Register of Port 3.
14	4	PCRP4	Port Configuration Register of Port 4.
1C	4	PCRP6	Port Configuration Register of Port 6 (Ext. P0).
20	4	PCRP7	Port Configuration Register of Port 7 (Ext. P1).
24	4	PCRP8	Port Configuration Register of Port 8 (Ext. P2).
28	4	PSRP0	Port Status Register of Port 0.
2C	4	PSRP1	Port Status Register of Port 1.
30	4	PSRP2	Port Status Register of Port 2.
34	4	PSRP3	Port Status Register of Port 3.
38	4	PSRP4	Port Status Register of Port 4.
40	4	PSRP6	Port Status Register of Port 6.
44	4	PSRP7	Port Status Register of Port 7.
48	4	PSRP8	Port Status Register of Port 8.

11.2.1. Port Interface Type Control Register (0xBB80_4100)

Table 63. Port Interface Type Control Register (0xBB80_4100)

Reg.bit	Name	Description	Mode	Default
31:10	-	Reserved.	-	-
9:8	Port4_TypeCfg[1:0]	Port 4 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
7:6	Port3_TypeCfg[1:0]	Port 3 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
5:4	Port2_TypeCfg[1:0]	Port 2 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
3:2	Port1_TypeCfg[1:0]	Port 1 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B
1:0	Port0_TypeCfg[1:0]	Port 0 Interface Type Configuration. 00: UTP (10/100M embedded PHY) 01: Reserved 1x: Reserved	RW	00B

11.2.2. Port Configuration Register of Port N (N=0~4)

Table 64. Port Configuration Register of Port N (N=0~4)

Reg.bit	Name	Description	Mode	Default
31	ByPassTCRC	1: Do not recalculate CRC for CRC error frame 0: Recalculate CRC for CRC error frame	RW	0B
30:26	ExtPHYID[4:0]	PHY ID Assign for PHY MII Register Polling Addressing. Identifies the external PHY ID for MDC/MDIO polling addressing. Only valid for ports 0~4.	RW	Port0~4 =0x0~4
25	EnForceMode	Enable Port Property (Link/Speed/Duplex/Flow Control) to be Set by Force Mode. 0: Disable (enable Auto-Negotiation) In this mode, the port link/speed/duplex /flow control setting is based on the MDC/MDIO polling result. 1: Enable (Force Mode) (Disable Auto-Negotiation) In this mode, the port speed/duplex /flow control setting is set by the force mode control bits in this register. Note that the method of determining the link status depends on the PollinkStatus setting.	RW	0
24	PollinkStatus	Polling PHY Link Status {EnForceMode, PollinkStatus}. 00, 01: Enable Auto-Negotiation 10: Force Mode (Disables Auto-Negotiation) This mode should be set for MAC-to-MAC connection. 11: Force Mode with polling link status (Disables Auto-Negotiation but polls the PHY's link status).	RW	0
23	ForceLink	Force Link-Up or Link-Down Setting. Available Only if {EnForceMode, PollinkStatus}=10. 0: Force link down 1: Force link up *Note: If {EnForceMode, PollinkStatus}=11, the link status information is derived from PHY register 1 via the ASIC's auto-polling mechanism.*	RW	0
22:18	FrcAbi_AnAbi_sel	If EnForceMode=1 FrcAbi_AnAbi_sel is used to indicate the force mode operation for MAC or PHY mode operations. FrcAbi_AnAbi_sel[0]: ForceDuplex 1: Force FULL duplex 0: Force HALF duplex FrcAbi_AnAbi_sel[2:1]: ForceSpeed 00: Force 10Mbps 01: Force 100Mbps 10: Reserved 11: Reserved FrcAbi_AnAbi_sel[4:3]: Reserved If EnForceMode=0 FrcAbi_AnAbi_sel is used to indicate Auto-Negotiation advertising ability. FrcAbi_AnAbi_sel[0]: 10Mbps Half-duplex FrcAbi_AnAbi_sel[1]: 10Mbps Full-duplex FrcAbi_AnAbi_sel[2]: 100Mbps Half-duplex FrcAbi_AnAbi_sel[3]: 100Mbps Full-duplex FrcAbi_AnAbi_sel[4]: Reserved	RW	5'b11111 for port#0~4

<table>
<tr><th>Reg.bit</th><th>Name</th><th>Description</th><th>Mode</th><th>Default</th></tr>
<tr><td>17:16</td><td>PauseFlowControl[1:0]
(ADVERTISE_
PAUSEABY)</td><td>If EnForceMode=1
This register controls PAUSE flow control.
0: Enable TX pause ability
1: Enable RX pause ability

If EnForceMode=0
The PHY advertises PAUSE flow control.
0: PAUSE operation for full duplex links
1: Asymmetric PAUSE operation for full duplex links</td><td>RW</td><td>2’b11</td></tr>
<tr><td>15:12</td><td>-</td><td>Reserved.</td><td>-</td><td>-</td></tr>
<tr><td>11:9</td><td>BCSC_Types[2:0]</td><td>Broadcast Storm Control Packet Types Selection.
When Broadcast storm control is enabled, the control packet types can be selected.
Bit[0]: Enable control for broadcast packets
Bit[1]: Enable control for multicast packet
Bit[2]: Reserved
0: Disable
1: Enable
When Bit[3:0] are set as ‘000’, the port’s broadcast storm function is disabled.</td><td>RW</td><td>0B</td></tr>
<tr><td>8</td><td>EnBCSC</td><td>Enable Broadcast Storm Control.
0: Disable
1: Enable
When enabled, the broadcast storm control rate and control packet type should be defined in the broadcast storm control register.</td><td>RW</td><td>0B</td></tr>
<tr><td>7</td><td>EnLoopBack</td><td>Enable MAC – PHY Interface for MII Loopback.
Enable internal and external loopback. Sets the MAC as an internal loopback, and sets the PHY side as an external loopback.
0: Disable 1: Enable</td><td>RW</td><td>0B</td></tr>
<tr><td>6</td><td>DisBKP</td><td>Per-Port Disable Backpressure Function for Half Duplex Mode.
1: Disable 0: Enable</td><td>RW</td><td>0B</td></tr>
<tr><td>5:4</td><td>STP_PortST[1:0]</td><td>Spanning Tree Protocol Port State Control.
00: Disable State 01: Blocking/Listen State
10: Learning State 11: Forwarding State
<table>
<tr><th>802.1d Port State</th><th>Pass Received Non-BPDU Frames</th><th>Pass Received BPDU Frames</th><th>Learning Station Location Into Address Database</th></tr>
<tr><td>Disabled</td><td>No</td><td>No</td><td>No</td></tr>
<tr><td>Blocking</td><td>No</td><td>Yes</td><td>No</td></tr>
<tr><td>Listening</td><td>No</td><td>Yes</td><td>No</td></tr>
<tr><td>Learning</td><td>No</td><td>Yes</td><td>Yes</td></tr>
<tr><td>Forwarding</td><td>Yes</td><td>Yes</td><td>Yes</td></tr>
</table></td><td>RW</td><td>11</td></tr>
</table>

Reg.bit	Name	Description	Mode	Default
3	MAC S/W Reset	MAC S/W Reset Supports a Method to Reset the MAC by Software. It can reset the circuit in the RXC and TXC domain via an active-low signal. To reset the MAC, software should write a 1 following the writing of a 0. 0: Reset state 1: Normal state	RW	1
2:1	AcptMaxLen[1:0]	Configures the Maximum Acceptable Packet Length Supported. This control is valid only when jumbo packet accept is disabled on a port. 00: 1536 bytes 01: 1552 bytes 10: 9k bytes (jumbo packet: 9216 bytes) 11: 16k~14 bytes (jumbo packet: 16370 bytes)	RW	00B
0	EnablePHYIf	Enable PHY Interface. The bit controls the MAC vs. PHY interface, irrelevant as to whether the port interface is UTP. 0: Disable When disabled, the PHY interface will be isolated from the MAC. Packets will not be transmitted or received to/from the PHY to/from the MAC interface. 1: Enable	RW	0B

11.2.3. Port Status Register of Port N (N=0~4)

Table 65. Port Status Register of Port N (N=0~4)

Reg.bit	Name	Description	Mode	Default
31:14	-	Reserved.	-	-
13:12	EEE Status[1:0]	Port Link Status. In NWay Mode, the status shown is that of PHY local and PHY remote ability. In Force mode, the status is the configuration result of the force mode configuration registers. Bit 1: Reserved Bit 0: 100M EEE ability	R	0
11:9	-	Reserved.	-	-
8	LinkDownEventFlag	Port Link Down Event Detection Monitor Flag. 0: Idle 1: Link Down event detected When the Port link status changes from link-up to link-down, the flag bit will be latched as '1' until read to clear and updated to the new status.	Latch, RW	0
7:0	PortStatus[7:0]	Port Link Status. In an NWay Mode port, the status shown is that of PHY local and PHY remote ability. In Force mode, the status is the configuration result of the force mode configuration registers. This report is valid for UTP Interface mode. Bit 7: NWay Enable (link by auto-negotiation) Bit 6: RX PAUSE ability Bit 5: TX PAUSE ability Bit 4: LinkUp Bit 3: Duplex Bit 2: Reserved Bit [1:0]: LinkSpeed[1:0] 00: 10M 01: 100M 10: Reserved 11: Reserved	R	0

11.3. LED Control Register

11.3.1. LED Topology Operation

The RTL8197DN supports single and Bi-Color LED displays. Table 66 illustrates all combinations of LED topologies.

Mixed mode LED display is supported. E.g., designers may design some ports in single-color and some ports in Bi-color mode. Note the topology (LedTopology) field should be the same in all ports.

Table 66. Display Arrangement of Each SCAN LED Mode

Location	LED Mode=SCAN 0	LED Mode=SCAN 1	LED Mode=SCAN 2
LED#0	OFF=Link Down ON/Blink=Link/Act	OFF=Link Down Y=10/100M Link/Act *Note: Y=Yellow color (when signal LINKN[0:4] active high).*	OFF=Link Down Y=10M Link/Act G=100M Link Act *Note: Y=Yellow color (when signal LINKN[0:4] active high).* *G=Green color (when signal LINKN[0:4] active low).*
Topology Description	SCAN Mode Signal LED#0: Single-Color LED	SCAN Mode Signal LED#0: Single-Color LED	SCAN Mode Signal LED#0: 2-Pin Dual-Color LED

Note: 'Y' indicates yellow color LED, and 'G' indicates green color LED (depends on the external LED component). 'ON' means this LED is turned on. 'OFF' means this LED is turned off. 'N/A' means this LED is not applicable. The CPU can still control this LED using the CPUCtrlPort/CPUCtrlMask register.

11.3.2. SCAN Mode LED

The 2-pin dual-color LEDs are supported in SCAN mode. The dual-color LEDs are controlled by the polarity of LED_PORT[n] and LEDSCAN. The LEDSCAN signal should change polarity to turn on the target LED, and turn off other LEDs in the target port's scan phase. When the port is IDLE, the LED_PORT[n] is driven low in its scan phase.

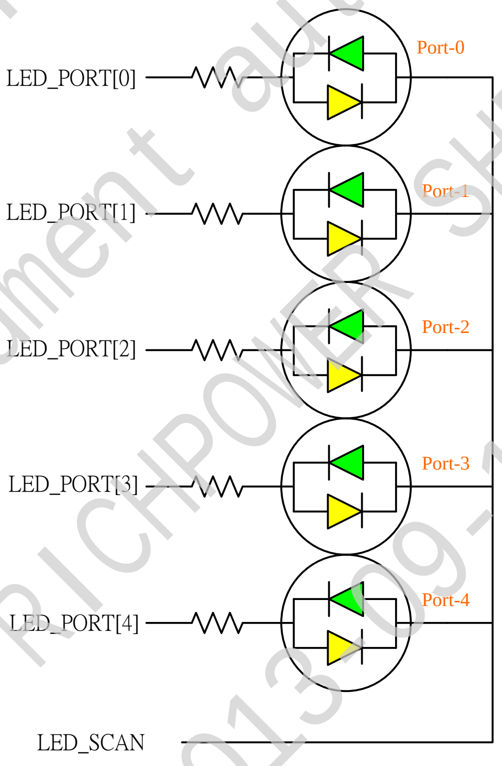


Figure 3. Bi-Color LED SCAN Mode interconnections

11.3.3. LED Control Register Address Mapping (Base: 0xBB80_4300)

Table 67. LED Control Register Address Mapping (Base: 0xBB80_4300)

Offset	Size (byte)	Name	Description
00	4	LEDCR0	LED Control Register 0.
04	4	LEDCR1	LED Control Register 1.
0C	4	LEDBCR	LED Blinking Control Register.
10	4	EEELCR	EEE LED Configuration Register.
14	4	DIRECTLCR	DIRECT Mode LED Configuration Register.

11.3.4. LED Control Register 0 (0xBB80_4300)

Table 68. LED Control Register 0 (0xBB80_4300)

Reg.bit	Name	Description	Mode	Default
31:22	-	Reserved.	-	-
21:20	LedTopology	LED Topology Selection. Selects the Scan mode of LED topology. 00: Scan mode Topology 01: Reserved 10: Reserved 11: Reserved	RW	0B
19:18	P0_LedDefSel[1:0]	Select P0 LED Display Mode Definition. Selects LED bit display definition. 00: Mode Scan 0 01: Mode Scan 1 10: Mode Scan 2 11: Reserved	RW	00B
17:16	P1_LedDefSel[1:0]	Select P1 LED Display Mode Definition.	RW	00B
15:14	P2_LedDefSel[1:0]	Select P2 LED Display Mode Definition.	RW	00B
13:12	P3_LedDefSel[1:0]	Select P3 LED Display Mode Definition.	RW	00B
11:10	P4_LedDefSel[1:0]	Select P4 LED Display Mode Definition.	RW	00B
9:8	-	Reserved.	-	-
7	DisLEDBlinking	Disable LED Initial Blinking. 0: Enable LED blinking 1: Disable LED blinking	RW	0B
6	BlinkTime	0: 40ms 1: 120ms	RW	0B
5	-	Reserved.	-	-

Reg.bit	Name	Description	Mode	Default
4:2	CPUCtrlMask[2:0]	CPU Control LED Masking. When any bit of CPUCtrlMask[2:0] is 0b, it means the corresponding LED is controlled by internal circuit. Conversely, when any bit of CPUCtrlMask[2:0] is 1b, the corresponding LED is controlled by CPU and the indication is controlled by CPUCtrlPort. 0: LED is controlled by internal circuit 1: LED is controlled by CPU CPUCtrlMask[2:0] are mapped to LED[2:0] respectively. The developer could make a specific LED display a designated mode through CPUCtrlPort without influencing other LEDs. The other LEDs will still operate with the LedTopology, EnBiColor, and LedType settings. This setting effects all ports. **NOTE**: Only the CPUCtrlMask [0] is valid, CPUCtrlMask [2:1] is reserved in LED SCAN Mode .	RW	000B
1:0	-	Reserved.	-	-

11.3.5. LED Control Register 1 (0xBB80_4304)

Table 69. LED Control Register 1 (0xBB80_4304)

Reg.bit	Name	Description	Mode	Default
31:21	-	Reserved.	-	-
20:18	CPUCtrlPort0[2:0]	CPU Control Manner for Port 0. CPUCtrlPort0[2:0] are mapped to LED[2:0] respectively. Only valid when CPUCtorlMask bit is 1b. 0: LED off 1: LED on **NOTE**: Only the LED[0] is valid, LED[2:1] is reserved in LED SCAN Mode .	RW	000B
17:15	CPUCtrlPort1[2:0]	CPU Control Mode for Port 1.	RW	000B
14:12	CPUCtrlPort2[2:0]	CPU Control Mode for Port 2.	RW	000B
11:9	CPUCtrlPort3[2:0]	CPU Control Mode for Port 3.	RW	000B
8:6	CPUCtrlPort4[2:0]	CPU Control Mode for Port 4.	RW	000B
5:0	-	Reserved.	-	-

11.3.6. LED Blinking Control Register (0xBB80_430C)

Table 70. LED Blinking Control Register (0xBB80_430C)

Reg.bit	Name	Description	Mode	Default
31:20	-	Reserved.	-	-

Reg.bit	Name	Description	Mode	Default
19:17	LEDBlinkP0[2:0]	CPU Controls the LED to Blink for Port 0. LEDBlinkP0[2:0] are mapped to LED[2:0] respectively. Only valid when CPUCtorlMask bit is 1b. 0: Disable LED blinking 1: Enable LED blinking When LED blinking is enabled, no matter whether the designated LED is on or off, the designated LED will be forced to start blinking until the CPU disables it. **NOTE**: Only the LED[0] is valid, LED[2:1] is reserved in LED SCAN Mode .	RW	000B
16:14	LEDBlinkP1[2:0]	CPU Controls the LED to Blink for Port 1.	RW	000B
13:11	LEDBlinkP2[2:0]	CPU Controls the LED to Blink for Port 2.	RW	000B
10:8	LEDBlinkP3[2:0]	CPU Controls the LED to Blink for Port 3.	RW	000B
7:5	LEDBlinkP4[2:0]	CPU Controls the LED to Blink for Port 4.	RW	000B
4:0	-	Reserved.	-	-

11.3.7. EEE LED Configuration Register (0xBB80_4310)

Table 71. EEE LED Configuration Register (0xBB80_4310)

Reg.bit	Name	Description	Mode	Default
31:16	-	Reserved.	-	-
15:11	LPI_SBTOFF[4:0]	LPI Slow Blink Timer OFF-Period Time (Unit=100ms). Default=2000ms.	RW	0x14
10:6	LPI_SBTON[4:0]	LPI Slow Blink Timer ON-Period Time (Unit=100ms). Default=400ms.	RW	0x4
5:2	LPI_MT[3:0]	LPI Mask Off Time (Unit=100ms). To define the LED mask off time in a LPI LED state. Default=600ms.	RW	0xA
1	En10MLP	Enable 10Mbps port to show low power driving indication on LPI LED (same as the 10/100M port). 0: Disable 1: Enable	RW	0
0	enLPILED	Enable EEE LED Display Ability. 1: Enable 0: Disable *Note: When set to 1, the LPI LED display feature will remain disabled until after detecting a port has been linked-up for longer than 5 seconds.*	RW	0

11.3.8. Direct Mode LED Configuration Register (0xBB80_4314)

Table 72. Direct Mode LED Configuration Register (0xBB80_4314)

Reg.bit	Name	Description	Mode	Default
31	LEDOnPolarity	0: Normal Mode (LED output is Low active) 1: Reverse Mode (LED output is High active)	RW	0B
30:28	LEDBlinkTime	Blink Timer Period Time for All Port (Unit 40ms). 000: No blink 001: 40ms 010: 80ms 011: 120ms 100: 160ms 101: 200ms 110: 240ms 111: 280ms	RW	001B
27:18	-	Reserved.	-	-
17:15	LEDOnScaleP0[2:0]	Select the LED Turn On Scale for Port 0. 000: 12% 001: 25% 010: 37% 011: 50% 100: 62% 101: 75% 110: 87% 111: 100%	RW	111B
14:12	LEDOnScaleP1[2:0]	Select the LED Turn On Scale for Port 1.	RW	111B
11:9	LEDOnScaleP2[2:0]	Select the LED Turn On Scale for Port 2.	RW	111B
8:6	LEDOnScaleP3[2:0]	Select the LED Turn On Scale for Port 3.	RW	111B
5:3	LEDOnScaleP4[2:0]	Select the LED Turn On Scale for Port 4.	RW	111B
2:0	-	Reserved.	-	-

12. Green Ethernet

12.1. Cable Length Power Saving

The RTL8196E-VE1/2/3provides link-on and dynamic detection of cable length, and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

12.2. Link-Down Power Saving

The RTL8196E-VE1/2/3implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. A port automatically enters link-down power saving mode ten seconds after the cable is disconnected from it. Once a port enters link-down power saving mode, it transmits normal link pulses on its TXOP/TXON pins and continues to monitor the RXIP/RXIN pins to detect incoming signals, which might be 100Base-TX MLT-3 idle pattern, 10Base-T link pulses, or Auto-Negotiation's FLP (Fast Link Pulse). After it detects an incoming signal, it wakes up from link-down power saving mode and operates in normal mode according to the result of the connection's auto-negotiation.

12.3. Energy Efficient Ethernet (EEE)

The RTL8196E-VE1/2/3supports IEEE 802.3az, also known as Energy Efficient Ethernet (EEE) in 100Base-TX in full duplex operation, and 10Base-T in full/half duplex mode. It provides a protocol to coordinate transitions to/from a lower power consumption level (Low Power Idle mode) based on link utilization. When no packets are being transmitted, the system goes to Low Power Idle mode to save power. Once packets need to be transmitted, the system returns to normal mode, and does this without changing the link status and without dropping/corrupting frames.

To save power, when the system is in Low Power Idle mode, most of the circuits are disabled, however, the transition time to/from Low Power Idle mode is kept small enough to be transparent to upper layer protocols and applications.

EEE also specifies a negotiation method to enable link partners to determine whether EEE is supported and to select the best set of parameters common to both devices.

- For 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 10Base-T, EEE defines a 10Mbps PHY (10Base-Te) with reduced transmit amplitude requirements. 10Base-Te is fully interoperable with 10Base-T PHYs over 100m of Class-D (Cat-5) cable

The RTL8196E-VE1/2/3MAC uses Low Power Idle signaling to indicate to the PHY and to the link partner that a break in the data stream is expected. Components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

13. DC Specifications

13.1. Operating Conditions

Table 73. Operating Conditions

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD33	Digital I/O Power Supply 3.3V	3.135	3.3	3.465	V
AVDD33	Analog Power Supply 3.3V	3.135	3.3	3.465	V
VDD10	Core Power Supply 1.0V	0.95	1.00	1.1	V
SWR_VDD10	SWR Power Supply 1.0V input	0.95	1.00	1.1	V
AVDD10	Analog Power Supply 1.0V	0.95	1.00	1.1	V
AVDD33X	25/40MHz Crystal Power 3.3V	3.135	3.3	3.465	V
AVDD33_BG	System Bandgap Power Supply 3.3V	3.135	3.3	3.465	V
AVDD10_PCIE	PCI Express Analog Power 1.0V	0.95	1.00	1.1	V
AVDD10_PHYPLL	Ethernet PHY PLL Power 1.0V	0.95	1.00	1.1	V
AVDD33_PHYPLL	Ethernet PHY PLL Power 3.3V	3.135	3.3	3.465	V
AVDD33_USB	USB2.0 Analog Power 3.3V	3.135	3.3	3.465	V
AVDD10_USB	USB2.0 Analog Power 1.0V	0.95	1.00	1.1	V
AVDD33_SWR	SWR Power Input 3.3V	3.135	3.3	3.465	V
VDD33_LDO	LDO Power Input 3.3V	3.135	3.3	3.465	V
VDD33_25_18	SDR DRAM I/O Power Supply 3.3V DDR1 DRAM I/O Power Supply 2.5V DDR2 DRAM I/O Power Supply 1.8V	3.135 2.4 1.7	3.3 2.5 1.8	3.465 2.7 1.9	V
VREF	DDR1/DDR2 Reference Voltage	0.49* VDD33_25_18	0.5* VDD33_25_18	0.51* VDD33_25_18	V

13.2. Total Power Consumption

Table 74. Total Power Consumption

SYM	Conditions	Min	Typ.	Max	Units
PS	All LAN Ports Idle LAN Full Load Active for Link at 100Base-TX	- -	0.46 0.97	- -	Watt

Note: Power consumption is measured at full load of the chip system.

13.3. SDR DRAM Bus DC Parameters

Table 75. SDR DRAM Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	μA	-
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	μA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshoot: $V_{IH\ (MAX)}=V_{DDH}$ + 2V for a pulse width ≤3ns, and the pulse width not greater than one third of the cycle rate.

Note 2: V_{IL} undershoot: $V_{IL\ (MIN)}$=-2V for a pulse width ≤3ns cannot be exceeded.

Note 3: The output current buffer is 16mA for SDR DRAM clock, address, and data bus.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

13.4. DDR DRAM Bus DC Parameters

Table 76. DDR DRAM Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	SSTL_2	VREF+0.15	-	VREF+0.3	V
V_{IL}	Input-Low Voltage	SSTL_2	-0.3	-	VREF-0.15	V
V_{TT}	I/O Termination Voltage	-	VREF-0.04	-	VREF+0.04	V
I_{IL}	Input-Leakage Current	V_{IN}=VREF or 0	-10	±1	10	μA
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	μA

13.5. Flash Bus DC Parameters

Table 77. Flash Bus DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	1
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	3
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	3
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	μA	-
I_{OZ}	Tri-State Output-Leakage Current	-	-10	±1	10	μA	-
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	4
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	4

Note 1: V_{IH} overshoot: VIH (MAX)=VDDH + 2V for a pulse width ≤3ns.

Note 2: V_{IL} undershoot: $V_{IL\ (MIN)}$=-2V for a pulse width ≤3ns.

Note 3: The output current buffer is 8mA for the flash address and data bus; and is 8mA for Flash control signals.

Note 4: These values are typical values checked in the manufacturing process and are not tested.

13.6. USB v1.1 DC Parameters

Table 78. USB v1.1 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	2.0	-	-	V	2
V_{IL}	Input-Low Voltage	-	-	-	0.8	V	2
V_{OH}	Output-High Voltage	-	2.4	-	-	V	2
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	2
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-	-	-	µA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.

Note 2: For additional information, see the USB v1.1 Specification.

13.7. USB v2.0 DC Parameters

Table 79. USB v2.0 DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	-	200	-	-	mV	2
V_{IL}	Input-Low Voltage	-	-	-	10	mV	2
V_{OH}	Output-High Voltage	-	300	-	500	mV	2
V_{OL}	Output-Low Voltage	-	-10	-	10	mV	2
I_{IL}	Input-Leakage Current	-	-	-	-	µA	1

Note 1: These values are typical values checked in the manufacturing process and are not tested.

Note 2: For additional information, see the USB v2.0 Specification.

13.8. UART DC Parameters

Table 80. UART DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	V_{IN}=3.3V or 0	-10	±1	10	µA	2
R_{PU}	Input Pull-Up Resistance	-	-	75	-	KΩ	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for UART related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

13.9. GPIO DC Parameters

Table 81. GPIO DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	-	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	-	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	µA	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 8mA for GPIO related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

13.10. JTAG DC Parameters

Table 82. JTAG DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V	-
V_{OH}	Output-High Voltage	$\lvert I_{OH}\rvert$ =2~16mA	2.4	-	-	V	1
V_{OL}	Output-Low Voltage	$\lvert I_{OL}\rvert$ =2~16mA	-	-	0.4	V	1
I_{IL}	Input-Leakage Current	-	-10	±1	10	µA	2
R_{PD}	Input Pull-Down Resistance	-	-	75	-	KΩ	2

Note 1: The output current buffer is 4mA for JTAG related signals.

Note 2: These values are typical values checked in the manufacturing process and are not tested.

13.11. Reset DC Parameters

Table 83. Reset DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	LVTTL	2.0	-	-	V
V_{IL}	Input-Low Voltage	LVTTL	-	-	0.8	V

13.12. LED DC Parameters

Table 84. LED DC Parameters

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{OHED}	Output-High Voltage	-	2.4	-	-	V
V_{OLLED}	Output-Low Voltage	-	-	-	0.4	V

Note: The output current buffer for LED signals is 8mA.

14. AC Specifications

14.1. Clock Signal Timing

14.1.1. 25MHz System Clock Timing

Table 85. 25MHz System Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
V_{IH}	Input-High Voltage	2.0	-	-	V	-
V_{IL}	Input-Low Voltage	-	-	0.8	V	-
$T_{FREQUENCY}$	Clock Frequency for RTL8196E-VE1/2/3Crystal or Oscillator	-	25	-	MHz	1
$\Delta_{FREQUENCY}$	Clock Tolerance Over 0℃ to 50℃	-50	-	50	ppm	-
C_{SHUNT}	Crystal Parameter (Sometimes Referred to as the Holder Capacitance)	-	-	7	pF	2
C_1	Load Capacitance	-	-	30	pF	3
C_2	Load Capacitance	-	-	30	pF	3
T_{DC}	Duty Cycle	-	50	-	%	-

Note 1: This value could be an oscillator input or a series resonant frequency from a crystal. If used as an oscillator input, tie to the crystal input pin and leave the crystal output pin disconnected.

Note 2: The 25MHz Crystal CL=16pF is used on the RTL8196E.

Note 3: The RTL8196E-VE1/2/3PLL circuit requires an external 25MHz crystal with shunt capacitors. These shunt capacitors cannot be over 30pF due to chip design requirements.

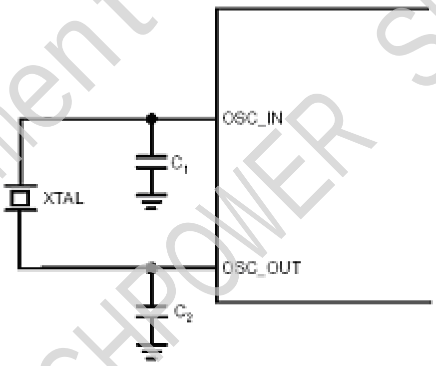


Figure 4. Typical Connection to a Crystal

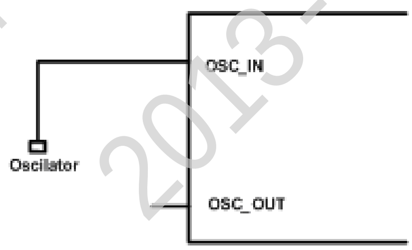


Figure 5. Typical Connection to an Oscillator

14.1.2. 40MHz System Clock Timing

Table 86. 40MHz System Clock Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
V_{IH}	Input-High Voltage	1.2	1.4	2.0	V
V_{IL}	Input-Low Voltage	-	-	0.2	V
$T_{FREQUENCY}$	Clock Frequency	-	40	-	MHz
$\Delta_{FREQUENCY}$	Clock Tolerance (between 0℃~70℃)	-50	-	50	ppm
T_{DC}	Duty Cycle	-	50	-	%

14.1.3. SDR DRAM Clock Timing

Table 87. SDR DRAM Clock Timing

Symbol	Parameter	Min.	Typ. (156.25MHz)	Max.	Units	Notes
$T_{PERIOD\_SDRAMCLK}$	Clock Period for SDR DRAM Clock	-	6.4	-	ns	-
$T_{CLKHIGH}$	SDR DRAM Clock High Time	-	3.2	-	ns	-
T_{CLKLOW}	SDR DRAM Clock Low Time	-	3.2	-	ns	-
$T_{RISE/FALL}$	Rise and Fall Time Requirements for SDR DRAM Clock	-	-	2	ns	-
$T_{RISE/FALL\_OUTPUT}$	Propagation Delay for Output Rising and Falling	-	NA	-	ns	1

Note 1: For detailed information, contact Realtek for the IBIS model.

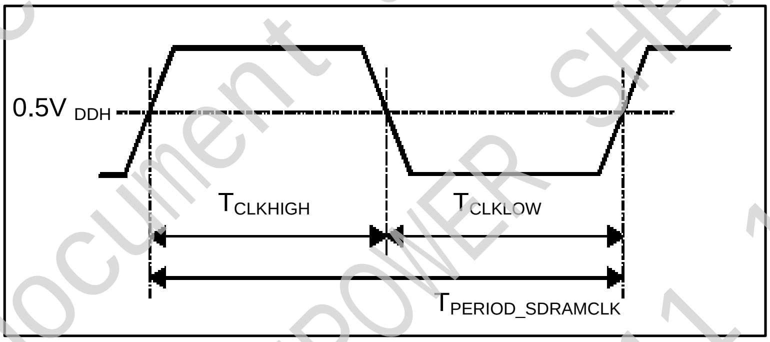


Figure 6. SDR DRAM Clock Specifications-1

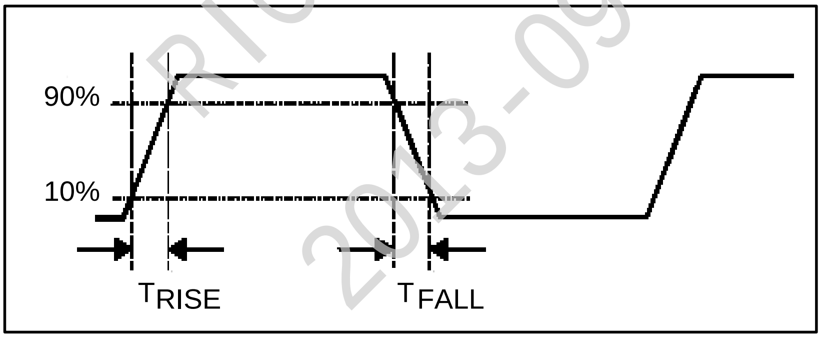


Figure 7. SDR DRAM Clock Specifications-2

14.2. Bus Signal Timing

14.2.1. SDR DRAM Bus

14.2.1.1 SDR DRAM Input Timing

Table 88. SDR DRAM Input Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{SETUP}	Input Setup Prior to Rising Edge of Clock Inputs included in this timing are MD[15:0] (during a read operation)	-	1.13	-	ns
T_{HOLD}	Input Hold Time after the Rising Edge of Clock Inputs included in this timing are MD[15:0] (during a read operation)	-	0	-	ns

Note: The RTL8196E-VE1/2/3integrates some timing controls on the interface. Here the timing parameters listed in the table are extracted in the default situation (without specific controls).

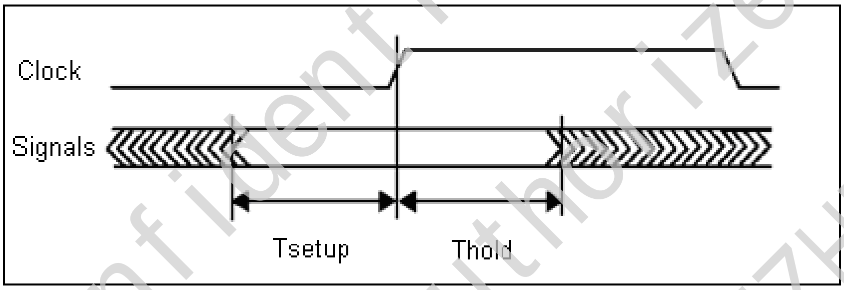


Figure 8. SDR DRAM Input Timing

14.2.1.2 SDR DRAM Output Timing

Table 89. SDR DRAM Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
$T_{CLK2OUT}$	Rising Edge of Clock-to-Signal Output Outputs include this timing are MD[15:0], MCS0#, MCS1#, RAS#, CAS#, LDQM, UDQM, WE# (during a write operation)	-	-	2.3	ns
$T_{HOLDOUT}$	Signal Output Hold Time after the Rising Edge of the Clock Outputs included in this timing are MD[15:0] (during a write operation)	0.8	-	-	ns

Note: Timing was tested with 75-pF capacitor to ground.

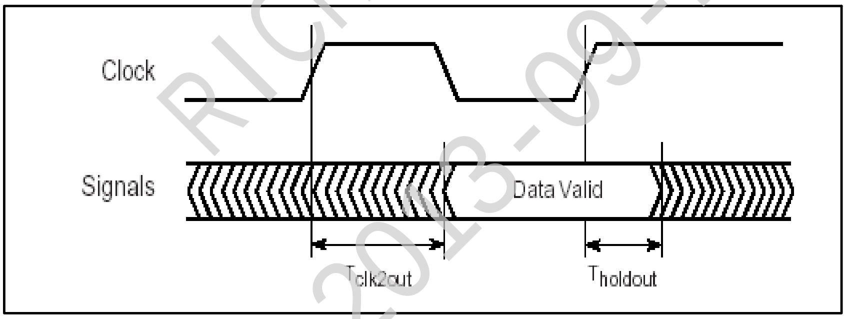


Figure 9. SDR DRAM Output Timing

14.2.1.3 SDR DRAM Access Control Timing

Table 90. SDR DRAM Access Control Timing

Symbol	Parameter	Units	Notes
$T_{REFRESH}$	Auto-Refresh Timing Controlled by Reg. 0xB8001008 (DTR)	µs	-
T_{RCD}	The Time Interval between RAS# Active and CAS# Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RP}	The Time Interval between Pre-Charge and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RAS}	The Time Interval between Active and Pre-Charge Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RC}	The Time Interval between Active and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	1
T_{RFC}	The Time Interval between Auto-Refresh and Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
$T_{CAS\_LATENCY}$	The Data Output Delay after CAS# Active Controlled by Reg. 0xB8001004 (DCR)	ns	-

Note 1: TRC=TRAS+TRP.

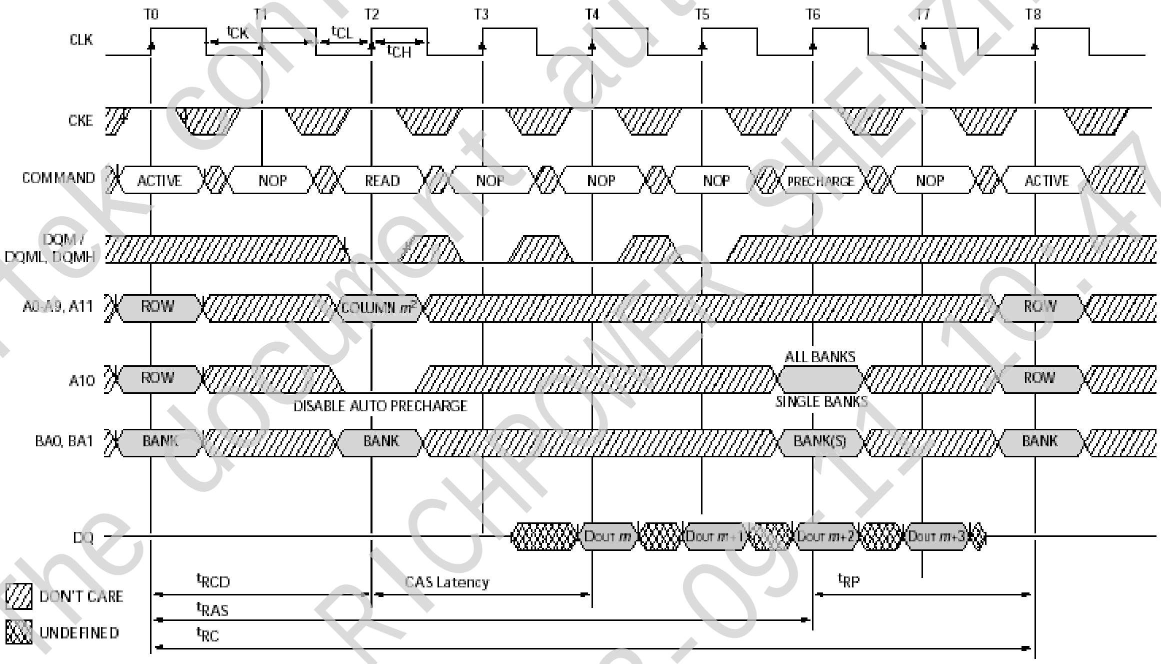


Figure 10. SDR DRAM Access Control Timing

14.2.2. DDR DRAM Bus

14.2.2.1 DDR DRAM Input Timing

Table 91. DDR DRAM Input Timing

Symbol	Parameter	Units	Notes
T_{SETUP}	Input Setup Prior to Rising Edge of Clock Inputs included in this timing are D[31:0] (during a read operation)	ns	1
T_{HOLD}	Input Hold Time after the Rising Edge of Clock Inputs included in this timing are D[31:0] (during a read operation)	ns	1

Note 1: The RTL8196E-VE1/2/3integrates some timing control registers on the interface.

14.2.2.2 DDR DRAM Output Timing

Table 92. DDR DRAM Output Timing

Symbol	Parameter	Units	Notes
$T_{CLK2OUT}$	Rising Edge of Clock-to-Signal Output Outputs include this timing are D[31:0], CS0#, CS1#, RAS#, CAS#, LDQM, UDQM, WE#, LDQS, UDQS (during a write operation)	ns	1
$T_{HOLDOUT}$	Signal Output Hold Time after the Rising Edge of the Clock Outputs included in this timing are D[31:0] (during a write operation)	ns	1

Note 1: The RTL8196E-VE1/2/3integrates some timing control registers on the interface.

14.2.2.3 DDR DRAM Access Control Timing

Table 93. DDR DRAM Access Control Timing

Symbol	Parameter	Units	Notes
$T_{REFRESH}$	Auto-Refresh Timing Controlled by Reg. 0xB8001008 (DTR)	µs	-
T_{RCD}	The Time Interval between RAS# Active and CAS# Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RP}	The Time Interval between Pre-Charge and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RAS}	The Time Interval between Active and Pre-Charge Controlled by Reg. 0xB8001008 (DTR)	ns	-
T_{RC}	The Time Interval between Active and the Next Active Controlled by Reg. 0xB8001008 (DTR)	ns	1
T_{RFC}	The Time Interval between Auto-Refresh and Active Controlled by Reg. 0xB8001008 (DTR)	ns	-
$T_{CAS\_LATENCY}$	The Data Output Delay after CAS# Active Controlled by Reg. 0xB8001004 (DCR)	ns	-

Note 1: TRC=TRAS+TRP.

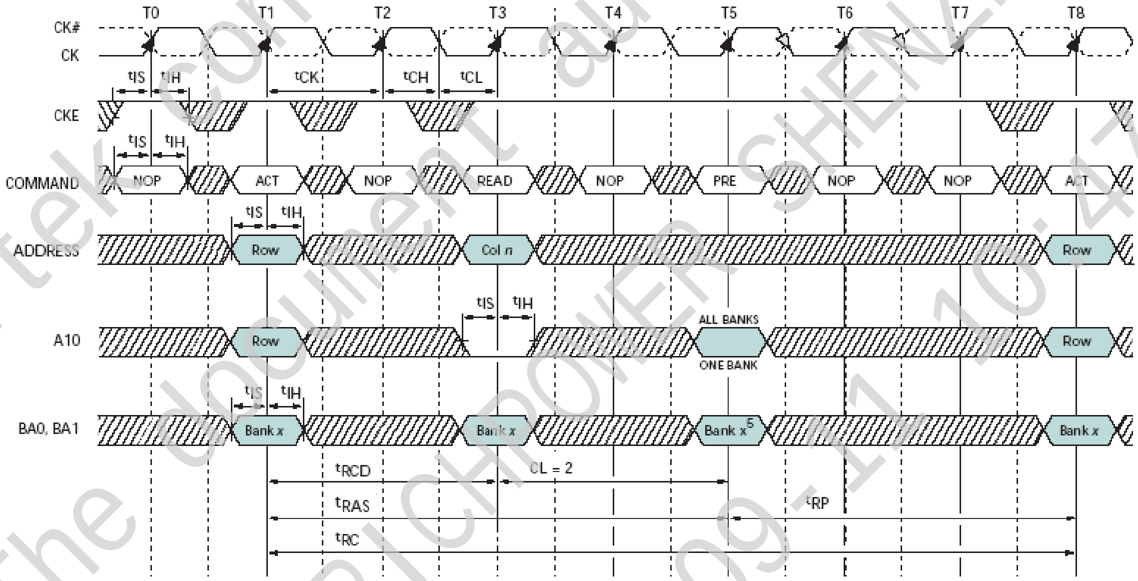


Figure 11. DDR DRAM Access Control Timing

14.2.3. Serial Flash Interface

14.2.3.1 Serial Flash Interface Output Timing

Table 94. Serial Flash Interface Output Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{SLCH}	The Timing Interval from Chip-Select Activated to the First Clock Rising Edge	2	-	-	ns
T_{CHSH}	The Timing Interval from the Last Clock Rising Edge to Chip-Select De-Activated	5	-	-	ns
T_{CLQV}	The Timing Interval from the Last Clock Falling Edge to Data-Out Validated	-	-	10	ns
T_{CLQX}	The Timing Interval from the Next Clock Falling Edge to Data-Out Invalidated	0	-	-	ns

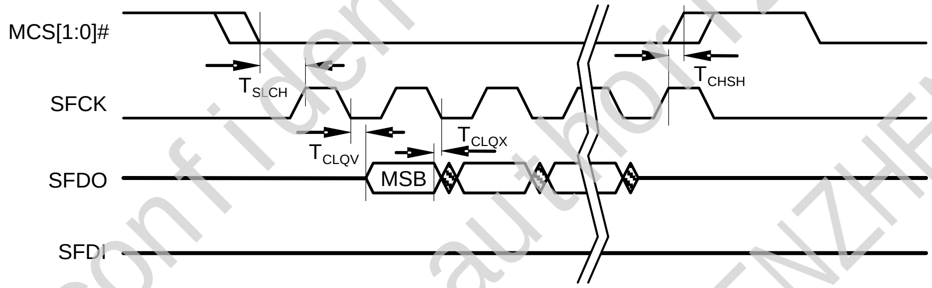


Figure 12. Serial Flash Interface Output Timing

14.2.3.2 Serial Flash Interface Input Timing

Table 95. Serial Flash Interface Input Timing

Symbol	Parameter	Min.	Typ.	Max.	Units
T_{DVCH}	The Timing Interval from Data-Input Ready to the Clock Rising Edge	2	-	-	ns
T_{CHDX}	The Timing Interval from the Clock Rising Edge to Data-Input Invalidated	5	-	-	ns

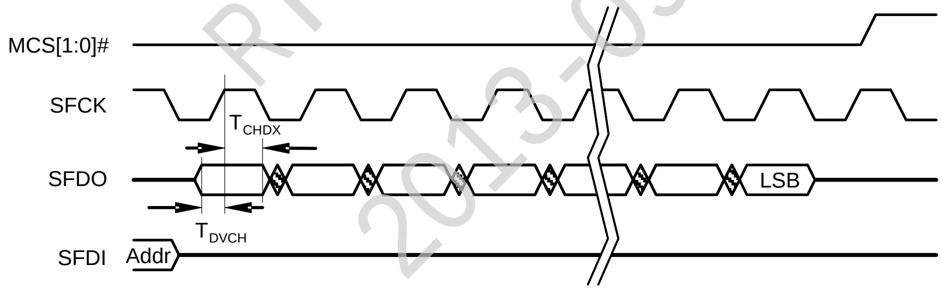


Figure 13. Serial Flash Interface Input Timing

14.2.4. JTAG Boundary Scan

Table 96. JTAG Boundary Scan Interface Timing Values

Symbol	Parameter	Min.	Typ.	Max.	Units	Notes
T_{bscl}	JTAG Clock Low Time	50	-	-	ns	1
T_{bsch}	JTAG Clock High Time	50	-	-	ns	1
T_{bsis}	TDI, TMS Setup Time to Rising Edge of TCK	10	-	-	ns	-
T_{bsih}	TDI, TMS Hold Time from Rising Edge of TCK	10	-	-	ns	-
T_{bsoh}	TDO Hold Time after Falling Edge of TCK	1.5	-	-	ns	-
T_{bsod}	TDO Output from Falling Edge of TCK	-	-	40	ns	-
T_{bsr}	JTAG Reset Period	30	-	-	ns	-
T_{bsrs}	TMS Setup Time to Rising Edge of JTAG Reset	10	-	-	ns	-
T_{bsrh}	TMS Hold Time from Rising Edge of JTAG Reset	10	-	-	ns	-

Note 1: JTAG clock TCK may be stopped indefinitely in either the low or high phase.

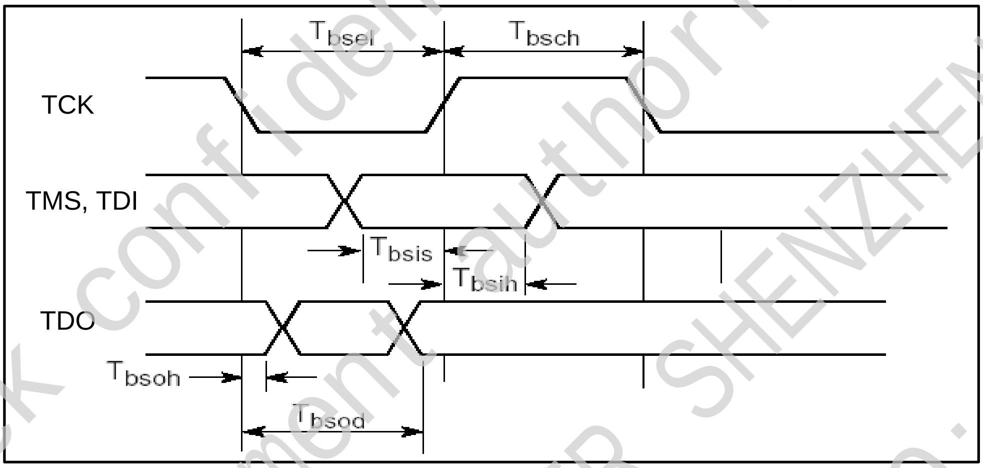


Figure 14. Boundary-Scan General Timing

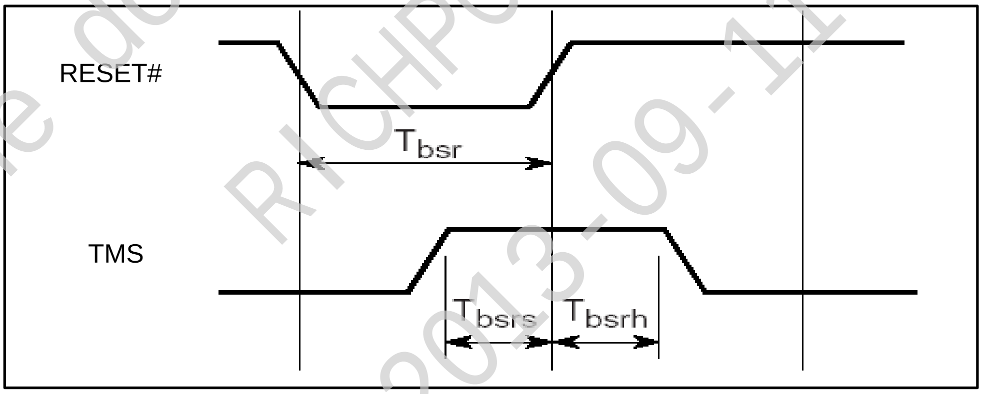


Figure 15. Boundary-Scan Reset Timing

14.2.5. Power Configuration Timing

Power up configuration only relates to internal timing. The external hardware pin reset is unconcerned with power up configuration. The Hardware reset pin is valid when an internal reset ends the active state.

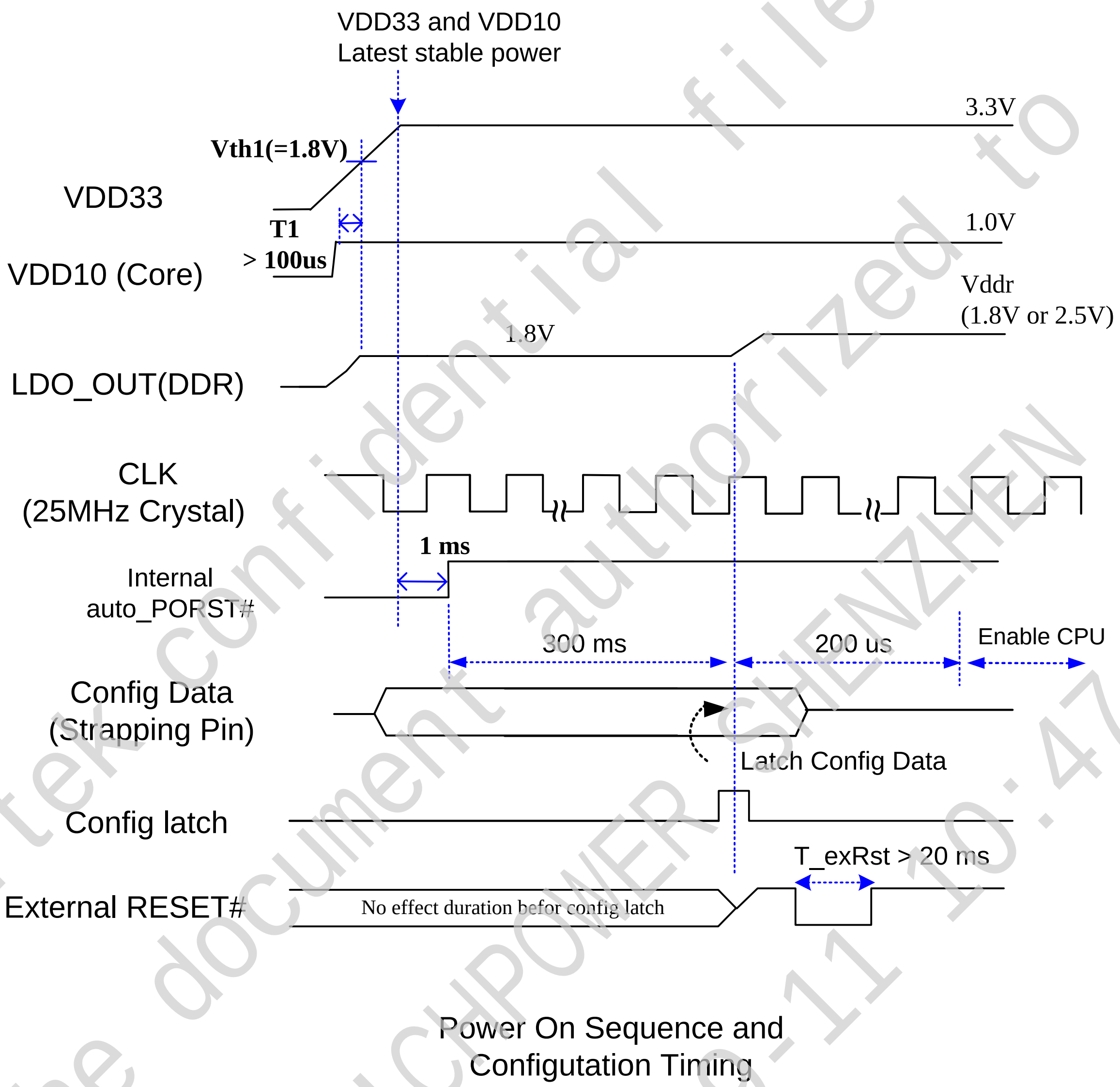


Figure 16. Power Up Configuration Timing

14.3. PCI Express Bus Parameters

14.3.1. Differential Transmitter Parameters

Table 97. Differential Transmitter Parameters

Symbol	Parameter	Min	Typical	Max	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{TX-DIFFp-p}$	Differential Peak-to-Peak Output Voltage	0.800	-	1.2	V
$V_{TX-DE-RATIO}$	De-Emphasized Differential Output Voltage (Ratio)	-3.0	-3.5	-4.0	dB
T_{TX-EYE}	Minimum TX Eye Width	0.75	-	-	UI
$T_{TX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time between the Jitter Median and Maximum Deviation from the Median	-	-	0.125	UI
$T_{TX-RISE}$, $T_{TX-FALL}$	D+/D- TX Output Rise/Fall Time	0.125	-	-	UI
$V_{TX-CM-ACp}$	RMS AC Peak Common Mode Output Voltage	-	-	20	mV
$V_{TX-CM-DCACTIVE-IDLEDELTA}$	Absolute Delta of DC Common Mode Voltage During L0 and Electrical Idle	0	-	100	mV
$V_{TX-CM-DCLINE-DELTA}$	Absolute Delta of DC Common Mode Voltage between D+ and D-	0	-	25	mV
$V_{TX-IDLE-DIFFp}$	Electrical Idle Differential Peak Output Voltage	0	-	20	mV
$V_{TX-RCV-DETECT}$	The Amount of Voltage Change Allowed During Receiver Detection	-	-	600	mV
$V_{TX-DC-CM}$	TX DC Common Mode Voltage	0	-	3.6	V
$I_{TX-SHORT}$	TX Short Circuit Current Limit	-	-	90	mA
$T_{TX-IDLE-MIN}$	Minimum Time Spent in Electrical Idle	50	-	-	UI
$T_{TX-IDLE-SETTO-IDLE}$	Maximum Time to Transition to A Valid Electrical Idle After Sending An Electrical Idle Ordered Set	-	-	20	UI
$T_{TX-IDLE-TOTO-DIFF-DATA}$	Maximum Time to Transition to Valid TX Specifications After Leaving An Electrical Idle Condition	-	-	20	UI
$RL_{TX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{TX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{TX-DIFF-DC}$	DC Differential TX Impedance	80	100	120	Ω
$L_{TX-SKEW}$	Lane-to-Lane Output Skew	-	-	500+2*UI	ps
C_{TX}	AC Coupling Capacitor	75	-	200	nF
$T_{crosslink}$	Crosslink Random Timeout	0	-	1	ms

Note 1: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

Note 2: The data rate can be modulated with an SSC (Spread Spectrum Clock) from +0 to -0.5% of the nominal data rate frequency, at a modulation rate in the range not exceeding 30kHz – 33kHz. The ±300ppm requirement still holds, which requires the two communicating ports be modulated such that they never exceed a total of 600ppm difference.

14.3.2. Differential Receiver Parameters

Table 98. Differential Receiver Parameters

Symbol	Parameter	Min.	Typical	Max.	Units
UI	Unit Interval	399.88	400	400.12	ps
$V_{RX-DIFFp-p}$	Differential Input Peak-to-Peak Voltage	0.175	-	1.200	V
T_{RX-EYE}	Minimum Receiver Eye Width	0.4	-	-	UI
$T_{RX-EYE-MEDIAN-to-MAX-JITTER}$	Maximum Time Between the Jitter Median and Maximum Deviation from the Median	-	-	0.3	UI
$V_{RX-CM-ACp}$	AC Peak Common Mode Input Voltage	-	-	150	mV
$RL_{RX-DIFF}$	Differential Return Loss	10	-	-	dB
RL_{RX-CM}	Common Mode Return Loss	6	-	-	dB
$Z_{RX-DIFF-DC}$	DC Differential Input Impedance	80	100	120	Ω
Z_{RX-DC}	DC Input Impedance	40	50	60	Ω
$Z_{RX-HIGH-IMP-DC}$	Powered Down DC Input Impedance	200k	-	-	Ω
$V_{RX-IDLE-DET-DIFFp-p}$	Electrical Idle Detect Threshold	65	-	175	mV
$T_{RX-IDLE-DET-DIFFENTERTIME}$	Unexpected Electrical Idle Enter Detect Threshold Integration Time	-	-	10	ms
$L_{RX-SKEW}$	Total Skew	-	-	20	ns

Note: Refer to PCI Express Base Specification, rev.1.1, for correct measurement environment setting of each parameter.

14.3.3. REFCLK Parameters

Table 99. REFCLK Parameters

Symbol	Parameter	100MHz Input		Units	Note
		Min	Max		
Rise Edge Rate	Rising Edge Rate	0.6	4.0	V/ns	2, 3
Fall Edge Rate	Falling Edge Rate	0.6	4.0	V/ns	2, 3
V_{IH}	Differential Input High Voltage	+150	-	mV	2
V_{IL}	Differential Input Low Voltage	-	-150	mV	2
V_{CROSS}	Absolute Crossing Point Voltage	+250	+550	mV	1, 4, 5
$V_{CROSS\ DELTA}$	Variation of V_{CROSS} Over All Rising Clock Edges	-	+140	mV	1, 4, 9
V_{RB}	Ring-Back Voltage Margin	-100	+100	mV	2, 12
T_{STABLE}	Time before V_{RB} is Allowed	500	-	ps	2, 12
$T_{PERIOD\ AVG}$	Average Clock Period Accuracy	-300	+2800	ppm	2, 10, 13
$T_{PERIOD\ ABS}$	Absolute Period (Including Jitter and Spread Spectrum)	9.847	10.203	ns	2, 6
$T_{CCJITTER}$	Cycle to Cycle Jitter	-	150	ps	2
V_{MAX}	Absolute Maximum Input Voltage	-	+1.15	V	1, 7
V_{MIN}	Absolute Minimum Input Voltage	-	-0.3	V	1, 8
Duty Cycle	Duty Cycle	40	60	%	2

Symbol	Parameter	100MHz Input Min	Max	Units	Note
Rise-Fall Matching	Rising Edge Rate (REFCLK+) to Falling Edge Rate (REFCLK-) Matching	-	20	%	1, 14
$Z_{C\text{-}DC}$	Clock Source DC Impedance	40	60	Ω	1, 11

Note 1: Measurement taken from single-ended waveform.

Note 2: Measurement taken from differential waveform.

Note 3: Measured from -150mV to +150mV on the differential waveform (derived from REFCLK+ minus REFCLK-). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing. See Figure 20, page 70.

Note 4: Measured at crossing point where the instantaneous voltage value of the rising edge of REFCLK+ equals the falling edge of REFCLK-. See Figure 17, page 69.

Note 5: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement. See Figure 17, page 69.

Note 6: Defines as the absolute minimum or maximum instantaneous period. This includes cycle to cycle jitter, relative ppm tolerance, and spread spectrum modulation. See Figure 19, page 69.

Note 7: Defined as the maximum instantaneous voltage including overshoot. See Figure 17, page 69.

Note 8: Defined as the minimum instantaneous voltage including undershoot. See Figure 17, page 69.

Note 9: Defined as the total variation of all crossing voltages of Rising REFCLK+ and Falling REFCLK-. This is the maximum allowed variance in VCROSS for any particular system. See Figure 17, page 69.

Note 10: Refer to Section 4.3.2.1 of the PCI Express Base Specification, Revision 1.1 for information regarding ppm considerations.

Note 11: System board compliance measurements must use the test load card described in Figure 23, page 71. REFCLK+ and REFCLK- are to be measured at the load capacitors CL. Single ended probes must be used for measurements requiring single ended measurements. Either single ended probes with math or differential probe can be used for differential measurements. Test load CL=2pF.

Note 12: T_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to droop back into the V_{RB} ±100mV differential range. See Figure 22, page 71.

*Note 13: PPM refers to parts per million and is a DC absolute period accuracy specification. 1ppm is 1/1,000,000th of 100.000000MHz exactly, or 100Hz. For 300ppm then we have an error budget of 100Hz/ppm*300ppm=30kHz. The period is to be measured with a frequency counter with measurement window set to 100ms or greater. The ±300ppm applies to systems that do not employ Spread Spectrum or that use common clock source. For systems employing Spread Spectrum there is an additional 2500ppm nominal shift in maximum period resulting from the 0.5% down spread resulting in a maximum average period specification of +2800ppm.*

Note 14: Matching applies to rising edge rate for REFCLK+ and falling edge rate for REFCLK-. It is measured using a ±75mV window centered on the median cross point where REFCLK+ rising meets REFCLK- falling. The median cross point is used to calculate the voltage thresholds the oscilloscope is to use for the edge rate calculations. The Rise Edge Rate of REFCLK+ should be compared to the Fall Edge Rate of REFCLK-; the maximum allowed difference should not exceed 20% of the slowest edge rate. See Figure 18, page 69.

Note 15: Refer to PCI Express Card Electromechanical Specification, rev.1.1, for correct measurement environment setting of each parameter.

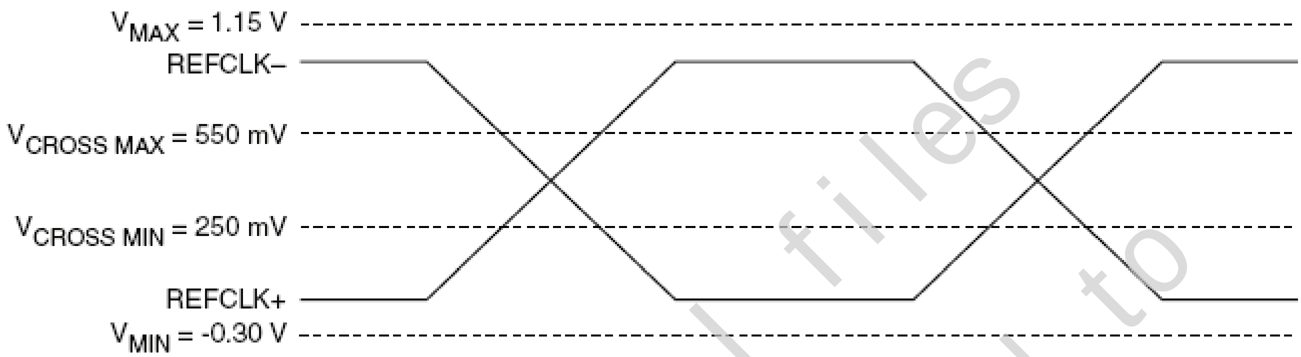


Figure 17. Single-Ended Measurement Points for Absolute Cross Point and Swing

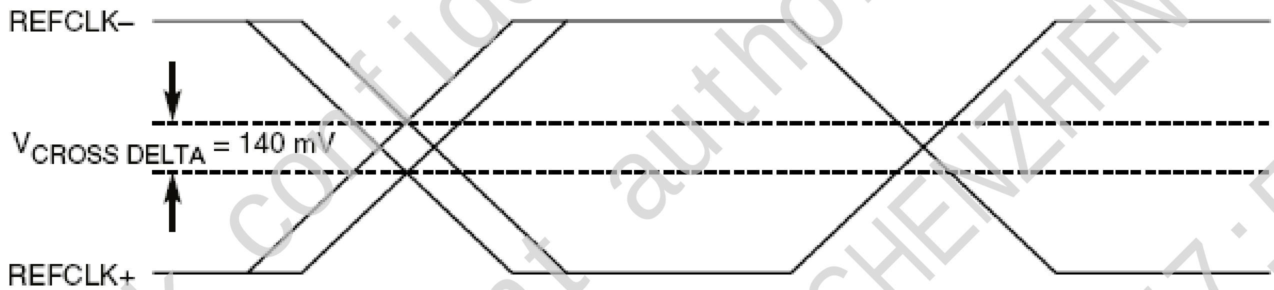


Figure 18. Single-Ended Measurement Points for Delta Cross Point

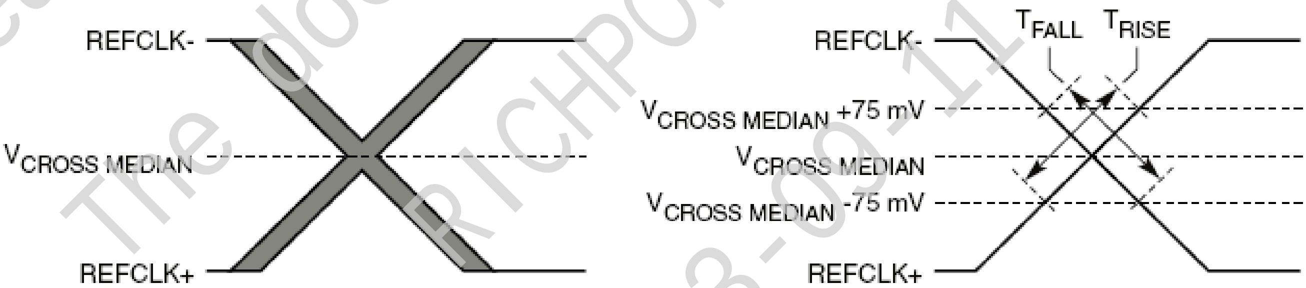


Figure 19. Single-Ended Measurement Points for Rise and Fall Time Matching

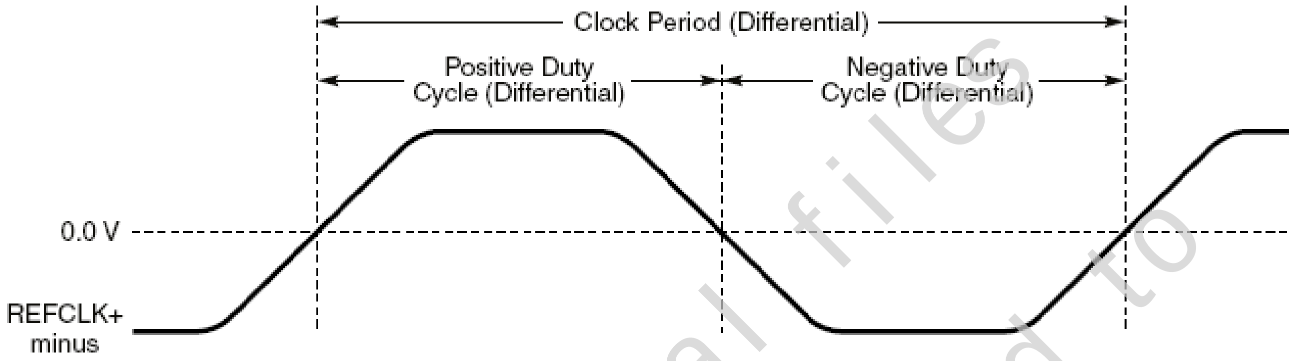


Figure 20. Differential Measurement Points for Duty Cycle and Period

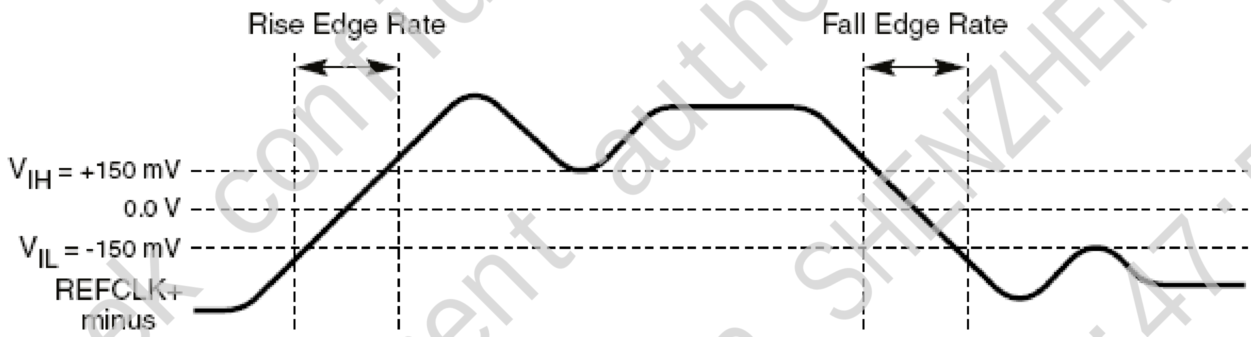


Figure 21. Differential Measurement Points for Rise and Fall Time

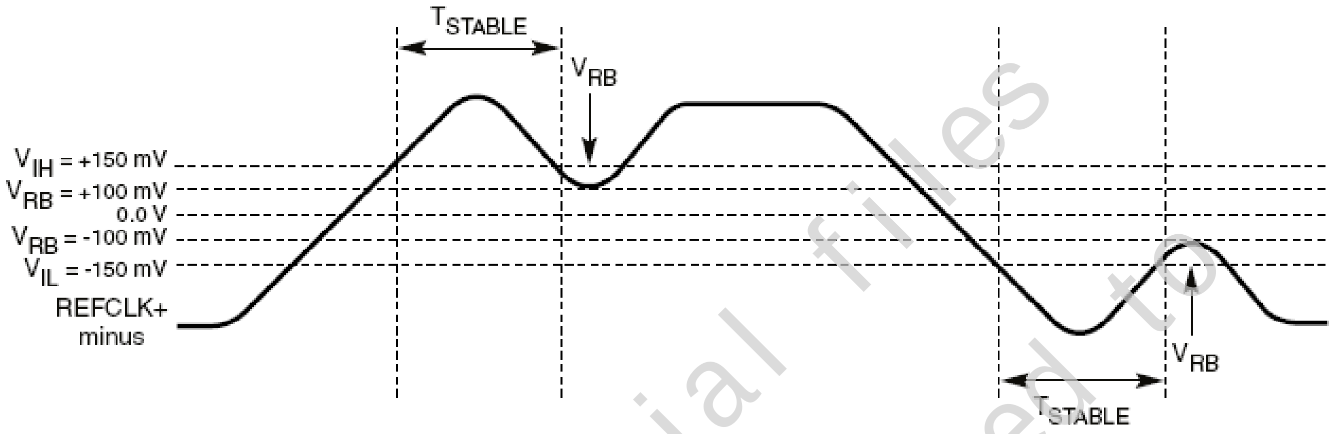


Figure 22. Differential Measurement Points for Ringback

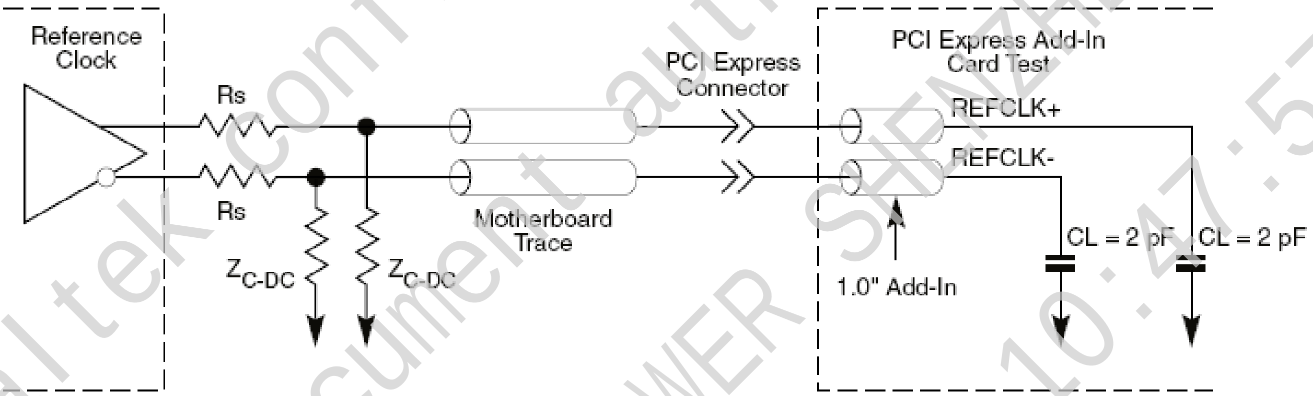


Figure 23. Reference Clock System Measurement Point and Loading

15. Thermal Characteristics

Heat generated by the chip causes a temperature rise of the package. If the temperature of the chip (Tj, junction temperature) is beyond the design limits, there will be negative effects on operation and the life of the IC package. Heat dissipation, either through a heat sink or electrical fan, is necessary to provide a reasonable environment (Ta, ambient temperature) in a closed case. As power density increases, thermal management becomes more critical. A method to estimate the possible Ta is outlined below.

Thermal parameters are defined as below according to JEDEC standard JESD 51-2, 51-6:

(1) θja (Thermal resistance from junction to ambient), represents resistance to heat flow from the chip to ambient air. This is an index of heat dissipation capability. A lower θja means better thermal performance.

θja=(Tj-Ta)/P

Where Tj is the die junction temperature, Ta is the ambient air temperature,

P is the power dissipation by device (Watts)

(2) θjc (Thermal Resistance Junction-to-Case, °C/W), measures the heat flow resistance between the die surface and the surface of the package (case). This data is relevant for packages used with external heatsinks.

θjc=(Tj-Tc)/P

Where Tj is the die junction temperature, Tc is the package case temperature.

P is the power dissipation by device (Watts)

(3) Ψjt (Thermal Characterization Parameter: Junction to package top), represents the correlation between the temperature of the chip and the package top.

Ψjt=(Tj-Tt)/P

Where Tj is the die junction temperature, Tt is the top of package temperature.

P is the power dissipation by the device (Watts)

Thermal Terminology

The major thermal dissipation paths can be illustrated as following:

Tj: The maximum junction temperature

Ta: The ambient or environment temperature

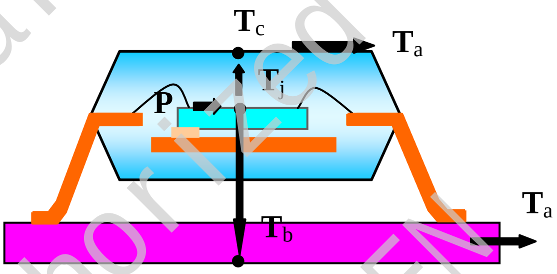
Tc: The maximum compound surface temperature

Tb: The maximum surface temperature of PCB bottom

P: Total input power

PQFP Junction to ambient thermal resistance, θja, defined as:

$$\theta ja = \frac{TJ - TA}{P}$$



Thermal Dissipation of PQFP Package

15.1. Thermal Operating Range

Table 100. Thermal Operating Range

Parameter	SYM	Condition	Min	Typ.	Max	Units
Storage Temperature	-	-	-55	-	125	°C
Junction Operating Temperature	Tj	-	0	-	125	°C
Ambient Operating Temperature	Ta	4-layer FR4 PCB (without heat sink)	0	25	65	°C

Note: PCB conditions (JEDEC JESD51-7). Dimensions: 120mm x 90mm. Thickness: 1.6mm.

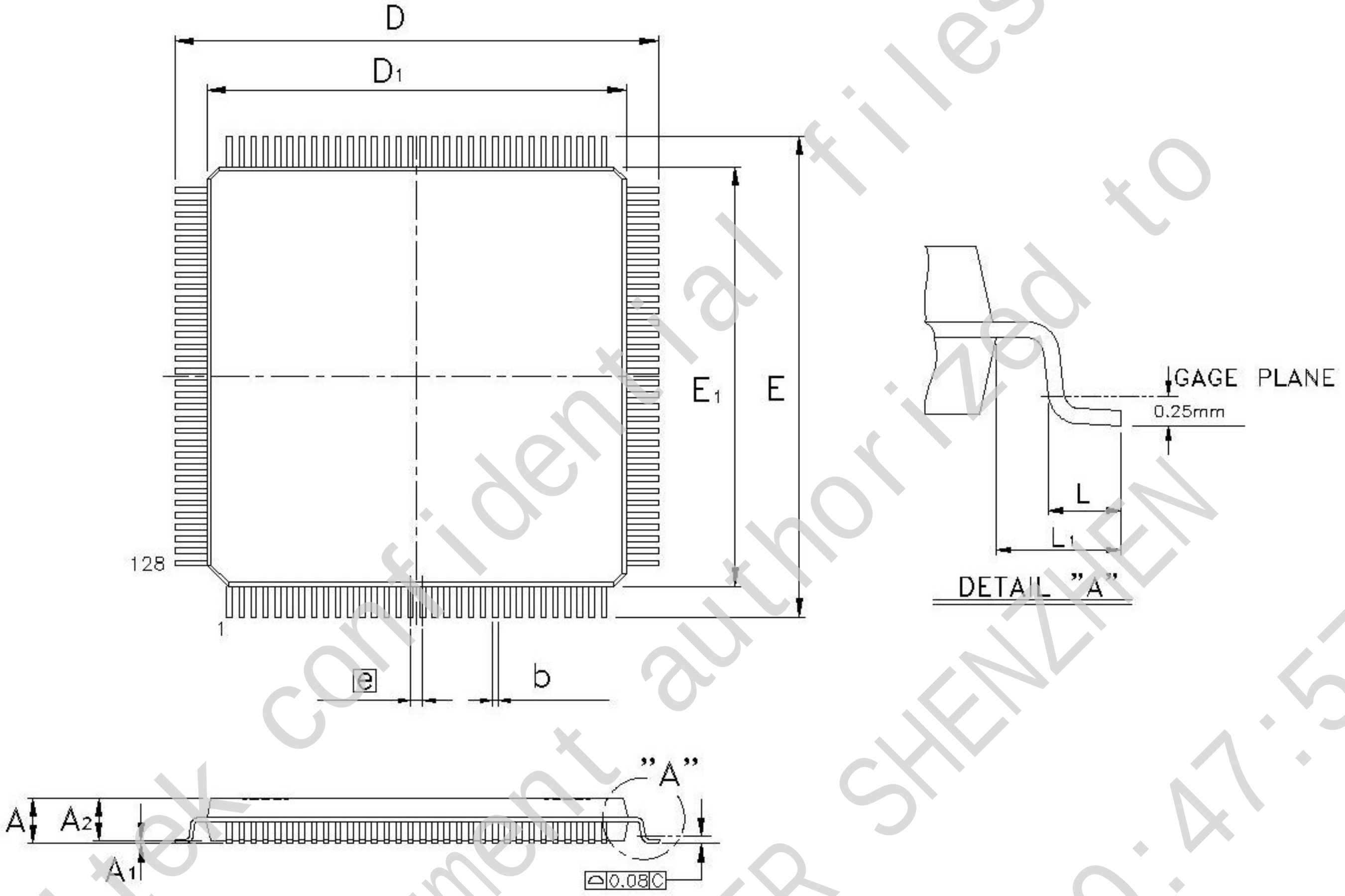
15.2. Thermal Parameters

Table 101. Thermal Parameters

Parameter	SYM	Condition	Air Flow 0 m/s	Units
Thermal Resistance: Junction to Ambient	θja	4-layer FR4 PCB	43.45	°C/W
Thermal Resistance: Junction to Ambient	θja	2-layer FR4 PCB	48.53	°C/W
Thermal Characterization: Junction to Package Top	Ψjt	4-layer FR4 PCB	2.84	°C/W
Thermal Characterization: Junction to Package Top	Ψjt	2-layer FR4 PCB	2.94	°C/W
Thermal Resistance: Junction to Case	θjc	4-layer FR4 PCB	13.98	°C/W
Thermal Resistance: Junction to Case	θjc	2-layer FR4 PCB	14.29	°C/W

16. Mechanical Dimensions

Low Profile Plastic Quad Flat Package 128 Lead 14x14mm Outline



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A_1	0.05	-	0.15	0.002	-	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.13	0.18	0.23	0.005	0.007	0.090
D/E	16.00BSC			0.630BSC		
D_1/E_1	14.00BSC			0.551BSC		
e	0.40BSC			0.016BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-026.

17. Ordering Information

Table 102. Ordering Information

Part Number	Package	Status
RTL8196E-VE*n*-CG *n*=1 : 8M byte DRAM embedded *n*=2 : 16M byte DRAM embedded *n*=3 : 32M byte DRAM embedded	Low Profile Plastic Quad Flat Package 128 'Green' Package	Mass Production

Note: See page 5 for package identification information.

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