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RTL8370-GR

LAYER 2 MANAGED 8-PORT 10/100/1000 SWITCH CONTROLLER

RTL8370M-GR

LAYER 2 MANAGED 8+2-PORT 10/100/1000 SWITCH CONTROLLER

DATASHEET

(CONFIDENTIAL: Development Partners Only)

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USING THIS DOCUMENT

This document is intended for the hardware and software engineer's general information on the Realtek RTL8370(M) ICs.

Though every effort has been made to ensure that this document is current and accurate, more information may have become available subsequent to the production of this guide.

REVISION HISTORY

Revision	Release Date	Summary
1.0	2010/08/20	First release.
1.1	2011/03/25	Added section 13.5.3 MDIO Slave Mode Timing Characteristics, page 84. Revised section 13.6 Power and Reset Characteristics, page 90. Revised Table 2 Pin Assignment Table (RTL8370M: TQFP-176), page 12 (Pin 107 and Pin 108). Revised Table 15 Extension GMAC0 MII Pins (MII MAC Mode or MII PHY Mode) of the RTL8370M (TQFP176), page 31. Revised Table 20 Configuration Strapping Pins (DISAUTOLOAD, DIS_8051, and EN_FLASH) (RTL8370M), page 39. Revised Table 27 RTL8370M General Purpose Interfaces Pin Definitions, page 63. Revised Table 32 Extension GMAC0 MII Pins, page 67. Revised Table 60 EEPROM SMI Host Mode Timing Characteristics, page 83. Revised Figure 25 EEPROM SMI Slave Mode Timing Characteristics, page 83.

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1. General Description

The RTL8370 is an LQFP128 E-PAD, high-performance 8-port Gigabit Ethernet switch, and the RTL8370M is a TQFP176 E-PAD, high-performance 8+2-port Gigabit Ethernet switch.

Both the RTL8370 and RTL8370M feature low-power integrated 8-port Giga-PHYs that support 1000Base-T, 100Base-T, and 10Base-T.

The RTL8370M supports two extra GMII/RGMII/MII ports for specific applications. The RTL8370 and RTL8370M integrate all the functions of a high-speed switch system; including SRAM for packet buffering, non-blocking switch fabric, and internal register management into a single CMOS device. Only a 25MHz crystal is required; an optional EEPROM is offered for internal register configuration.

The embedded packet storage SRAM in the RTL8370(M) features superior memory management technology to efficiently utilize memory space. The RTL8370(M) integrates an 8K-entry look-up table with a 4-way XOR Hashing algorithm for address searching and learning. The table provides read/write access from the EEPROM Serial Management Interface (SMI), and each of the entries can be configured as a static entry. The entry aging time is between 200 and 400 seconds. Eight Filtering Databases are used to provide Independent VLAN Learning and Shared VLAN Learning (IVL/SVL) functions.

Unfinished file and contains much errors. Do not use for anything. The Extension GMAC0 and Extension GMAC1 of the RTL8370M implement dual GMII/RGMII/MII interfaces for connecting with an external PHY or MAC in specific applications. This interface could be connected to an external CPU or RISC as 8-port Gigabit Router applications. In router applications, the RTL8370(M) supports Port VID (PVID) for each port to insert a PVID in the VLAN tag on egress. When using this function, VID information carried in the VLAN tag will be changed to PVID.

Note: The RTL8370M (only) Extra Interface (Extension GMAC0 and Extension GMAC1) supports:
Gigabit Media Independent Interface (GMII)
Reduced Gigabit Media Independent Interface (RGMII)
Media Independent Interface (MII)

The RTL8370(M) supports standard 802.3x flow control frames for full duplex, and optional backpressure for half duplex. It determines when to invoke the flow control mechanism by checking the availability of system resources, including the packet buffers and transmitting queues. The RTL8370(M) supports broadcast/multicast output dropping, and will forward broadcast/multicast packets to non-blocked ports only. For IP multicast applications, the RTL8370(M) supports IPv4 IGMPv1/v2/v3 and IPv6 MLDv1/v2 snooping.

In order to support flexible traffic classification, the RTL8370(M) supports 64-entry ACL rule check and multiple actions options. Each port can optionally enable or disable the ACL rule check function. The ACL rule key can be based on packet physical port, Layer2, Layer3, and Layer4 information. When an ACL rule matches, the action taken is configurable to Drop/Permit/Redirect/Mirror, change priority value in 802.1q/Q tag, and rate policing. The rate policing mechanism supports from 8Kbps to 1Gbps (in 8Kbps steps).

In Bridge operation the RTL8370(M) supports 16 sets of port configurations: disable, block, learning, and forwarding for Spanning Tree Protocol and Multiple Spanning Tree Protocol. To meet security and management application requirements, the RTL8370(M) supports IEEE 802.1x Port-based/MAC-based Access Control. For those ports that do not pass IEEE 802.1x authentication, the RTL8370(M) provides a

Port-based/MAC-based Guest VLAN function for them to access limited network resources. A 1-set Port Mirroring function is configured to mirror traffic (RX, TX, or both) appearing on one of the switch's ports. Support is provided on each port for multiple RFC MIB Counters, for easy debug and diagnostics.

To improve real-time or multimedia networking applications, the RTL8370(M) supports eight priority assignments for each received packet. These are based on (1) Port-based priority; (2) 802.1p/Q VLAN tag priority; (3) DSCP field in IPv4/IPv6 header; and (4) ACL-assigned priority. Each output port supports a weighted ratio of eight priority queues to fit bandwidth requirements in different applications. The input bandwidth control function helps limit per-port traffic utilization. There is one leaky bucket for average packet rate control for each queue of all ports. Queue scheduling algorithm can use Strict Priority (SP) or Weighted Fair Queue (WFQ) or mixed.

The RTL8370(M) provides a 4K-entry VLAN table for 802.1Q port-based, tag-based, and protocol-based VLAN operation to separate logical connectivity from physical connectivity. The RTL8370(M) supports four Protocol-based VLAN configurations that can optionally select EtherType, LLC, and RFC1042 as the search key. Each port may be set to any topology via EEPROM upon reset, or EEPROM SMI Slave after reset.

In router applications, the router may want to know the input port of the incoming packet. The RTL8370(M) supports an option to insert a VLAN tag with VID=Port VID (PVID) on each egress port. The RTL8370(M) also provides an option to admit VLAN tagged packet with a specific PVID only. If this function is enabled, the RTL8370(M) will drop all non-tagged packets and packets with an incorrect PVID.

2. Features

- RTL8370M: Single-chip 8+2-port gigabit non-blocking switch architecture; RTL8370: Single-chip 8-port gigabit non-blocking switch architecture
- Embedded 8-port 10/100/1000Base-T PHY
- Each port supports full duplex 10/100/1000M connectivity (half duplex only supported in 10/100M mode)
- Full-duplex and half-duplex operation with IEEE 802.3x flow control and backpressure
- Supports 9216-byte jumbo packet length forwarding at wire speed
- Supports Realtek Cable Test (RTCT) function
- RTL8370M Extra Interface (Extension GMAC0 and Extension GMAC1) supports
  - Dual-port Media Independent Interface (MII)
  - Dual-port Reduced Gigabit Media Independent Interface (RGMII)
  - Dual-port Gigabit Media Independent Interface (GMII)
- Supports 64-entry ACL Rules
  - Search keys support physical port, Layer2, Layer3, and Layer4 information
  - Actions support mirror, redirect, dropping, priority adjustment, traffic policing, CVLAN decision, and SVLAN assignment
  - Supports 5 types of user defined ACL rule format for 64 ACL rules
  - Optional per-port enable/disable of ACL function
  - Optional setting of per-port action to take when ACL mismatch
- Supports IEEE 802.1Q VLAN
  - Supports 4K VLANs and 32 Extra Enhanced VLANs
  - Supports Un-tag definition in each VLAN
  - Supports VLAN policing and VLAN forwarding decision
  - Supports Port-based, Tag-based, and Protocol-based VLAN
  - Up to 4 Protocol-based VLAN entries
  - Supports per-port and per-VLAN egress VLAN tagging and un-tagging
- Supports IVL, SVL, and IVL/SVL
  - Supports 8K-entry MAC address table with 4-way hash algorithm
  - Up to 8K L2/L3 Filtering Database
- Supports Spanning Tree port behavior configuration
  - IEEE 802.1w Rapid Spanning Tree
  - IEEE 802.1s Multiple Spanning Tree with up to 16 Spanning Tree instances
- Supports IEEE 802.1x Access Control Protocol
  - Port-Based Access Control
  - MAC-Based Access Control
  - Guest VLAN

- Supports Quality of Service (QoS)
  - Supports per port Input Bandwidth Control
  - Traffic classification based on IEEE 802.1p/Q priority definition, physical Port, IP DSCP field, ACL definition, VLAN based priority, MAC based priority, and SVLAN based priority
  - Eight Priority Queues per port
  - Per queue flow control
  - Min-Max Scheduling
  - Strict Priority and Weighted Fair Queue (WFQ) to provide minimum bandwidth
  - One leaky bucket to constrain the average packet rate of each queue
- Supports rate limiting (64 shared meters, with 8kpbs granulation)
- Supports RFC MIB Counter
  - MIB-II (RFC 1213)
  - Ethernet-Like MIB (RFC 3635)
  - Interface Group MIB (RFC 2863)
  - RMON (RFC 2819)
  - Bridge MIB (RFC 1493)
  - Bridge MIB Extension (RFC 2674)
- Supports Stacking VLAN and Port Isolation with 8 Enhanced Filtering Databases
- Supports IEEE 802.1ad Stacking VLAN
  - Supports 64 SVLANs
  - Supports 32 L2/IPv4 Multicast mappings to SVLAN
- Supports 4 IEEE 802.3ad Link aggregation port groups
- Supports OAM and EEE LLDP (Energy Efficient Ethernet Link Layer Discovery Protocol
- Supports Loop Detection
- Security Filtering
  - Disable learning for each port
  - Disable learning-table aging for each port
  - Drop unknown DA for each port
- Broadcast/Multicast/Unknown DA storm control protects system from attack by hackers
- Supports Realtek Green Ethernet features
  - Link-On Cable Length Power Saving
  - Link-Down Power Saving
- Supports 1 interrupt output to external CPU for notification (RTL8370M only)
- Each port supports 3 parallel LED or scan LED outputs
- Supports EEPROM SMI Slave interface to access configuration register
- Supports 16K-byte EEPROM space for configuration
- Integrated 8051 microprocessor
- Supports Flash Interface
- 25MHz crystal or 3.3V OSC input
- RTL8370M: TQFP 176-pin E-PAD package
  RTL8370: LQFP 128-pin E-PAD package

3. System Applications

- 8-Port 1000Base-T Switch
- 8-Port 1000Base-T Router with Dual MII/RGMII/GMII

4. Application Examples

4.1. 8-Port 1000Base-T Switch

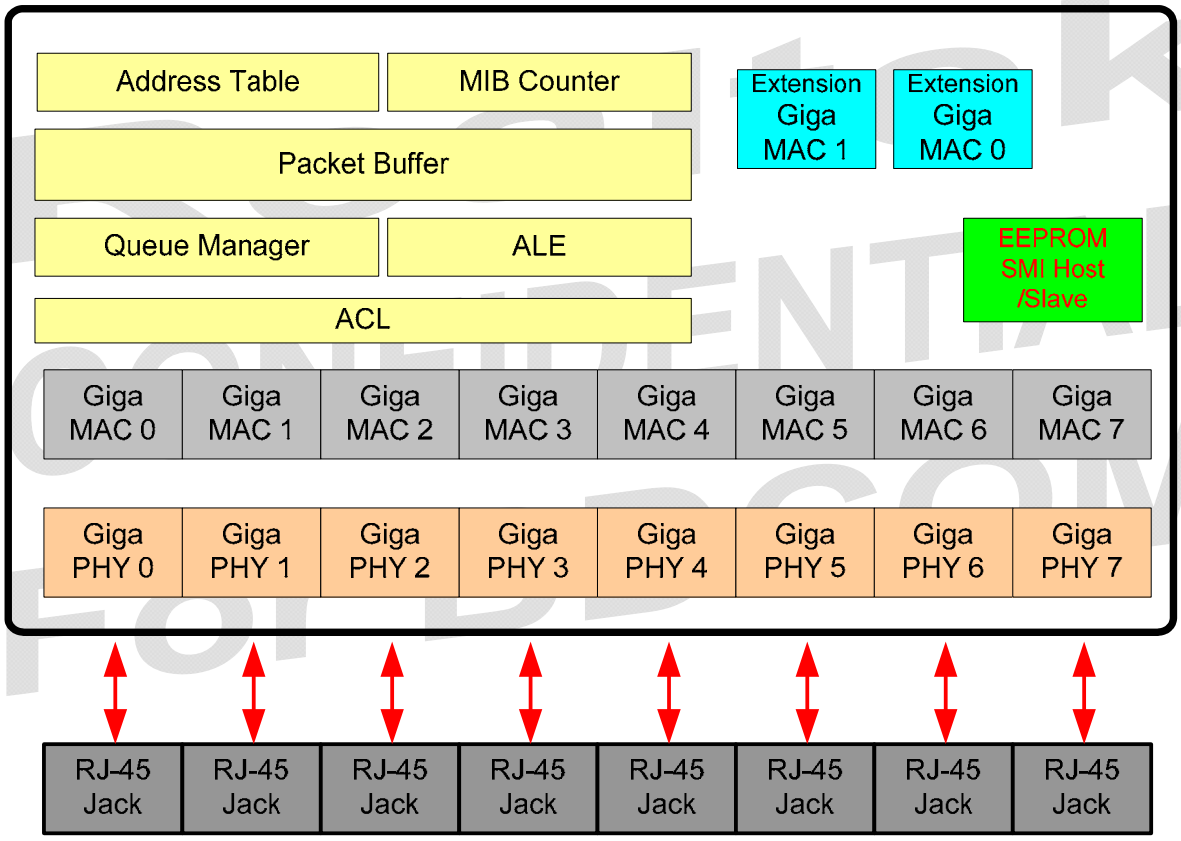


Figure 1. 8-Port 1000Base-T Switch

4.2. 8-Port 1000Base-T Router with Dual MII/RGMII/GMII (RTL8370M)

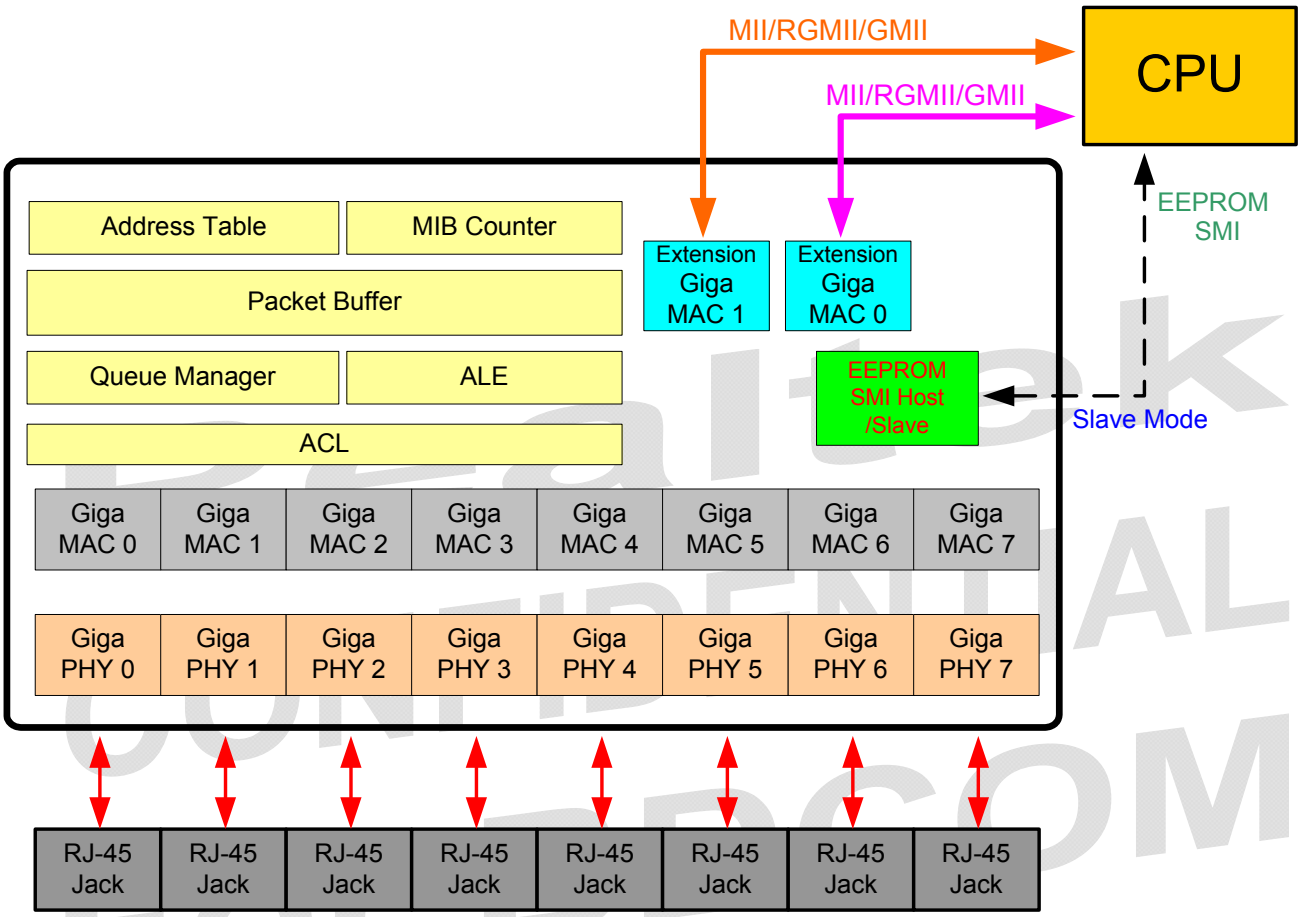


Figure 2. 8-Port 1000Base-T Router with Dual MII/RGMII/GMII

Note: Extra Interface (Extension GMAC0 and Extension GMAC1) in MII/RGMII/GMII Mode.

5. Block Diagram

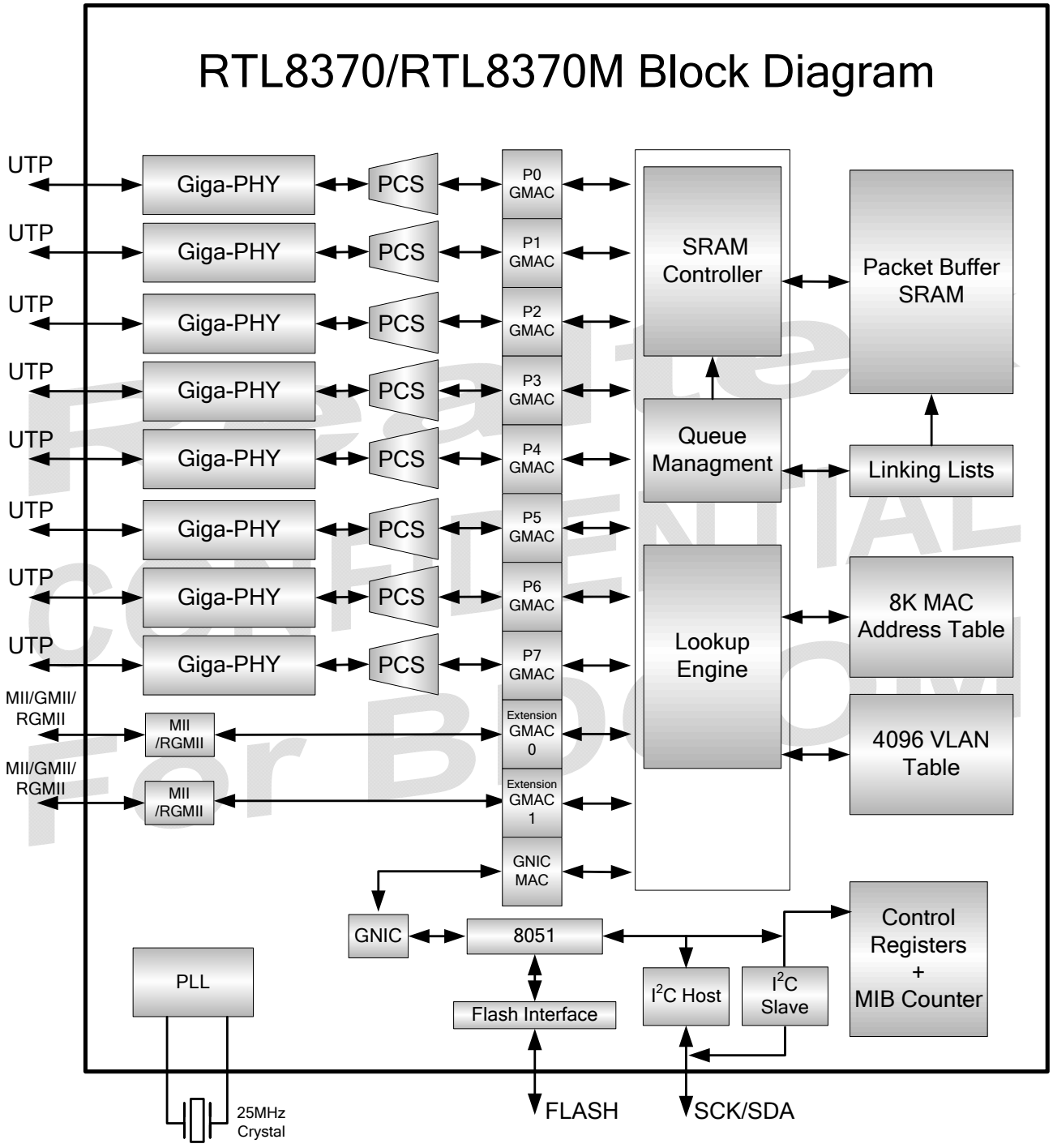


Figure 3. RTL8370(M) Block Diagram

6. Pin Assignments

6.1. RTL8370 Pin Assignments (LQFP-128)

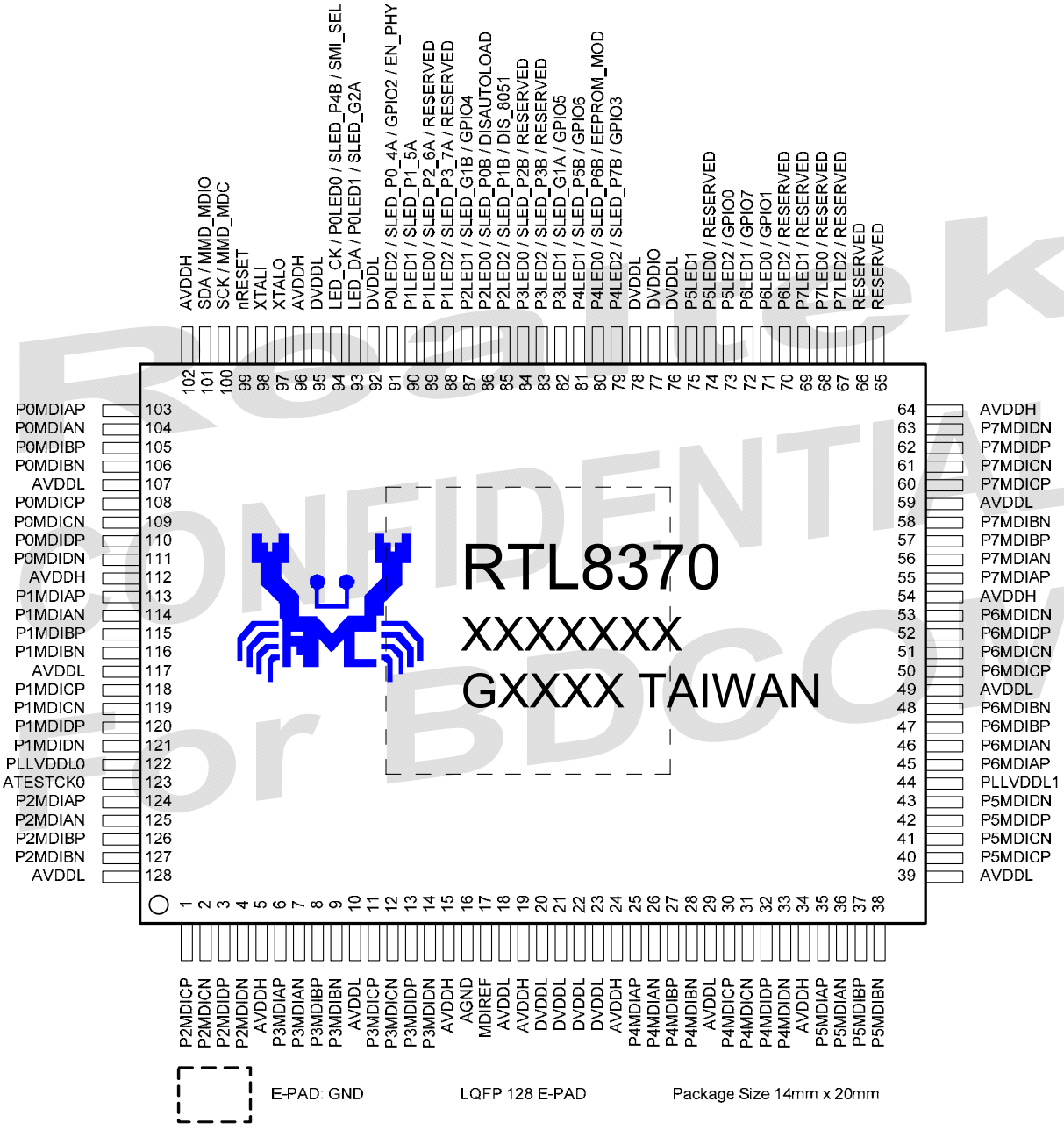


Figure 4. RTL8370 Pin Assignments (LQFP-128)

6.2. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 4).

6.3. RTL8370M Pin Assignments (TQFP-176)

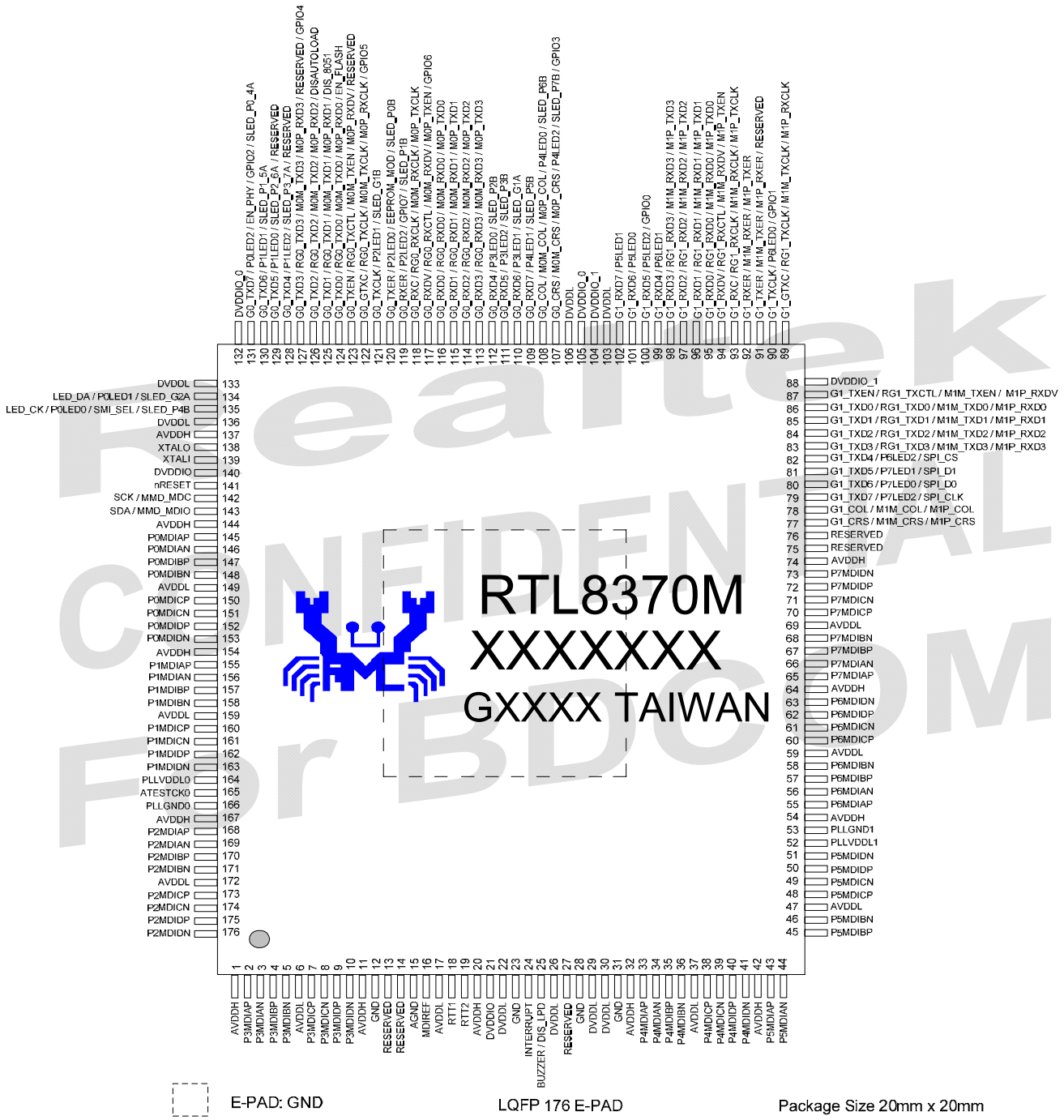


Figure 5. RTL8370M Pin Assignments (TQFP-176)

6.4. Package Identification

Green package is indicated by the 'G' in GXXXX (Figure 5).

6.5. Pin Assignment Table (RTL8370: LQFP-128)

Upon Reset: Defined as a short time after the end of a hardware reset.

After Reset: Defined as the time after the specified 'Upon Reset' time.

I: Input Pin

O: Output Pin

I/O: Bi-Direction Input/Output Pin

P: Digital Power Pin

G: Digital Ground Pin

I_{PU}: Input Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

I_S: Input Pin With Schmitt Trigger

AI: Analog Input Pin

AO: Analog Output Pin

AI/O: Analog Bi-Direction Input/Output Pin

AP: Analog Power Pin

AG: Analog Ground Pin

O_{PU}: Output Pin With Pull-Up Resistor; (Typical Value = 75K Ohm)

Table 1. Pin Assignment Table (RTL8370: LQFP-128)

Name	Pin No.	Type	Name	Pin No.	Type
P2MDICP	1	AI/O	P4MDIAP	25	AI/O
P2MDICN	2	AI/O	P4MDIAN	26	AI/O
P2MDIDP	3	AI/O	P4MDIBP	27	AI/O
P2MDIDN	4	AI/O	P4MDIBN	28	AI/O
AVDDH	5	AP	AVDDL	29	AP
P3MDIAP	6	AI/O	P4MDICP	30	AI/O
P3MDIAN	7	AI/O	P4MDICN	31	AI/O
P3MDIBP	8	AI/O	P4MDIDP	32	AI/O
P3MDIBN	9	AI/O	P4MDIDN	33	AI/O
AVDDL	10	AP	AVDDH	34	AP
P3MDICP	11	AI/O	P5MDIAP	35	AI/O
P3MDICN	12	AI/O	P5MDIAN	36	AI/O
P3MDIDP	13	AI/O	P5MDIBP	37	AI/O
P3MDIDN	14	AI/O	P5MDIBN	38	AI/O
AVDDH	15	AP	AVDDL	39	AP
AGND	16	AG	P5MDICP	40	AI/O
MDIREF	17	AO	P5MDICN	41	AI/O
AVDDL	18	AP	P5MDIDP	42	AI/O
AVDDH	19	AP	P5MDIDN	43	AI/O
DVDDL	20	P	PLLVDDL1	44	AP
DVDDL	21	P	P6MDIAP	45	AI/O
DVDDL	22	P	P6MDIAN	46	AI/O
DVDDL	23	P	P6MDIBP	47	AI/O
AVDDH	24	AP	P6MDIBN	48	AI/O

Name	Pin No.	Type
AVDDL	49	AP
P6MDICP	50	AI/O
P6MDICN	51	AI/O
P6MDIDP	52	AI/O
P6MDIDN	53	AI/O
AVDDH	54	AP
P7MDIAP	55	AI/O
P7MDIAN	56	AI/O
P7MDIBP	57	AI/O
P7MDIBN	58	AI/O
AVDDL	59	AP
P7MDICP	60	AI/O
P7MDICN	61	AI/O
P7MDIDP	62	AI/O
P7MDIDN	63	AI/O
AVDDH	64	AP
RESERVED	65	AO
RESERVED	66	AO
P7LED2/RESERVED	67	I/O_{PU}
P7LED0/RESERVED	68	I/O_{PU}
P7LED1/RESERVED	69	I/O_{PU}
P6LED2/RESERVED	70	I/O_{PU}
P6LED0/GPIO1	71	I/O_{PU}
P6LED1/GPIO7	72	I/O_{PU}
P5LED2/GPIO0	73	I/O_{PU}
P5LED0/RESERVED	74	I/O_{PU}
P5LED1	75	I/O_{PU}
DVDDL	76	P
DVDDIO	77	P
DVDDL	78	P
P4LED2/SLED_P7B/GPIO3	79	I/O_{PU}
P4LED0/SLED_P6B/ EEPROM_MOD	80	I/O_{PU}
P4LED1/SLED_P5B/GPIO6	81	I/O_{PU}
P3LED1/SLED_G1A/GPIO5	82	I/O_{PU}
P3LED2/SLED_P3B/ RESERVED	83	I/O_{PU}
P3LED0/SLED_P2B/RESERVED	84	I/O_{PU}
P2LED2/SLED_P1B/DIS_8051	85	I/O_{PU}
P2LED0/SLED_P0B/ DISAUTOLOAD	86	I/O_{PU}
P2LED1/SLED_G1B/GPIO4	87	I/O_{PU}
P1LED2/SLED_P3_7A/ RESERVED	88	I/O_{PU}

Name	Pin No.	Type
P1LED0/SLED_P2_6A/ RESERVED	89	I/O_{PU}
P1LED1/SLED_P1_5A	90	I/O_{PU}
P0LED2/SLED_P0_4A/GPIO2/ EN_PHY	91	I/O_{PU}
DVDDL	92	P
LED_DA/P0LED1/SLED_G2A	93	I/O_{PU}
LED_CK/P0LED0/SLED_P4B/ SMI_SEL	94	I/O_{PU}
DVDDL	95	P
AVDDH	96	AP
XTALO	97	AO
XTALI	98	AI
nRESET	99	I_S
SCK/MMD_MDC	100	I/O
SDA/MMD_MDIO	101	I/O
AVDDH	102	AP
P0MDIAP	103	AI/O
P0MDIAN	104	AI/O
P0MDIBP	105	AI/O
P0MDIBN	106	AI/O
AVDDL	107	AP
P0MDICP	108	AI/O
P0MDICN	109	AI/O
P0MDIDP	110	AI/O
P0MDIDN	111	AI/O
AVDDH	112	AP
P1MDIAP	113	AI/O
P1MDIAN	114	AI/O
P1MDIBP	115	AI/O
P1MDIBN	116	AI/O
AVDDL	117	AP
P1MDICP	118	AI/O
P1MDICN	119	AI/O
P1MDIDP	120	AI/O
P1MDIDN	121	AI/O
PLLVDDL0	122	AP
ATESTCK0	123	AO
P2MDIAP	124	AI/O
P2MDIAN	125	AI/O
P2MDIBP	126	AI/O
P2MDIBN	127	AI/O
AVDDL	128	AP
GND	EPAD	G

6.6. Pin Assignment Table (RTL8370M: TQFP-176)

Table 2. Pin Assignment Table (RTL8370M: TQFP-176)

Name	Pin No.	Type
AVDDH	1	AP
P3MDIAP	2	AI/O
P3MDIAN	3	AI/O
P3MDIBP	4	AI/O
P3MDIBN	5	AI/O
AVDDL	6	AP
P3MDICP	7	AI/O
P3MDICN	8	AI/O
P3MDIDP	9	AI/O
P3MDIDN	10	AI/O
AVDDH	11	AP
GND	12	G
RESERVED	13	AI
RESERVED	14	AO
AGND	15	AG
MDIREF	16	AO
AVDDL	17	AP
RTT1	18	AO
RTT2	19	AO
AVDDH	20	AP
DVDDIO	21	P
DVDDL	22	P
GND	23	G
INTERRUPT	24	O_{PU}
BUZZER/DIS_LPD	25	I/O_{PU}
DVDDL	26	P
RESERVED	27	I_{PU}
GND	28	G
DVDDL	29	P
DVDDL	30	P
GND	31	G
AVDDH	32	AP
P4MDIAP	33	AI/O
P4MDIAN	34	AI/O
P4MDIBP	35	AI/O
P4MDIBN	36	AI/O
AVDDL	37	AP
P4MDICP	38	AI/O
P4MDICN	39	AI/O
P4MDIDP	40	AI/O
P4MDIDN	41	AI/O

Name	Pin No.	Type
AVDDH	42	AP
P5MDIAP	43	AI/O
P5MDIAN	44	AI/O
P5MDIBP	45	AI/O
P5MDIBN	46	AI/O
AVDDL	47	AP
P5MDICP	48	AI/O
P5MDICN	49	AI/O
P5MDIDP	50	AI/O
P5MDIDN	51	AI/O
PLLVDDL1	52	AP
PLLGND1	53	AG
AVDDH	54	AP
P6MDIAP	55	AI/O
P6MDIAN	56	AI/O
P6MDIBP	57	AI/O
P6MDIBN	58	AI/O
AVDDL	59	AP
P6MDICP	60	AI/O
P6MDICN	61	AI/O
P6MDIDP	62	AI/O
P6MDIDN	63	AI/O
AVDDH	64	AP
P7MDIAP	65	AI/O
P7MDIAN	66	AI/O
P7MDIBP	67	AI/O
P7MDIBN	68	AI/O
AVDDL	69	AP
P7MDICP	70	AI/O
P7MDICN	71	AI/O
P7MDIDP	72	AI/O
P7MDIDN	73	AI/O
AVDDH	74	AP
RESERVED	75	AO
RESERVED	76	AO
G1_CRS/M1M_CRS/M1P_CRS	77	I/O
G1_COL/M1M_COL/M1P_COL	78	I/O
G1_TXD7/P7LED2/SPI_CLK	79	I/O_{PU}
G1_TXD6/P7LED0/SPI_D0	80	I/O_{PU}
G1_TXD5/P7LED1/SPI_D1	81	I/O_{PU}
G1_TXD4/P6LED2/SPI_CS	82	I/O_{PU}

Name	Pin No.	Type
G1_TXD3/RG1_TXD3/ M1M_TXD3/M1P_RXD3	83	O
G1_TXD2/RG1_TXD2/ M1M_TXD2/M1P_RXD2	84	O
G1_TXD1/RG1_TXD1/ M1M_TXD1/M1P_RXD1	85	O
G1_TXD0/RG1_TXD0/ M1M_TXD0/M1P_RXD0	86	O
G1_TXEN/RG1_TXCTL/ M1M_TXEN/M1P_RXDV	87	O
DVDDIO_1	88	P
G1_GTXC/RG1_TXCLK/ M1M_TXCLK/M1P_RXCLK	89	I/O
G1_TXCLK/P6LED0/GPIO1	90	I/O_{PU}
G1_TXER/M1M_TXER/ M1P_RXER/RESERVED	91	I/O_{PU}
G1_RXER/M1M_RXER/ M1P_TXER	92	I
G1_RXC/RG1_RXCLK/ M1M_RXCLK/M1P_TXCLK	93	I/O
G1_RXDV/RG1_RXCTL/ M1M_RXDV/M1P_TXEN	94	I
G1_RXD0/RG1_RXD0/ M1M_RXD0/M1P_TXD0	95	I
G1_RXD1/RG1_RXD1/ M1M_RXD1/M1P_TXD1	96	I
G1_RXD2/RG1_RXD2/ M1M_RXD2/M1P_TXD2	97	I
G1_RXD3/RG1_RXD3/ M1M_RXD3/M1P_TXD3	98	I
G1_RXD4/P6LED1	99	I/O_{PU}
G1_RXD5/P5LED2/GPIO0	100	I/O_{PU}
G1_RXD6/P5LED0	101	I/O_{PU}
G1_RXD7/P5LED1	102	I/O_{PU}
DVDDL	103	P
DVDDIO_1	104	P
DVDDIO_0	105	P
DVDDL	106	P
G0_CRS/M0M_CRS/M0P_CRS/ P4LED2/SLED_P7B/GPIO3	107	I/O_{PU}
G0_COL/M0M_COL/M0P_COL/ P4LED0/SLED_P6B	108	I/O_{PU}
G0_RXD7/P4LED1/SLED_P5B	109	I/O_{PU}
G0_RXD6/P3LED1/SLED_G1A	110	I/O_{PU}
G0_RXD5/P3LED2/SLED_P3B	111	I/O_{PU}
G0_RXD4/P3LED0/SLED_P2B	112	I/O_{PU}

Name	Pin No.	Type
G0_RXD3/RG0_RXD3/ M0M_RXD3/M0P_TXD3	113	I
G0_RXD2/RG0_RXD2/ M0M_RXD2/M0P_TXD2	114	I
G0_RXD1/RG0_RXD1/ M0M_RXD1/M0P_TXD1	115	I
G0_RXD0/RG0_RXD0/ M0M_RXD0/M0P_TXD0	116	I
G0_RXDV/RG0_RXCTL/ M0M_RXDV/M0P_TXEN/GPIO6	117	I/O
G0_RXC/RG0_RXCLK/ M0M_RXCLK/M0P_TXCLK	118	I/O
G0_RXER/P2LED2/GPIO7/ SLED_P1B	119	I/O_{PU}
G0_TXER/P2LED0/EEPROM_MOD /SLED_P0B	120	I/O_{PU}
G0_TXCLK/P2LED1/SLED_G1B	121	I/O_{PU}
G0_GTXC/RG0_TXCLK/ M0M_TXCLK/M0P_RXCLK/GPIO5	122	I/O
G0_TXEN/RG0_TXCTL/ M0M_TXEN/M0P_RXDV/ RESERVED	123	I/O
G0_TXD0/RG0_TXD0/M0M_TXD0 /M0P_RXD0/EN_FLASH	124	I/O_{PU}
G0_TXD1/RG0_TXD1/ M0M_TXD1/M0P_RXD1/DIS_8051	125	I/O_{PU}
G0_TXD2/RG0_TXD2/M0M_TXD2 /M0P_RXD2/DISAUTOLOAD	126	I/O_{PU}
G0_TXD3/RG0_TXD3/ M0M_TXD3/M0P_RXD3/ RESERVED/GPIO4	127	I/O_{PU}
G0_TXD4/P1LED2/SLED_P3_7A/ RESERVED	128	I/O_{PU}
G0_TXD5/P1LED0/SLED_P2_6A/ RESERVED	129	I/O_{PU}
G0_TXD6/P1LED1/SLED_P1_5A	130	I/O_{PU}
G0_TXD7/P0LED2/EN_PHY/GPIO2 /SLED_P0_4A	131	I/O_{PU}
DVDDIO_0	132	P
DVDDL	133	P
LED_DA/P0LED1/SLED_G2A	134	I/O_{PU}
LED_CK/P0LED0/SLED_P4B/ SMI_SEL	135	I/O_{PU}
DVDDL	136	P
AVDDH	137	AP
XTALO	138	AO

Name	Pin No.	Type
XTALI	139	AI
DVDDIO	140	P
nRESET	141	I_S
SCK/MMD_MDC	142	I/O
SDA/MMD_MDIO	143	I/O
AVDDH	144	AP
P0MDIAP	145	AI/O
P0MDIAN	146	AI/O
P0MDIBP	147	AI/O
P0MDIBN	148	AI/O
AVDDL	149	AP
P0MDICP	150	AI/O
P0MDICN	151	AI/O
P0MDIDP	152	AI/O
P0MDIDN	153	AI/O
AVDDH	154	AP
P1MDIAP	155	AI/O
P1MDIAN	156	AI/O
P1MDIBP	157	AI/O
P1MDIBN	158	AI/O

Name	Pin No.	Type
AVDDL	159	AP
P1MDICP	160	AI/O
P1MDICN	161	AI/O
P1MDIDP	162	AI/O
P1MDIDN	163	AI/O
PLLVDDL0	164	AP
ATESTCK0	165	AO
PLLGND0	166	AG
AVDDH	167	AP
P2MDIAP	168	AI/O
P2MDIAN	169	AI/O
P2MDIBP	170	AI/O
P2MDIBN	171	AI/O
AVDDL	172	AP
P2MDICP	173	AI/O
P2MDICN	174	AI/O
P2MDIDP	175	AI/O
P2MDIDN	176	AI/O
GND	EPAD	G

7. Pin Descriptions (RTL8370)

7.1. Media Dependent Interface Pins (RTL8370)

Table 3. Media Dependent Interface Pins (RTL8370) (LQFP128)

Pin Name	Pin No. RTL8370	Type	Drive (mA)	Description
P0MDIAP/N P0MDIBP/N P0MDICP/N P0MDIDP/N	103 104 105 106 108 109 110 111	AI/O	10	Port 0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	113 114 115 116 118 119 120 121	AI/O	10	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P2MDIAP/N P2MDIBP/N P2MDICP/N P2MDIDP/N	124 125 126 127 1 2 3 4	AI/O	10	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	6 7 8 9 11 12 13 14	AI/O	10	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P4MDIAP/N P4MDIBP/N P4MDICP/N P4MDIDP/N	25 26 27 28 30 31 32 33	AI/O	10	Port 4 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

Pin Name	Pin No. RTL8370	Type	Drive (mA)	Description
P5MDIAP/N P5MDIBP/N P5MDICP/N P5MDIDP/N	35 36 37 38 40 41 42 43	AI/O	10	Port 5 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P6MDIAP/N P6MDIBP/N P6MDICP/N P6MDIDP/N	45 46 47 48 50 51 52 53	AI/O	10	Port 6 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P7MDIAP/N P7MDIBP/N P7MDICP/N P7MDIDP/N	55 56 57 58 60 61 62 63	AI/O	10	Port 7 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

7.2. Parallel LED Pins (RTL8370)

Table 4. Parallel LED Pins (RTL8370) (LQFP128)

Pin Name	Pin No. RTL8370	Type	Drive (mA)	Description
P7LED2/ RESERVED	67	I/O_{PU}	-	Port 7 LED2 Output Signal. P7LED2 indicates information is defined by register or EEPROM.
P7LED1/ RESERVED	69	I/O_{PU}	-	Port 7 LED1 Output Signal. P7LED1 indicates information is defined by register or EEPROM.
P7LED0/ RESERVED	68	I/O_{PU}	-	Port 7 LED0 Output Signal. P7LED0 indicates information is defined by register or EEPROM.
P6LED2/ RESERVED	70	I/O_{PU}	-	Port 6 LED2 Output Signal. P6LED2 indicates information is defined by register or EEPROM.
P6LED1/GPIO7	72	I/O_{PU}	-	Port 6 LED1 Output Signal. P6LED1 indicates information is defined by register or EEPROM.
P6LED0/GPIO1	71	I/O_{PU}	-	Port 6 LED0 Output Signal. P6LED0 indicates information is defined by register or EEPROM.
P5LED2/GPIO0	73	I/O_{PU}	-	Port 5 LED2 Output Signal. P5LED2 indicates information is defined by register or EEPROM.

Pin Name	Pin No. RTL8370	Type	Drive (mA)	Description
P5LED1	75	I/O_{PU}	-	Port 5 LED1 Output Signal. P5LED1 indicates information is defined by register or EEPROM.
P5LED0/ RESERVED	74	I/O_{PU}	-	Port 5 LED0 Output Signal. P5LED0 indicates information is defined by register or EEPROM.
P4LED2	79	I/O_{PU}	-	Port 4 LED2 Output Signal. P4LED2 indicates information is defined by register or EEPROM.
P4LED1	81	I/O_{PU}	-	Port 4 LED1 Output Signal. P4LED1 indicates information is defined by register or EEPROM.
P4LED0/ EEPROM_MOD	80	I/O_{PU}	-	Port 4 LED0 Output Signal. P4LED0 indicates information is defined by register or EEPROM.
P3LED2/ RESERVED	83	I/O_{PU}	-	Port 3 LED2 Output Signal. P3LED2 indicates information is defined by register or EEPROM.
P3LED1	82	I/O_{PU}	-	Port 3 LED1 Output Signal. P3LED1 indicates information is defined by register or EEPROM.
P3LED0/ RESERVED	84	I/O_{PU}	-	Port 3 LED0 Output Signal. P3LED0 indicates information is defined by register or EEPROM.
P2LED2/ DIS_8051	85	I/O_{PU}	-	Port 2 LED2 Output Signal. P2LED2 indicates information is defined by register or EEPROM.
P2LED1	87	I/O_{PU}	-	Port 2 LED1 Output Signal. P2LED1 indicates information is defined by register or EEPROM.
P2LED0/ DISAUTOLOAD	86	I/O_{PU}	-	Port 2 LED0 Output Signal. P2LED0 indicates information is defined by register or EEPROM.
P1LED2/ RESERVED	88	I/O_{PU}	-	Port 1 LED2 Output Signal. P1LED2 indicates information is defined by register or EEPROM.
P1LED1	90	I/O_{PU}	-	Port 1 LED1 Output Signal. P1LED1 indicates information is defined by register or EEPROM.
P1LED0/ RESERVED	89	I/O_{PU}	-	Port 1 LED0 Output Signal. P1LED0 indicates information is defined by register or EEPROM.
P0LED2/ EN_PHY	91	I/O_{PU}	-	Port 0 LED2 Output Signal. P0LED2 indicates information is defined by register or EEPROM.
P0LED1/ LED_DA	93	I/O_{PU}	-	Port 0 LED1 Output Signal. P0LED1 indicates information is defined by register or EEPROM.
P0LED0/ LED_CK/ SMI_SEL	94	I/O_{PU}	-	Port 0 LED0 Output Signal. P0LED0 indicates information is the same as P7LED0 and is defined by register or EEPROM.

Note: See section 10.19 LED Indicator, page 57 for details.

7.3. Scan Mode LED Pins (RTL8370) (LQFP128)

Table 5. Scan Mode LED Pins (RTL8370) (LQFP128)

Pin Name	Pin No. RTL8370	Type	Drive (mA)	Description
SLED_G1A/P3LED1 /GPIO5	82	I/O_{PU}	-	Scan Mode LED Group A G1A Output Signal.
SLED_G2A/LED_DA /P0LED1	93	I/O_{PU}	-	Scan Mode LED Group A G2A Output Signal.
SLED_P0_4A/GPIO2 /EN_PHY/P0LED2	91	I/O_{PU}	-	Scan Mode LED Group A P0_4A Output Signal.
SLED_P1_5A /P1LED1	90	I/O_{PU}	-	Scan Mode Group A LED P1_5A Output Signal.
SLED_P2_6A/ P1LED0/RESERVED	89	I/O_{PU}	-	Scan Mode LED Group A P2_6A Output Signal.
SLED_P3_7A /P1LED2/RESERVED	88	I/O_{PU}	-	Scan Mode LED Group A P3_7A Output Signal.
SLED_G1B/P2LED1 /GPIO4	87	I/OPU	-	Scan Mode LED Group B G1B Output Signal.
SLED_P0B/P2LED0 /DISAUTOLOAD	86	I/O_{PU}	-	Scan Mode LED Group B P0B Output Signal.
SLED_P1B/P2LED2 /DIS_8051	85	I/O_{PU}	-	Scan Mode LED Group B P1B Output Signal.
SLED_P2B/P3LED0 /RESERVED	84	I/O_{PU}	-	Scan Mode LED Group B P2B Output Signal.
SLED_P3B/P3LED2 /RESERVED	83	I/O_{PU}	-	Scan Mode LED Group B P3B Output Signal.
SLED_P4B/LED_CK /P0LED0/SMI_SEL	94	I/O_{PU}	-	Scan Mode LED Group B P4B Output Signal.
SLED_P5B/P4LED1 /GPIO6	81	I/O_{PU}	-	Scan Mode LED Group B P5B Output Signal.
SLED_P6B/P4LED0 /EEPROM_MOD	80	I/O_{PU}	-	Scan Mode LED Group B P6B Output Signal.
SLED_P7B/P4LED2 /GPIO3	79	I/O_{PU}	-	Scan Mode LED Group B P7B Output Signal.

Note: See section 10.19.2 Scan LED Mode, page 58 for details.

7.4. Configuration Strapping Pins (RTL8370)

Table 6. Configuration Strapping Pins (RTL8370) (LQFP128)

Pin Name	Pin No. RTL8370	Type	Description
RESERVED/P5LED0	74	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*
EEPROM_MOD/P4LED0	80	I/O_{PU}	EEPROM Mode Selection. Pull Up: EEPROM 24Cxx Size greater than 16Kbits (24C32~) Pull Down: EEPROM 24Cxx Size less than or equal to 16Kbit (24C02~24C16). *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 10.19 LED Indicator, page 57 for more details.*
RESERVED/P3LED2	83	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*
RESERVED/P3LED0	84	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset.* *When pulled low, the LED output polarity will be high active. See section 10.19 LED Indicator, page 57 for more details.*
DIS_8051/P2LED2	85	I/O_{PU}	Disable Embedded 8051. Pull Up: Disable embedded 8051 upon power on or reset Pull Down: Enable embedded 8051 upon power on or reset *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 10.19 LED Indicator, page 57 for more details.*

Pin Name	Pin No. RTL8370	Type	Description
DISAUTOLOAD/P2LED0	86	I/O_{PU}	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload upon power on or reset Pull Down: Enable EEPROM autoload upon power on or reset *Note1: When DIS_8051=1 and DISAUTOLOAD=0, the EEPROM data will be treat as register configuration data upon power on or reset initial stage. When DIS_8051 = 0 and DISAUTOLOAD =0, the EEPROM data will be loaded to embedded 8051 instruction memory upon power on or reset.* *Note2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 10.19 LED Indicator, page 57 for more details.*
RESERVED/P1LED2	88	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*
RESERVED/P1LED0	89	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*
EN_PHY/P0LED2	91	I/O_{PU}	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*
SMI_SEL/P0LED0/ LED_CK	94	I/O_{PU}	EEPROM SMI/MII Management Interface Selection. Pull Up: EEPROM SMI interface Pull Down: MII Management Interface *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*

7.5. Miscellaneous Pins (RTL8370)

Table 7. Miscellaneous Pins (RTL8370) (LQFP128)

Pin Name	Pin No. RTL8370	Type	Description
XTALI	98	AI	25MHz Crystal Clock Input and Feedback Pin. 25MHz +/-50ppm tolerance crystal reference or oscillator input.
XTALO	97	AO	25MHz Crystal Clock Output Pin. 25MHz +/-50ppm tolerance crystal output.
MDIREF	17	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
RESERVED	65	AO	Reserved. Must be left floating in normal operation.
RESERVED	66	AO	Reserved. Must be left floating in normal operation.
SCK/MMD_MDC	100	I/O	EEPROM SMI Interface Clock/MII Management Interface Clock (selected via the hardware strapping pin 94, SMI_SEL).
SDA/MMD_MDIO	101	I/O	EEPROM SMI Interface Data/MII Management Interface Data (selected via the hardware strapping pin 94, SMI_SEL).
nRESET	99	I_S	System Reset Input Pin. When low active will reset the RTL8370.
P5LED2/GPIO0	73	I/O_{PU}	General Purpose Input/Output Interfaces IO0.
P6LED0/GPIO1	71	I/O_{PU}	General Purpose Input/Output Interfaces IO1.
P0LED2/SLED_P0_4A/ GPIO2/EN_PHY	91	I/O_{PU}	General Purpose Input/Output Interfaces IO2.
P4LED2/SLED_P7B/ GPIO3	79	I/O_{PU}	General Purpose Input/Output Interfaces IO3.
P2LED1/SLED_G1B/ GPIO4	87	I/O_{PU}	General Purpose Input/Output Interfaces IO4.
P3LED1/SLED_G1A/ GPIO5	82	I/O_{PU}	General Purpose Input/Output Interfaces IO5.
P4LED1/SLED_P5B/ GPIO6	81	I/O_{PU}	General Purpose Input/Output Interfaces IO6.
P6LED1/GPIO7	72	I/O_{PU}	General Purpose Input/Output Interfaces IO7.

7.6. Test Pins (RTL8370)

Table 8. Test Pins (RTL8370) (LQFP128)

Pin Name	Pin No. RTL8370	Type	Description
ATESTCK0	123	AO	Reserved for Internal Use. Must be left floating.

7.7. Power and GND Pins (RTL8370)

Table 9. Power and GND Pins (RTL8370) (LQFP128)

Pin Name	Pin No. RTL8370	Type	Description
DVDDIO	77	P	Digital I/O High Voltage Power for INTERRUPT, SMI, nRESET
DVDDL	20, 21, 22, 23, 76, 78, 92, 95	P	Digital Low Voltage Power.
AVDDH	5, 15, 19, 24, 34, 54, 64, 96, 102, 112	AP	Analog High Voltage Power.
AVDDL	10, 18, 29, 39, 49, 59, 107, 117, 128	AP	Analog Low Voltage Power.
PLLVDDL0	122	AP	PLL0 Low Voltage Power.
PLLVDDL1	44	AP	PLL1 Low Voltage Power.
GND	EPAD	G	GND.
AGND	15	AG	Analog GND.

8. Pin Descriptions (RTL8370M)

8.1. Media Dependent Interface Pins (RTL8370M)

Table 10. Media Dependent Interface Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
P0MDIAP/N P0MDIBP/N P0MDICP/N P0MDIDP/N	145 146 147 148 150 151 152 153	AI/O	10	Port 0 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P1MDIAP/N P1MDIBP/N P1MDICP/N P1MDIDP/N	155 156 157 158 160 161 162 163	AI/O	10	Port 1 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P2MDIAP/N P2MDIBP/N P2MDICP/N P2MDIDP/N	168 169 170 171 173 174 175 176	AI/O	10	Port 2 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P3MDIAP/N P3MDIBP/N P3MDICP/N P3MDIDP/N	2 3 4 5 7 8 9 10	AI/O	10	Port 3 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P4MDIAP/N P4MDIBP/N P4MDICP/N P4MDIDP/N	33 34 35 36 38 39 40 41	AI/O	10	Port 4 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
P5MDIAP/N P5MDIBP/N P5MDICP/N P5MDIDP/N	43 44 45 46 48 49 50 51	AI/O	10	Port 5 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P6MDIAP/N P6MDIBP/N P6MDICP/N P6MDIDP/N	55 56 57 58 60 61 62 63	AI/O	10	Port 6 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.
P7MDIAP/N P7MDIBP/N P7MDICP/N P7MDIDP/N	65 66 67 68 70 71 72 73	AI/O	10	Port 7 Media Dependent Interface A~D. For 1000Base-T operation, differential data from the media is transmitted and received on all four pairs. For 100Base-Tx and 10Base-T operation, only MDIAP/N and MDIBP/N are used. Auto MDIX can reverse the pairs MDIAP/N and MDIBP/N. Each of the differential pairs has an internal 100-ohm termination resistor.

8.2. General Purpose Interfaces (RTL8370M)

The RTL8370M supports multi-function General Purpose Interfaces that can be configured as extra interfaces of Extension GMAC0 and Extension GMAC1, LED interfaces, or other Digital I/O interfaces. The RTL8370M supports two extension interfaces (Extension GMAC0 and Extension GMAC1) for connecting with an external PHY, MAC, or CPU in specific applications. These two extension interfaces support GMII, RGMII, MII MAC mode, or MII PHY mode via register configuration. The extension interface 0 data path connects to extension GMAC0, and the extension interface 1 data path connects to extension GMAC1. The General Purpose Interface also could be configured to parallel mode LED or scan mode LED interface when the GMII interface is disabled.

8.2.1. GMII Interface Pins (RTL8370M)

The Extension GMAC0 and Extension GMAC1 of the RTL8370M support two GMII interfaces when register configuration is set to GMII mode interface. When the extension interface operates at 1Gbps, the interface will be GMII. When the extension interfaces operate at 100Mbps/10Mbps, the interface will be MII. Note that 1Gbps Half Duplex is not supported in this configuration.

Table 11. Extension GMAC0 GMII Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
G0_CRS	107	I_{PU}	-	G0_CRS Carrier Sense Input when the Extension GMAC0 GMII interface operates in 10/100 MII half duplex mode. G0_CRS is only valid in 10/100Mbps MII half duplex mode. It is asserted high when a valid carrier is detected on the media. This pin must be pulled low with a 1K ohm resistor when not used.
G0_COL	108	I_{PU}	-	G0_COL Collision Detect Input when the Extension GMAC0 GMII interface operates in 10/100 MII half duplex mode. G0_COL is only valid in 10/100Mbps MII half duplex mode. It is asserted high when a collision is detected on the media. This pin must be pulled low with a 1K ohm resistor when not used.
G0_RXD7 G0_RXD6 G0_RXD5 G0_RXD4 G0_RXD3 G0_RXD2 G0_RXD1 G0_RXD0	109 110 111 112 113 114 115 116	I_{PU} I_{PU} I_{PU} I_{PU} I I I I	-	G0_RXD[7:0] Extension GMAC0 GMII Receive Data Input. Received data is received synchronously at the rising edge of G0_RXC. In 10/100Mbps MII mode, only G0_RXD[3:0] are available. These pins must be pulled low with a 1K ohm resistor when not used.
G0_RXDV	117	I	-	G0_RXDV Extension GMAC0 GMII Receive Data Valid Input. Receive Data Valid is received synchronously at the rising edge of G0_RXC in both 1Gbps GMII and 10/100Mbps MII MAC mode. This pin must be pulled low with a 1K ohm resistor when not used.
G0_RXC	118	I	-	G0_RXC Extension GMAC0 GMII Receive Clock Input. In GMII mode: 125MHz receive clock. Used to synchronize G0_RXD[7:0], G0_RXER , and G0_RXDV. In MII 10/100Mbps mode: G0_RXC is 2.5/25MHz. Used to synchronize G0_RXD[3:0], G0_RXER, G0_RXDV, G0_CRS, and G0_COL. This pin must be pulled low with a 1K ohm resistor when not used.
G0_RXER	119	I_{PU}	-	G0_RXER Extension GMAC0 GMII Receive Data Error. Indicates that the received data contains errors. The switch filters the received packets once G0_RXER is asserted at the rising edge of G0_RXC. Valid both in 1000Mbps GMII mode and 10/100Mbps MII MAC mode. This pin must be pulled low with a 1K ohm resistor when not used.
G0_TXER	120	I/O_{PU}	-	G0_TXER Extension GMAC0 GMII Transmit Data Error Output. Indicates that the transmitted data contains errors.
G0_TXCLK	121	I/O_{PU}	-	G0_TXCLK 2.5/25MHz Transmit Clock Input when the Extension GMAC0 GMII interface operates in 10/100 MII mode. 2.5/25MHz clock driven by PHY when operating in 10/100Mbps MII mode. Used to synchronize G0_TX[3:0], G0_TXEN, and G0_TXER. This pin must be pulled low with a 1K ohm resistor when not used.
G0_GTXC	122	O	-	G0_GTXC Extension GMAC0 GMII Transmit Clock Output. 125MHz transmit clock output when GMII is operating at 1Gbps. Used to synchronize G0_TXD[7:0], G0_TXEN, and G0_TXER.

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
G0_TXEN/ RESERVED	123	O	-	G0_TXEN Extension GMAC0 GMII Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of G0_GTXC in GMII mode. Transmit enable that is sent synchronously at the rising edge of G0_TXCLK in 10/100Mbps MII mode. This pin must be pulled high with a 4.7K ohm resistor when in normal operation.
G0_TXD0/ EN_FLASH	124	I/O_{PU}	-	G0_TXD [7:0] Extension GMAC0 GMII Transmit Data Output. In 1000Mbps GMII mode, G0_TXD [7:0] transmitted data is sent synchronously at the rising edge of G0_GTXC. In 10/100Mbps MII mode, only G0_TXCLK [3:0] are available for transmitting and receiving data at the rising edge of G0_TXCLK. **G0_TXD0/EN_FLASH:** Pull Up: Enable FLASH interface Pull Down: Disable FLASH interface
G0_TXD1/ DIS_8051	125	I/O_{PU}		**G0_TXD1/DIS_8051:** Pulled High: Disable embedded 8051 upon power on or reset. Pulled Low: Enable embedded 8051 upon power on or reset.
G0_TXD2/ DISAUTOLOAD	126	I/O_{PU}		**G0_TXD2/DISAUTOLOAD:** Pulled High: Disable auto load EEPROM upon power on or reset. Pulled Low: Enable auto load EEPROM when power on/reset.
G0_TXD3/ RESERVED	127	I/O_{PU}		**G0_TXD3/RESERVED:** This pin must be pulled high with a 4.7K ohm resistor when in normal operation.
G0_TXD4/ RESERVED	128	I/O_{PU}		**G0_TXD4/RESERVED:** These pins must be pulled high with a 4.7K ohm resistor when in normal operation.
G0_TXD5/ RESERVED	129	I/O_{PU}		**G0_TXD5/RESERVED:** These pins must be pulled high with a 4.7K ohm resistor when in normal operation.
G0_TXD6 RESERVED	130	I/O_{PU}		**G0_TXD6/RESERVED:** Reserved.
G0_TXD7/ EN_PHY	131	I/O_{PU}		**G0_TXD7/EN_PHY:** Pulled High: Enables embedded PHY upon power on or reset. Pulled Low: Disables embedded PHY upon power on or reset.

Table 12. Extension GMAC1 GMII Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
G1_CRS	77	I	-	G1_CRS Carrier Sense Input when the Extension GMAC1 GMII interface operates in 10/100 MII half duplex mode. G1_CRS is only valid in 10/100Mbps MII half duplex mode. It is asserted high when a valid carrier is detected on the media. This pin must be pulled low with a 1K ohm resistor when not used.
G1_COL	78	I	-	G1_COL Collision Detect Input when the Extension GMAC1 GMII interface operates in 10/100 MII half duplex mode. G1_COL is only valid in 10/100Mbps MII half duplex mode. It is asserted high when a collision is detected on the media. This pin must be pulled low with a 1K ohm resistor when not used.
G1_TXD7 G1_TXD6 G1_TXD5 G1_TXD4 G1_TXD3 G1_TXD2 G1_TXD1 G1_TXD0	79 80 81 82 83 84 85 86	I/O_{PU} I/O_{PU} I/O_{PU} I/O_{PU} O O O O	-	G1_TXD [7:0] Extension GMAC1 GMII Transmit Data Output. In 1000Mbps GMII mode, G1_TXD [7:0] transmitted data is sent synchronously at the rising edge of G1_GTXC. In 10/100Mbps MII mode, only G1_TXCLK [3:0] are available for transmitting and receiving data at the rising edge of G1_TXCLK.
G1_TXEN	87	O	-	G1_TXEN Extension GMAC1 GMII Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of G1_GTXC in GMII mode. Transmit enable that is sent synchronously at the rising edge of G1_TXCLK in 10/100Mbps MII mode.
G1_GTXC	89	O	-	G1_GTXC Extension GMAC1 GMII Transmit Clock Output. 125MHz transmit clock output when GMII is operating at 1Gbps. Used to synchronize G1_TXD[7:0], G1_TXEN, and G1_TXER.
G1_TXCLK	90	I_{PU}	-	G1_TXCLK 2.5/25MHz Transmit Clock Input when the Extension GMAC1 GMII interface operates in 10/100 MII mode. 2.5/25MHz clock driven by PHY when operating in 10/100Mbps MII mode. Used to synchronize G1_TX[3:0], G1_TXEN, and G1_TXER. This pin must be pulled low with a 1K ohm resistor when not used.
G1_TXER/ RESERVED	91	I/O_{PU}	-	G1_TXER Extension GMAC1 GMII Transmit Data Error Output. Indicates that the transmitted data contains errors.
G1_RXER	92	I	-	G1_RXER Extension GMAC1 GMII Receive Data Error. Indicates that the received data contains errors. The switch filters the received packets once G1_RXER is asserted at the rising edge of G1_RXC. Valid both in 1000Mbps GMII mode and 10/100Mbps MII MAC mode. This pin must be pulled low with a 1K ohm resistor when not used.
G1_RXC	93	I	-	G1_RXC Extension GMAC1 GMII Receive Clock Input. In GMII mode: 125MHz receive clock. Used to synchronize G1_RXD[7:0], G1_RXER, and G1_RXDV. In MII 10/100Mbps mode: G1_RXC is 2.5/25MHz. Used to synchronize G1_RXD[3:0], G1_RXER, G1_RXDV, G1_CRS, and G1_COL. This pin must be pulled low with a 1K ohm resistor when not used.

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
G1_RXDV	94	I	-	G1_RXDV Extension GMAC1 GMII Receive Data Valid Input. Receive Data Valid is received synchronously at the rising edge of G1_RXC in both 1Gbps GMII and 10/100Mbps MII MAC mode. This pin must be pulled low with a 1K ohm resistor when not used.
G1_RXD0 G1_RXD1 G1_RXD2 G1_RXD3 G1_RXD4 G1_RXD5 G1_RXD6 G1_RXD7	95 96 97 98 99 100 101 102	I I I I I_{PU} I_{PU} I_{PU} I_{PU}	-	G1_RXD[7:0] Extension GMAC1 GMII Receive Data Input. Received data is received synchronously at the rising edge of G1_RXC. In 10/100Mbps MII mode, only G1_RXD[3:0] are available. These pins must be pulled low with a 1K ohm resistor when not used.

8.2.2. RGMII Pins (RTL8370M)

The Extension GMAC0 and Extension GMAC1 of the RTL8370M support two RGMII interfaces to connect with an external MAC or PHY device when register configuration is set to RGMII mode interface.

Table 13. Extension GMAC0 RGMII Pins (RTL8370M) (TQFP176))

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
RG0_RXD3 RG0_RXD2 RG0_RXD1 RG0_RXD0	113 114 115 116	I	-	RG0_RXD[3:0] Extension GMAC0 RGMII Receive Data Input. Received data is received synchronously by RG0_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.
RG0_RXCTL	117	I	-	RG0_RXCTL Extension GMAC0 RGMII Receive Control signal input. The RG0_RXCTL indicates RX_DV at the rising of RG0_RXCLK and RX_ER at the falling edge of RG0_RXCLK. At RG0_RXCLK falling edge, RG0_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG0_RXCLK	118	I	-	RG0_RXCLK Extension GMAC0 RGMII Receive Clock Input. RG0_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG0_RXD[3:0] and RG0_RXCTL synchronization at both RG0_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.
RG0_TXCLK	122	O	-	RG0_TXCLK Extension GMAC0 RGMII Transmit Clock Output. RG0_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG0_TXD[3:0] and RG0_TXCTL synchronization at RG0_TXCLK on both rising and falling edges.

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
RG0_TXCTL/ RESERVED	123	O	-	RG0_TXCTL Extension GMAC0 RGMII Transmit Control signal Output. The RG0_TXCTL indicates TX_EN at the rising edge of RG0_TXCLK, and TX_ER at the falling edge of RG0_TXCLK. At the RG0_TXCLK falling edge, RG0_TXCTL= TX_EN (XOR) TX_ER. This pin must be pulled high with a 4.7K ohm resistor when in normal operation.
RG0_TXD0/ EN_FLASH	124	I/O_{PU}	-	RG0_TXD[3:0] Extension GMAC0 RGMII Transmit Data Output. Transmitted data is sent synchronously to RG0_TXCLK. **RG0_TXD0/EN_FLASH:** Pull Up: Enable FLASH interface Pull Down: Disable FLASH interface
RG0_TXD1/ DIS_8051	125	I/O_{PU}		**RG0_TXD1/DIS_8051:** Pulled High: Disable embedded 8051 upon power on or reset. Pulled Low: Enable embedded 8051 upon power on or reset.
RG0_TXD2/ DISAUTOLOAD	126	I/O_{PU}		**RG0_TXD2/DISAUTOLOAD:** Pulled High: Disable auto load EEPROM upon power on or reset. Pulled Low: Enable auto load EEPROM upon power on or reset.
RG0_TXD3/ RESERVED	127	I/O_{PU}		**RG0_TXD3/RESERVED:** This pin must be pulled high with a 4.7K ohm resistor when in normal operation.

Table 14. Extension GMAC1 RGMII Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
RG1_TXD3 RG1_TXD2 RG1_TXD1 RG1_TXD0	83 84 85 86	O	-	RG1_TXD[3:0] Extension GMAC1 RGMII Transmit Data Output. Transmitted data is sent synchronously to RG1_TXCLK.
RG1_TXCTL	87	O	-	RG1_TXCTL Extension GMAC1 RGMII Transmit Control signal Output. The RG1_TXCTL indicates TX_EN at the rising edge of RG1_TXCLK, and TX_ER at the falling edge of RG1_TXCLK. At the RG1_TXCLK falling edge, RG1_TXCTL= TX_EN (XOR) TX_ER.
RG1_TXCLK	89	O	-	RG1_TXCLK Extension GMAC1 RGMII Transmit Clock Output. RG1_TXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_TXD[3:0] and RG1_TXCTL synchronization at RG1_TXCLK on both rising and falling edges.
RG1_RXCLK	93	I	-	RG1_RXCLK Extension GMAC1 RGMII Receive Clock Input. RG1_RXCLK is 125MHz @ 1Gbps, 25MHz @ 100Mbps, and 2.5MHz @ 10Mbps. Used for RG1_RXD[3:0] and RG1_RXCTL synchronization at both RG1_RXCLK rising and falling edges. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXCTL	94	I	-	RG1_RXCTL Extension GMAC1 RGMII Receive Control signal input. The RG1_RXCTL indicates RX_DV at the rising of RG1_RXCLK and RX_ER at the falling edge of RG1_RXCLK. At RG1_RXCLK falling edge, RG1_RXCTL= RX_DV (XOR) RX_ER. This pin must be pulled low with a 1K ohm resistor when not used.
RG1_RXD0 RG1_RXD1 RG1_RXD2 RG1_RXD3	95 96 97 98	I	-	RG1_RXD[3:0] Extension GMAC1 RGMII Receive Data Input. Received data is received synchronously by RG1_RXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

8.2.3. MII Pins (RTL8370M)

The Extension GMAC0 and Extension GMAC1 of the RTL8370M also support two MII interfaces to connect with an external MAC or PHY device when register configuration is set to MII mode interface. These two MII interfaces also can be configured as MII MAC mode or MII PHY mode by register.

Table 15. Extension GMAC0 MII Pins (MII MAC Mode or MII PHY Mode) of the RTL8370M (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
M0M_CRS/ M0P_CRS	107	I/O_{PU}	-	M0M_CRS Extension GMAC0 MII MAC Mode Carrier Sense Input when operating in 10/100 MII half duplex mode. M0P_CRS Extension GMAC0 MII MAC Mode Carrier Sense Output when operating in 10/100 MII half duplex mode. This pin must be pulled low with a 1K ohm resistor when not used.
M0M_COL/ M0P_COL	108	I/O_{PU}	-	M0M_COL Extension GMAC0 MII MAC Mode Collision Detect Input when operating in 10/100 MII half duplex mode. M0P_COL Extension GMAC0 MII MAC Mode Collision Detect Output when operating in 10/100 MII half duplex mode. This pin must be pulled low with a 1K ohm resistor when not used.
M0M_RXD3/ M0P_TXD3 M0M_RXD2/ M0P_TXD2 M0M_RXD1/ M0P_TXD1 M0M_RXD0/ M0P_TXD0	113 114 115 116	I	-	M0M_RXD[3:0] Extension GMAC0 MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of M0M_RXCLK. M0P_TXD[3:0] Extension GMAC0 MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of M0P_TXCLK. These pins must be pulled low with a 1K ohm resistor when not used.
M0M_RXDV/ M0P_TXEN	117	I	-	M0M_RXDV Extension GMAC0 MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of M0M_RXCLK. M0P_TXEN Extension GMAC0 MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of M0P_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M0M_RXCLK/ M0P_TXCLK	118	I/O	-	M0M_RXCLK Extension GMAC0 MII MAC Mode Receive Clock Input. In MII 100Mbps, M0M_RXCLK is 25MHz Clock Input. In MII 10Mbps, M0M_RXCLK is 2.5MHz Clock Input. Used to synchronize M0M_RXD[3:0], and M0M_RXDV. M0P_TXCLK GMAC0 MII PHY Mode Transmit Clock Output. In MII 100Mbps, M0P_TXCLK is 25MHz Clock Output. In MII 10Mbps, M0P_TXCLK is 2.5MHz Clock Output. Used to synchronize M0P_TXD[3:0], and M0P_TXEN. This pin must be pulled low with a 1K ohm resistor when not used.

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
M0M_TXCLK/ M0P_RXCLK	122	I/O	-	M0M_TXCLK Extension GMAC0 MII MAC Mode Transmit Clock Input. In MII 100Mbps, M0M_TXCLK is 25MHz Clock Input. In MII 10Mbps, M0M_TXCLK is 2.5MHz Clock Input. Used to synchronize M0M_TXD[3:0], and M0M_TXEN. M0P_RXCLK Extension GMAC0 MII PHY Mode Receive Clock Output. In MII 100Mbps, M0P_RXCLK is 25MHz Clock Output. In MII 10Mbps, M0P_RXCLK is 2.5MHz Clock Output. Used to synchronize M0P_RXD[3:0], and M0P_RXDV. This pin must be pulled low with a 1K ohm resistor when not used.
M0M_TXEN/ M0P_RXDV/ RESERVED	123	O	-	M0M_TXEN Extension GMAC0 MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M0M_TXCLK. M0P_RXDV Extension GMAC0 MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of M0P_RXCLK. This pin must be pulled high with a 4.7K ohm resistor when in normal operation.
M0M_TXD0/ M0P_RXD0/ EN_FLASH	124	I/O_{PU}	-	M0M_TXD[3:0] Extension GMAC0 MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of M0M_TXCLK. M0P_RXD[3:0] Extension GMAC0 MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of M0P_RXCLK. **M0M_TXD0/M0P_RXD0/EN_FLASH:** Pull Up: Enable FLASH interface Pull Down: Disable FLASH interface
M0M_TXD1/ M0P_RXD1/ DIS_8051	125	I/O_{PU}		**M0M_TXD1/M0P_RXD1/DIS_8051:** Pulled High: Disable embedded 8051 upon power on or reset. Pulled Low: Enable embedded 8051 upon power on or reset.
M0M_TXD2/ M0P_RXD2/ DISAUTOLOAD	126	I/O_{PU}		**M0M_TXD2/M0P_RXD2/DISAUTOLOAD:** Pulled High: Disable auto load EEPROM upon power on or reset. Pulled Low: Enable auto load EEPROM upon power on or reset.
M0M_TXD3/ M0P_RXD3/ RESERVED	127	I/O_{PU}		**M0M_TXD3/M0P_RXD3/RESERVED:** This pin must be pulled high with a 4.7K ohm resistor when in normal operation.

Table 16. Extension GMAC1 MII Pins (MII MAC Mode or MII PHY Mode) of the RTL8370M (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
M1M_CRS/ M1P_CRS	77	I/O	-	M1M_CRS Extension GMAC1 MII MAC Mode Carrier Sense Input when operating in 10/100 MII half duplex mode. M1P_CRS Extension GMAC1 MII MAC Mode Carrier Sense Output when operating in 10/100 MII half duplex mode. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_COL/ M1P_COL	78	I/O	-	M1M_COL Extension GMAC1 MII MAC Mode Collision Detect Input when operating in 10/100 MII half duplex mode. M1P_COL Extension GMAC1 MII MAC Mode Collision Detect Output when operating in 10/100 MII half duplex mode. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_TXD3/ M1P_RXD3 M1M_TXD2/ M1P_RXD2 M1M_TXD1/ M1P_RXD1 M1M_TXD0/ M1P_RXD0	83 84 85 86	O	-	M1M_TXD[3:0] Extension GMAC1 MII MAC Mode Transmit Data Output. Transmitted data is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXD[3:0] Extension GMAC1 MII PHY Mode Receive Data Output. Received data is received synchronously at the rising edge of M1P_RXCLK.
M1M_TXEN/ M1P_RXDV	87	O	-	M1M_TXEN Extension GMAC1 MII MAC Mode Transmit Data Enable Output. Transmit enable that is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXDV Extension GMAC1 MII PHY Mode Receive Data Valid Output. Receive Data Valid signal that is sent synchronously at the rising edge of M1P_RXCLK.
M1M_TXCLK/ M1P_RXCLK	89	I/O	-	M1M_TXCLK Extension GMAC1 MII MAC Mode Transmit Clock Input. In MII 100Mbps, M1M_TXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_TXCLK is 2.5MHz Clock Input. Used to synchronize M1M_TXD[3:0], M1M_TXEN, and M1M_TXER. M1P_RXCLK Extension GMAC1 MII PHY Mode Receive Clock Output. In MII 100Mbps, M1P_RXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_RXCLK is 2.5MHz Clock Output. Used to synchronize M1P_RXD[3:0], M1P_RXDV, M1P_RXER, M1P_CRS, and M1P_COL. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_TXER/ M1P_RXER/ RESERVED	91	I/O_{PU}	-	M1M_TXER Extension GMAC1 MII MAC Mode Transmit Data Error Output. Transmit Error that is sent synchronously at the rising edge of M1M_TXCLK. M1P_RXER Extension GMAC1 MII PHY Mode Receive Error Output. Receive Error signal that is sent synchronously at the rising edge of M1P_RXCLK.

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
M1M_RXER/ M1P_TXER	92	I	-	M1M_RXER Extension GMAC1 MII MAC Mode Transmit Data Error Input. Receive Error that is received synchronously at the rising edge of M1M_TXCLK. M1P_TXER Extension GMAC1 MII PHY Mode Receive Error Input. Transmit Error signal that is received synchronously at the rising edge of M1P_RXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXCLK/ M1P_TXCLK	93	I/O	-	M1M_RXCLK Extension GMAC1 MII MAC Mode Receive Clock Input. In MII 100Mbps, M1M_RXCLK is 25MHz Clock Input. In MII 10Mbps, M1M_RXCLK is 2.5MHz Clock Input. Used to synchronize M1M_RXD[3:0], M1M_RXDV, M1M_TXER, M1P_CRS, and M1P_COL. M1P_TXCLK GMAC1 MII PHY Mode Transmit Clock Output. In MII 100Mbps, M1P_TXCLK is 25MHz Clock Output. In MII 10Mbps, M1P_TXCLK is 2.5MHz Clock Output. Used to synchronize M1P_TXD[3:0], M1P_TXEN, and M1P_TXER. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXDV/ M1P_TXEN	94	I	-	M1M_RXDV Extension GMAC1 MII MAC Mode Receive Data Valid Input. Receive Data Valid sent synchronously at the rising edge of M1M_RXCLK. M1P_TXEN Extension GMAC1 MII PHY Mode Transmit Data Enable Input. Transmit Data Enable is received synchronously at the rising edge of M1P_TXCLK. This pin must be pulled low with a 1K ohm resistor when not used.
M1M_RXD0/ M1P_TXD0 M1M_RXD1/ M1P_TXD1 M1M_RXD2/ M1P_TXD2 M1M_RXD3/ M1P_TXD3	95 96 97 98	I	-	M1M_RXD[3:0] Extension GMAC1 MII MAC Mode Receive Data Input. Received data that is received synchronously at the rising edge of M1M_RXCLK. M1P_TXD[3:0] Extension GMAC1 MII PHY Mode Transmit Data Input. Transmitted data is received synchronously at the rising edge of M1P_TXCLK. These pins must be pulled low with a 1K ohm resistor when not used.

8.2.4. LED Pins (RTL8370M)

The General Purpose Interface can be configured to parallel mode LED, scan mode LED, or serial mode LED interface via Register configuration. When the LED is configured as parallel mode LED, dual RGMII or dual MII interfaces are also supported, however the GMII interface is not supported. When the LED is configured to scan mode LED, dual RGMII, dual MII, or extension port 1 GMII interface are also supported, however extension port 0 GMII interface is not supported. When the LED is configured to serial mode LED, all extension port interfaces are supported. LED0, LED1, and LED2 of Port n indicate information that can be defined via register or EEPROM.

In parallel mode LED interface, when the LED pin is pulled low, the LED output polarity will be high active. When the LED pin is pulled high, the LED output polarity will change from high active to low active. See section 10.19 LED Indicator, page 57 for more details.

Table 17. Parallel Mode LED Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
P7LED2/G1_TXD7 /SPI_CLK	79	I/O_{PU}	-	Port 7 LED2 Output Signal. P7LED2 indicates information is defined by register or EEPROM.
P7LED1/G1_TXD5 /SPI_D1	81	I/O_{PU}	-	Port 7 LED1 Output Signal. P7LED1 indicates information is defined by register or EEPROM.
P7LED0/G1_TXD6 /SPI_D0	80	I/O_{PU}	-	Port 7 LED0 Output Signal. P7LED0 indicates information is defined by register or EEPROM.
P6LED2/G1_TXD4 /SPI_CS	82	I/O_{PU}	-	Port 6 LED2 Output Signal. P6LED2 indicates information is defined by register or EEPROM.
P6LED1/G1_RXD4	99	I/O_{PU}	-	Port 6 LED1 Output Signal. P6LED1 indicates information is defined by register or EEPROM.
P6LED0/ G1_TXCLK/GPIO1	90	I/O_{PU}	-	Port 6 LED0 Output Signal. P6LED0 indicates information is defined by register or EEPROM.
P5LED2/G1_RXD5 /GPIO0	100	I/O_{PU}	-	Port 5 LED2 Output Signal. P5LED2 indicates information is defined by register or EEPROM.
P5LED1/G1_RXD7	102	I/O_{PU}	-	Port 5 LED1 Output Signal. P5LED1 indicates information is defined by register or EEPROM.
P5LED0/G1_RXD6	101	I/O_{PU}	-	Port 5 LED0 Output Signal. P5LED0 indicates information is defined by register or EEPROM.
P4LED2/G0_CRS/ M0M_CRS/ M0P_CRS/ SLED_P7B/GPIO3	107	I/O_{PU}	-	Port 4 LED2 Output Signal. P4LED2 indicates information is defined by register or EEPROM.
P4LED1/G0_RXD7 /SLED_P5B	109	I/O_{PU}	-	Port 4 LED1 Output Signal. P4LED1 indicates information is defined by register or EEPROM.
P4LED0/G0_COL/ M0M_COL/ M0P_COL/ SLED_P6B	108	I/O_{PU}	-	Port 4 LED0 Output Signal. P4LED0 indicates information is defined by register or EEPROM.
P3LED2/G0_RXD5 /SLED_P3B	111	I/O_{PU}	-	Port 3 LED2 Output Signal. P3LED2 indicates information is defined by register or EEPROM.
P3LED1/G0_RXD6 /SLED_G1A	110	I/O_{PU}	-	Port 3 LED1 Output Signal. P3LED1 indicates information is defined by register or EEPROM.

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
P3LED0/G0_RXD4 /SLED_P2B	112	I/O_{PU}	-	Port 3 LED0 Output Signal. P3LED0 indicates information is defined by register or EEPROM.
P2LED2/G0_RXER /SLED_P1B/GPIO7	119	I/O_{PU}	-	Port 2 LED2 Output Signal. P2LED2 indicates information is defined by register or EEPROM.
P2LED1 /G0_TXCLK /SLED_G1B	121	I/O_{PU}	-	Port 2 LED1 Output Signal. P2LED1 indicates information is defined by register or EEPROM.
P2LED0/G0_TXER /SLED_P0B /EEPROM_MOD	120	I/O_{PU}	-	Port 2 LED0 Output Signal. P2LED0 indicates information is defined by register or EEPROM.
P1LED2/G0_TXD4 /SLED_P3_7A /RESERVED	128	I/O_{PU}	-	Port 1 LED2 Output Signal. P1LED2 indicates information is defined by register or EEPROM.
P1LED1/G0_TXD6 /SLED_P1_5A	130	I/O_{PU}	-	Port 1 LED1 Output Signal. P1LED1 indicates information is defined by register or EEPROM.
P1LED0/G0_TXD5 /SLED_P2_6A/ /RESERVED	129	I/O_{PU}	-	Port 1 LED0 Output Signal. P1LED0 indicates information is defined by register or EEPROM.
P0LED2/G0_TXD7 /EN_PHY /SLED_P0_4A /GPIO2	131	I/O_{PU}	-	Port 0 LED2 Output Signal. P0LED2 indicates information is defined by register or EEPROM.
P0LED1/LED_DA/ SLED_G2A	134	I/O_{PU}	-	Port 0 LED1 Output Signal. P0LED1 indicates information is defined by register or EEPROM.
P0LED0/LED_CK /SLED_P4B /SMI_SEL	135	I/O_{PU}	-	Port 0 LED0 Output Signal. P0LED0 indicates information is defined by register or EEPROM.

Note: See section 10.19 LED Indicator, page 57 for more details.

Table 18. Scan Mode LED Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Drive (mA)	Description
SLED_G1A/ G0_RXD6/P3LED1	110	I/O_{PU}	-	Scan Mode LED Group A G1A Output Signal.
SLED_G2A/LED_DA /P0LED1	134	I/O_{PU}	-	Scan Mode LED Group A G2A Output Signal.
SLED_P0_4A/ G0_TXD7/P0LED2/ EN_PHY/GPIO2	131	I/O_{PU}	-	Scan Mode LED Group A P0_4A Output Signal.
SLED_P1_5A/ G0_TXD6/P1LED1	130	I/O_{PU}	-	Scan Mode Group A LED P1_5A Output Signal.
SLED_P2_6A/ G0_TXD5/P1LED0/ RESERVED	129	I/O_{PU}	-	Scan Mode LED Group A P2_6A Output Signal.
SLED_P3_7A/ G0_TXD4/P1LED/ RESERVED	128	I/O_{PU}	-	Scan Mode LED Group A P3_7A Output Signal.
SLED_G1B/ G0_TXCLK/P2LED1	121	I/O_{PU}	-	Scan Mode LED Group B G1B Output Signal.
SLED_P0B/ G0_TXER/P2LED0/ EEPROM_MOD	120	I/O_{PU}	-	Scan Mode LED Group B P0B Output Signal.
SLED_P1B/ G0_RXER/P2LED2/ GPIO7	119	I/O_{PU}	-	Scan Mode LED Group B P1B Output Signal.
SLED_P2B/ G0_RXD4/P3LED0	112	I/O_{PU}	-	Scan Mode LED Group B P2B Output Signal.
SLED_P3B/ G0_RXD5/P3LED2	111	I/O_{PU}	-	Scan Mode LED Group B P3B Output Signal.
SLED_P4B/LED_CK/ P0LED0/SMI_SEL	135	I/O_{PU}	-	Scan Mode LED Group B P4B Output Signal.
SLED_P5B/ G0_RXD7/P4LED1	109	I/O_{PU}	-	Scan Mode LED Group B P5B Output Signal.
SLED_P6B/G0_COL/ M0M_COL/ M0P_COL/P4LED0	108	I/O_{PU}	-	Scan Mode LED Group B P6B Output Signal.
SLED_P7B/G0_CRS/ M0M_CRS/M0P_CRS /P4LED2/GPIO3	107	I/O_{PU}	-	Scan Mode LED Group B P7B Output Signal.

Note: See section 10.19.2 Scan LED Mode, page 58 for details.

8.3. Configuration Strapping Pins (RTL8370M)

Table 19. Configuration Strapping Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Description
RESERVED/G1_TXER/ M1M_TXER/M1P_RXER	91	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be pulled low via an external 4.7k ohm resistor upon power on or reset for normal operation.*
EEPROM_MOD/ G0_TXER/P2LED0/ SLED_P0B	120	I/O_{PU}	EEPROM mode selection. Pull Up: EEPROM 24Cxx Size great than 16Kbits (24C32~) Pull Down: EEPROM 24Cxx Size less or equal than 16Kbit (24C02~24C16). *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When this pin is pulled low, the LED output polarity will be high active. When this pin is pulled high, the LED output polarity will change from high active to low active. See section 10.19 LED Indicator, page 57 for more details.*
RESERVED/G0_TXEN/ RG0_TXCTL/ M0M_TXEN/M0P_RXDV	123	I/O	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.*
EN_FLASH/G0_TXD0/ RG0_TXD0/M0M_TXD0/ M0P_RXD0	124	I/O_{PU}	Enable FLASH Interface. Pull Up: Enable FLASH interface Pull Down: Disable FLASH interface *Note1: The strapping pin DISAUTOLOAD, DIS_8051, and EN_FLASH are for power on or reset initial stage configuration. Refer to Table 20 Configuration Strapping Pins (DISAUTOLOAD, DIS_8051, and EN_FLASH) (RTL8370M), page 39 for details.* *Note2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
DIS_8051/G0_TXD1/ RG0_TXD1/M0M_TXD1/ M0P_RXD1	125	I/O_{PU}	Disable Embedded 8051. Pull Up: Disable embedded 8051 Pull Down: Enable embedded 8051 *Note1: The strapping pin DISAUTOLOAD, DIS_8051, and EN_FLASH are for power on or reset initial stage configuration. Refer to Table 20 Configuration Strapping Pins (DISAUTOLOAD, DIS_8051, and EN_FLASH) (RTL8370M), page 39 for details.* *Note2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*
DISAUTOLOAD/ G0_TXD2/RG0_TXD2/ M0M_TXD2/M0P_RXD2	126	I/O_{PU}	Disable EEPROM Autoload. Pull Up: Disable EEPROM autoload Pull Down: Enable EEPROM autoload *Note1: The strapping pin DISAUTOLOAD, DIS_8051, and EN_FLASH are for power on or reset initial stage configuration. Refer to Table 20 Configuration Strapping Pins (DISAUTOLOAD, DIS_8051, and EN_FLASH) (RTL8370M), page 39 for details.* *Note2: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.*

Pin Name	Pin No. RTL8370M	Type	Description
RESERVED/G0_TXD3/ RG0_TXD3/M0M_TXD3/ M0P_RXD3	127	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.*
RESERVED	27	I_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.*
RESERVED/G0_TXD4/ P1LED2/SLED_P3_7A	128	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*
RESERVED/G0_TXD5/ P1LED0/SLED_P2_6A	129	I/O_{PU}	Internal Use/Reserved. *Note: This pin must be kept floating, or pulled high via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*
EN_PHY/G0_TXD7/ P0LED2/SLED_P0_4A/ GPIO2	131	I/O_{PU}	Enable Embedded PHY. Pull Up: Enable embedded PHY Pull Down: Disable embedded PHY *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*
SMI_SEL/LED_CK/ P0LED0/SLED_P4B	135	I/O_{PU}	EEPROM SMI/MII Management Interface Selection. Pull Up: EEPROM SMI interface Pull Down: MII Management Interface *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset.* *When pulled high, the LED output polarity will be low active. See section 10.19 LED Indicator, page 57 for more details.*
BUZZER/DIS_LPD	25	I/O_{PU}	Realtek Loop Detection Configuration. Pull Up: Disable Loop detection function Pull Down: Enable Loop detection function *Note: This pin must be kept floating, or pulled high or low via an external 4.7k ohm resistor upon power on or reset. 2KHz signal out when looping is detected.*

Table 20. Configuration Strapping Pins (DISAUTOLOAD, DIS_8051, and EN_FLASH) (RTL8370M)

DISAUTOLOAD	DIS_8051	EN_FLASH	Initial Stage (Power On or Reset) Loading Data	
			From	To
0	0	0	EEPROM	Embedded 8051 Instruction Memory
		1	FLASH	Embedded 8051 Instruction Memory
	1	0	EEPROM	Register
1	Irrelevant	Irrelevant	Do Nothing	Do Nothing

8.4. Miscellaneous Pins (RTL8370M)

Table 21. Miscellaneous Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Description
XTALI	139	AI	25MHz Crystal Clock Input and Feedback Pin. 25MHz +/-50ppm tolerance crystal reference or oscillator input.
XTALO	138	AO	25MHz Crystal Clock Output Pin. 25MHz +/-50ppm tolerance crystal output.
MDIREF	16	AO	Reference Resistor. A 2.49K ohm (1%) resistor must be connected between MDIREF and GND.
RESERVED	13	AI	This pin must be pulled low via a 1k ohm resister when in normal operation.
RESERVED	14	AO	Reserved. Must be left floating in normal operation.
RESERVED	75	AO	Reserved. Must be left floating in normal operation.
RESERVED	76	AO	Reserved. Must be left floating in normal operation.
SCK/MMD_MDC	142	I/O	EEPROM SMI Interface Clock/MII Management Interface Clock (selected via the hardware strapping pin 135, SMI_SEL).
SDA/MMD_MDIO	143	I/O	EEPROM SMI Interface Data/MII Management Interface Data (selected via the hardware strapping pin 135, SMI_SEL).
INTERRUPT	24	O	Interrupt Output for External CPU.
nRESET	141	I_S	System Reset Input Pin. When low active will reset the RTL8370M.
G1_TXD7/SPI_CLK/ P7LED2	79	I/O_{PU}	Serial Clock (FLASH Interface).
G1_TXD6/SPI_D0/ P7LED0	80	I/O_{PU}	Serial Data 0 (FLASH Interface).
G1_TXD5/SPI_D1/ P7LED1	81	I/O_{PU}	Serial Data 1 (FLASH Interface).
G1_TXD4/SPI_CS/ P6LED2	82	I/O_{PU}	Chip Selection (FLASH Interface).
G1_RXD5/P5LED2/ GPIO0	100	I/O_{PU}	General Purpose Input/Output Interfaces IO0.
G1_TXCLK/P6LED0/ GPIO1	90	I/O_{PU}	General Purpose Input/Output Interfaces IO1.
G0_TXD7/P0LED2/ SLED_P0_4A/EN_PHY/ GPIO2	131	I/O_{PU}	General Purpose Input/Output Interfaces IO2.
G0_CRS/M0M_CRS/ M0P_CRS/P4LED2/ GPIO3	107	I/O_{PU}	General Purpose Input/Output Interfaces IO3.
G0_TXD3/RG0_TXD3/ M0M_TXD3/ M0P_RXD3/RESERVED /GPIO4	127	I/O_{PU}	General Purpose Input/Output Interfaces IO4.
G0_GTXC/RG0_TXCLK /M0M_TXCLK/ M0P_RXCLK/GPIO5	122	I/O	General Purpose Input/Output Interfaces IO5.

Pin Name	Pin No. RTL8370M	Type	Description
G0_RXDV/RG0_RXCTL /M0M_RXDV/ M0P_TXEN/GPIO6	117	I/O	General Purpose Input/Output Interfaces IO6.
G0_RXER/P2LED2/ GPIO7	119	I/O_{PU}	General Purpose Input/Output Interfaces IO7.

8.5. Test Pins (RTL8370M)

Table 22. Test Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Description
RTT1	18	AO	Reserved for Internal Use. Must be left floating.
RTT2	19	AO	Reserved for Internal Use. Must be left floating.
ATESTCK0	165	AO	Reserved for Internal Use. Must be left floating.

8.6. Power and GND Pins (RTL8370M)

Table 23. Power and GND Pins (RTL8370M) (TQFP176)

Pin Name	Pin No. RTL8370M	Type	Description
DVDDIO_0	105, 132	P	Digital I/O High Voltage Power for Extension Port 0 General Purpose Interfaces.
DVDDIO_1	88, 104	P	Digital I/O High Voltage Power for Extension Port 1 General Purpose Interfaces.
DVDDIO	21, 140	P	Digital I/O High Voltage Power for INTERRUPT, SMI, nRESET
DVDDL	22, 26, 29, 30, 103, 106, 133, 136	P	Digital Low Voltage Power.
AVDDH	1, 11, 20, 32, 42, 54, 64, 74, 137, 144, 154, 167	AP	Analog High Voltage Power.
AVDDL	6, 17, 37, 47, 59, 69, 149, 159, 172	AP	Analog Low Voltage Power.
PLLVDDL0	164	AP	PLL0 Low Voltage Power.
PLLVDDL1	52	AP	PLL1 Low Voltage Power.
GND	12, 23, 28, 31, EPAD	G	GND.
AGND	15	AG	Analog GND.
PLLGND0	166	AG	PLL0 GND.
PLLGND1	53	AG	PLL1 GND.

9. Physical Layer Functional Overview

9.1. MDI Interface

The RTL8370(M) embeds eight Gigabit Ethernet PHYs in one chip. Each port uses a single common MDI interface to support 1000Base-T, 100Base-Tx, and 10Base-T. This interface consists of four signal pairs-A, B, C, and D. Each signal pair consists of two bi-directional pins that can transmit and receive at the same time. The MDI interface has internal termination resistors, and therefore reduces BOM cost and PCB complexity. For 1000Base-T, all four pairs are used in both directions at the same time. For 10/100 links and during auto-negotiation, only pairs A and B are used.

9.2. 1000Base-T Transmit Function

The 1000Base-TX transmit function performs 8B/10B coding, scrambling, and 4D-PAM5 encoding. These code groups are passed through a waveform-shaping filter to minimize EMI effects, and are transmitted onto 4-pair CAT5 cable at 125MBaud/s through a D/A converter.

9.3. 1000Base-T Receive Function

Input signals from the media pass through the sophisticated on-chip hybrid circuit to subtract the transmitted signal from the input signal for effective reduction of near-end echo. The received signal is then processed with state-of-the-art technology, e.g., adaptive equalization, BLW (Baseline Wander) correction, cross-talk cancellation, echo cancellation, timing recovery, error correction, and 4D-PAM5 decoding. The 8-bit-wide data is recovered and is sent to the GMII interface at a clock speed of 125MHz. The RX MAC retrieves the packet data from the internal receive MII/GMII interface and sends it to the packet buffer manager.

9.4. 100Base-TX Transmit Function

The 100Base-TX transmit function performs parallel to serial conversion, 4B/5B coding, scrambling, NRZ/NRZI conversion, and MLT-3 encoding. The 5-bit serial data stream after 4B/5B coding is then scrambled as defined by the TP-PMD Stream Cipher function to flatten the power spectrum energy such that EMI effects can be reduced significantly.

The scrambled seed is based on PHY addresses and is unique for each port. After scrambling, the bit stream is driven onto the network media in the form of MLT-3 signaling. The MLT-3 multi-level signaling technology moves the power spectrum energy from high frequency to low frequency, which also reduces EMI emissions.

9.5. 100Base-TX Receive Function

The receive path includes a receiver composed of an adaptive equalizer and DC restoration circuits (to compensate for an incoming distorted MLT-3 signal), an MLT-3 to NRZI and NRZI to NRZ converter to convert analog signals to digital bit-stream, and a PLL circuit to clock data bits with minimum bit error rate. A de-scrambler, 5B/4B decoder, and serial-to-parallel conversion circuits are followed by the PLL circuit. Finally, the converted parallel data is fed into the MAC.

9.6. 10Base-T Transmit Function

The output 10Base-T waveform is Manchester-encoded before it is driven onto the network media. The internal filter shapes the driven signals to reduce EMI emissions, eliminating the need for an external filter.

9.7. 10Base-T Receive Function

The Manchester decoder converts the incoming serial stream to NRZ data when the squelch circuit detects the signal level is above squelch level.

9.8. Auto-Negotiation for UTP

The RTL8370(M) obtains the states of duplex, speed, and flow control ability for each port in UTP mode through the auto-negotiation mechanism defined in the IEEE 802.3 specifications. During auto-negotiation, each port advertises its ability to its link partner and compares its ability with advertisements received from its link partner. By default, the RTL8370(M) advertises full capabilities (1000Full, 100Full, 100Half, 10Full, 10Half) together with flow control ability.

9.9. Crossover Detection and Auto Correction

The RTL8370(M) automatically determines whether or not it needs to crossover between pairs (see Table 24) so that an external crossover cable is not required. When connecting to another device that does not perform MDI crossover, when necessary, the RTL8370(M) automatically switches its pin pairs to communicate with the remote device. When connecting to another device that does have MDI crossover capability, an algorithm determines which end performs the crossover function.

The crossover detection and auto correction function can be disabled via register configuration. The pin mapping in MDI and MDI Crossover mode is given below.

Table 24. Media Dependent Interface Pin Mapping

Pairs	MDI			MDI Crossover		
	1000Base-T	100Base-TX	10Base-T	1000Base-T	100Base-TX	10Base-T
A	A	TX	TX	B	RX	RX
B	B	RX	RX	A	TX	TX
C	C	Unused	Unused	D	Unused	Unused
D	D	Unused	Unused	C	Unused	Unused

9.10. Polarity Correction

The RTL8370(M) automatically corrects polarity errors on the receiver pairs in 1000Base-T and 10Base-T modes. In 100Base-TX mode, the polarity is irrelevant.

In 1000Base-T mode, receive polarity errors are automatically corrected based on the sequence of idle symbols. Once the de-scrambler is locked, the polarity is also locked on all pairs. The polarity becomes unlocked only when the receiver loses lock.

In 10Base-T mode, polarity errors are corrected based on the detection of valid spaced link pulses. The detection begins during the MDI crossover detection phase and locks when the 10Base-T link is up. The polarity becomes unlocked when the link is down.

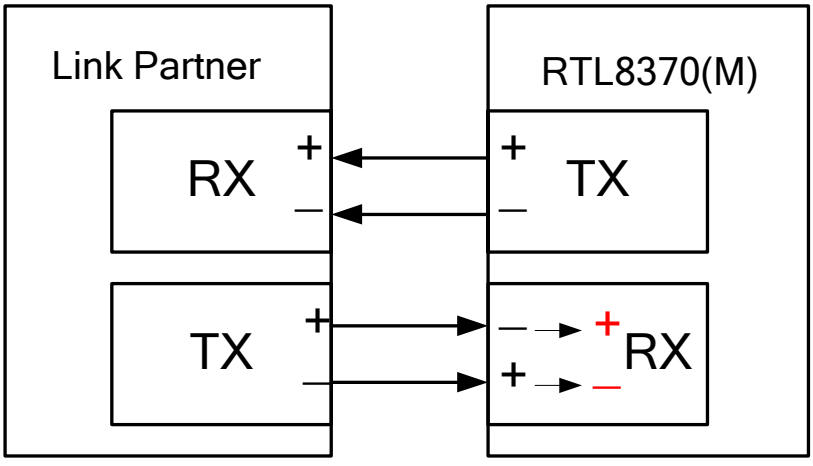


Figure 6. Conceptual Example of Polarity Correction

10. General Function Description

10.1. Reset

10.1.1. Hardware Reset

In a power-on reset, an internal power-on reset pulse is generated and the RTL8370(M) will start the reset initialization procedures. These are:

- Determine various default settings via the hardware strap pins at the end of the nRESET signal
- Autoload the configuration from EEPROM if EEPROM is detected
- Complete the embedded SRAM BIST process
- Initialize the packet buffer descriptor allocation
- Initialize the internal registers and prepare them to be accessed by the external CPU

10.1.2. Software Reset

The RTL8370(M) supports two software resets; a chip reset and a soft reset.

10.1.2.1 CHIP_RESET

When CHIP_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Download configuration from strap pin and EEPROM
2. Start embedded SRAM BIST (Built-In Self Test)
3. Clear all the Lookup and VLAN tables
4. Reset all registers to default values
5. Restart the auto-negotiation process

10.1.2.2 SOFT_RESET

When SOFT_RESET is set to 0b1 (write and self-clear), the chip will take the following steps:

1. Clear the FIFO and re-start the packet buffer link list
2. Restart the auto-negotiation process

10.2. IEEE 802.3x Full Duplex Flow Control

The RTL8370(M) supports IEEE 802.3x flow control in 10/100/1000M modes. Flow control can be decided in two ways:

- When Auto-Negotiation is enabled, flow control depends on the result of NWay
- When Auto-Negotiation is disabled, flow control depends on register definition

10.3. Half Duplex Flow Control

In half duplex mode, the CSMA/CD media access method is the means by which two or more stations share a common transmission medium. To transmit, a station waits (defers) for a quiet period on the medium (that is, no other station is transmitting) and then sends the intended message in bit-serial form. If the message collides with that of another station, then each transmitting station intentionally transmits for an additional predefined period to ensure propagation of the collision throughout the system. The station remains silent for a random amount of time (backoff) before attempting to transmit again.

When a transmission attempt has terminated due to a collision, it is retried until it is successful. The scheduling of the retransmissions is determined by a controlled randomization process called "truncated binary exponential backoff". At the end of enforcing a collision (jamming), the switch delays before attempting to retransmit the frame. The delay is an integer multiple of slot time (512 bit times). The number of slot times to delay before the nth retransmission attempt is chosen as a uniformly distributed random integer 'r' in the range:

$0 \leq r < 2^k$

where:

k = min (n, backoffLimit). The backoffLimit for the RTL8370(M) is 9.

The half duplex back-off algorithm in the RTL8370(M) does not have the maximum retry count limitation of 16 (as defined in IEEE 802.3). This means packets in the switch will not be dropped if the back-off retry count is over 16.

10.3.1. Back-Pressure Mode

In Back-Pressure mode, the RTL8370(M) sends a 4-byte jam pattern (data=0xAA) to collide with incoming packets when congestion control is activated. The Jam pattern collides at the fourth byte counted from the preamble. RTL8370(M) supports 48PASS1, which receives one packet after 48 consecutive jam collisions (data collisions are not included in the 48). Enable this function to prevent port partition after 63 consecutive collisions (data collisions + consecutive jam collisions).

10.4. Search and Learning

Search

When a packet is received, the RTL8370(M) uses the destination MAC address, Filtering Identifier (FID) and enhanced Filtering Identifier (FID) to search the 8K-entry look-up table. The 48-bit MAC address, 12-bit FID and 3-bit EFID use a hash algorithm to calculate an 11-bit index value. The RTL8370(M) uses the index to compare the packet MAC address with the entries (MAC addresses) in the look-up table. This is the 'Address Search'. If the destination MAC address is not found, the switch will broadcast the packet according to VLAN configuration.

Learning

The RTL8370(M) uses the source MAC address, FID, and EFID of the incoming packet to hash into a 11-bit index. It then compares the source MAC address with the data (MAC addresses) in this index. If there is a match with one of the entries, the RTL8370(M) will update the entry with new information. If there is no match and the 8K entries are not all occupied by other MAC addresses, the RTL8370(M) will record the source MAC address and ingress port number into an empty entry. This process is called 'Learning'.

The RTL8370(M) supports a 64-entry Content Addressable Memory (CAM) to avoid look-up table hash collisions. When all 8K entries in the look-up table index are occupied, the source MAC address can be learned into the 64-entry CAM. If both the look-up table and the CAM are full, the source MAC address will not be learned in the RTL8370(M).

Address aging is used to keep the contents of the address table correct in a dynamic network topology. The look-up engine will update the time stamp information of an entry whenever the corresponding source MAC address appears. An entry will be invalid (aged out) if its time stamp information is not refreshed by the address learning process during the aging time period. The aging time of the RTL8370(M) is between 200 and 400 seconds (typical is 300 seconds).

10.5. SVL and IVL/SVL

The RTL8370(M) supports a 4K-group Filtering Identifier (FID) for L2 search and learning. In default operation, all VLAN entries belong to the same FID. This is called Shared VLAN Learning (SVL). If VLAN entries are configured to different FIDs, then the same source MAC address with multiple FIDs can be learned into different look-up table entries. This is called Independent VLAN Learning and Shared VLAN Learning (IVL/SVL).

10.6. Illegal Frame Filtering

Illegal frames such as CRC error packets, runt packets (length <64 bytes), and oversize packets (length >maximum length) will be discarded by the RTL8370(M). The maximum packet length may be set to 1522, 1536, 1552, or 16K bytes.

10.7. IEEE 802.3 Reserved Group Addresses Filtering Control

The RTL8370(M) supports the ability to drop/forward IEEE 802.3 specified reserved group MAC addresses: 01-80-C2-00-00-00 to 01-80-C2-00-00-2F. The default setting enables forwarding of these reserved group MAC address control frames. Frames with group MAC address 01-80-C2-00-00-01 (802.3x Pause) and 01-80-C2-00-00-02 (802.3ad LACP) will always be filtered. Table 25 shows the Reserved Multicast Address (RMA) configuration mode from 01-80-C2-00-00-00 to 01-80-C2-00-00-2F.

Table 25. Reserved Multicast Address Configuration Table

Assignment	Value
Bridge Group Address	01-80-C2-00-00-00
IEEE Std 802.3, 1988 Edition, Full Duplex PAUSE Operation	01-80-C2-00-00-01
IEEE Std 802.3ad Slow Protocols-Multicast Address	01-80-C2-00-00-02
IEEE Std 802.1X PAE Address	01-80-C2-00-00-03
All LANs Bridge Management Group Address	01-80-C2-00-00-10
GMRP Address	01-80-C2-00-00-20
GVRP Address	01-80-C2-00-00-21
Undefined 802.1 Bridge Address	01-80-C2-00-00-04 | 01-80-C2-00-00-0F
Undefined GARP Address	01-80-C2-00-00-22 | 01-80-C2-00-00-2F

10.8. Broadcast/Multicast/Unknown DA Storm Control

The RTL8370(M) enables or disables per-port broadcast/multicast/unknown DA storm control by setting registers (default is disabled). After the receiving rate of broadcast/multicast/unknown DA packets exceeds a reference rate, all other broadcast/multicast/unknown DA packets will be dropped. The reference rate is set via register configuration.

10.9. Port Security Function

The RTL8370(M) supports three types of security function to prevent malicious attacks:

- Per-port enable/disable SA auto-learning for an ingress packet
- Per-port enable/disable look-up table aging update function for an ingress packet
- Per-port enable/disable drop all unknown DA packets

10.10. MIB Counters

The RTL8370(M) supports a set of counters to support management functions.

- MIB-II (RFC 1213)
- Ethernet-Like MIB (RFC 3635)
- Interface Group MIB (RFC 2863)
- RMON (RFC 2819)
- Bridge MIB (RFC 1493)
- Bridge MIB Extension (RFC 2674)

10.11. Port Mirroring

The RTL8370(M) supports one set of port mirroring functions for all ports. The TX, or RX, or both TX/RX packets of the source port can be monitored from a mirror port.

10.12. VLAN Function

The RTL8370(M) supports 4K VLAN groups. These can be configured as port-based VLANs, IEEE 802.1Q tag-based VLANs, and Protocol-based VLANs. Two ingress-filtering and egress-filtering options provide flexible VLAN configuration:

Ingress Filtering

- The acceptable frame type of the ingress process can be set to 'Admit All' or 'Admit All Tagged'
- 'Admit' or 'Discard' frames associated with a VLAN for which that port is not in the member set

Egress Filtering

- 'Forward' or 'Discard' Leaky VLAN frames between different VLAN domains
- 'Forward' or 'Discard' Multicast VLAN frames between different VLAN domains

The VLAN tag can be inserted or removed at the output port. The RTL8370(M) will insert a Port VID (PVID) for untagged frames, or remove the tag from tagged frames. The RTL8370(M) also supports a special insert VLAN tag function to separate traffic from the WAN and LAN sides in Router and Gateway applications.

In router applications, the router may want to know which input port this packet came from. The RTL8370(M) supports Port VID (PVID) for each port and can insert a PVID in the VLAN tag on egress. Using this function, VID information carried in the VLAN tag will be changed to PVID. The RTL8370(M) also provides an option to admit VLAN tagged packets with a specific PVID only. If this function is enabled, it will drop non-tagged packets and packets with an incorrect PVID.

10.12.1. Port-Based VLAN

This default configuration of the VLAN function can be modified via an attached serial EEPROM or EEPROM SMI Slave interface. The 4K-entry VLAN Table designed into the RTL8370(M) provides full flexibility for users to configure the input ports to associate with different VLAN groups. Each input port can join with more than one VLAN group.

Port-based VLAN mapping is the simplest implicit mapping rule. Each ingress packet is assigned to a VLAN group based on the input port. It is not necessary to parse and inspect frames in real-time to determine their VLAN association. All the packets received on a given input port will be forwarded to this port's VLAN members.

10.12.2. IEEE 802.1Q Tag-Based VLAN

The RTL8370(M) supports 4K VLAN entries to perform 802.1Q tag-based VLAN mapping. In 802.1Q VLAN mapping, the RTL8370(M) uses a 12-bit explicit identifier in the VLAN tag to associate received packets with a VLAN. The RTL8370(M) compares the explicit identifier in the VLAN tag with the 4K VLAN Table to determine the VLAN association of this packet, and then forwards this packet to the member set of that VLAN. Two VIDs are reserved for special purposes. One of them is all 1's, which is reserved and currently unused. The other is all 0's, which indicates a priority tag. A priority-tagged frame should be treated as an untagged frame.

When '802.1Q tag aware VLAN' is enabled, the RTL8370(M) performs 802.1Q tag-based VLAN mapping for tagged frames, but still performs port-based VLAN mapping for untagged frames. If '802.1Q tag aware VLAN' is disabled, the RTL8370(M) performs only port-based VLAN mapping both on non-tagged and tagged frames. The processing flow when '802.1Q tag aware VLAN' is enabled is illustrated below.

Two VLAN ingress filtering functions are supported in registers by the RTL8370(M). One is the 'VLAN tag admit control, which provides the ability to receive VLAN-tagged frames only. Untagged or priority tagged (VID=0) frames will be dropped. The other is 'VLAN member set ingress filtering', which will drop frames if the ingress port is not in the member set.

10.12.3. Protocol-Based VLAN

The RTL8370(M) supports a 4-group Protocol-based VLAN configuration. The packet format can be RFC 1042, LLC, or Ethernet, as shown in Figure 7. There are 4 configuration tables to assign the frame type and corresponding field value. Taking IP packet configuration as an example, the user can configure the frame type to be 'Ethernet' and value to be '0x0800'. Each table will index to one of the entries in the 4K-entry VLAN table. The packet stream will match the protocol type and the value will follow the VLAN member configuration of the indexed entry to forward the packets.

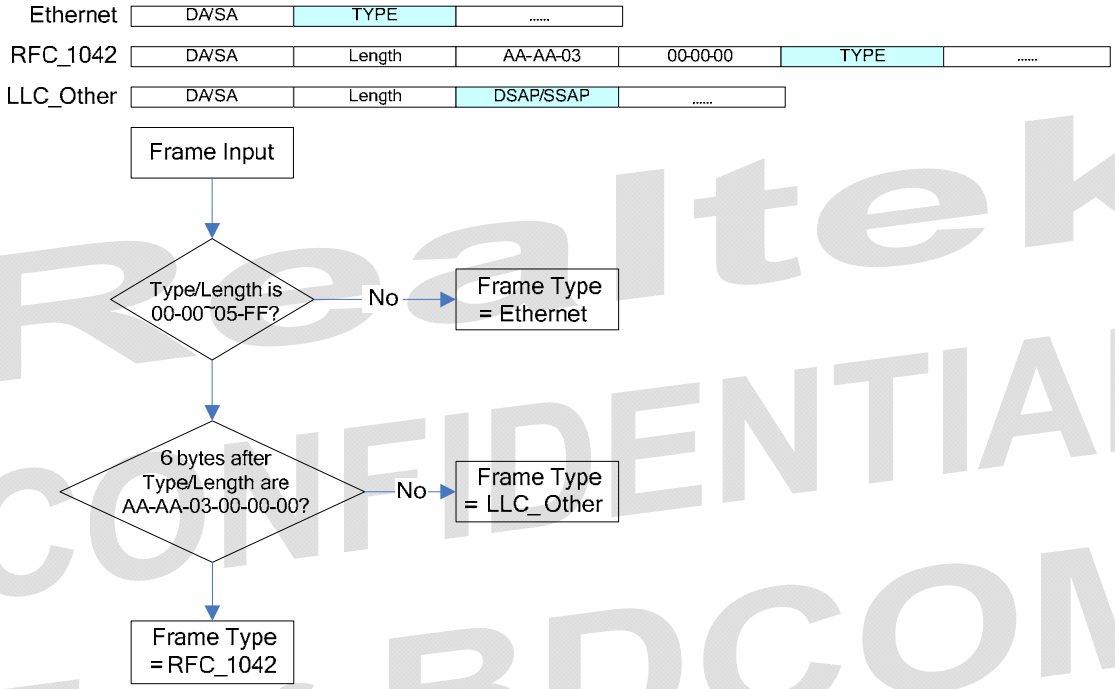


Figure 7. Protocol-Based VLAN Frame Format and Flow Chart

10.12.4. Port VID

In a router application, the router may want to know which input port this packet came from. The RTL8370(M) supports Port VID (PVID) for each port to insert a PVID in the VLAN tag for untagged or priority tagged packets on egress. When 802.1Q tag-aware VLAN is enabled, VLAN tag admit control is enabled, and non-PVID Discard is enabled at the same time. When these functions are enabled, the RTL8370(M) will drop non-tagged packets and packets with an incorrect PVID.

10.13. QoS Function

The RTL8370(M) supports 8 priority queues and input bandwidth control. Packet priority selection can depend on Port-based priority, 802.1p/Q Tag-based priority, IPv4/IPv6 DSCP-based priority, and ACL-based priority. When multiple priorities are enabled in the RTL8370(M), the packet's priority will be assigned based on the priority selection table.

Each queue has one leaky bucket for Average Packet Rate. Per-queue in each output port can be set as Strict Priority (SP) or Weighted Fair Queue (WFQ) for packet scheduling algorithm.

10.13.1. Input Bandwidth Control

Input bandwidth control limits the input bandwidth. When input traffic is more than the RX Bandwidth parameter, this port will either send out a 'pause ON' frame, or drop the input packet depending on register setup. Per-port input bandwidth control rates can be set from 8Kbps to 1Gbps (in 8Kbps steps).

10.13.2. Priority Assignment

Priority assignment specifies the priority of a received packet according to various rules. The RTL8370(M) can recognize the QoS priority information of incoming packets to give a different egress service priority.

The RTL8370(M) identifies the priority of packets based on several types of QoS priority information:

- Port-based priority
- 802.1p/Q-based priority
- IPv4/IPv6 DSCP-based priority
- ACL-based priority

10.13.3. Priority Queue Scheduling

The RTL8370(M) supports MAX-MIN packet scheduling.

Packet scheduling offers two modes:

- APR leaky bucket, which specifies the average rate of one queue
- Weighted Fair Queue (WFQ), which decides which queue is selected in one slot time to guarantee the minimal packet rate of one queue

In addition, each queue of each port can select Strict Priority or WFQ packet scheduling according to packet scheduling mode. Figure 8 shows the RTL8370(M) packet-scheduling diagram.

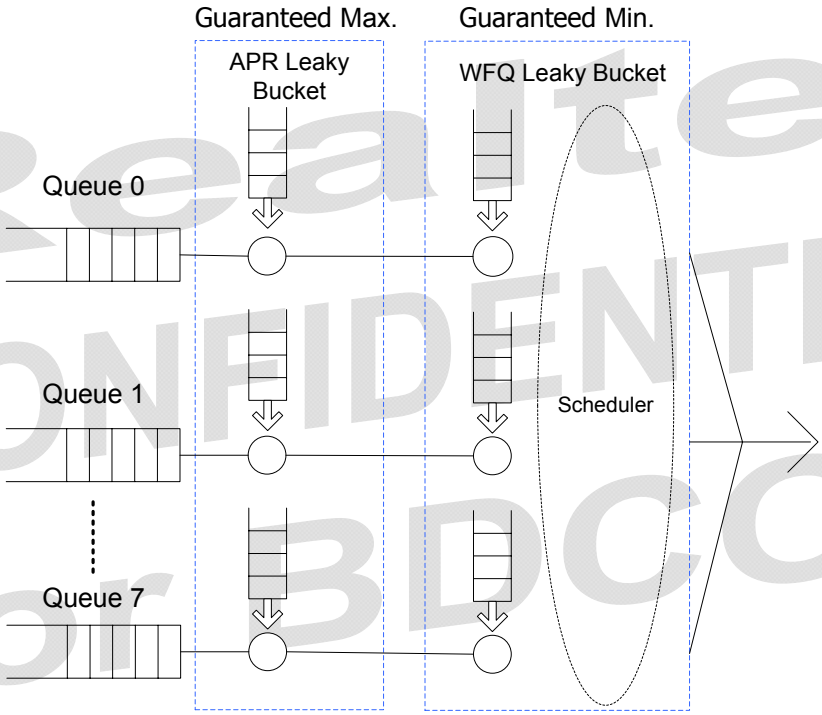


Figure 8. RTL8370(M) MAX-MIN Scheduling Diagram

10.13.4. IEEE 802.1p/Q and DSCP Remarking

The RTL8370(M) supports the IEEE 802.1p/Q and IP DSCP (Differentiated Services Code Point) remarking function. When packets egress from one of the 4 queues, the packet's 802.1p/Q priority and IP DSCP can optionally be remarked to a configured value. Each output queue has a 3-bit 802.1p/Q, and a 6-bit IP DSCP value configuration register.

10.13.5. ACL-Based Priority

The RTL8370(M) supports 64-entry ACL (Access Control List) rules. When a packet is received, its physical port, Layer2, Layer3, and Layer4 information are recorded and compared to ACL entries.

If a received packet matches multiple entries, the entry with the lowest address is valid. If the entry is valid, the action bit and priority bit will be applied.

- If the action bit is 'Drop', the packet will be dropped. If the action bit is 'CPU', the packet will be trapped to the CPU instead of forwarded to non-CPU ports (except where it will be dropped by rules other than the ACL rule)
- If the action bit is 'Permit', ACL rules will override other rules
- If the action bit is 'Mirror', the packet will be forwarded to the mirror port and the L2 lookup result destination port. The mirror port indicates the port configured in the port mirror mechanism
- The priority bit will take effect only if the action bit is 'CPU', 'Permit', and 'Mirror'. The Priority bit is used to determine the packet queue ID according to the priority assignment mechanism

10.14. IGMP & MLD Snooping Function

The RTL8370(M) supports IGMP v1/v2/v3 and MLD v1/v2 snooping. The RTL8370(M) can trap all IGMP and MLD packets to the CPU port. The CPU processes these packets, gets the IP multicast group information of all ports, and writes the correct multicast entry to the lookup table via EEPROM SMI.

10.15. IEEE 802.1x Function

The RTL8370(M) supports IEEE 802.1x Port-based/MAC-based Access Control.

- Port-Based Access Control for each port
- Authorized Port-Based Access Control for each port
- Port-Based Access Control Direction for each port
- MAC-Based Access Control for each port
- MAC-Based Access Control Direction
- Optional Unauthorized Behavior
- Guest VLAN

10.15.1. Port-Based Access Control

Each port of the RTL8370(M) can be set to 802.1x port-based authenticated checking function usage and authorized status. Ports with 802.1X unauthorized status will drop received/transmitted frames.

10.15.2. Authorized Port-Based Access Control

If a dedicated port is set to 802.1x port-based access control, and passes the 802.1x authorization, then its port authorization status can be set to authorized.

10.15.3. Port-Based Access Control Direction

Ports with 802.1X unauthorized status will drop received/transmitted frames only when port authorization direction is 'BOTH'. If the authorization direction of an 802.1X unauthorized port is IN, incoming frames to that port will be dropped, but outgoing frames will be transmitted.

10.15.4. MAC-Based Access Control

MAC-Based Access Control provides authentication for multiple logical ports. Each logical port represents a source MAC address. There are multiple logical ports for a physical port. When a logical port or a MAC address is authenticated, the relevant source MAC address has the authorization to access the network. A frame with a source MAC address that is not authenticated by the 802.1x function will be dropped or trapped to the CPU.

10.15.5. MAC-Based Access Control Direction

Unidirectional and Bi-directional control are two methods used to process frames in 802.1x. As the system cannot predict which port the DA is on, a system-wide MAC-based access control direction setup is provided for determining whether receiving or bi-direction must be authorized.

If MAC-based access control direction is BOTH, then received frames with unauthenticated SA or unauthenticated DA will be dropped. When MAC-based access control direction is IN, only received frames with unauthenticated SA will be dropped.

10.15.6. Optional Unauthorized Behavior

Both in Port-Based Network Access Control and MAC-Based Access Control, a whole system control setup is provided to determine unauthorized frame dropping, trapping to CPU, or tagging as belonging to a Guest VLAN (see the following 'Guest VLAN' section).

10.15.7. Guest VLAN

When the RTL8370(M) enables the Port-based or MAC-based 802.1x function, and the connected PC does not support the 802.1x function or does not pass the authentication procedure, the RTL8370(M) will drop all packets from this port.

The RTL8370(M) also supports one Guest VLAN to allow unauthorized ports or packets to be forwarded to a limited VLAN domain. The user can configure one VLAN ID and member set for these unauthorized packets.

10.16. IEEE 802.1D Function

When using IEEE 802.1D, the RTL8370(M) supports 16 sets and four status' for each port for CPU implementation 802.1D (STP) and 802.1s (MSTP) function:

- Disabled: The port will not transmit/receive packets, and will not perform learning
- Blocking: The port will only receive BPDU spanning tree protocol packets, but will not transmit any packets, and will not perform learning
- Learning: The port will receive any packet, including BPDU spanning tree protocol packets, and will perform learning, but will only transmit BPDU spanning tree protocol packets
- Forwarding: The port will transmit/receive all packets, and will perform learning

The RTL8370(M) also supports a per-port transmission/reception enable/disable function. Users can control the port state via register.

10.17. Embedded 8051

An 8051 MCU is embedded in the RTL8370(M) to support management functions. The 8051 MCU can access all of the registers in the RTL8370(M) through the internal bus. With the Network Interface Circuit (NIC) acting as the data path, the 8051 MCU connects to the switch core and can transmit frames to or receive frames from the Ether network. The features of the 8051 MCU are listed below:

- 256 Bytes fast internal RAM
- On-chip 32K data memory
- On-chip 16K code memory
- Supports code-banking
- 12KBytes NIC buffer
- EEPROM read/write ability

10.18. Realtek Cable Test (RTCT)

The RTL8370(M) physical layer transceivers use DSP technology to implement the Realtek Cable Test (RTCT) feature. The RTCT function can be used to detect short, open, or impedance mismatch in each differential pair. The RTL8370(M) also provides LED support to indicate test status and results.

10.19. LED Indicator

The RTL8370(M) supports parallel LEDs and scan mode LEDs for each port. Each port has three LED indicator pins, LED0, LED1, and LED2. Each pin may have different indicator information (defined in Table 26). Refer to section 7.2 Parallel LED Pins (RTL8370), page 16 and section 8.2.4 LED Pins (RTL8370M), page 35 for details. Upon reset, the RTL8370(M) supports chip diagnostics and LED operation test by blinking all LEDs once.

Table 26. LED Definitions

LED Statuses	Description
LED_Off	LED pin Output disable.
Dup/Col	Duplex/Collision, Indicator. Blinking when collision occurs. Low for full duplex, and high for half duplex mode.
Link/Act	Link, Activity Indicator. Low for link established. Link/Act Blinking when the corresponding port is transmitting or receiving.
Spd1000	1000Mbps Speed Indicator. Low for 1000Mbps.
Spd100	100Mbps Speed Indicator. Low for 100Mbps.
Spd10	10Mbps Speed Indicator. Low for 10Mbps.
Spd1000/Act	1000Mbps Speed/Activity Indicator. Low for 1000Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100/Act	100Mbps Speed/Activity Indicator. Low for 100Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd10/Act	10Mbps Speed/Activity Indicator. Low for 10Mbps. Blinking when the corresponding port is transmitting or receiving.
Spd100 (10)/Act	10/100Mbps Speed/Activity Indicator. Low for 10/100Mbps. Blinking when the corresponding port is transmitting or receiving.
Act	Activity Indicator. Act blinking when the corresponding port is transmitting or receiving.

10.19.1. Parallel LED Mode

The RTL8370(M) supports parallel LED mode. The parallel LED pin also supports pin strapping configuration functions. The PnLED0, PnLED1, and PnLED2 pins are dual-function pins: input operation for configuration upon reset, and output operation for LED after reset. If the pin input is pulled high upon reset, the pin output is active low after reset. If the pin input is pulled down upon reset, the pin output is active high after reset. For details refer to Figure 9, page 58, and Figure 10, page 58. Typical values for pull-up/pull-down resistors are 4.7KΩ.

The PnLED1 can be combined with PnLED1 or PnLED2 as a Bi-color LED.

LED_PnLED1 should operate with the same polarity as other Bi-color LED pins. For example:

- P0LED1 should pull up upon reset if P0LED1 is combined with P0LED2 as a Bi-color LED, and P0LED2 input is pulled high upon reset. In this configuration, the output of these pins is active low after reset
- P0LED1 should be pulled down upon reset if P0LED1 is combined with P0LED2 as a Bi-color LED, and P0LED2 input is pulled down upon reset. In this configuration, the output of these pins is active high after reset

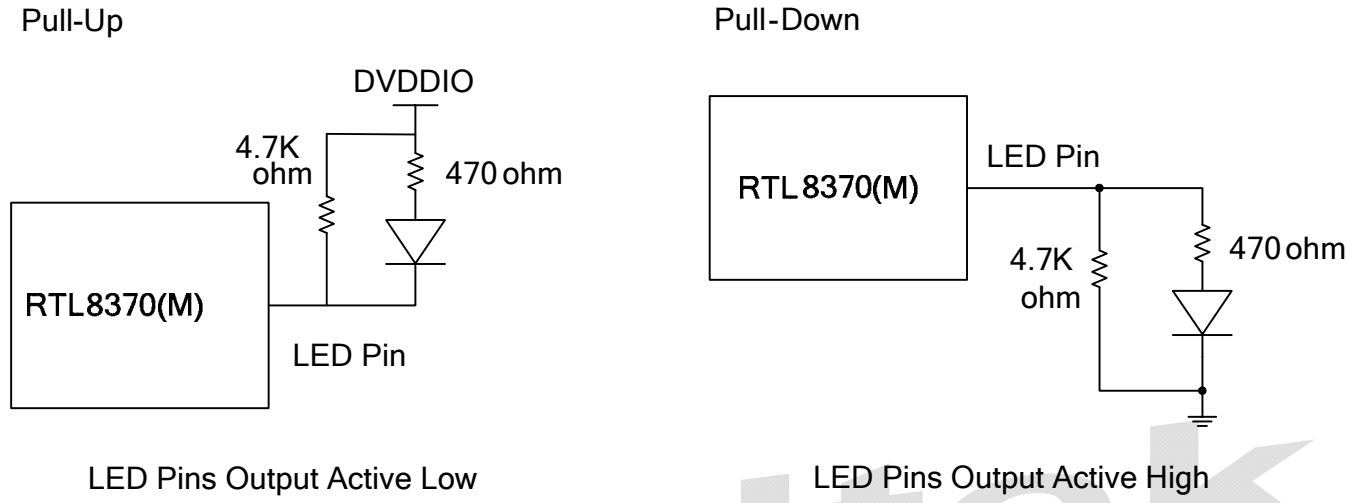


Figure 9. Pull-Up and Pull-Down of LED Pins for Single-Color LED

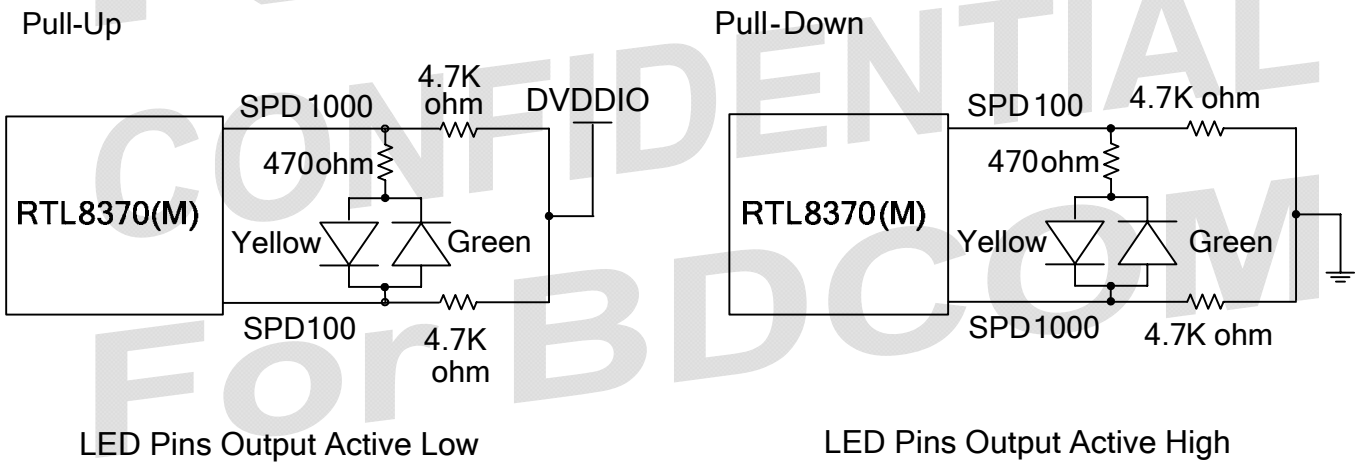


Figure 10. Pull-Up and Pull-Down of LED Pins for Bi-Color LED

10.19.2. Scan LED Mode

The RTL8370(M) provides scan LED mode to reduce LED pins but keep the same number of LED indicators as parallel LED mode. Each port includes one bi-color and one single-color LED. The bi-color LED consists of LED1 & LED 2 (Figure 12) and the single-color LED is driven by LED0 (Figure 11).

In the bi-color LED circuit, the 30K ohm parallel connected resistor must be used if the strapping pin on either side of the bi-color LED is pulled low. Otherwise it is not required. Some Scan mode LED pins also support strapping pins and will not affect the LED polarity.

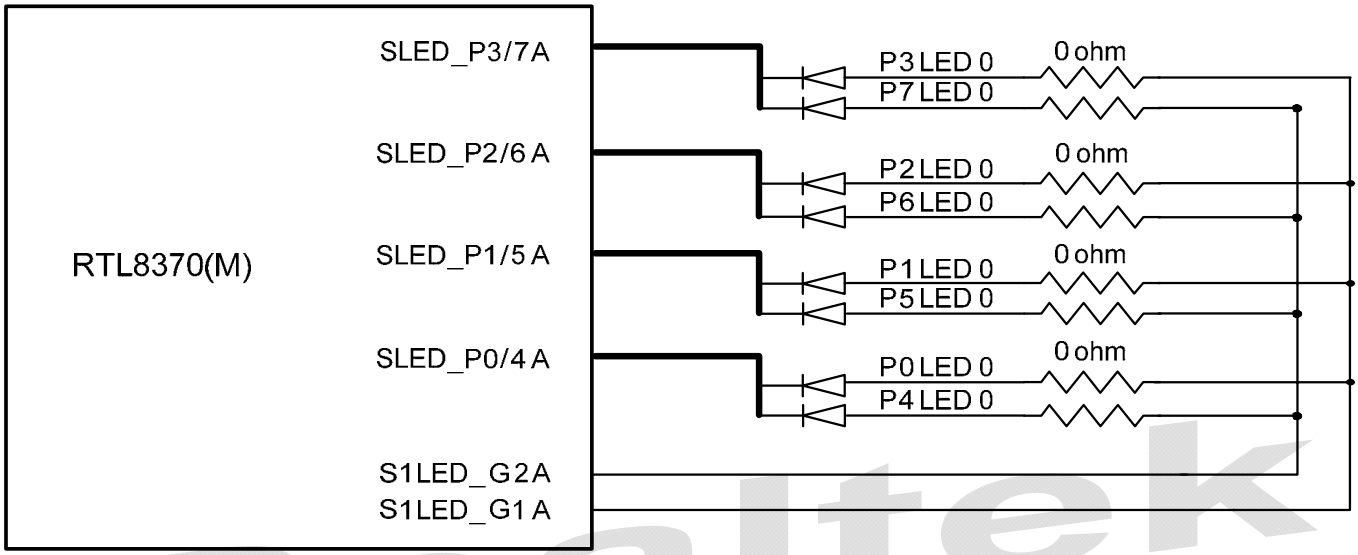


Figure 11. Scan Mode LED Connection Diagram (Group A: Single-Color LED (LED0))

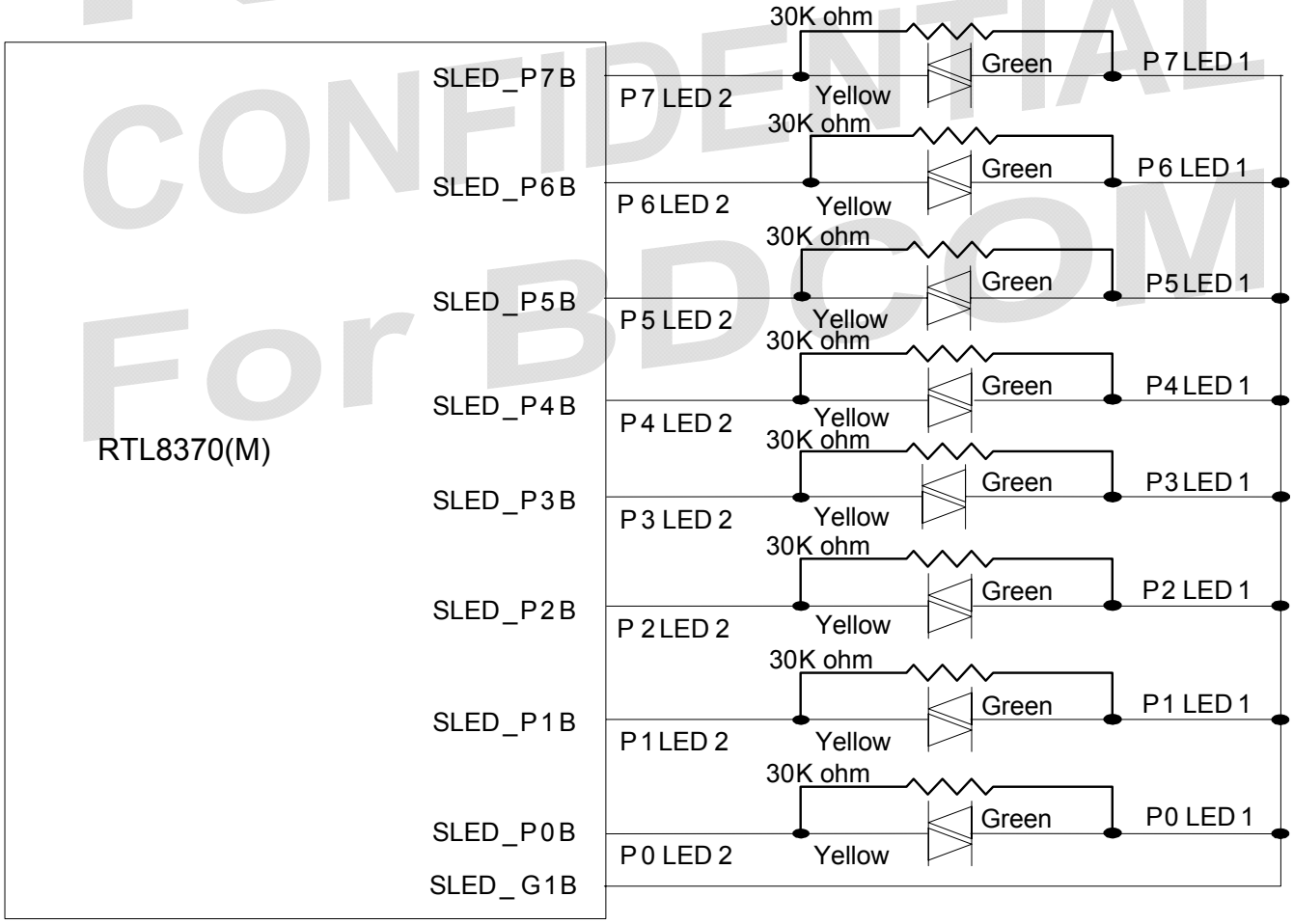


Figure 12. Scan Mode LED Connection Diagram (Group B: Bi-Color LED (LED1 & LED2))

10.20. Green Ethernet

10.20.1. Link-On and Cable Length Power Saving

The RTL8370(M) provides link-on and dynamic detection of cable length and dynamic adjustment of power required for the detected cable length. This feature provides high performance with minimum power consumption.

10.20.2. Link-Down Power Saving

The RTL8370(M) implements link-down power saving on a per-port basis, greatly cutting power consumption when the network cable is disconnected. After it detects an incoming signal, it wakes up from link-down power saving and operates in normal mode.

10.21. IEEE 802.3az Energy Efficient Ethernet (EEE) Function

The RTL8370(M) support IEEE 802.3az Energy Efficient Ethernet ability for 1000Base-T, 100Base-TX in full duplex operation, and 10Base-T in full/half duplex mode.

The Energy Efficient Ethernet (EEE) optional operational mode combines the IEEE 802.3 Media Access

Control (MAC) sub-layer with 100Base-T and 1000Base-T Physical Layers defined to support operation in Low Power Idle mode. When Low Power Idle mode is enabled, systems on both sides of the link can disable portions of the functionality and save power during periods of low link utilization.

- For 1000Base-T PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 100Base-TX PHY: Supports Energy Efficient Ethernet with the optional function of Low Power Idle
- For 10Base-T, EEE defines a 10Mbps PHY (10Base-Te) with reduced transmit amplitude requirements. 10Base-Te is fully interoperable with 10Base-T PHYs over 100m of class-D (Cat-5) cable

The RTL8370(M) MAC uses Low Power Idle signaling to indicate to the PHY, and to the link partner, that a break in the data stream is expected, and components may use this information to enter power saving modes that require additional time to resume normal operation. Similarly, it informs the LPI Client that the link partner has sent such an indication.

10.22. Interrupt Pin for External CPU

The RTL8370(M) provides one Interrupt output pin to interrupt an external CPU. The polarity of the Interrupt output pin can be configured via register access. In configuration registers, each port has link-up and link-down interrupt flags with mask.

When port link-up or link-down interrupt mask is enabled, the RTL8370(M) will raise the interrupt signal to alarm the external CPU. The CPU can read the interrupt flag to determine which port has changed to which status.

11. Interface Descriptions

11.1. EEPROM SMI Host to EEPROM

The EEPROM interface of the RTL8370(M) uses the serial bus EEPROM Serial Management Interface (SMI) to read the 8K-bit 24C08 EEPROM. When the RTL8370(M) is powered up, it drives SCK and SDA to read the registers from the EEPROM.

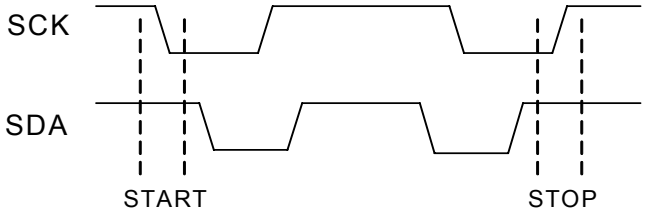


Figure 13. SMI Start and Stop Command

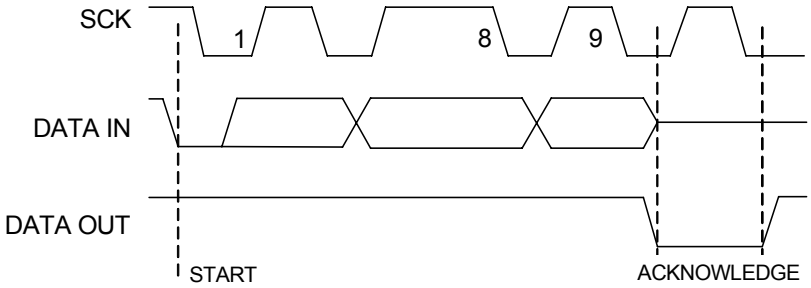


Figure 14. EEPROM SMI Host to EEPROM

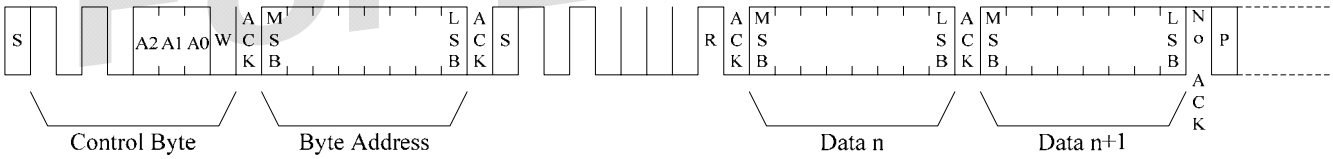


Figure 15. EEPROM SMI Host Mode Frame

11.2. EEPROM SMI Slave for External CPU

When EEPROM auto-load is complete, the RTL8370(M) registers can be accessed via SCK and SDA via an external CPU. The device address of the RTL8370(M) is 0x4. For the start and end of a write/read command, SCK needs one extra clock before/after the start/stop signals.

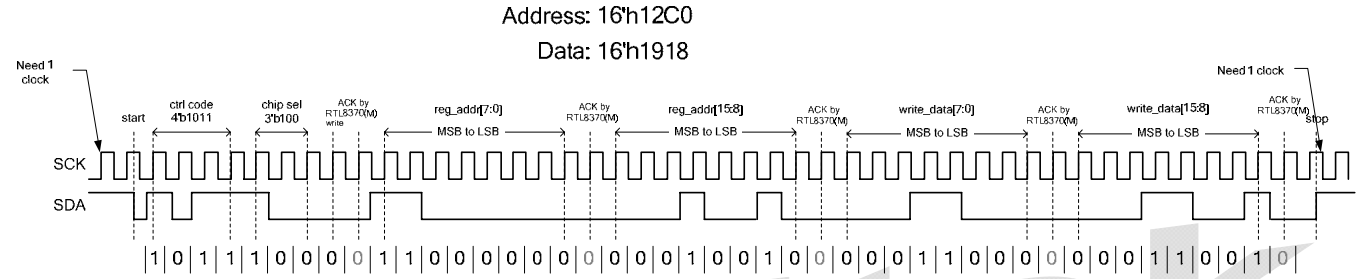


Figure 16. EEPROM SMI Write Command for Slave Mode

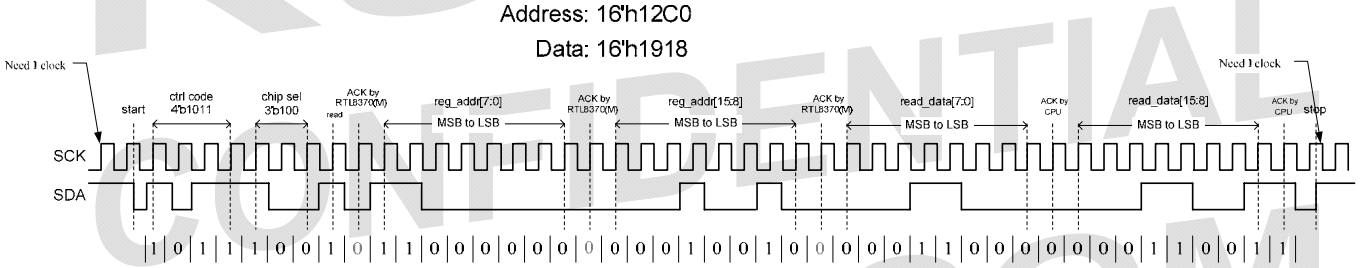


Figure 17. EEPROM SMI Read Command for Slave Mode

11.3. General Purpose Interface (RTL8370M Only)

The RTL8370M shares two extension interfaces and an LED interface with the General Purpose Interface. The interface function mux is summarized in Table 27. When the extension interfaces are configured as dual RGMII or MII mode, the LED interface can support per-port 3 LED pins for 8 UTP ports. When the extension interfaces are configured as dual GMII mode, the LED interface only supports LED_DA and LED_CK pins in serial LED mode.

Table 27. RTL8370M General Purpose Interfaces Pin Definitions

Pin No.	GMII	RGMII	MII MAC Mode	MII PHY Mode	Parallel LED	Serial LED
77	G1_CRS	-	M1M_CRS	M1P_CRS	-	-
78	G1_COL	-	M1M_COL	M1P_COL	-	-
79	G1_TXD7	-	-	-	P7LED2	-
80	G1_TXD6	-	-	-	P7LED0	-
81	G1_TXD5	-	-	-	P7LED1	-
82	G1_TXD4	-	-	-	P6LED2	-
83	G1_TXD3	RG1_TXD3	M1M_TXD3	M1P_RXD3	-	-
84	G1_TXD2	RG1_TXD2	M1M_TXD2	M1P_RXD2	-	-
85	G1_TXD1	RG1_TXD1	M1M_TXD1	M1P_RXD1	-	-
86	G1_TXD0	RG1_TXD0	M1M_TXD0	M1P_RXD0	-	-
87	G1_TXEN	RG1_TXCTL	M1M_TXEN	M1P_RXDV	-	-
89	G1_GTXC	RG1_TXCLK	M1M_TXCLK	M1P_RXCLK	-	-
90	G1_TXCLK	-	-	-	P6LED0	-
91	G1_TXER	-	M1M_TXER	M1P_RXER	-	-
92	G1_RXER	-	M1M_RXER	M1P_TXER	-	-
93	G1_RXC	RG1_RXCLK	M1M_RXCLK	M1P_TXCLK	-	-
94	G1_RXDV	RG1_RXCTL	M1M_RXDV	M1P_TXEN	-	-
95	G1_RXD0	RG1_RXD0	M1M_RXD0	M1P_TXD0	-	-
96	G1_RXD1	RG1_RXD1	M1M_RXD1	M1P_TXD1	-	-
97	G1_RXD2	RG1_RXD2	M1M_RXD2	M1P_TXD2	-	-
98	G1_RXD3	RG1_RXD3	M1M_RXD3	M1P_TXD3	-	-
99	G1_RXD4	-	-	-	P6LED1	-
100	G1_RXD5	-	-	-	P5LED2	-
101	G1_RXD6	-	-	-	P5LED0	-
102	G1_RXD7	-	-	-	P5LED1	-
107	G0_CRS	-	M0M_CRS	M0P_CRS	P4LED2	-
108	G0_COL	-	M0M_COL	M0P_COL	P4LED0	-
109	G0_RXD7	-	-	-	P4LED1	-
110	G0_RXD6	-	-	-	P3LED1	-
111	G0_RXD5	-	-	-	P3LED2	-
112	G0_RXD4	-	-	-	P3LED0	-
113	G0_RXD3	RG0_RXD3	M0M_RXD3	M0P_TXD3	-	-
114	G0_RXD2	RG0_RXD2	M0M_RXD2	M0P_TXD2	-	-
115	G0_RXD1	RG0_RXD1	M0M_RXD1	M0P_TXD1	-	-
116	G0_RXD0	RG0_RXD0	M0M_RXD0	M0P_TXD0	-	-
117	G0_RXDV	RG0_RXCTL	M0M_RXDV	M0P_TXEN	-	-

Pin No.	GMII	RGMII	MII MAC Mode	MII PHY Mode	Parallel LED	Serial LED
118	G0_RXC	RG0_RXCLK	M0M_RXCLK	M0P_TXCLK	-	-
119	G0_RXER	-	-	-	P2LED2	-
120	G0_TXER	-	-	-	P2LED0	-
121	G0_TXCLK	-	-	-	P2LED1	-
122	G0_GTXC	RG0_TXCLK	M0M_TXCLK	M0P_RXCLK	-	-
123	G0_TXEN	RG0_TXCTL	M0M_TXEN	M0P_RXDV	-	-
124	G0_TXD0	RG0_TXD0	M0M_TXD0	M0P_RXD0	-	-
125	G0_TXD1	RG0_TXD1	M0M_TXD1	M0P_RXD1	-	-
126	G0_TXD2	RG0_TXD2	M0M_TXD2	M0P_RXD2	-	-
127	G0_TXD3	RG0_TXD3	M0M_TXD3	M0P_RXD3	-	-
128	G0_TXD4	-	-	-	P1LED2	-
129	G0_TXD5	-	-	-	P1LED0	-
130	G0_TXD6	-	-	-	P1LED1	-
131	G0_TXD7	-	-	-	P0LED2	-
134	-	-	-	-	P0LED1	LED_DA
135	-	-	-	-	P0LED0	LED_CK

11.3.1. Extension Port 0 and Port 1 GMII Mode Interface (1Gbps)

The Extension GMAC0 and Extension GMAC1 of the RTL8370M support GMII interfaces to an external CPU.

Table 28 and Table 29 show the pin numbers and names in the RTL8370M. Figure 18 shows the signal diagram for the MAC in GMII interface.

Table 28. Extension GMAC0 GMII Mode Pins

Pin No.	Type	Extension Port 0 GMII
107	I	G0_CRS
108	I	G0_COL
131, 130, 129, 128	O	G0_TXD[7:4]
127, 126, 125, 124	O	G0_TXD[3:0]
123	O	G0_TXEN
122	O	G0_GTXC (125MHz)
121	I	G0_TXCLK (25/2.5MHz)
120	O	G0_TXER
119	I	G0_RXER
118	I	G0_RXC (125/25/2.5MHz)
117	I	G0_RXDV
116, 115, 114, 113	I	G0_RXD[0:3]
112, 111, 110, 109	I	G0_RXD[4:7]

Table 29. Extension GMAC1 GMII Mode Pins

Pin No.	Type	Extension Port 1 GMII
77	I	G1_CRS
78	I	G1_COL
79, 80, 81, 82	O	G1_TXD[7:4]
83, 84, 85, 86	O	G1_TXD[3:0]
87	O	G1_TXEN
89	O	G1_GTXC (125MHz)
90	I	G1_TXCLK (25/2.5MHz)
91	O	G1_TXER
92	I	G1_RXER
93	I	G1_RXC (125/25/2.5MHz)
94	I	G1_RXDV
95, 96, 97, 98	I	G1_RXD[0:3]
99, 100, 101, 102	I	G1_RXD[4:7]

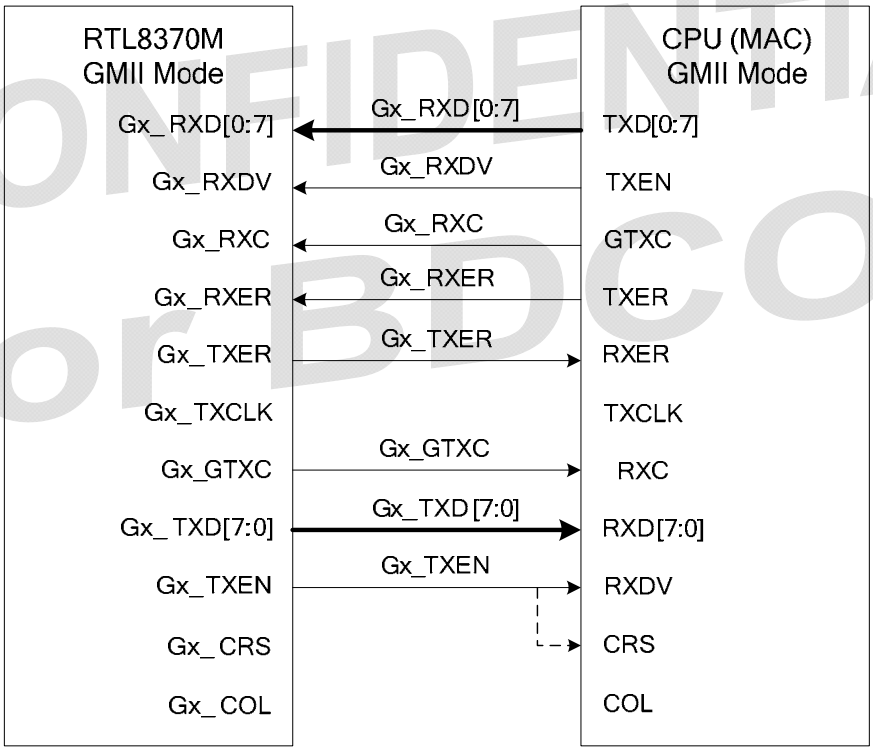


Figure 18. MAC GMII Mode Interface (1Gbps) Signal Diagram

11.3.2. Extension Port 0 and Port 1 RGMII Mode (1Gbps)

The Extension GMAC0 and Extension GMAC1 of the RTL8370M support RGMII interfaces to an external CPU. The pin numbers and names are shown in Table 30 and Table 31. Figure 19 shows the signal diagram for Extension Port 0 and Extension Port 1 in RGMII interfaces.

Table 30. Extension GMAC0 RGMII Pins

Pin No.	Type	Extension Port 0 RGMII
127, 126, 125, 124	O	RG0_TXD[3:0]
123	O	RG0_TXCTL
122	O	RG0_TXCLK
118	I	RG0_RXCLK
117	I	RG0_RXCTL
116, 115, 114, 113	I	RG0_RXD[0:3]

Table 31. Extension GMAC1 RGMII Pins

Pin No.	Type	Extension Port 1 RGMII
83, 84, 85, 86	O	RG1_TXD[3:0]
87	O	RG1_TXCTL
89	O	RG1_TXCLK
93	I	RG1_RXCLK
94	I	RG1_RXCTL
95, 96, 97, 98	I	RG1_RXD[0:3]

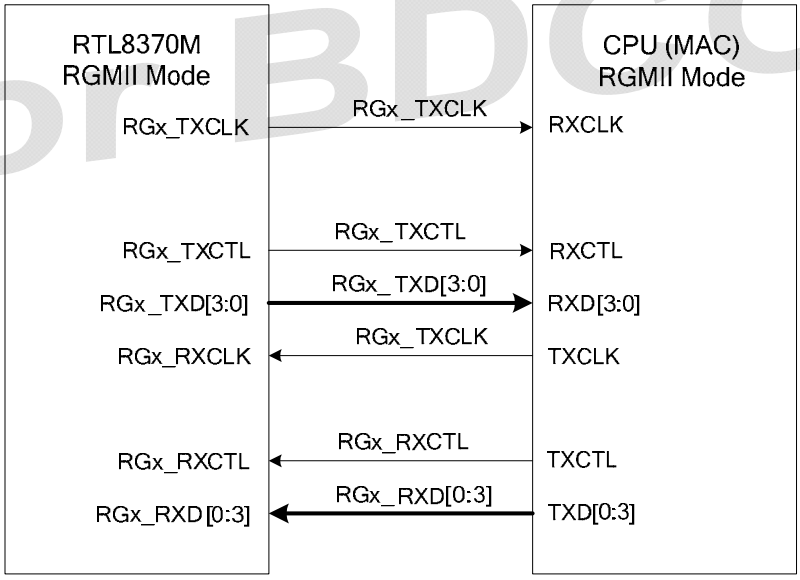


Figure 19. RGMII Mode Interface Signal Diagram

11.3.3. Extension Port 0 and Port 1 MII MAC/PHY Mode Interface (10/100Mbps)

Both the Extension GMAC0 and Extension GMAC1 of the RTL8370M support MII MAC/PHY mode interfaces to an external CPU. The pin numbers and names are shown in Table 32 and Table 33. Figure 20, page 68 shows the signal diagram for the MII PHY mode interface, and Figure 21, page 68 for the MII MAC mode interface.

Table 32. Extension GMAC0 MII Pins

Pin No.	Type	Extension Port 0 MII MAC Mode	Type	Extension Port 0 MII PHY Mode
107	I	M0M_CRS	O	M0P_CRS
108	I	M0M_COL	O	M0P_COL
113, 114, 115, 116	I	M0M_RXD[3:0]	I	M0P_TXD[3:0]
117	I	M0M_RXDV	I	M0P_TXEN
118	I	M0M_RXCLK	O	M0P_TXCLK
122	I	M0M_TXCLK	O	M0P_RXCLK
123	O	M0M_TXEN	O	M0P_RXDV
127, 126, 125, 124	O	M0M_TXD[3:0]	O	M0P_RXD[3:0]

Table 33. Extension GMAC1 MII Pins

Pin No.	Type	Extension Port 1 MII MAC Mode	Type	Extension Port 1 MII PHY Mode
77	I	M1M_CRS	O	M1P_CRS
78	I	M1M_COL	O	M1P_COL
91	O	M1M_TXER	O	M1P_RXER
92	I	M1M_RXER	I	M1P_TXER
98, 97, 96, 95	I	M1M_RXD[3:0]	I	M1P_TXD[3:0]
94	I	M1M_RXDV	I	M1P_TXEN
93	I	M1M_RXCLK	O	M1P_TXCLK
89	I	M1M_TXCLK	O	M1P_RXCLK
87	O	M1M_TXEN	O	M1P_RXDV
83, 84, 85, 86	O	M1M_TXD[3:0]	O	M1P_RXD[3:0]

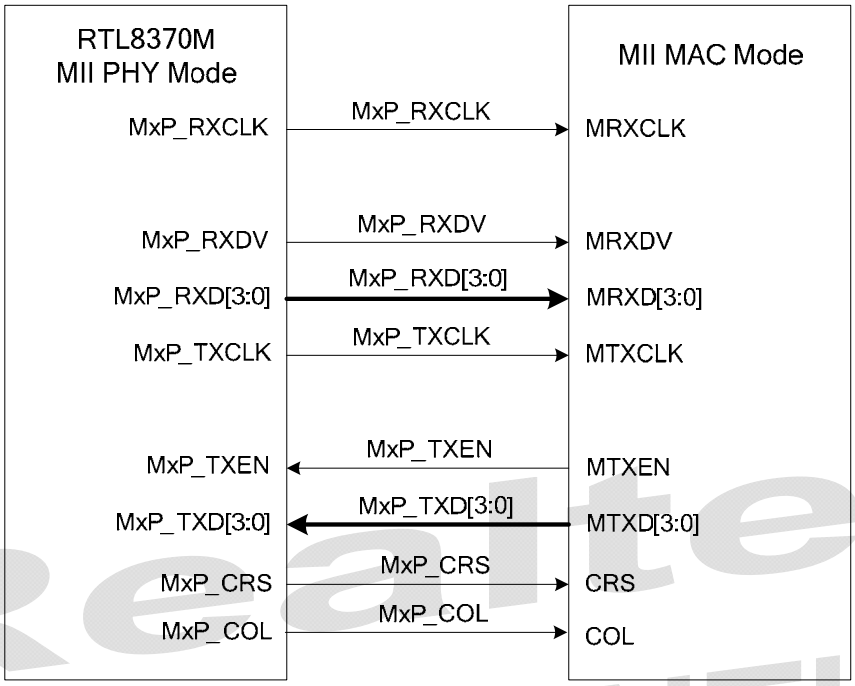


Figure 20. Signal Diagram of MII PHY Mode Interface (100Mbps)

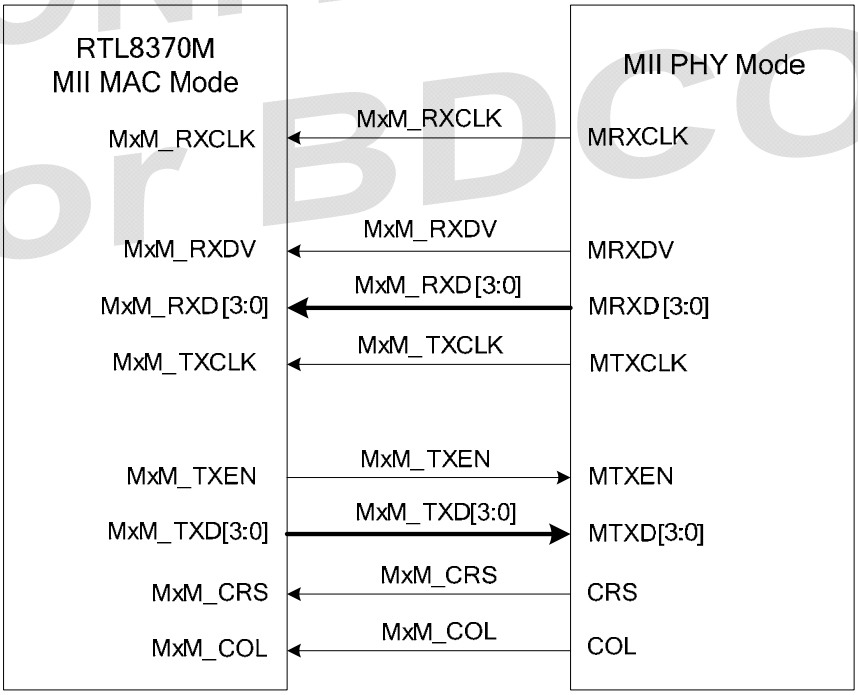


Figure 21. Signal Diagram of MII MAC Mode Interface (100Mbps)

12. Register Descriptions

In this section the following abbreviations are used:

RO: Read Only
RW: Read/Write
LL: Latch Low until clear
LH: Latch High until clear
SC: Self Clearing

12.1. Page 0: PCS Register (PHY 0~7)

Table 34. Page 0: PCS Register (PHY 0~7)

Register	Register Description	Default
0	Control Register	0x1140
1	Status Register	0x7949
2	PHY Identifier 1	0x001C
3	PHY Identifier 2	0xC980
4	Auto-Negotiation Advertisement Register	0x0DE1
5	Auto-Negotiation Link Partner Ability Register	0x0000
6	Auto-Negotiation Expansion Register	0x0004
7	Auto-Negotiation Page Transmit Register	0x2001
8	Auto-Negotiation Link Partner Next Page Register	0x0000
9	1000Base-T Control Register	0x0E00
10	1000Base-T Status Register	0x0000
11~14	Reserved	0x0000
15	Extended Status	0x2000
16~31	ASIC Control Register	-

12.2. Register 0: Control

Table 35. Register 0: Control

Reg.bit	Name	Mode	Description	Default
0.15	Reset	RW/SC	1: PHY reset 0: Normal operation This bit is self-clearing.	0
0.14	Loopback (Digital loopback)	RW	1: Enable loopback. This will loopback TXD to RXD and ignore all activity on the cable media 0: Normal operation This function is usable only when this PHY is operated in 10Base-T full duplex, 100Base-TX full duplex, or 1000Base-T full duplex.	0
0.13	Speed Selection[0]	RW	[0.6,0.13] Speed Selection[1:0] 11: Reserved 10: 1000Mbps 01: 100Mbps 00: 10Mbps This bit can be set through SMI (Read/Write).	0
0.12	Auto Negotiation Enable	RW	1: Enable auto-negotiation process 0: Disable auto-negotiation process This bit can be set through SMI (Read/Write).	1
0.11	Power Down	RW	1: Power down. All functions will be disabled except SMI function 0: Normal operation	0
0.10	Isolate	RW	1: Electrically isolates the PHY from GMII. The PHY is still able to respond to MDC/MDIO 0: Normal operation	0
0.9	Restart Auto Negotiation	RW/SC	1: Restart Auto-Negotiation process 0: Normal operation	0
0.8	Duplex Mode	RW	1: Full duplex operation 0: Half duplex operation This bit can be set through SMI (Read/Write).	1
0.7	Collision Test	RO	1: Collision test enabled 0: Normal operation When set, this bit will cause the COL signal to be asserted in response to the assertion of TXEN within 512-bit times. The COL signal will be de-asserted within 4-bit times in response to the de-assertion of TXEN.	0
0.6	Speed Selection[1]	RW	See Bit 13	1
0.[5:0]	Reserved	RO	Reserved	000000

12.3. Register 1: Status

Table 36. Register 1: Status

Reg.bit	Name	Mode	Description	Default
1.15	100Base-T4	RO	0: No 100Base-T4 capability The RTL8370(M) does not support 100Base-T4 mode and this bit should always be 0.	0
1.14	100Base-TX-FD	RO	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
1.13	100Base-TX-HD	RO	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1
1.12	10Base-T-FD	RO	1: 10Base-T full duplex capable 0: Not 10Base-TX full duplex capable	1
1.11	10Base-T-HD	RO	1: 10Base-T half duplex capable 0: Not 10Base-TX half duplex capable	1
1.10	100Base-T2-FD	RO	0: Not 100Base-T2 full duplex capable The RTL8370(M) does not support 100Base-T2 mode and this bit should always be 0.	0
1.9	100Base-T2-HD	RO	0: Not 100Base-T2 half duplex capable The RTL8370(M) does not support 100Base-T2 mode and this bit should always be 0.	0
1.8	Extended Status	RO	1: Extended status information in Register 15 The RTL8370(M) always supports Extended Status Register.	1
1.7	Reserved	RO	Reserved	0
1.6	MF Preamble Suppression	RO	The RTL8370(M) will accept management frames with preamble suppressed.	1
1.5	Auto-negotiate Complete	RO	1: Auto-negotiation process completed 0: Auto-negotiation process not completed	0
1.4	Remote Fault	RO/LH	1: Remote fault condition detected 0: No remote fault detected This bit will remain set until it is cleared by reading register 1 via the management interface.	0
1.3	Auto-Negotiation Ability	RO	1: Auto-negotiation capable (permanently =1)	1
1.2	Link Status	RO/LL	1: Link is established. If the link fails, this bit will be 0 until after reading this bit again 0: Link has failed since previous read If the link fails, this bit will be set to 0 until bit is read.	0
1.1	Jabber Detect	RO/LH	1: Jabber detected 0: No Jabber detected Jabber is supported only in 10Base-T mode.	0
1.0	Extended Capability	RO	1: Extended register capable (permanently =1)	1

12.4. Register 2: PHY Identifier 1

The PHY Identifier Registers #1 and #2 together form a unique identifier for the PHY section of this device. The Identifier consists of a concatenation of the Organizationally Unique Identifier (OUI), the vendor's model number, and the model revision number. A PHY may return a value of zero in each of the 32 bits of the PHY Identifier if desired. The PHY Identifier is intended to support network management.

Table 37. Register 2: PHY Identifier 1

Reg.bit	Name	Mode	Description	Default
2.[15:0]	OUI	RO	Composed of the 3rd to 18th bits of the Organizationally Unique Identifier (OUI), respectively.	0x001C

12.5. Register 3: PHY Identifier 2

Table 38. Register 3: PHY Identifier 2

Reg.bit	Name	Mode	Description	Default
3.[15:10]	OUI	RO	Assigned to the 19th through 24th bits of the OUI	110010
3.[9:4]	Model Number	RO	Manufacturer's model number	011000
3.[3:0]	Revision Number	RO	Manufacturer's revision number	0000

12.6. Register 4: Auto-Negotiation Advertisement

This register contains the advertisement abilities of this device as they will be transmitted to its Link Partner during Auto-negotiation.

Note: Each time the link ability of the RTL8370(M) is reconfigured, the auto-negotiation process should be executed to allow the configuration to take effect.

Table 39. Register 4: Auto-Negotiation Advertisement

Reg.bit	Name	Mode	Description	Default
4.15	Next Page	RO	1: Additional next pages exchange desired 0: No additional next pages exchange desired	0
4.14	Acknowledge	RO	Permanently=0	0
4.13	Remote Fault	RW	1: Advertises that the RTL8370(M) has detected a remote fault 0: No remote fault detected	0
4.12	Reserved	RO	Reserved	0
4.11	Reserved	RW	Reserved	0
4.10	Pause	RW	1: Advertises that the RTL8370(M) has flow control capability 0: No flow control capability	1
4.9	100Base-T4	RO	1: 100Base-T4 capable 0: Not 100Base-T4 capable (Permanently =0)	0
4.8	100Base-TX-FD	RW	1: 100Base-TX full duplex capable 0: Not 100Base-TX full duplex capable	1
4.7	100Base-TX	RW	1: 100Base-TX half duplex capable 0: Not 100Base-TX half duplex capable	1

Reg.bit	Name	Mode	Description	Default
4.6	10Base-T-FD	RW	1: 10Base-TX full duplex capable 0: Not 10Base-TX full duplex capable	1
4.5	10Base-T	RW	1: 10Base-TX half duplex capable 0: Not 10Base-TX half duplex capable	1
4.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00001

Note 1: The setting of Register 4 has no effect unless auto-negotiation is restarted or the link goes down.
Note 2: If 1000Base-T is advertised, then the required next pages are automatically transmitted.

12.7. Register 5: Auto-Negotiation Link Partner Ability

This register contains the advertised abilities of the Link Partner as received during Auto-negotiation. The content changes after a successful Auto-negotiation.

Table 40. Register 5: Auto-Negotiation Link Partner Ability

Reg.bit	Name	Mode	Description	Default
5.15	Next Page	RO	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
5.14	Acknowledge	RO	1: Link Partner acknowledges reception of Fast Link Pulse (FLP) words 0: Not acknowledged by Link Partner	0
5.13	Remote Fault	RO	1: Remote Fault indicated by Link Partner 0: No remote fault indicated by Link Partner	0
5.12	Reserved	RO	Reserved	0
5.11	Asymmetric Pause	RO	1: Asymmetric Flow control supported by Link Partner 0: No Asymmetric flow control supported by Link Partner. When auto-negotiation is enabled, this bit reflects Link Partner ability	0
5.10	Pause	RO	1: Flow control supported by Link Partner. 0: No flow control supported by Link Partner. When auto-negotiation is enabled, this bit reflects Link Partner ability	0
5.9	100Base-T4	RO	1: 100Base-T4 supported by Link Partner 0: 100Base-T4 not supported by Link Partner	0
5.8	100Base-TX-FD	RO	1: 100Base-TX full duplex supported by Link Partner 0: 100Base-TX full duplex not supported by Link Partner	0
5.7	100Base-TX	RO	1: 100Base-TX half duplex supported by Link Partner 0: 100Base-TX half duplex not supported by Link Partner	0
5.6	10Base-T-FD	RO	1: 10Base-TX full duplex supported by Link Partner 0: 10Base-TX full duplex not supported by Link Partner	0
5.5	10Base-T	RO	1: 10Base-TX half duplex supported by Link Partner 0: 10Base-TX half duplex not supported by Link Partner	0
5.[4:0]	Selector Field	RO	[00001]=IEEE 802.3	00000

12.8. Register 6: Auto-Negotiation Expansion

Table 41. Register 6: Auto-Negotiation Expansion

Reg.bit	Name	Mode	Description	Default
6.[15:5]	Reserved	RO	Ignore on read	0
6.4	Parallel Detection Fault	RO/LH	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
6.3	Link Partner Next Page Ability	RO	1: Link Partner is Next Page able 0: Link Partner is not Next Page able	0
6.2	Local Next Page Ability	RO	Not supported. Permanently =0	1
6.1	Page Received	RO/LH	1: A New Page has been received 0: A New Page has not been received	0
6.0	Link Partner Auto-Negotiation Ability	RO	If Auto-Negotiation is enabled, this bit means: 1: Link Partner is Auto-Negotiation able 0: Link Partner is not Auto-Negotiation able	0

12.9. Register 7: Auto-Negotiation Page Transmit Register

Table 42. Register 7: Auto-Negotiation Page Transmit Register

Reg.bit	Name	Mode	Description	Default
7.15	Next Page	RW	1: Link partner desires Next Page transfer 0: Link partner does not desire Next Page transfer	0
7.14	Reserved	RO	1: A fault has been detected via the Parallel Detection function 0: No fault has been detected via the Parallel Detection function	0
7.13	Message Page	RW	1: Message page 0: No Message page ability	1
7.12	Acknowledge 2	RW	1: Local device has the ability to comply with the message received 0: Local device has no ability to comply with the message received	0
7.11	Toggle	RO	Toggle bit	0
7.[10:0]	Message/ Unformatted Field	RW	Content of message/unformatted page	1

12.10. Register 8: Auto-Negotiation Link Partner Next Page Register

Table 43. Register 8: Auto-Negotiation Link Partner Next Page Register

Reg.bit	Name	Mode	Description	Default
8.15	Next Page	RO	Received Link Code Word Bit 15	0
8.14	Acknowledge	RO	Received Link Code Word Bit 14	0
8.13	Message Page	RO	Received Link Code Word Bit 13	0
8.12	Acknowledge 2	RO	Received Link Code Word Bit 12	0
8.11	Toggle	RO	Received Link Code Word Bit 11	0
8.[10:0]	Message/ Unformatted Field	RO	Received Link Code Word Bit 10:0	0

12.11. Register 9: 1000Base-T Control Register

Table 44. Register 9: 1000Base-T Control Register

Reg.bit	Name	Mode	Description	Default
9.[15:13]	Test Mode	RW	Test Mode Select. 000: Normal mode 001: Test mode 1 – Transmit waveform test 010: Test mode 2 – Transmit jitter test in MASTER mode 011: Test mode 3 – Transmit jitter test in SLAVE mode 100: Test mode 4 – Transmitter distortion test 101, 110, 111: Reserved	000
9.12	MASTER/SLAVE Manual Configuration Enable	RW	1: Enable MASTER/SLAVE manual configuration 0: Disable MASTER/SLAVE manual configuration	0
9.11	MASTER/SLAVE Configuration Value	RW	1: Configure PHY as MASTER during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one 0: Configure PHY as SLAVE during MASTER/SLAVE negotiation, only when bit 9.12 is set to logical one	1
9.10	Port Type	RW	1: Multi-port device 0: Single-port device	1
9.9	1000Base-T Full Duplex	RW	1: Advertise PHY is 1000Base-T full duplex capable 0: Advertise PHY is not 1000Base-T full duplex capable	1
9.8	1000Base-T Half Duplex	RW	1: Advertise PHY is 1000Base-T half duplex capable 0: Advertise PHY is not 1000Base-T half duplex capable	0
9.[7:0]	Reserved	RW	Reserved	0

12.12. Register 10: 1000Base-T Status Register

Table 45. Register 10: 1000Base-T Status Register

Reg.bit	Name	Mode	Description	Default
10.15	MASTER/SLAVE Configuration Fault	RO/LH/SC	1: MASTER/SLAVE configuration fault detected 0: No MASTER/SLAVE configuration fault detected	0
10.14	MASTER/SLAVE Configuration Resolution	RO	1: Local PHY configuration resolved to MASTER 0: Local PHY configuration resolved to SLAVE	0
10.13	Local Receiver Status	RO	1: Local receiver OK 0: Local receiver not OK	0
10.12	Remote Receiver Status	RO	1: Remote receiver OK 0: Remote receiver not OK	0
10.11	Link Partner 1000Base-T Full Duplex	RO	1: Link partner is capable of 1000Base-T full duplex 0: Link partner is not capable of 1000Base-T full duplex	0
10.10	1000Base-T Half Duplex	RO	1: Link partner is capable of 1000Base-T half duplex 0: Link partner is not capable of 1000Base-T half duplex	0
10.[9:8]	Reserved	RO	Reserved	0
10.[7:0]	Idle Error Count	RO/SC	Idle Error Counter. The counter stops automatically when it reaches 0xFF	0

12.13. Register 15: Extended Status

Table 46. Register 15: Extended Status

Reg.bit	Name	Mode	Description	Default
15.15	1000Base-X Full Duplex	RO	1: 1000Base-X full duplex capable 0: Not 1000Base-X full duplex capable	0
15.14	1000Base-X Half Duplex	RO	1: 1000Base-X half duplex capable 0: Not 1000Base-X half duplex capable	0
15.13	1000Base-T Full Duplex	RO	1: 1000Base-T full duplex capable 0: Not 1000Base-T full duplex capable	1
15.12	1000Base-T Half Duplex	RO	1: 1000Base-T half duplex capable 0: Not 1000Base-T half duplex capable	0
15.[11:0]	Reserved	RO	Reserved	0

13. Electrical Characteristics

13.1. Absolute Maximum Ratings

WARNING: Absolute maximum ratings are limits beyond which permanent damage may be caused to the device, or device reliability will be affected. All voltages are specified reference to GND unless otherwise specified.

Table 47. Absolute Maximum Ratings

Parameter	Min	Max	Units
Junction Temperature (Tj)	-	+125	°C
Storage Temperature	-45	+125	°C
DVDDIO, DVDDIO_0, DVDDIO_1, AVDDH, Supply Referenced to GND and AGND	GND-0.3	+3.63	V
DVDDL, AVDDL, PLLVDDL0, PLLVDDL1 Supply Referenced to GND, AGND, PLLGND0, and PLLGND1	GND-0.3	+1.1	V
Digital Input Voltage	GND-0.3	VDDIO+0.3	V

13.2. Recommended Operating Range

Table 48. Recommended Operating Range

Parameter		Min	Typical	Max	Units
Ambient Operating Temperature (Ta)		0	-	70	°C
DVDDIO, AVDDH Supply Voltage Range		3.135	3.3	3.465	V
DVDDIO_0, DVDDIO_1 Supply Voltage Range	3.3V	3.135	3.3	3.465	V
	2.5V	2.375	2.5	2.626	V
DVDDL, AVDDL, PLLVDDL0, PLLVDDL1 Supply Voltage Range		0.95	1.0	1.05	V

13.3. Thermal Characteristics

13.3.1. TQFP 176

13.3.1.1 Assembly Description

Table 49. Assembly Description

Package	Type	E-Pad TQFP-176
	Dimension (L x W)	20 x 20mm
	Thickness	1.0mm
PCB	PCB Dimension (L x W)	130 x 75mm
	PCB Thickness	1.6mm
	Number of Cu Layer-PCB	2-Layer: - Top layer (1oz): 20% coverage of Cu - Bottom layer (1oz): 75% coverage of Cu 4-Layer: - 1st layer (1oz): 20% coverage of Cu - 2nd layer (1oz): 80% coverage of Cu - 3rd layer (1oz): 80% coverage of Cu - 4th layer (1oz): 75% coverage of Cu

13.3.1.2 Material Properties

Table 50. Material Properties

Item		Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	2.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.9
PCB		Cu	400
		FR4	0.2

13.3.1.3 Simulation Conditions

Table 51. Simulation Conditions

Input Power	2.8W
Test Board (PCB)	2L (2S)/4L (2S2P)
Control Condition	Air Flow = 0, 1, 2 m/s

13.3.1.4 Thermal Performance of E-Pad TQFP-176 on PCB Under Still Air Convection

Table 52. Thermal Performance of E-Pad TQFP-176 on PCB Under Still Air Convection

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JB}
4L PCB	25.3	18.2	6.2	15.7
2L PCB	38.2	24.5	6.9	18.8

Note:
θ_{JA}: Junction to ambient thermal resistance
θ_{JB}: Junction to board thermal resistance
θ_{JC}: Junction to case thermal resistance
Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization

13.3.1.5 Thermal Performance of E-Pad TQFP-176 on PCB under Forced Convection

Table 53. Thermal Performance of E-Pad TQFP-176 on PCB Under Forced Convection

	Air Flow (m/s)	0	1	2
4L PCB	θ_{JA}	25.3	22.8	21.8
	Ψ_{JB}	15.7	15.6	15.4
2L PCB	θ_{JA}	38.2	34.9	33
	Ψ_{JB}	18.8	18.7	18.4

13.3.2. LQFP-128

13.3.2.1 Assembly Description

Table 54. Assembly Description

Package	Type	E-Pad LQFP128
	Dimension (L x W)	14 x 20 mm
	Thickness	1.4 mm
PCB	PCB Dimension (L x W)	130 x 75mm
	PCB Thickness	1.6 mm
	Number of Cu Layer-PCB	2-Layer: - Top layer (1oz): 20% coverage of Cu - Bottom layer (1oz): 75% coverage of Cu 4-Layer: - 1st layer (1oz): 20% coverage of Cu - 2nd layer (1oz): 80% coverage of Cu - 3rd layer (1oz): 80% coverage of Cu - 4th layer (1oz): 75% coverage of Cu

13.3.2.2 Material Properties

Table 55. Material Properties

Item		Material	Thermal Conductivity K (W/m-k)
Package	Die	Si	147
	Silver Paste	1033BF	2.5
	Lead Frame	CDA7025	168
	Mold Compound	7372	0.88
PCB		Cu	400
		FR4	0.2

13.3.2.3 Simulation Conditions

Table 56. Simulation Conditions

Input Power	2.6W
Test Board (PCB)	2L (2S)/4L (2S2P)
Control Condition	Air Flow = 0, 1, 2 m/s

13.3.2.4 Thermal Performance of E-Pad LQFP-128 on PCB under Still Air Convection

Table 57. Thermal Performance of E-Pad LQFP-128 on PCB under Still Air Convection

	θ_{JA}	θ_{JB}	θ_{JC}	Ψ_{JT}	Ψ_{JB}
4L PCB	18.2	8.2	7.5	2.5	8.8
2L PCB	30.1	10.0	8.9	3.4	11

Note:
θ_{JA}: Junction to ambient thermal resistance
θ_{JB}: Junction to board thermal resistance
θ_{JC}: Junction to case thermal resistance
Ψ_{JT}: Junction to top center of package thermal characterization
Ψ_{JB}: Junction to bottom surface center of PCB thermal characterization

13.3.2.5 Thermal Performance of E-Pad LQFP-128 on PCB under Forced Convection

Table 58. Thermal Performance of E-Pad LQFP-128 on PCB under Forced Convection

	Air Flow (m/s)	0	1	2
4L PCB	θ_{JA}	18.2	15.2	14.2
	Ψ_{JT}	2.5	2.8	3.5
	Ψ_{JB}	8.8	8.6	8.3
2L PCB	θ_{JA}	30.1	25.9	24.2
	Ψ_{JT}	3.4	4.5	5.6
	Ψ_{JB}	11	10.7	10.5

13.4. DC Characteristics

Table 59. DC Characteristics

Parameter	SYM	Min	Typical	Max	Units
Power Supply Current for GMII0 DVDDIO_0 (3.3V) (For General Purpose Interface)	I_{DVDDIO_0}	-	56	-	mA
Power Supply Current for GMII1 DVDDIO_1 (3.3V) (For General Purpose Interface)	I_{DVDDIO_1}	-	56	-	mA
Power Supply Current for RGMII0 DVDDIO_0 (2.5V) (For General Purpose Interface)	I_{DVDDIO_0}	-	32	-	mA
Power Supply Current for RGMII1 DVDDIO_1 (2.5V) (For General Purpose Interface)	I_{DVDDIO_1}	-	32	-	mA
System Idle (No UTP Port Link Up, 1 System Power LED)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	55	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	282	-	mA
Total Power Consumption for All Ports	PS	-	464	-	mW
1000M Active (8 UTP Ports Link Up, 1 System Power LED, 8 Activity LEDs, 8 Speed LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	391	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	1301	-	mA
Total Power Consumption for All Ports	PS	-	2591	-	mW
100M Active (8 UTP Ports Link Up, 1 System Power LED, 8 Activity LEDs, 8 Speed LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	261	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	467	-	mA
Total Power Consumption for All Ports	PS	-	1328	-	mW
10M Active (8 UTP Ports Link Up, 1 System Power LED, 8 Activity LEDs)					
Power Supply Current for VDDH	I_{DVDDIO}, I_{AVDDH}	-	370	-	mA
Power Supply Current for VDDL	I_{DVDDL}, I_{AVDDL}, $I_{PLLVDDL}$	-	291	-	mA
Total Power Consumption for All Ports	PS	-	1512	-	mW
VDDIO=3.3V					
TTL Input High Voltage	V_{ih}	1.9	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.7	V
Output High Voltage	V_{oh}	2.7	-	-	V
Output Low Voltage	V_{ol}	-	-	0.6	V
VDDIO=2.5V					
TTL Input High Voltage	V_{ih}	1.7	-	-	V
TTL Input Low Voltage	V_{il}	-	-	0.7	V
Output High Voltage	V_{oh}	2.25	-	-	V
Output Low Voltage	V_{ol}	-	-	0.4	V

Note1: DVDDIO=3.3V, AVDDH=3.3V, DVDDIO_0=3.3V, DVDDIO_1=3.3V, DVDDL=1.0V, AVDDL=1.0V PLLVDDL=1.0V.

Note2: Both I_{DVDDIO_0} & I_{DVDDIO_1} should be added to the total current consumption when the dual extension ports of the RTL8370M are enabled.

13.5. AC Characteristics

13.5.1. EEPROM SMI Host Mode Timing Characteristics

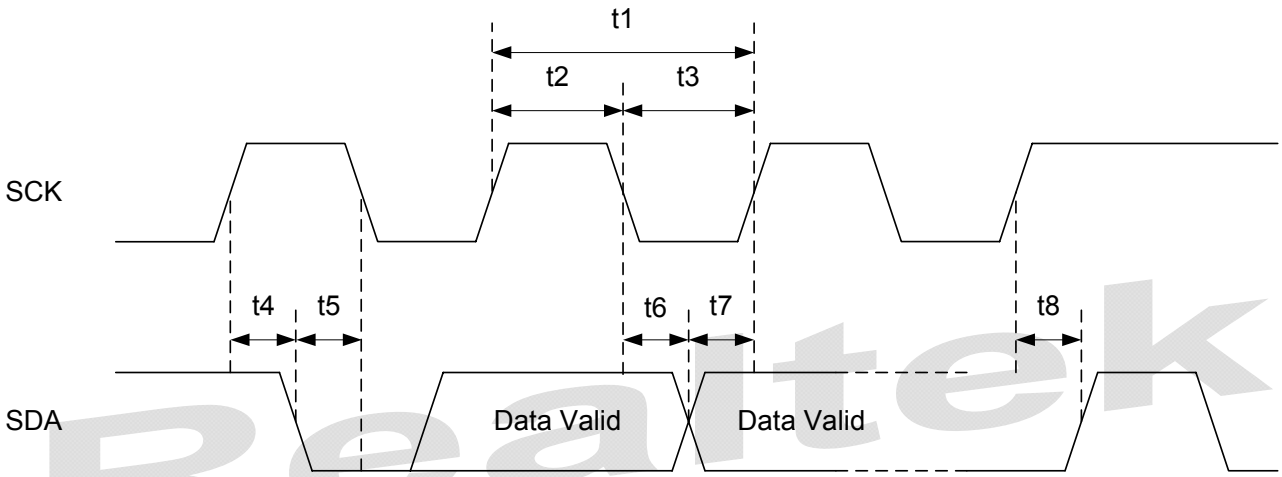


Figure 22. EEPROM SMI Host Mode Timing Characteristics

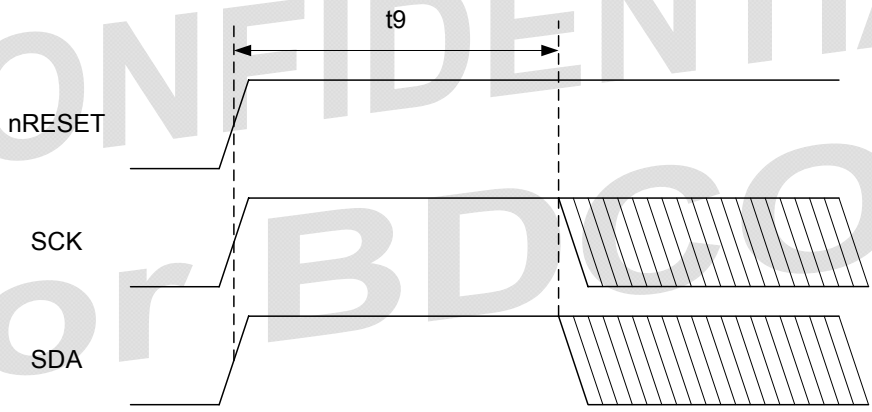


Figure 23. SCK/SDA Power on Timing

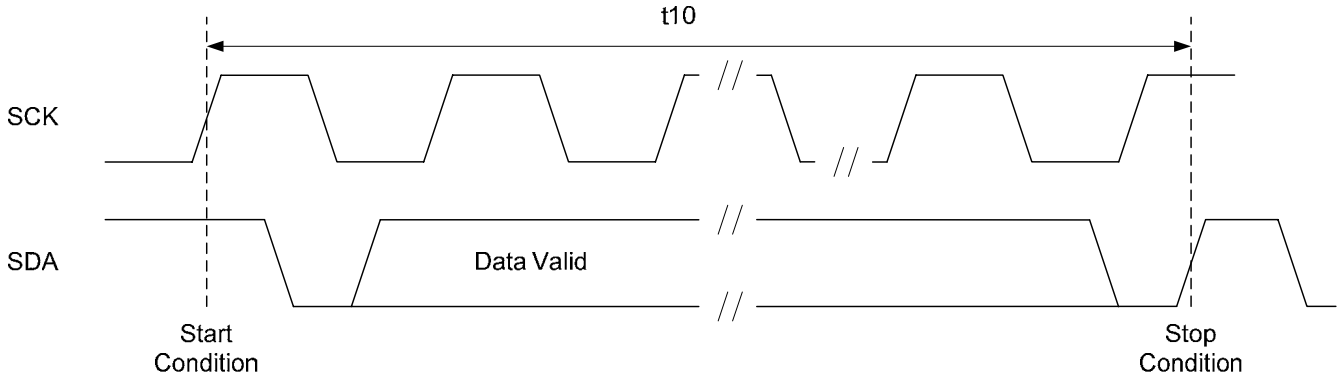


Figure 24. EEPROM Auto-Load Timing

Table 60. EEPROM SMI Host Mode Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK Clock Period	O	4.7	5.04	-	µs
t2	SCK High Time	O	1.7	2.52	-	µs
t3	SCK Low Time	O	1.7	2.52	-	µs
t4	START Condition Setup Time	O	2.2	2.54	-	µs
t5	START Condition Hold Time	O	2.2	2.5	-	µs
t6	Data Hold Time	O	1	1.24	-	µs
t7	Data Setup Time	O	1	1.28	-	µs
t8	STOP Condition Setup Time	O	2.2	2.6	-	µs
t9	SCK/SDA Active from Reset Ready	O	100	105.6	-	ms
t10	8K-bits EEPROM Auto-Load Time	O	120	124.8	-	ms
-	SCK Rise Time (10% to 90%)	O	-	0.7	1.0	ns
-	SCK Fall Time (10% to 90%)	O	-	0.7	1.0	ns
-	Duty Cycle	O	40	50	60	%

Note: t6, t7, and t10 are measured with the ATMEL AT24C08 EEPROM.

13.5.2. EEPROM SMI Slave Mode Timing Characteristics

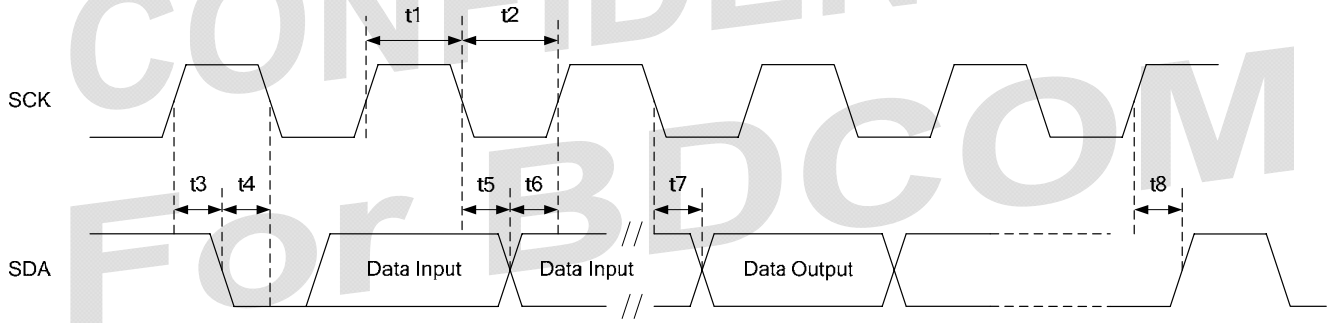


Figure 25. EEPROM SMI Slave Mode Timing Characteristics

Table 61. EEPROM SMI Slave Mode Timing Characteristics

Symbol	Description	Type	Min	Typical	Max	Units
t1	SCK High Time	I	4.0	-	-	µs
t2	SCK Low Time	I	4.0	-	-	µs
t3	START Condition Setup Time	I	4.0	-	-	µs
t4	START Condition Hold Time	I	4.0	-	-	µs
t5	Data Hold Time	I	5.0	-	-	µs
t6	Data Setup Time	I	250	-	-	ns
t7	Clock to Data Output Delay	O	-	100	-	ns
t8	STOP Condition Setup Time	I	4.0	-	-	µs

13.5.3. MDIO Slave Mode Timing Characteristics

The RTL8370(M) supports MDIO slave mode. The Master (the RTL8370(M) link partner CPU) can access the Slave (RTL8370(M)) registers via the MDIO interface. The MDIO is a bi-directional signal that can be sourced by the Master or the Slave. In a write command, the Master sources the MDIO signal. In a read command, the Slave sources the MDIO signal.

- The timing characteristics (t1, t2, and t3 in Table 62) of the Master (the RTL8370(M) link partner CPU) are provided by the Master when the Master sources the MDIO signal (Write command)
- The timing characteristics (t4 in Table 62)of the Slave (RTL8370(M)) are provided by the RTL8370(M) when the RTL8370(M) sources the MDIO signal (Read command)

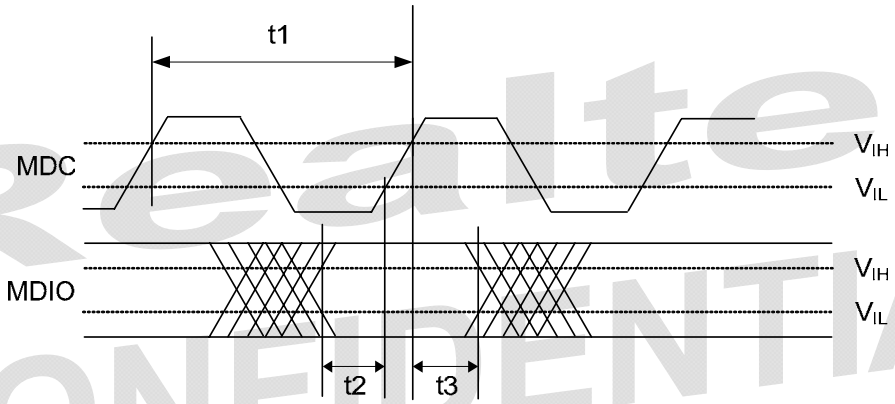


Figure 26. MDIO Sourced by Master (RTL8370(M) Link Partner CPU)

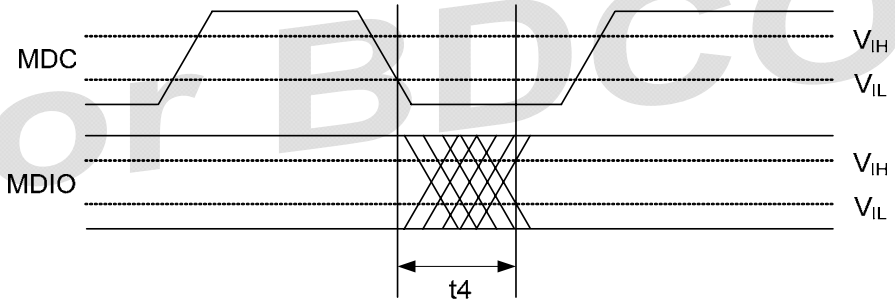


Figure 27. MDIO Sourced by Slave (RTL8370(M))

Table 62. MDIO Timing Characteristics and Requirements

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
MDC Clock Period	t1	Clock Period	I	125	-	-	ns
MDIO to MDC Rising Setup Time (Write Data)	t2	Input Setup Time	I	26	-	-	ns
MDIO to MDC Rising Hold Time (Write Data)	t3	Input Hold Time	I	26	-	-	ns
MDC to MDIO Delay Time (Read Data)	t4	Clock (Falling Edge) to Data Delay Time	O	0	-	40	ns

13.5.4. GMII Timing Characteristics

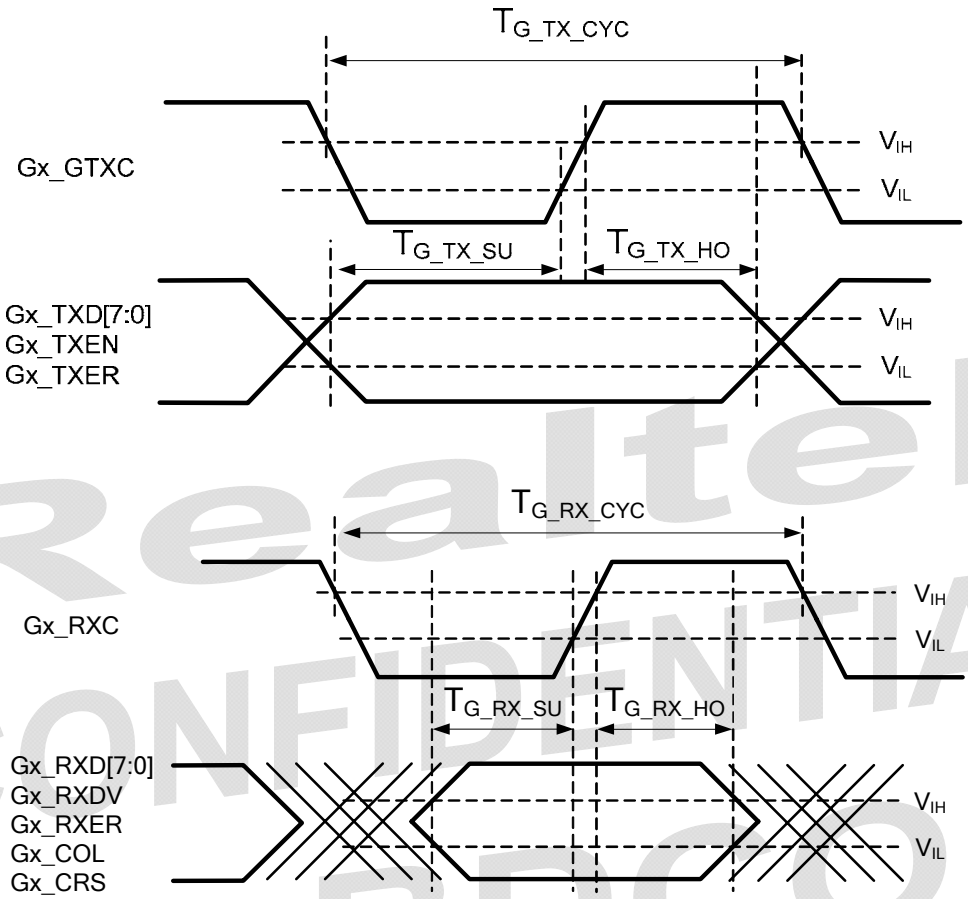


Figure 28. GMII Timing Characteristics

Table 63. GMII Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
1000Base-T Gx_GTXC Output Cycle Time	$T_{G\_TX\_CYC}$	125MHz Clock Output	O	7.5	8.0	8.4	ns
1000Base-T Gx_RXC Input Cycle Time	$T_{G\_RX\_CYC}$	125MHz Clock Input	I	7.5	-	-	ns
1000Base-T Gx_TXD[7:0], Gx_TXER, Gx_TXEN to Gx_GTXC Output Setup Time	$T_{G\_TX\_SU}$	-	O	1	-	-	ns
1000Base-T Gx_TXD[7:0], Gx_TXER, Gx_TXEN to Gx_GTXC Output Hold Time	$T_{G\_TX\_HO}$	-	O	0.5	-	-	ns
1000Base-T Gx_RXD[7:0], Gx_RXDV, Gx_RXER, Gx_CRS, Gx_COL to Gx_RXC Input Setup Time	$T_{G\_RX\_SU}$	-	I	0.9	-	-	ns
1000Base-T Gx_RXD[7:0], Gx_RXDV, Gx_RXER, G0_CRS, Gx_COL to Gx_RXC Input Hold Time	$T_{G\_RX\_HO}$	-	I	0	-	-	ns

13.5.5. MII MAC Mode Timing

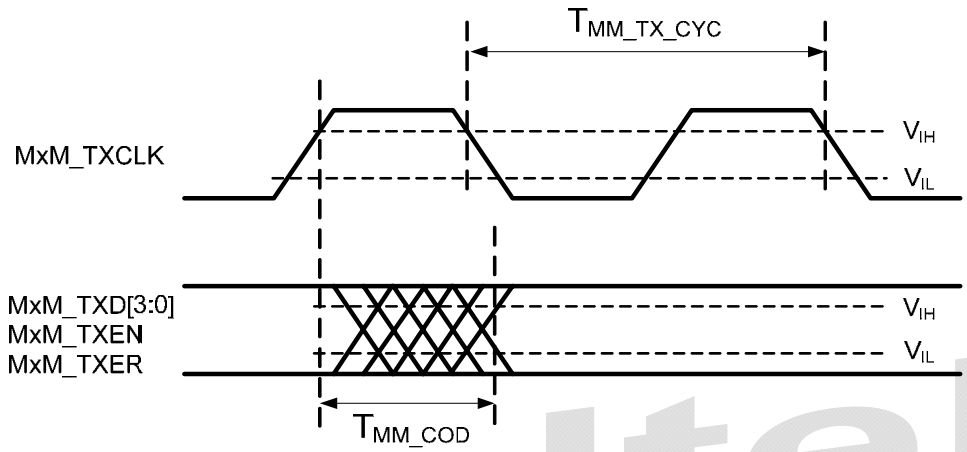


Figure 29. MII MAC Mode Clock to Data Output Delay Timing

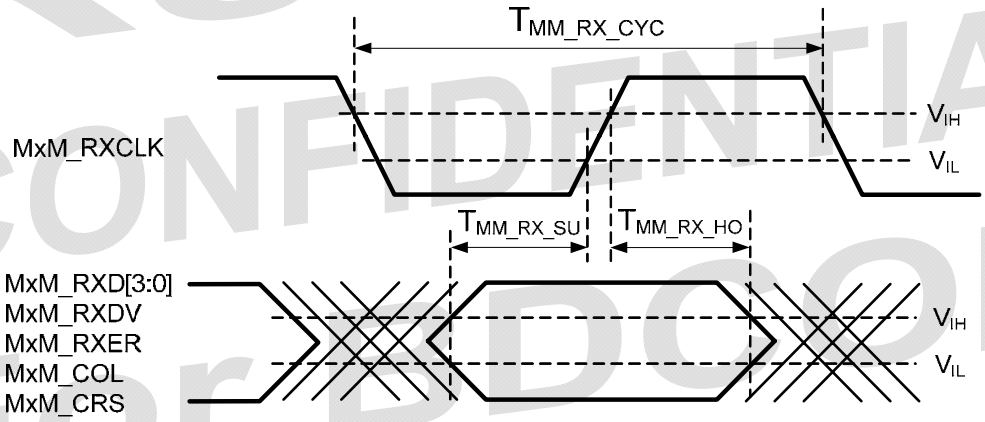


Figure 30. MII MAC Mode Input Timing

Table 64. MII MAC Mode Timing

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100Base-T MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	25MHz Clock Input.	I	-	40	-	ns
10Base-T MxM_TXCLK and MxM_RXCLK Input Cycle Time	$T_{MM\_TX\_CYC}$ $T_{MM\_RX\_CYC}$	2.5MHz Clock Input.	I	-	400	-	ns
MxM_TXCLK to MxM_TXD[3:0], MxM_TXEN, and MxM_TXER Output Delay Time	T_{MM_COD}	-	O	-	4.6	-	ns
MxM_RXD[3:0], MxM_RXDV, MxM_RXER, MxM_COL, and MxM_CRS Input Setup Time	$T_{MM\_RX\_SU}$	-	I	10	-	-	ns
MxM_RXD[3:0], MxM_RXDV, MxM_RXER, MxM_COL, and MxM_CRS Input Hold Time	$T_{MM\_RX\_HO}$	-	I	10	-	-	ns

13.5.6. MII PHY Mode Timing

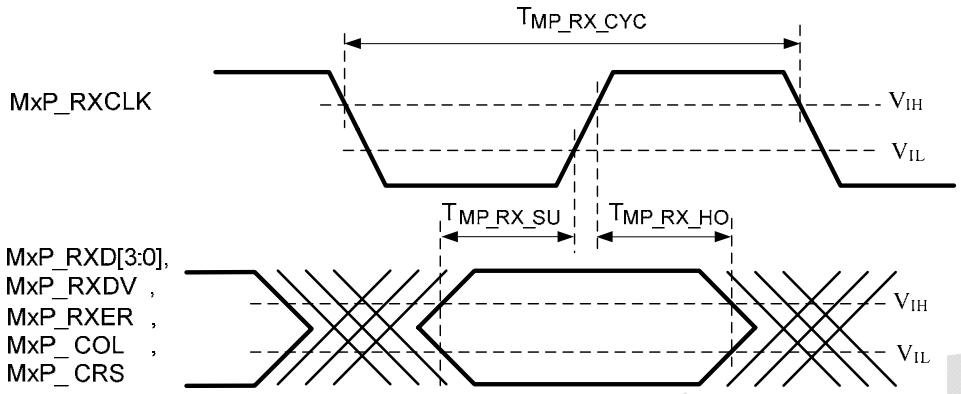


Figure 31. MII PHY Mode Output Timing

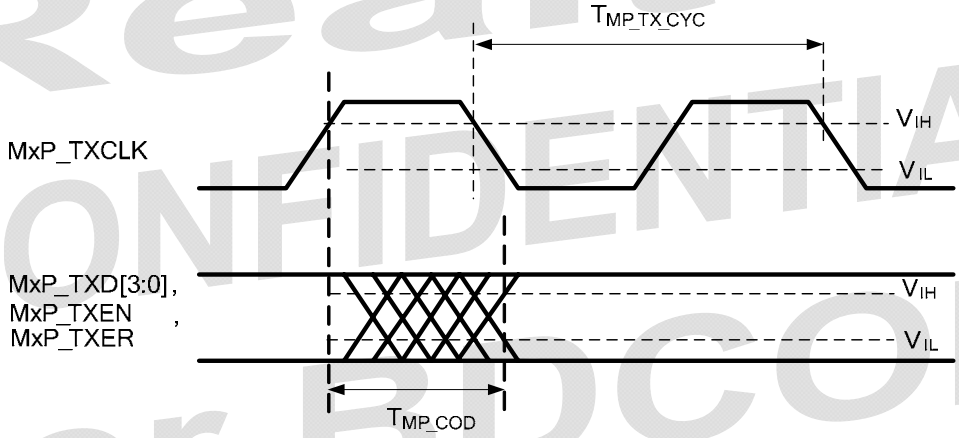


Figure 32. MII PHY Mode Clock Output to Data Input Delay Timing

Table 65. MII PHY Mode Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
100M MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	25MHz Clock Output.	O	-	40	-	ns
10M MxP_RXCLK and MxP_TXCLK Output Cycle Time	$T_{MP\_RX\_CYC}$ $T_{MP\_TX\_CYC}$	2.5MHz Clock Output.	O	-	400	-	ns
100M MxP_RXD[3:0], MxP_RXDV, MxP_RXER, MxP_COL, and MxP_CRS to MxP_RXCLK Output Setup Time	$T_{MP\_RX\_SU}$	-	O	-	19.2	-	ns
100M MxP_RXD[3:0], MxP_RXDV, MxP_RXER, MxP_COL, and MxP_CRS to MxP_RXCLK Output Hold Time	$T_{MP\_RX\_HO}$	-	O	-	20.4	-	ns
100M MxP_TXCLK Clock Output to MxP_TXD[3:0], MxP_TXEN and MxP_TXER Input Delay Time	T_{MP_COD}	-	I	0	-	25	ns

13.5.7. RGMII Timing Characteristics

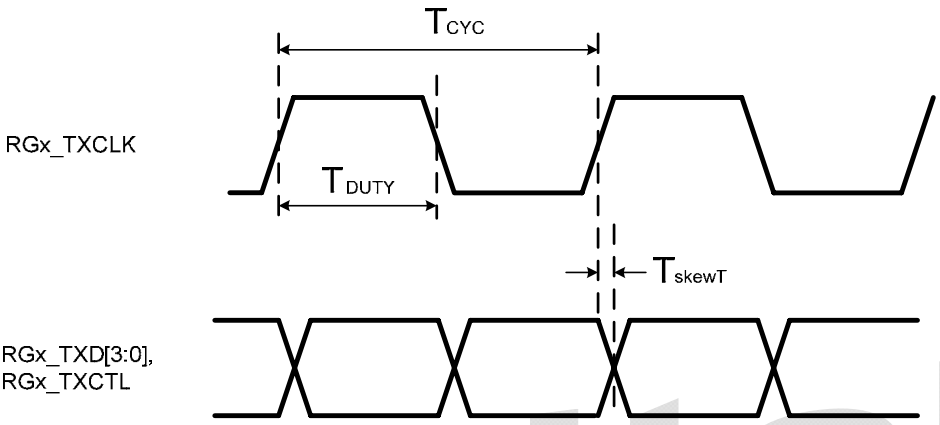


Figure 33. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=0)

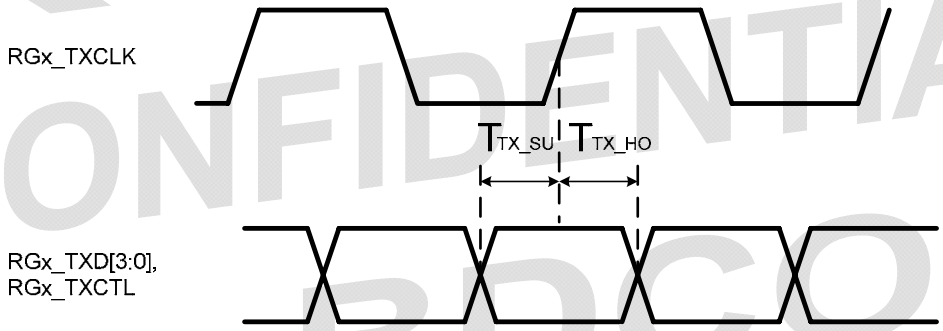


Figure 34. RGMII Output Timing Characteristics (RGx_TXCLK_DELAY=2ns)

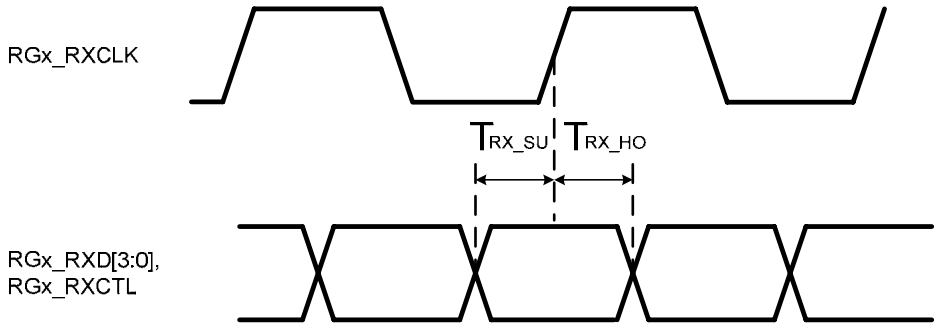


Figure 35. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=0)

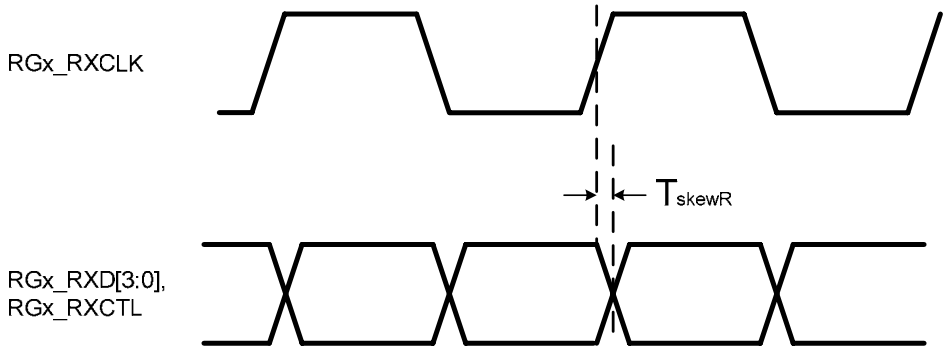


Figure 36. RGMII Input Timing Characteristics (RGx_RXCLK_DELAY=2ns)

Table 66. RGMII Timing Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
1000M RGx_TXCLKc Output Cycle Time	T_{TX_CYC}	125MHz Clock Output. Refer to Figure 33, page 88.	O	7.7	8	8.3	ns
100M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	25MHz Clock Output. Refer to Figure 33, page 88.	O	38	40	42	ns
10M RGx_TXCLK Output Cycle Time	T_{TX_CYC}	2.5MHz Clock Output. Refer to Figure 33, page 88.	O	380	400	420	ns
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Skew	T_{skewT}	Disable Output Clock Delay. (RGx_TXCLK_DELAY=0). Refer to Figure 33, page 88.	O	-500	-140	500	ps
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Setup Time	T_{TX_SU}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1). Refer to Figure 34, page 88.	O	1.2	2.0	-	ns
RGx_TXD[3:0] and RGx_TXCTL to RGx_TXCLK Output Hold Time	T_{TX_HO}	Enable Output Clock Delay. (RGx_TXCLK_DELAY=1). Refer to Figure 34, page 88.	O	1.2	1.8	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Setup Time	T_{RX_SU}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0). Refer to Figure 35, page 88.	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Hold Time	T_{RX_HO}	Disable Input Clock Delay. (RGx_RXCLK_DELAY=0). Refer to Figure 35, page 88.	I	1.0	-	-	ns
RGx_RXD[3:0] and RGx_RXCTL to RGx_RXCLK Input Skew	T_{skewR}	Enable Input Clock Delay. (RGx_RXCLK_DELAY=1). Refer to Figure 36, page 89.	I	-600	-	600	ps

13.6. Power and Reset Characteristics

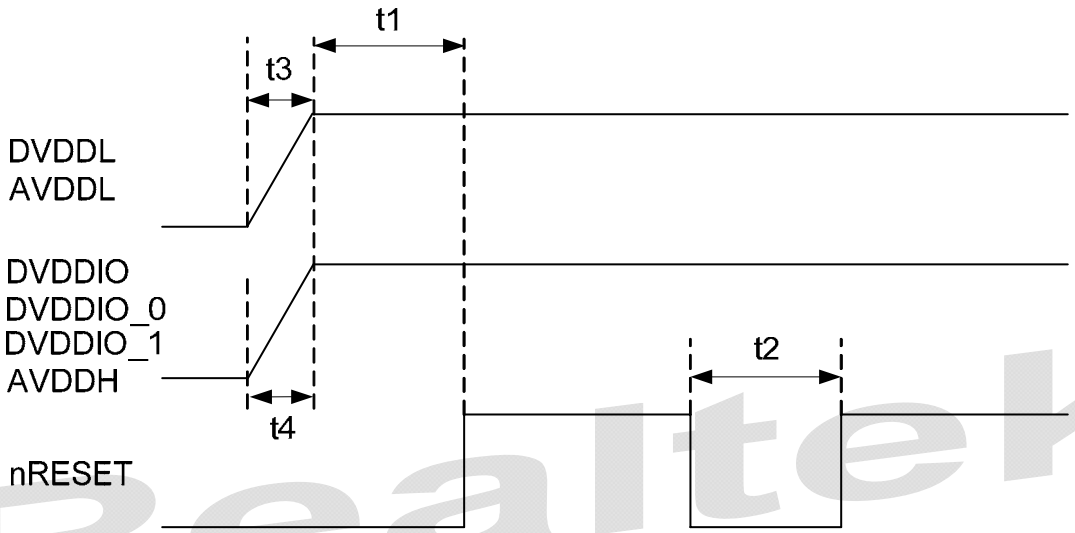


Figure 37. Power and Reset Characteristics

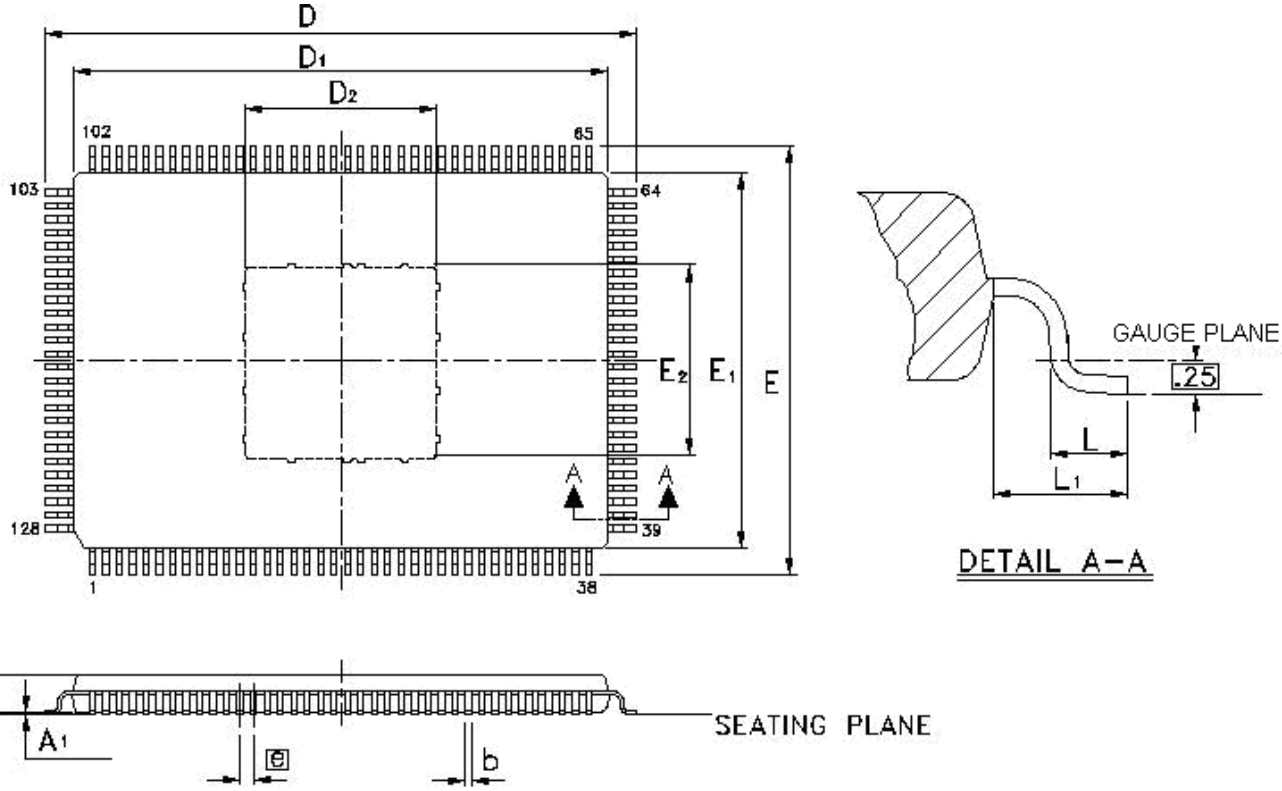
Table 67. Power and Reset Characteristics

Parameter	SYM	Description/Condition	Type	Min	Typical	Max	Units
Reset Delay Time	t1	The duration from all powers steady to the reset signal released to high.	I	10	-	-	ms
Reset Low Time	t2	The duration of reset signal remain low time for issuing a reset to RTL8370(M).	I	10	-	-	ms
VDDL Power Rising Settling Time	t3	DVDDL and AVDDL power rising settling time.	I	1	-	-	ms
VDDH Power Rising Settling Time	t4	DVDDIO, DVDDIO_0, DVDDIO_1, and AVDDH power rising settling time.	I	1	-	-	ms

14. Mechanical Dimensions

14.1. RTL8370: LQFP 128-Pin E-PAD Package

Thermally Enhanced Low-profile Quad Flat Package (LQFP) 128 Leads 14x20mm Outline.

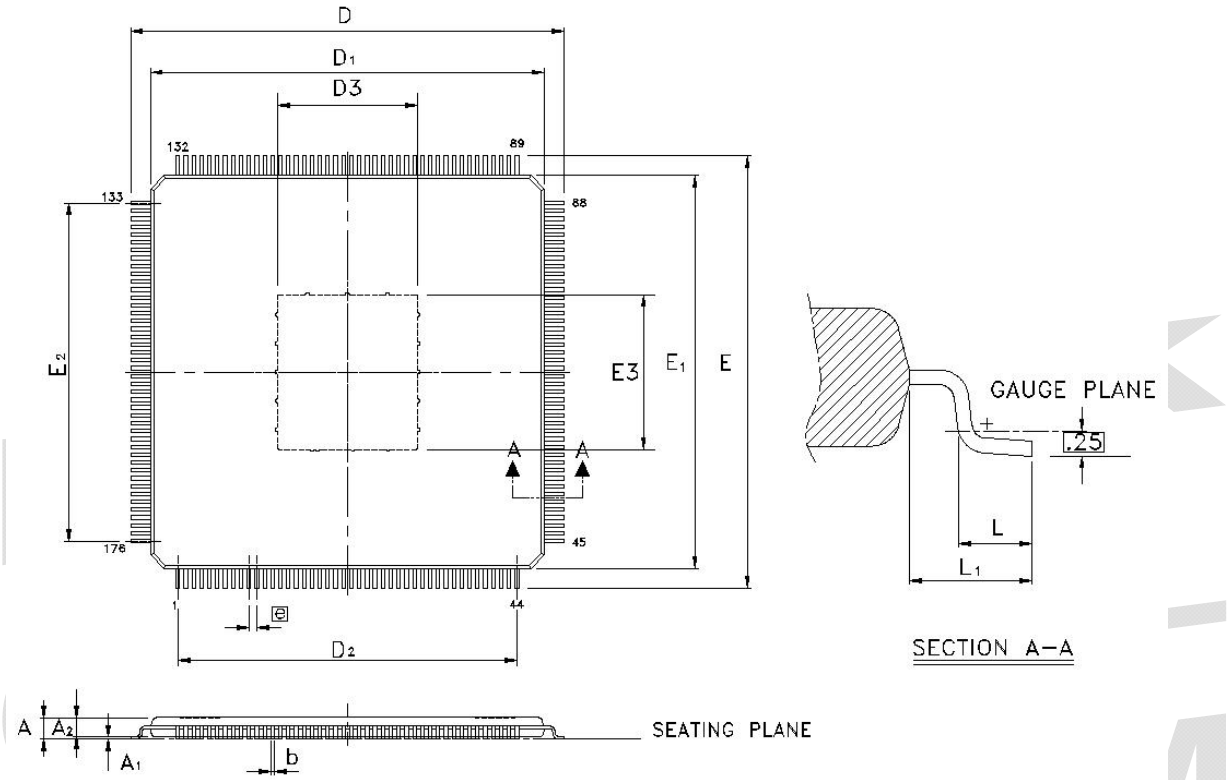


Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.60	-	-	0.063
A_1	0.05	-	0.15	0.002	-	0.006
A_2	1.35	1.40	1.45	0.053	0.055	0.057
b	0.17	0.2	0.27	0.007	0.009	0.011
D	22.00BSC			0.866BSC		
D_1	20.00BSC			0.787BSC		
D_2	-	6.60	-	-	0.260	-
E	16.00BSC			0.630BSC		
E_1	14.00BSC			0.551BSC		
E_2	-	6.10	-	-	0.240	-
e	0.50BSC			0.020BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-26.

14.2. RTL8370M: TQFP176-Pin E-PAD Package

Thermally Enhanced Thin Quad Flat Pack (TQFP) 176 Leads 20x20mm Outline.



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	-	-	1.20	-	-	0.047
A_1	0.05	-	0.15	0.002	-	0.006
A_2	0.95	1.00	1.05	0.037	0.039	0.041
b	0.13	0.18	0.23	0.005	0.007	0.009
D	22.00BSC			0.866BSC		
D_1	20.00BSC			0.787BSC		
D_2	17.20BSC			0.677BSC		
D_3	-	6.20	-	-	0.244	-
E	22.00BSC			0.866BSC		
E_1	20.00BSC			0.787BSC		
E_2	17.20BSC			0.677BSC		
E_3	-	6.00	-	-	0.236	-
e	0.40BSC			0.016BSC		
L	0.45	0.60	0.75	0.018	0.024	0.030
L1	1.00REF			0.039REF		

Note 1: CONTROLLING DIMENSION: MILLIMETER (mm).
Note 2: REFERENCE DOCUMENT: JEDEC MS-26.

15. Ordering Information

Table 68. Ordering Information

Part Number	Package	Status
RTL8370-GR	LQFP 128-Pin E-PAD 'Green' Package	-
RTL8370M-GR	TQFP 176-Pin E-PAD 'Green' Package	-

Note 1: RTL8370-GR is for 8-Port Gigabit Switch applications.
Note 2: RTL8370M-GR is for 8-Port Gigabit Router applications.
Note 3: See page 8 (RTL8370-GR) and page 9 (RTL8370M-GR) for package identification.

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