Digital Logic Circuit Experiment Project Report

-Rock Paper Scissors Game Machine-

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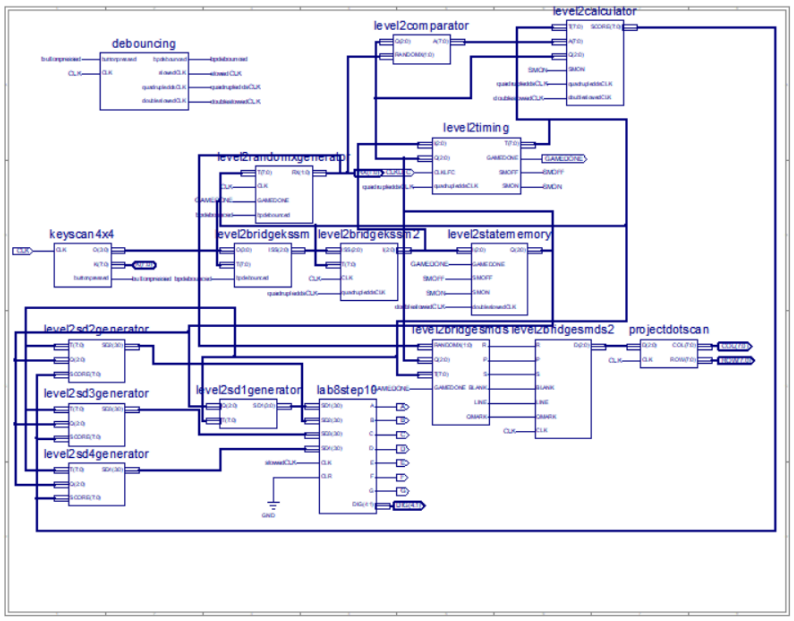
1. Final file, design summary and pin mapping



Schematic diagram

overallstructure Project Status (12/10/2021 - 22:14:57)			
Project File:	overallstructure.xise	**Parser Errors:**	No Errors
Module Name:	overallstructure	**Implementation State:**	Programming File Generated
Target Device:	xc6slx4-3cpg196	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	50 Warnings (5 new)
Design Goal:	Balanced	• **Routing Results:**	All Signals Completely Routed
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	All Constraints Met
Environment:	System Settings	• **Final Timing Score:**	0 (Timing Report)

Device Utilization Summary				
Slice Logic Utilization	**Used**	**Available**	**Utilization**	**Note(s)**
Number of Slice Registers	110	4,800	2%	
Number used as Flip Flops	106			
Number used as Latches	4			
Number used as Latch-thrus	0			
Number used as AND/OR logics	0			
Number of Slice LUTs	162	2,400	6%	
Number used as logic	158	2,400	6%	
Number using O6 output only	102			
Number using O5 output only	38			
Number using O5 and O6	18			
Number used as ROM	0			
Number used as Memory	0	1,200	0%	
Number used exclusively as route-thrus	4			
Number with same-slice register load	0			
Number with same-slice carry load	4			
Number with other load	0			
Number of occupied Slices	72	600	12%	
Number of MUXCYs used	56	1,200	4%	
Number of LUT Flip Flop pairs used	175			
Number with an unused Flip Flop	67	175	38%	
Number with an unused LUT	13	175	7%	
Number of fully used LUT-FF pairs	95	175	54%	

Number of unique control sets	21			
Number of slice register sites lost to control set restrictions	98	4,800	2%	
Number of bonded IOBs	40	106	37%	
Number of LOCed IOBs	40	40	100%	
Number of RAMB16BWERs	0	12	0%	
Number of RAMB8BWERs	0	24	0%	
Number of BUFIO2_2CLKs	0	32	0%	
Number of BUFIO2FB/BUFIO2FB_2CLKs	0	32	0%	
Number of BUFG/BUFGMUXs	2	16	12%	
Number used as BUFGs	2			
Number used as BUFGMUX	0			
Number of DCM/DCM_CLKGENs	0	4	0%	
Number of ILOGIC2/ISERDES2s	0	200	0%	
Number of IODELAY2/IODRP2/IODRP2_MCBs	0	200	0%	
Number of OLOGIC2/OSERDES2s	0	200	0%	
Number of BSCANs	0	4	0%	
Number of BUFHs	0	128	0%	
Number of BUFPLLs	0	8	0%	
Number of BUFPLL_MCBs	0	4	0%	
Number of DSP48A1s	0	8	0%	
Number of ICAPs	0	1	0%	
Number of PCILOGICSEs	0	2	0%	
Number of PLL_ADVs	0	2	0%	
Number of PMVs	0	1	0%	
Number of STARTUPs	0	1	0%	
Number of SUSPEND_SYNCs	0	1	0%	
Average Fanout of Non-Clock Nets	2.96			

Performance Summary

Final Timing Score:	0 (Setup: 0, Hold: 0)	**Pinout Data:**	Pinout Report
Routing Results:	All Signals Completely Routed	**Clock Data:**	Clock Report
Timing Constraints:	All Constraints Met		

Detailed Reports

Report Name	Status	Generated	Errors	Warnings	Infos
Synthesis Report	Current	12 22 16:52:45 2021	0	30 Warnings (5 new)	19 Infos (2 new)
Translation Report	Current	12 22 16:52:52 2021	0	8 Warnings (0 new)	0
Map Report	Current	12 22 16:53:04 2021	0	6 Warnings (0 new)	6 Infos (0 new)
Place and Route Report	Current	12 22 16:53:14 2021	0	0	3 Infos (0 new)
Power Report					
Post-PAR Static Timing Report	Current	12 22 16:53:22 2021	0	0	4 Infos (0 new)
Bitgen Report	Current	12 22 16:53:33 2021	0	6 Warnings (0 new)	0

Secondary Reports

Report Name	Status	Generated
WebTalk Report	Current	12 22 17:00:04 2021
WebTalk Log File	Current	12 22 17:00:05 2021

Date Generated: 12/22/2021 - 17:28:42

Design summary

All ports (40)							
COL (8)	Output			default (LVCM...	2,500	12 SLOW	NONE
COL[7]	Output	L13	☑	1 default (LVCM...	2,500	12 SLOW	NONE
COL[6]	Output	L14	☑	1 default (LVCM...	2,500	12 SLOW	NONE
COL[5]	Output	N12	☑	2 default (LVCM...	2,500	12 SLOW	NONE
COL[4]	Output	P12	☑	2 default (LVCM...	2,500	12 SLOW	NONE
COL[3]	Output	P7	☑	2 default (LVCM...	2,500	12 SLOW	NONE
COL[2]	Output	N6	☑	2 default (LVCM...	2,500	12 SLOW	NONE
COL[1]	Output	N5	☑	2 default (LVCM...	2,500	12 SLOW	NONE
COL[0]	Output	P5	☑	2 default (LVCM...	2,500	12 SLOW	NONE
DIG (4)	Output			3 default (LVCM...	2,500	12 SLOW	NONE
DIG[4]	Output	B1	☑	3 default (LVCM...	2,500	12 SLOW	NONE
DIG[3]	Output	C1	☑	3 default (LVCM...	2,500	12 SLOW	NONE
DIG[2]	Output	D1	☑	3 default (LVCM...	2,500	12 SLOW	NONE
DIG[1]	Output	D2	☑	3 default (LVCM...	2,500	12 SLOW	NONE
K (8)	In/Out			3 default (LVCM...	2,500	12 SLOW	(Multiple)*
K[7]	In/Out	J1	☑	3 default (LVCM...	2,500	12 SLOW	NONE
K[6]	In/Out	J2	☑	3 default (LVCM...	2,500	12 SLOW	NONE
K[5]	In/Out	K1	☑	3 default (LVCM...	2,500	12 SLOW	NONE
K[4]	In/Out	K2	☑	3 default (LVCM...	2,500	12 SLOW	NONE
K[3]	In/Out	L1	☑	3 default (LVCM...	2,500	12 SLOW	PULLDOW...
K[2]	In/Out	L2	☑	3 default (LVCM...	2,500	12 SLOW	PULLDOW...
K[1]	In/Out	M1	☑	3 default (LVCM...	2,500	12 SLOW	PULLDOW...
K[0]	In/Out	M2	☑	3 default (LVCM...	2,500	12 SLOW	PULLDOW...
ROW (8)	Output			1 default (LVCM...	2,500	12 SLOW	NONE
ROW[7]	Output	F13	☑	1 default (LVCM...	2,500	12 SLOW	NONE
ROW[6]	Output	F14	☑	1 default (LVCM...	2,500	12 SLOW	NONE
ROW[5]	Output	H13	☑	1 default (LVCM...	2,500	12 SLOW	NONE
ROW[4]	Output	H14	☑	1 default (LVCM...	2,500	12 SLOW	NONE
ROW[3]	Output	J13	☑	1 default (LVCM...	2,500	12 SLOW	NONE
ROW[2]	Output	J14	☑	1 default (LVCM...	2,500	12 SLOW	NONE
ROW[1]	Output	K13	☑	1 default (LVCM...	2,500	12 SLOW	NONE
ROW[0]	Output	K14	☑	1 default (LVCM...	2,500	12 SLOW	NONE
RX (2)	Output			2 default (LVCM...	2,500	12 SLOW	NONE
RX[1]	Output	P3	☑	2 default (LVCM...	2,500	12 SLOW	NONE
RX[0]	Output	N3	☑	2 default (LVCM...	2,500	12 SLOW	NONE
Scalar ports (10)							
A	Output	G2	☑	3 default (LVCM...	2,500	12 SLOW	NONE
B	Output	G1	☑	3 default (LVCM...	2,500	12 SLOW	NONE
C	Output	H2	☑	3 default (LVCM...	2,500	12 SLOW	NONE
CLK	Input	N8	☑	2 default (LVCM...			NONE
CLKLFC	Input	N7	☑	2 default (LVCM...			NONE
D	Output	H1	☑	3 default (LVCM...	2,500	12 SLOW	NONE
E	Output	F2	☑	3 default (LVCM...	2,500	12 SLOW	NONE
F	Output	F1	☑	3 default (LVCM...	2,500	12 SLOW	NONE
G	Output	E2	☑	3 default (LVCM...	2,500	12 SLOW	NONE
GAMEDONE	Output	G14	☑	1 default (LVCM...	2,500	12 SLOW	NONE

Pin mapping

2. Module-level Functionality

(1) Keyscan4x4

When a button on a 4x4 key matrix is pressed, it triggers the scan process to determine the number corresponding to the pressed button. Additionally, the fact that a button has been pressed is signaled as "buttonpressed."

(2) Debouncing

The "bouncing" effect in the "buttonpressed" signal is mitigated using two flip-flops in a debounce circuit. This circuit ensures that a stable signal is generated without noise or multiple transitions caused by the button's mechanical bouncing. The debounced signal can then be used to trigger or control signals at various frequencies. (slowedCLK:2^{12}Hz doubleslowedCLK: :2^{7}Hz quadrupleddsCLK: :2^{9}Hz)

(3) Level2timing

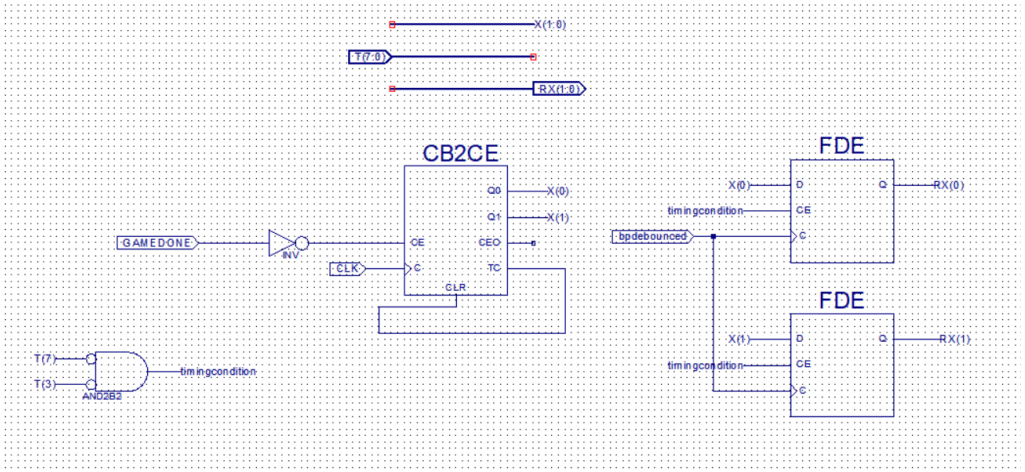
This circuit outputs the time variable T(7:0), and during the game, T(7:0) increases by 1 on the positive edge of CLK_LFC (every 1 second). The operation of the circuit is determined based on the value of T(7:0).

t3t2t1t0	output of Dot
0000~0001	off
0010~0011	R
0100~0101	P
0110~0111	S
1000~1011	off
1100~1111	Result

t6t5t4	output of d1 in 4dig7seg(=the number of games played)
000	5
001	4
010	3

011	2
100	1
101	0

(4) Level2randomxgenerator



This circuit outputs a random x using a 2-bit counter

How to determine the random variable "x":

A CLK signal with a frequency of 223Hz is connected to "CB2CE" as the clock input "C."

"CB2CE" generates an output "TC" (T7T6T5T4T3T2T1T0) that is connected to the CLR (Clear) input.

When "TC" reaches a value of 11 (binary Q1=1, Q0=1), the circuit is reset. This reset condition ensures that the circuit restarts when "TC" reaches 11.

The outputs "x1" and "x0" of "CB2CE" are connected to the inputs of two Flip-Flop D-Elements (FDE).

Each FDE has a CE (Clock Enable) and a C (Clock) input. CE is set as CE = T7'T3' and C = bpdebounced. This means that when a button is pressed during each of the five games, while "R," "P," and "S" are sequentially displayed on the screen, the values of "x1" and "x0" at the moment the button is pressed determine the values of "RX1" and "RX0."

The mappings change according to the values of "RX1" and "RX0" as follows:

If RX1RX0 = 00, it corresponds to "R."

If RX1RX0 = 01, it corresponds to "P."

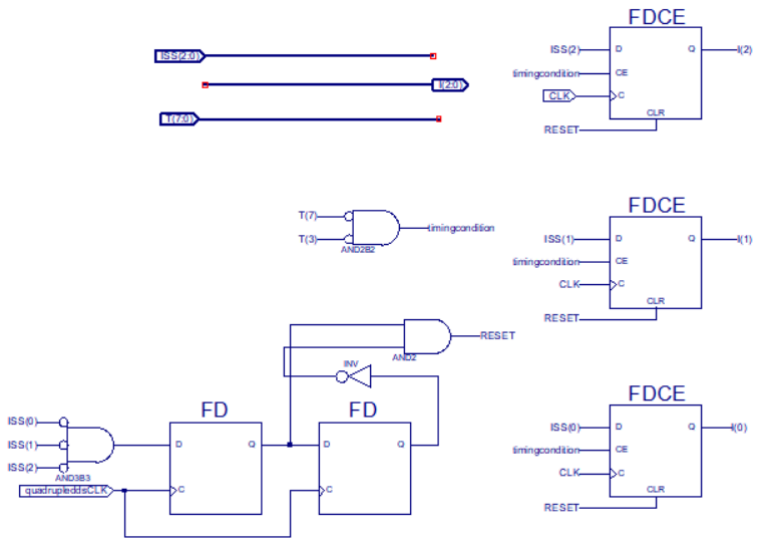
If RX1RX0 = 10, it corresponds to "S."

In essence, the circuit generates a random variable "x" based on the moment a button is pressed during the game, and this random variable corresponds to the game outcomes "R," "P," or "S."

(5) Level2bridgekssm1, 2

These two circuits serve to convert the output "O(3:0)" of the keyscan into "I(2:0)." The signal "I(2:0)" is then input into the "statememory" to determine the state of the circuit, represented by "Q(2:0)."

The condition "T7'T3'T2'T1'T0=1" is connected to the CLR input of each FDCE in "bridgekssm1." Therefore, one second after the start of each game, "I(2:0)=110" is set, which signifies the state of 'nothing has been pressed.'



How to apply a time limit:

In the "bridgekssm2" circuit, the CE (Clock Enable) of each FDCE is set as CE = T7'T3'. Therefore, during each round of the game when "R," "P," or "S" is displayed on the screen, only the button presses that occur during that time are reflected in "I." Button presses that occur after the game screen changes are not taken into account.

If no buttons are pressed during the time "R," "P," or "S" is displayed on the screen, "I" will maintain the value "110" (signifying that nothing has been pressed) until the end of that particular game round.

(6) Level2statememory

The transition table for this circuit, which determines the output Q(2:0) representing the state of the circuit based on the input I, is provided below.

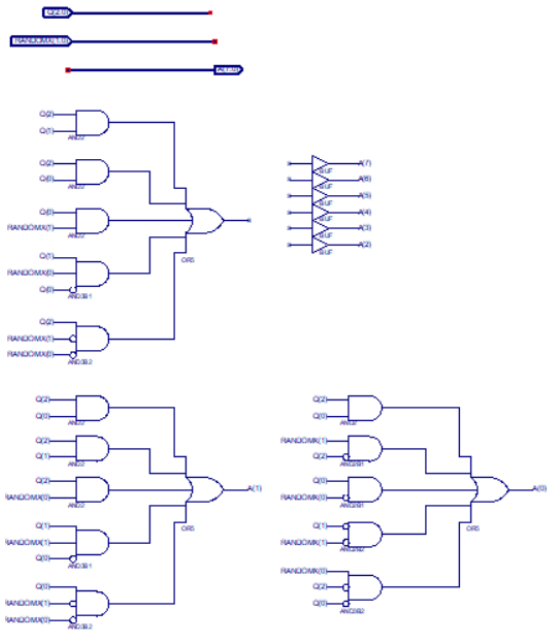
State	Q2Q1Q0	Q2*Q1*Q0*							
		I=000	001	011	010	100	101	111	110
		reset	start	P	R	S	other	illegal	none
OFF	000	000	001	000	000	000	000	xxx	000
ON	001	000	101	011	010	100	101	xxx	110
PA	011	000	101	011	010	100	101	xxx	110
RO	010	000	101	011	010	100	101	xxx	110
SCI	100	000	101	011	010	100	101	xxx	110
OTH	101	000	101	011	010	100	101	xxx	110
NULL	111	xxx	xxx	xxx	xxx	xxx	xxx	xxx	xxx
NONE	110	000	101	011	010	100	101	xxx	110

(7) Level2bridgesmds1, 2, Projectdotscan

형태	D2D1D0	col0	col1	col2	col3	col4	col5	col6	col7
None	000	00	00	00	00	00	00	00	00
Rock	001	00	18	3C	7E	7E	3C	18	00
Paper	010	F8	FF	E0	FF	E0	FF	E0	FF
Scissor	011	80	40	5F	30	30	5F	40	80
Question mark	100	00	06	05	A1	B1	1F	0E	00
Solid line	101	18	18	18	18	18	18	18	18
None	110	00	00	00	00	00	00	00	00
None	111	00	00	00	00	00	00	00	00

The "Bridgesmds1" and "Bridgesmds2" circuits operate based on the time "T," the comparison of "Q(2:0)," and "RX(1:0)." They generate an output "D(2:0)" that represents the picture to be displayed on the dot matrix. This "D(2:0)" value is then passed to the "projectdotscan," which is responsible for displaying the corresponding picture on the dot matrix. The "projectdotscan" circuit takes the "D(2:0)" value and uses it to determine which picture to display on the dot matrix.

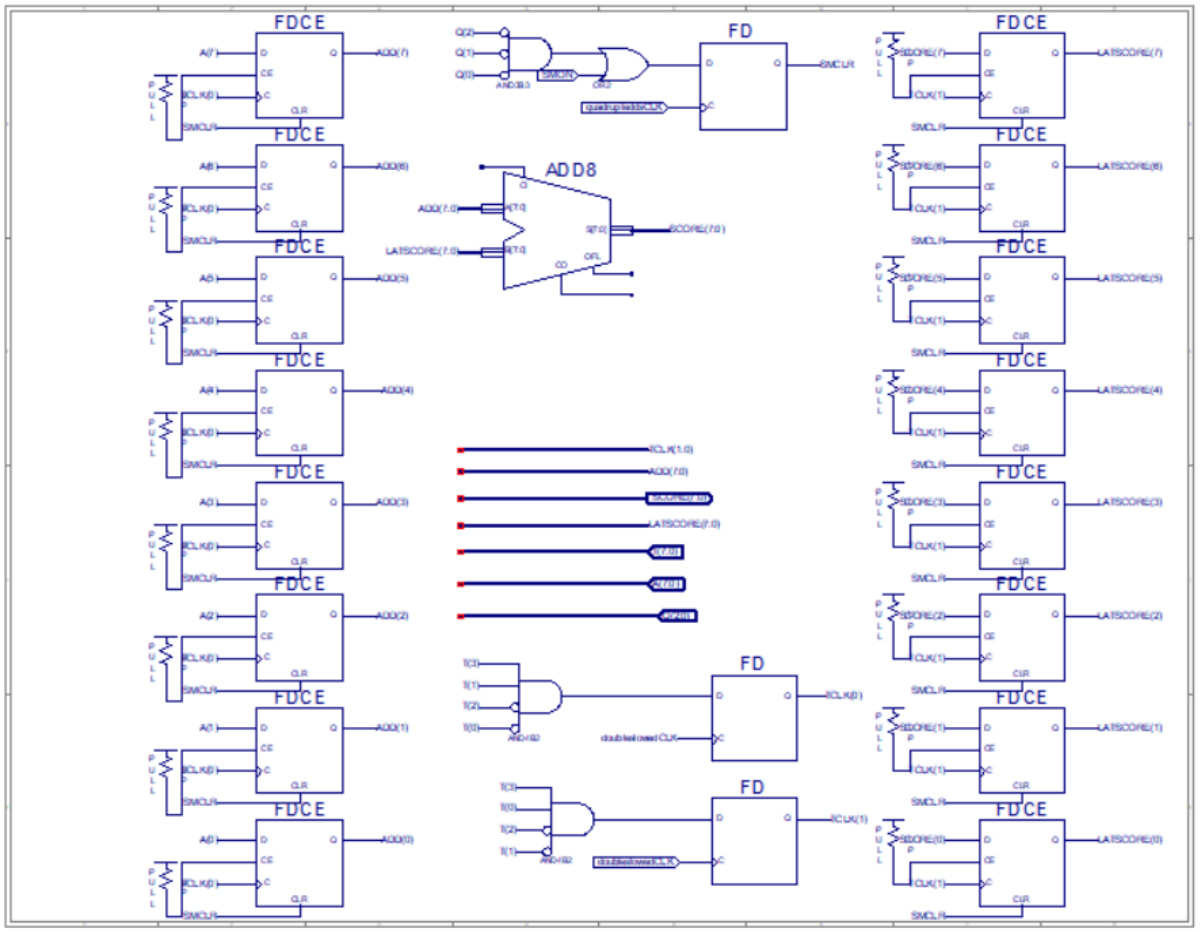
(8) Level2comparator



Q2Q1Q0	RX1RX0	Result	Score		
			Decimal	A7A6A5A4	A3A2A1A0
010	00	Tie	0	0000	0000
	01	Loss	-3	1111	1101
	10	Victory	+3	0000	0011
011	00	Victory	+3	0000	0011
	01	Tie	0	0000	0000
	10	Loss	-3	1111	1101
100	00	Loss	-3	1111	1101
	01	Victory	+3	0000	0011
	10	Tie	0	0000	0000
101	XX	Leftfield	-1	1111	1111
110	XX	Retirement	-2	1111	1110

To determine a win or draw, the comparison between "Q(2:0)" and "RX(1:0)" is used. Based on this comparison, the result is determined, and the score, represented by "A(7:0)," is generated as an output. The specific logic for comparing these values and determining the result is detailed in the provided table.

(9) Level2calculator



The scoring is calculated as follows:

The "Calculator" circuit receives the score for each round, represented as "A(7:0)," from the "Comparator" circuit. For each round, at T=10 seconds, the "Calculator" circuit inputs the score "A(7:0)" into "ADD8" to perform addition. The result from "ADD8" is "SCORE(7:0)." This score is input to "ADD8" again at T=9 seconds for each round, allowing the scores from each round to accumulate continuously. This process ensures that the scores are cumulative across rounds, and the total score is maintained.

(10) Level2sd1generator, Level2sd2generator

These circuits determine the outputs SD1(3:0) and SD2(3:0) for the first and second digits (d1 and d2) of the 4-digit 7-segment display based on the time T and the score Score(7:0).

(11) Level2sd3generator, Level2sd4generator

These circuits convert the score, Score(7:0) calculated in the Calculator circuit into decimal form so that it can be displayed on d3 and d4. Please refer to the following table:

SCORE(7:0)		OUTPUT	
decimal number	binary number	SD3(3:0)	SD4(3:0)
+0	(0000)0000	0000	0000
+1	(0000)0001	0000	0001
+2	(0000)0010	0000	0010
+3	(0000)0011	0000	0011
+4	(0000)0100	0000	0100
+5	(0000)0101	0000	0101
+6	(0000)0110	0000	0110
+7	(0000)0111	0000	0111
+8	(0000)1000	0000	1000
+9	(0000)1001	0000	1001
+10	(0000)1010	0001	0000
+11	(0000)1011	0001	0001
+12	(0000)1100	0001	0010
+13	(0000)1101	0001	0011
+14	(0000)1110	0001	0100
+15	(0000)1111	0001	0101

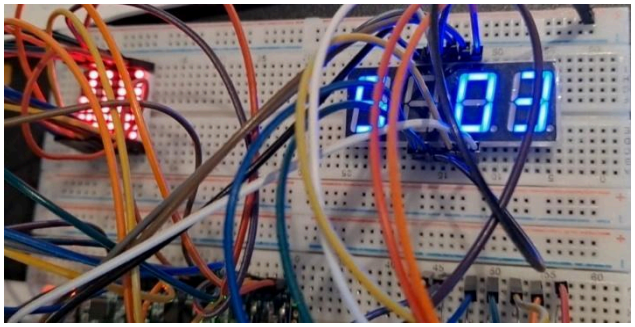
SCORE(7:0)		OUTPUT	
decimal number	binary number	SD3(3:0)	SD4(3:0)
-1	(1111)1111	0000	0001
-2	(1111)1110	0000	0010
-3	(1111)1101	0000	0011
-4	(1111)1100	0000	0100
-5	(1111)1011	0000	0101
-6	(1111)1010	0000	0110
-7	(1111)1001	0000	0111
-8	(1111)1000	0000	1000
-9	(1111)0111	0000	1001
-10	(1111)0110	0001	0000
-11	(1111)0101	0001	0001
-12	(1111)0100	0001	0010
-13	(1111)0011	0001	0011
-14	(1111)0010	0001	0100
-15	(1111)0001	0001	0101

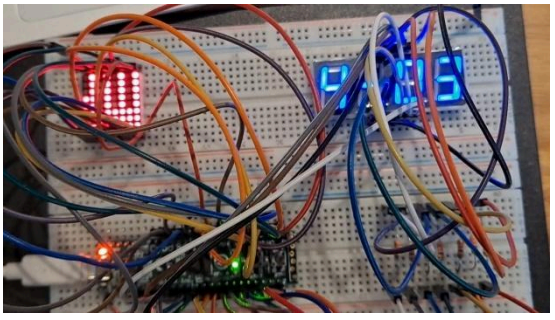
(12) Lab8step10

The received inputs SD4(3:0), SD3(3:0), SD2(3:0), and SD1(3:0) are used with the lut4segment to display the appropriate format on the display. The content stored in Lut4segment is as follows, based on the provided table.

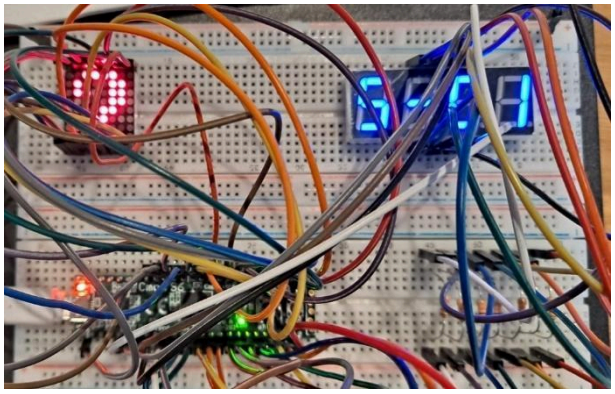
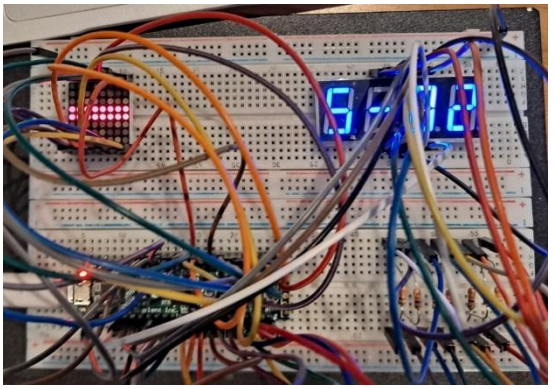
LUT4_a	INIT=1101/0111/1110/1101=D7ED
LUT4_b	INIT=0010/0111/1001/1111=279F
LUT4_c	INIT=0010/1111/1111/1011=2FFB
LUT4_d	INIT=0111/1011/0110/1101=7B6D
LUT4_e	INIT=1111/1101/0100/0101=FD45
LUT4_f	INIT=1101/1111/1111/0001=DFF1
LUT4_g	INIT=1110/1111/0111/1100=EF7C

3. Verification of Operation

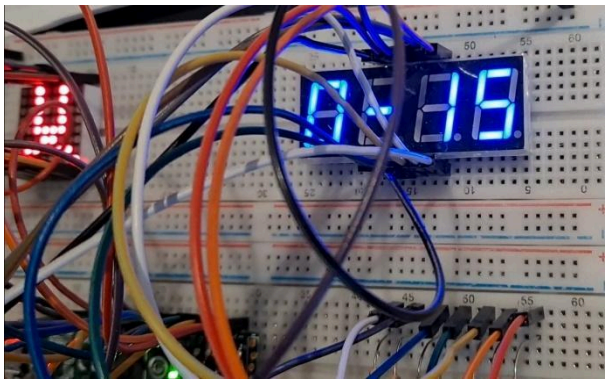
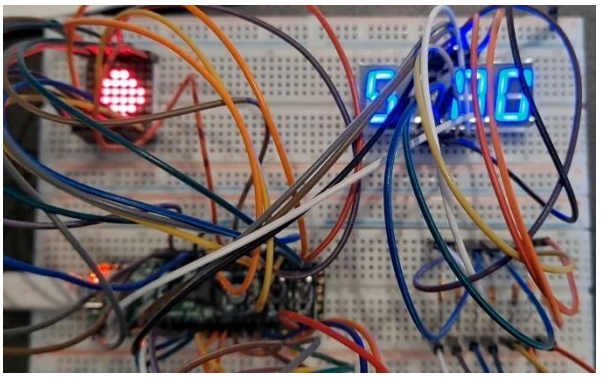




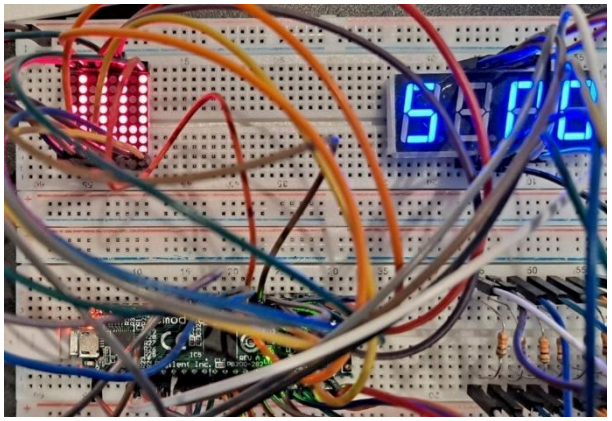
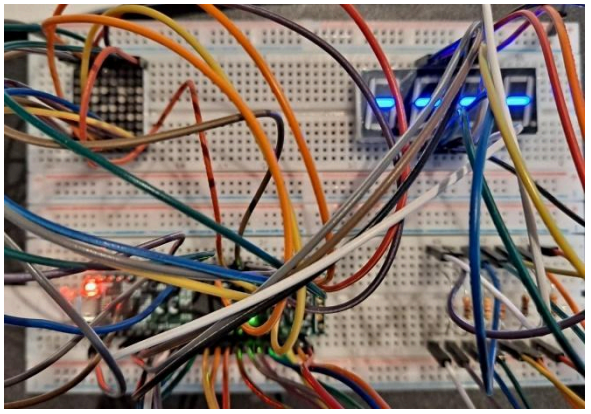
When the player wins in the game (left) and when the player loses in the game (right). The score is displayed correctly.

When a different button is pressed (left) and when no button is pressed within the designated time (right). The score is displayed correctly.

At the end of the game (left) and when the start button is pressed again (right). It works correctly.

While the game is running (left) and when the reset button is pressed (right). The game has been reset correctly.

4. Conclusion

The issue where occasionally unpressed buttons behaved as if they were pressed due to the Keyscan4x4 module's column scan signals K3 to K0 not being pulldown in the Pin mapping has been resolved. After resolving this problem, no other errors have been detected.