ST17H68T

Bluetooth Low Energy (BLE) System on Chip

Key Feature

- 32-bit Low-power Processor with SWD
- Memory
  - 96K ROM
  - 32KB SRAM, all programmable retention in sleep mode
  - 16KB OTP (embedded change pump)
- 3 General Purpose I/O Pins
  - All configurable as serial interface and programmable IO MUX function mapping
  - All pins can be configured for wake-up
  - All pins for triggering interrupt
  - 3 Quadrature Decoder (QDEC)
  - 3-channel PWM
  - I2C
  - 2-channel SPI (a master and a slave)
  - 2-channel UART
  - SWD
- 12-bit ADC
- 4-channel 32-bit Timer, 1 Watchdog Timer
- Real Timer Counter (RTC)
- Power, Clock and Reset Controller
- Flexible Power Management
  - Operating Voltage range 1.8V to 3.6V
  - Embedded LDOs
  - Battery monitor: support low battery
  - Support lithium battery charging
- Power Consumption
  - 2.8 uA@OFF Mode (IO wake up only)
  - 4uA@Sleep Mode with 32KHz RTC
  - Receive Mode: 10mA@3.3V Power Supply
  - Transmit Mode: 10mA (0dBm output power)
- RC Oscillator Hardware Calibrations
  - 32KHz RC osc for RTC with +/-200ppm accuracy
  - 32MHz RC osc for HCLK with 3% accuracy
- High Speed Throughput
  - Support BLE 2Mbps Protocol
  - Support Data Length Extension
  - Throughput up to 1.6Mbps (DLE+2Mbps)
- 2.4 GHz Transceiver
  - Support BLE 5.0 RF PHY 1Mbps/2Mbps
  - Proprietary 500K Protocol Stack
  - FSK with configurable Gaussian filter (configurable modulation index)
  - Sensitivity:
    -94dBm@BLE 1Mbps data rate
    -91dBm@BLE 2Mbps data rate
  - Tx power -20 to +6dBm in 3dB steps
  - Single-pin antenna: no RF matching or Rx/Tx switching required
  - RSSI (1dB resolution)
- AES-128 Encryption Hardware
- Operating Temperature: -40˚C ~+125 ˚C
- RoHS Package: SOP8

Revision History

Date	Version	Description
2022.8	1.0	First Edition.

Table of Contents

1 Introduction

ST17H68T is a System on Chip (SoC) for Bluetooth® low energy applications. It has high-performance low-power 32-bit processer with 32K retention SRAM, 96KB ROM, 16KB OTP, and an ultra-low power, high performance, multi-mode radio. Also, ST17H68T can support BLE with security, application and over-the-air download update. Serial peripheral IO and integrated application IP enables customer product to be built with minimum bill-of-material (BOM) cost.

2 Product Overview

2.1 Block Diagram

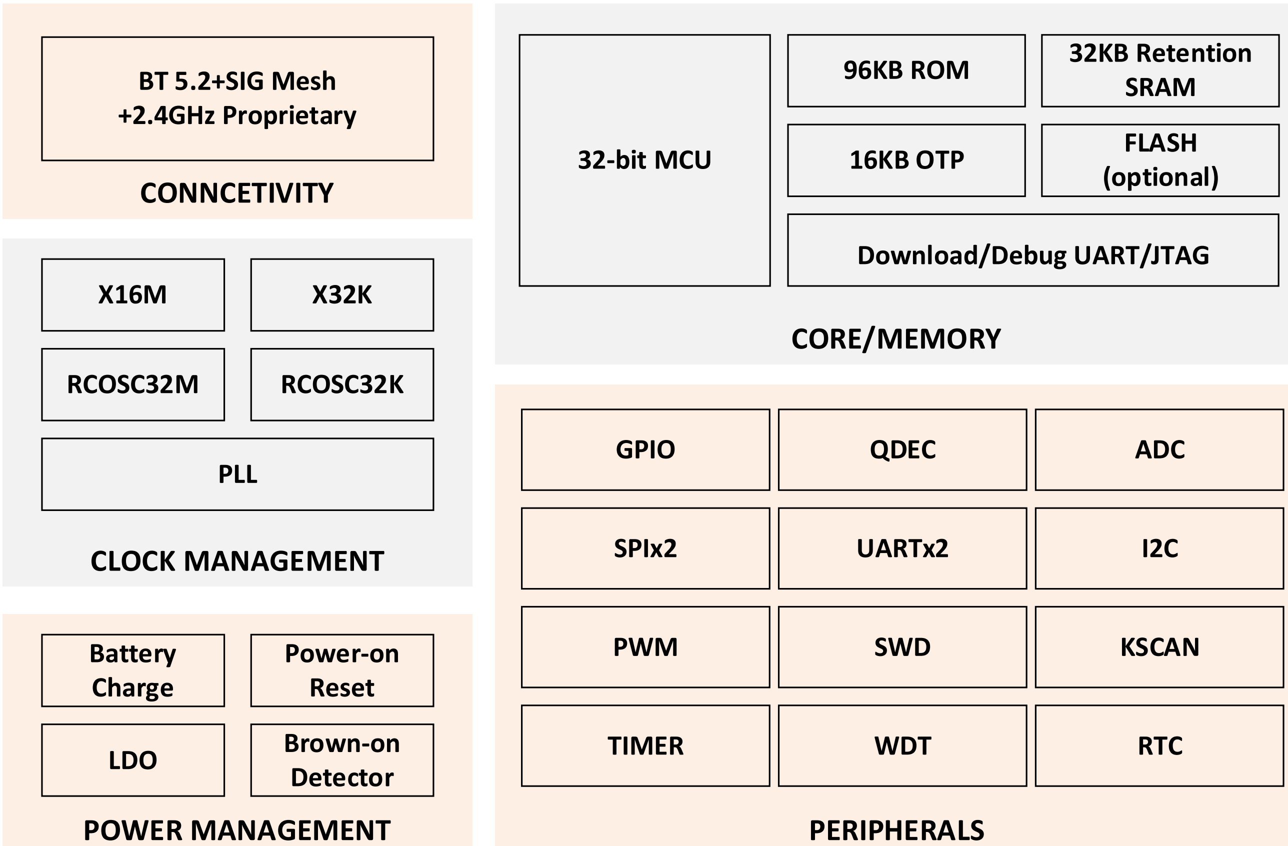


Figure 1: ST17H68T block diagram

2.2 Pin Assignments and Functions

This section describes the pin assignment and the pin functions for the package types of SOP8.

2.2.1 ST17H68T (SOP8)

2.2.1.1 Pin Assignment

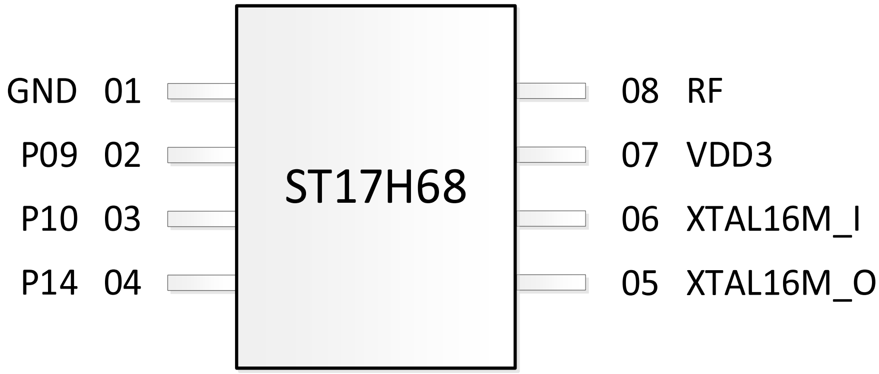


Figure 2: Pin Assignment – ST17H68T SOP8 package

2.2.1.2 Pin Functions

Pin	Pin name	Description
1	GND	GND
2	P09	GPIO 09
3	P10/SWS	GPIO 10/SWS
4	P14/AIO_3	GPIO 14/ADC input 3
5	XTAL16M_O	16MHz crystal output
6	XTAL16M_I	16MHz crystal input
7	VDD3	3.3V power supply
8	RF	RF antenna

Table 1: Pin Functions of ST17H68T SOP8 package

3 System Block

The system block diagram of ST17H68T is shown in **Figure 1**.

3.1 CPU

The ST17H68T has a low power CPU. The CPU, memories, and all peripherals are connected by AMBA bus matrix.

The CPU will play controller role in BLE modem and run all user applications.

3.2 Memory

ST17H68T has total 96KB ROM, 32KB SRAM and 16KB OTP. The physical address space of these memories is shown in **Figure 3**.

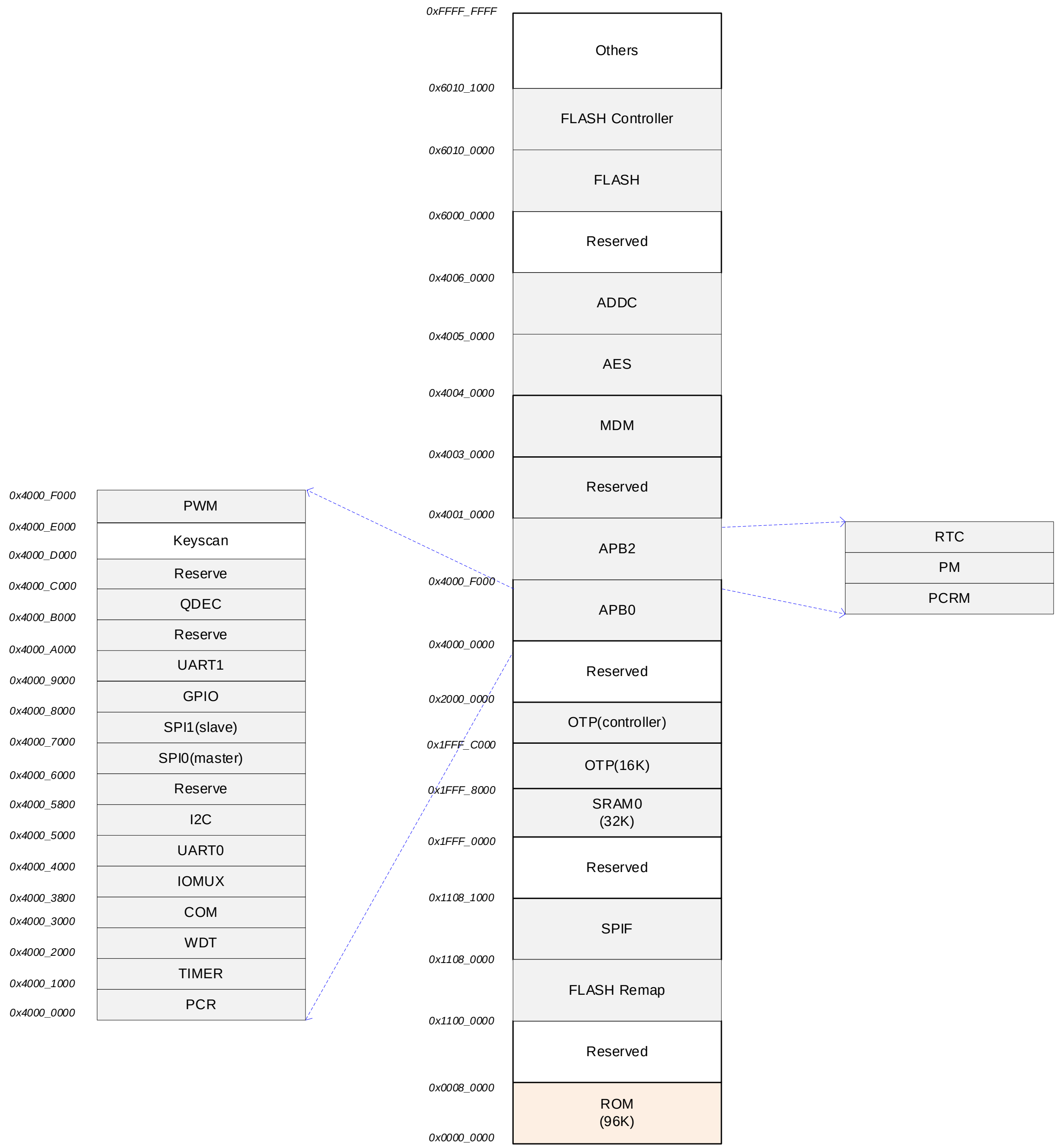


Figure 3: ST17H68T memory space

3.2.1 ROM

ST17H68T has 1 ROM.

	SIZE	CONTENT
ROM	96KB	Boot ROM. Protocol stack. Common peripheral drivers. ATE AT command.

Table 2: List of ROM

3.2.2 SRAM

ST17H68T has 1 SRAM blocks. The SRAM block have retention capability, which can be configured individually. Normal operating voltage is 1.2V, and the voltage is adjustable at retention. The SRAM block can be used to store program or data.

	SIZE	CONTENT
SRAM0	32KB	

Table 3: List of SRAM

3.2.3 OTP

The OTP is an antifuse based technology, which is capable for security code storage. This IP programming voltage is generated from an internal charge pump. The main memory is organized as 4,096 by 32 bits. The OTP cell design will provide a low-cost logic process OTP approach compared with alternative approaches. The OTP is programmed by 1.2V, 3.3V power supply.

3.2.4 Memory Address Mapping

Name	Size（KB）	Master	Physical Address
ROM	96K	MCU	1000_0000~1001_7FFF
RAM	32K	MCU	1FFF_0000~1FFF_7FFF
OTP	16K	MCU	1FFF_8000~1FFF_BFFF
RAM_BB	1K	MCU	

Table 4: Memory address mapping

3.3 Boot and Execution Modes

Only in CP Chip form, the chip enters CP boot mode after power on. ROM is then aliased to the 0x0 address and the chip program starts from ROM.

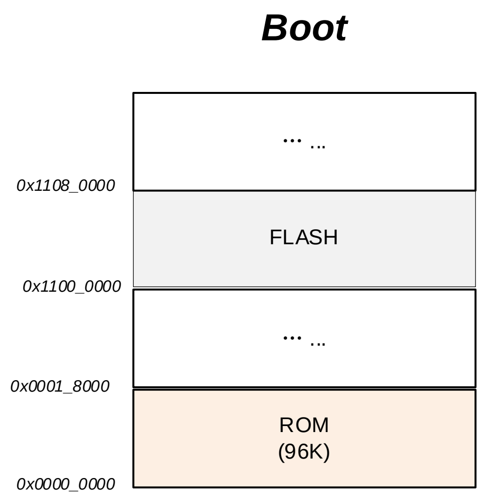


Figure 4: ST17H68T boot mode

3.4 Power, Clock and Reset (PCR)

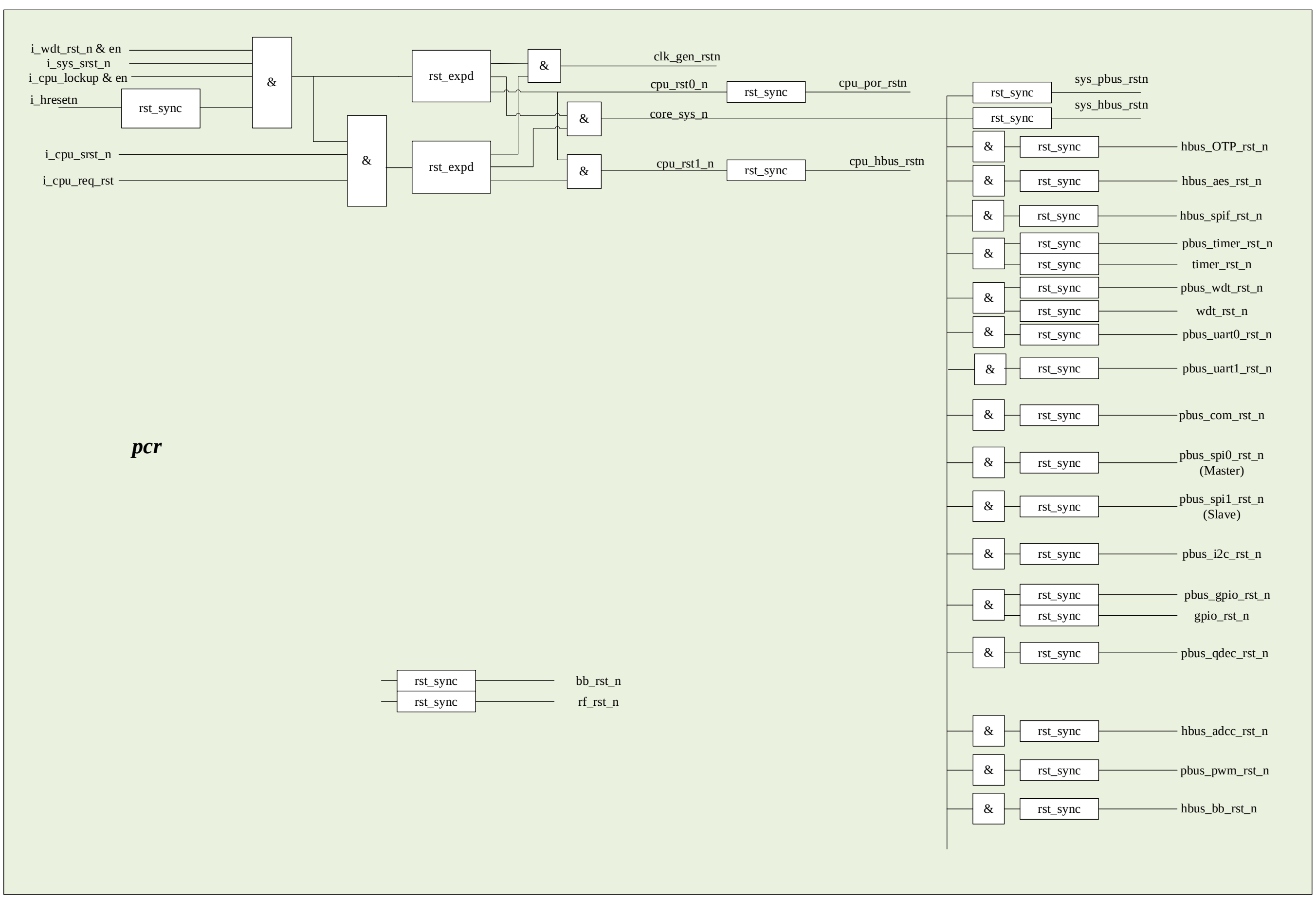


Figure 5: ST17H68T power, clock and reset

3.5 Power Management (POWER)

The power management system is highly flexible with functional blocks such as the CPU, radio transceiver, and peripherals saving separate power state control in addition to the System Sleep mode and OFF modes. When in System Normal mode, all functional blocks will independently be turned on depending on needed application functionality.

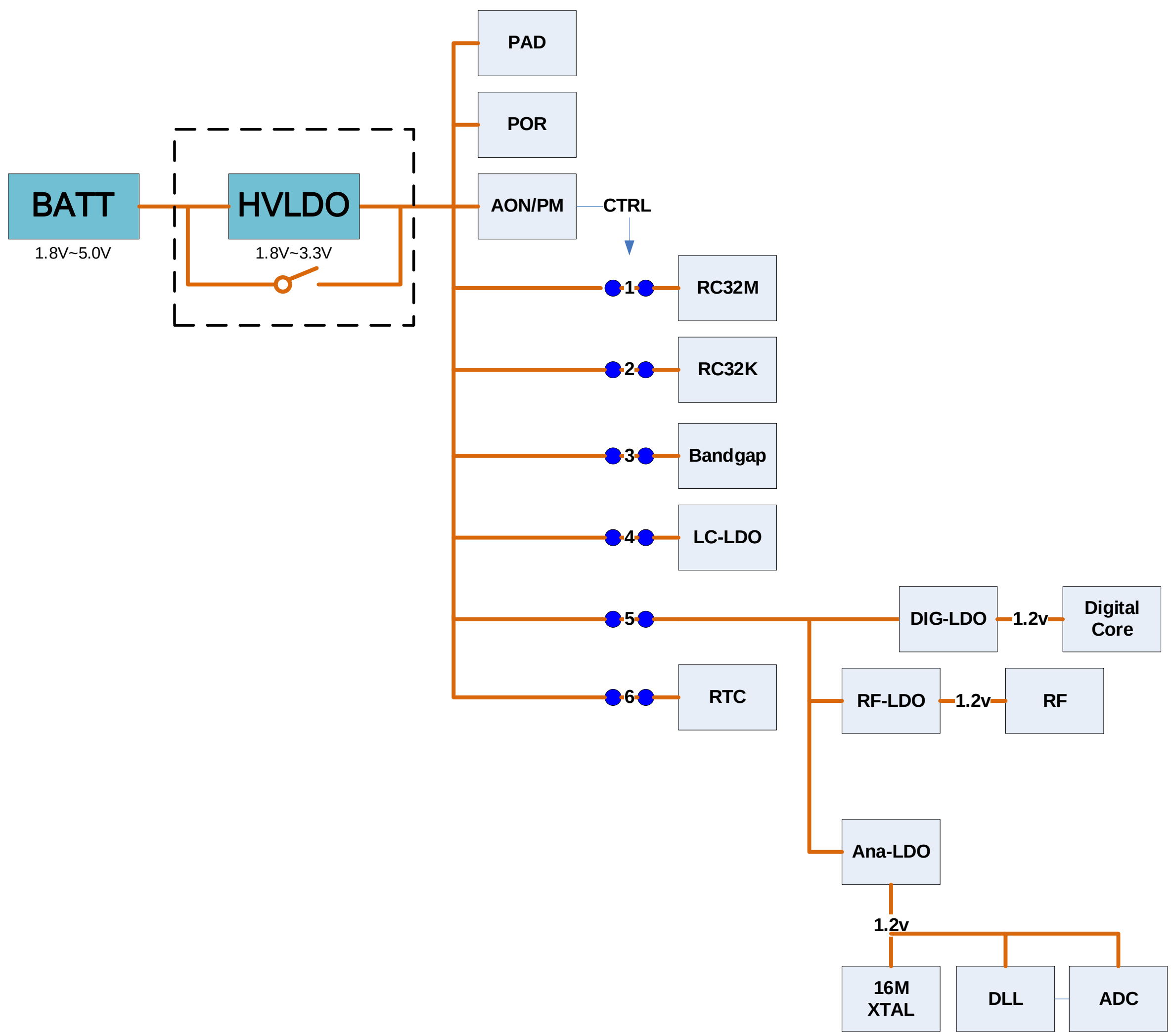


Figure 6: Power system

The following diagram is Normal, Sleep and Off mode. Switches are optional depending on user's request.

#	Switch	Normal	Sleep	Off
1	RC32M	On	Off	Off
2	RC32K	On	Optional	Off
3	bandgap	On	Off	Off
4	LC-LDO	On	on	Off
5	DIG-LDO	On	Off	Off
6	RTC	On	Optional	Off

Table 5: Flash Switches of different power modes

3.6 Low Power Features

3.6.1 Operation and Sleep States

3.6.1.1 Normal State

3.6.1.2 Clock Gate State

The CPU executes WFI/WFE to enter clock gate state. After wake-up from clock-gate state, the CPU continues to execute the program from where it stopped. The wake-up sources includes interrupts and events. The wake-up sources are configured by the software according to applications.

3.6.1.3 System Sleep State

The wake-up sources include:

- IO
- RTC
- RESET
- UVLO reset

3.6.1.4 System Off State

The wake-up sources include：

- IOs
- RESET
- UVLO reset

3.6.1.5 UVLO

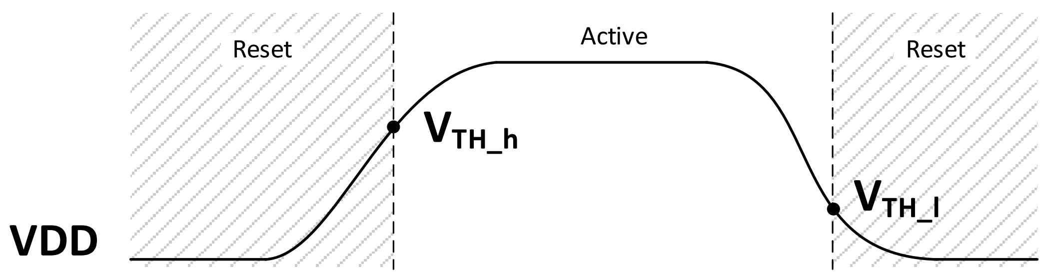


Figure 7: UVLO reset

VDD > VTH_h, release reset; VDD < VTH_l, enter reset.

VDD	Min.	TYP	Max.	Unit
V_{TH_h}	1.7	1.74	1.78	V
V_{TH_l}	1.63	1.66	1.69	V

Table 6: UVLO

If power supply VDD rises more than 0.6V within 100us, power monitor will trigger a whole chip reset event.

3.6.2 State Transition

3.6.2.1 Entering Clock Gate State and Wake-up

CPU executes WFI/WFE.

3.6.2.2 Entering Sleep/off States and Wake-up

The PM registers identify whether the CPU is in mirror mode before sleep or off, and record the remap and vectors. The CPU configures the corresponding PM registers to put the chip into sleep mode. After wake-up, the chip enters boot mode to execute boot code in the ROM. The ROM code checks the mode before sleep/off and the remap information, perform corresponding configurations, and starts to execute the program.

3.7 Interrupts

Interrupt Name	MCU Interrupt Number
	0
	1
	2
otp_irq	3
bb_irq	4
kscan_irq	5
rtc_irq	6
	9
wdt_irq	10
uart0_irq	11
i2c_irq	12
	13
spi0_irq	14
spi1_irq	15
gpio_irq	16
uart1_irq	17
spif_irq	18
	19
timer_irq[1]	20
timer_irq[2]	21
timer_irq[3]	22
timer_irq[4]	23
	24
	25
	26
	27
aes_irq	28
adcc_irq	29
qdec_irq	30
Hclk_mux_done	31

Table 7: Interrupts

3.8 Clock Management

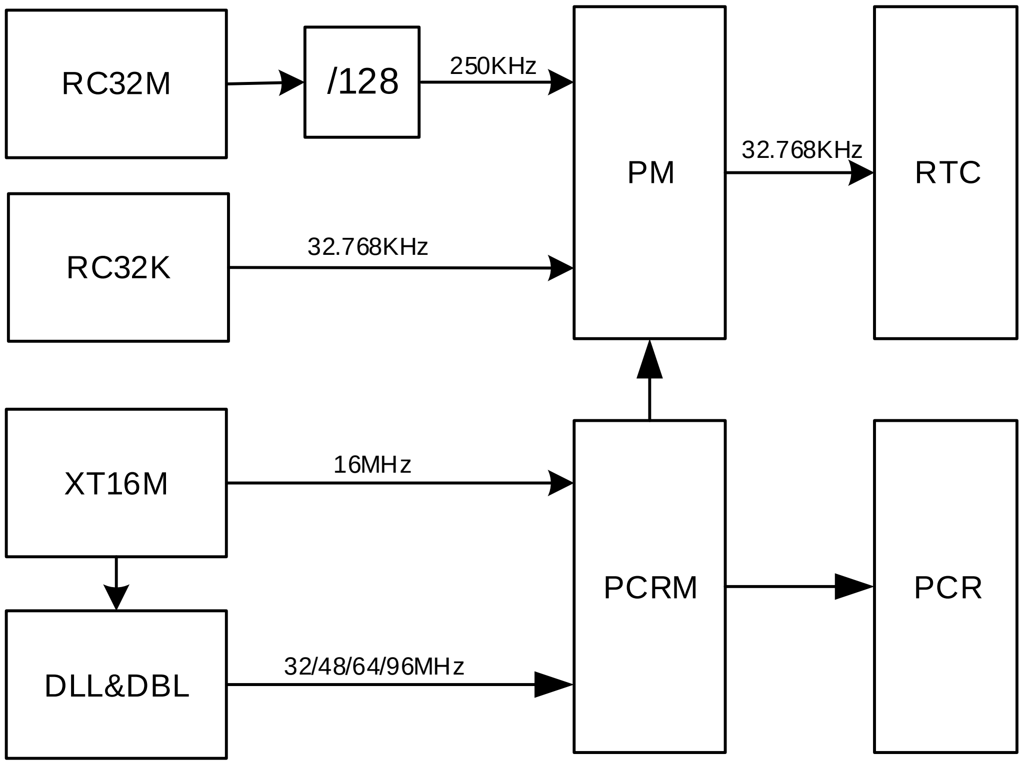


Figure 8: Clock management

There is only one crystal clock sources: 16MHz crystal oscillator (XT16M). There are also two on chip RC oscillators: 32MHz RC oscillator (RC32M) and 32kHz RC oscillator (RC32k), both of which can be calibrated with respect to 16MHz crystal oscillator. At initial power up or wake up before XT16M oscillator starts up, RC32M is used as the main clock. An on-chip DLL generates higher frequency clocks such as 32/48/64/96MHz.

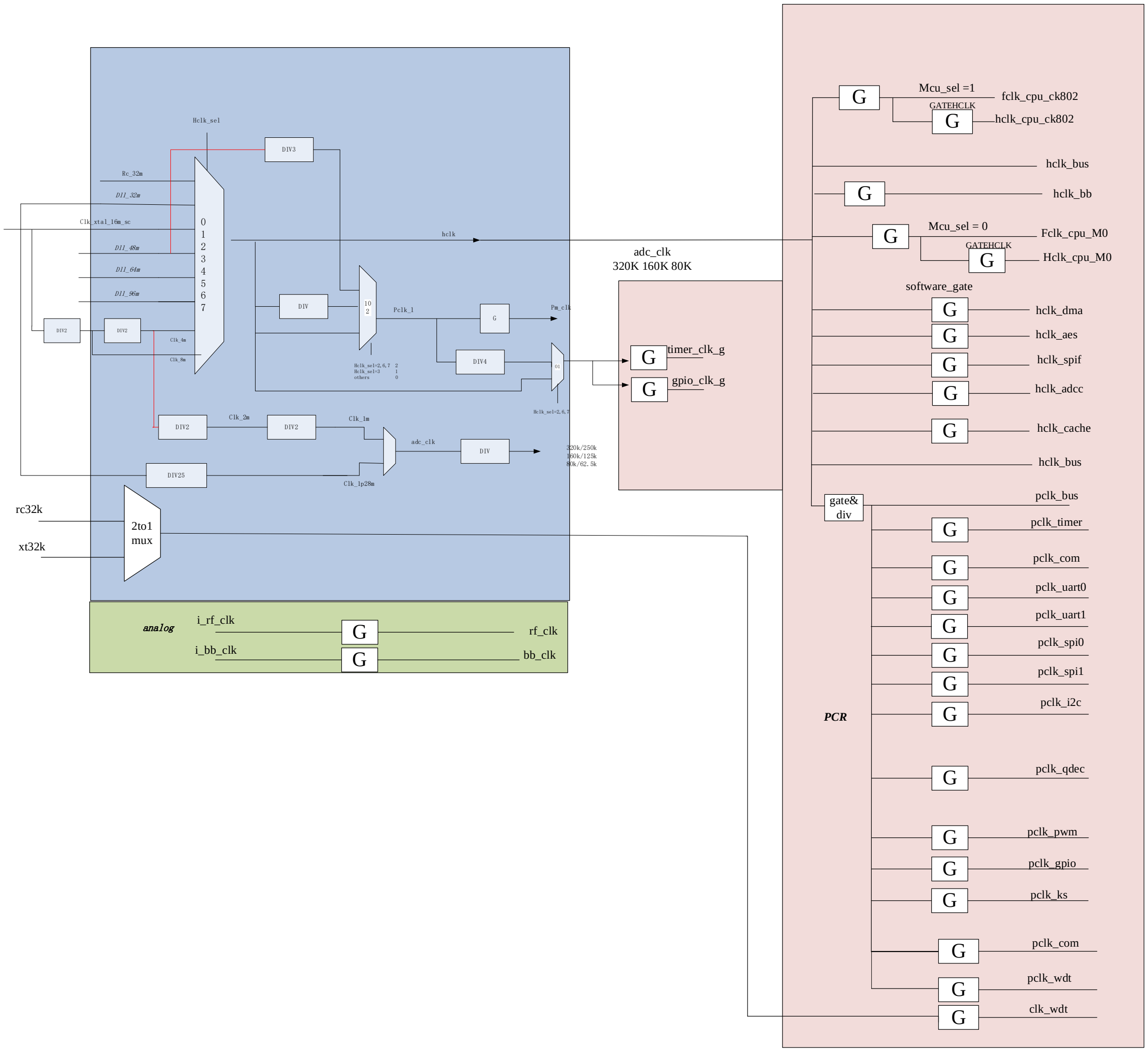


Figure 9: Clock structure diagram

3.9 IOMUX

The IOMUX provides a flexible I/O configuration, as the ports of most of the peripherals can be configured and mapped to any of the physical I/O pads (I/O at die boundary). These peripheral modules include I2C, UART0-1, PWM 0-5, SPI 0-1, Quadrature Decoder etc. However, for other specific purpose peripherals, their IOs mappings are fixed when they are enabled. These specific purpose peripherals include JTAG, analog_ios, GPIOs and key scan.

Figure 10 below shows the IOMUX functional diagram.

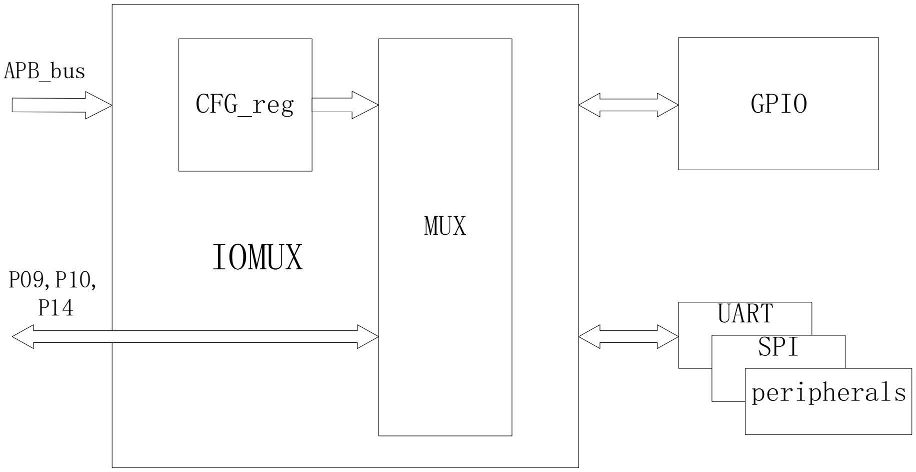


Figure 10: IOMUX structure diagram

There are 3 configurable pads. The table blow shows the mapping of the peripheral IOs that can be mapped through IOMUX. These include I2C, UART, PWM 0-2, SPI 0-1, Quadrature Decoder and 1.28MHz clock.

On the other hand, there are also special purpose peripherals, whose IOs are fixed to certain physical pads, when these peripheral functions are enabled. These special purpose peripherals include: JTAG, analog I/Os (ADC inputs), GPIO, and key scan. When they are enabled, their IOs are mapped to physical pads according to the following table.

#	ST17H68T			Name
0	GPIO_P09	GPIO		mk_out[4]
1	GPIO_P10	GPIO		mk_in[4]
2	GPIO_P14	GPIO	analog_io[3]	

Table 8: Peripheral IO Mapped Through IOMUX (special purpose)

3.10 GPIO

The General Purpose I/Os are a type of peripheral that can be mapped to physical I/O pads and programmed by software. The flexible GPIO are organized as PORT. The Port has bi-direction 30-bit lines, e.g., GPIO_PORT [28:0]. With default setting, physical pads: all pads are connected to the Port. When all GPIOs are enabled, as described in the IOMUX table in IOMUX section.

All Port pins can be configured as bi-directional serial interface, by selecting as input or output direction, and their corresponding data can be either read from or written to registers. All pins support wake-up and debounce function, and all Port pins support interrupt.

Each GPIO pins can be pulled up to VDD3 or pulled down to ground by adding pull up or pull down resistors to have default functions/states.

#	ST17H68T	Default Mode		Default IN_OUT		Pull up/dn		IRQ	Wakeup
		Burning	Boot	Burning	Boot	Burning	Boot		
0	GPIO_P09	UART_Tx	GPIO	OUT	IN	Pull up	Floating	√	√
1	GPIO_P10	UART_Rx	UART_Rx	IN	IN	Floating	Floating	√	√
2	GPIO_P14	GPIO	GPIO	IN	IN	Pull dn	Pull dn	√	√

Table 9: ST17H68T GPIO Application Notes

3.10.1 DC Characteristics

TA=25℃, VDD=3 V

PARAMETER	TEST CONDITIONS	Min.	TYP	Max.	Unit
Logic-0 input voltage				0.5	V
Logic-1 input voltage		2.4			V
Logic-0 input current	Input equals 0 V	-50		50	nA
Logic-1 input current	Input equals VDD	-50		50	nA
Logic-0 output voltage, 10-mA pins	Output load 10 mA			0.5	V
Logic-1 output voltage, 10-mA pins	Output load 10 mA	2.5			V

Table 10: DC Characteristics

4 Peripheral Blocks

4.1 2.4GHz Radio

The 2.4 GHz RF transceiver is designed to operate in the worldwide ISM frequency band at 2.4 to 2.4835 GHz. Radio modulation modes and configurable packet structure make the transceiver interoperable with *Bluetooth*® low energy (BLE) protocol implementations.

- General modulation format
  - FSK (configurable modulation index) with configurable Gaussian Filter Shaping
  - On-air data rates
  - 1Mbps/2Mbps
- Transmitter with programmable output power of -20dBm to +6dBm, in 3dB steps
- RSSI function (1 dB resolution, ± 2 dB accuracy)
- Receiver sensitivity
  - -94dBm@1Mbps BLE
  - -91dBm@2Mbps BLE
- Embedded RF balun
- Integrated frac-N synthesizer with phase modulation

4.2 Timer/Counters (TIMER)

The implementation can include a 32-bit SysTick system timer, that extends the functionality of both the processor and the NVIC. When present, the NVIC part of the extension provides:

- A 32-bit system timer (SysTick)
- Additional configurable priority SysTick interrupt.

General purpose timers are included in the design. With the input clock running at 4Mhz.

4.3 Real Time Counter (RTC)

The Real Time Counter (RTC) module provides a generic, low power timer on the low-frequency clock source (LFCLK). The RTC features a 24-bit COUNTER, 12-bit (1/X) prescaler, capture/compare registers, and a tick event generator for low power, tickless RTOS implementation.

4.4 AES-ECB Encryption (ECB)

The ECB encryption block supports 128-bit AES encryption. It can be used for a range of cryptographic functions like hash generation, digital signatures, and keystream generation for data encryption/decryption.

4.5 Watchdog Timer (WDT)

A count down watchdog timer using the low-frequency clock source (LFCLK) offers configurable and robust protection against application lock-up. The watchdog can be paused during long CPU sleep periods for low power applications and when the debugger has halted the CPU.

4.6 SPI (SPI0, SPI1 Two Independent Instances)

The SPI interface supports 3 serial synchronous protocols which are SPI, SSP and Microwire serial protocols. SPI0 is master, SPI1 is slave.

4.7 I2C

This I2C block support 100Khz, and 400Khz modes. It also supports 7-bit address and 10-bit address. It has built-in configurable spike suppression function for both lines.

4.8 UART (UART0, UART1 Two Independent Instances)

The Universal Asynchronous Receiver/Transmitter offers fast, full-duplex, asynchronous serial communication with built-in flow control (CTS, RTS) support in HW up to 1Mbps baud. Parity checking and generation for the 9th data bit are supported.

The GPIOs used for each UART interface line can be chosen from any GPIO on the device and are independently configurable. This enables great flexibility in device pin out and enables efficient use of board space and signal routing.

4.9 Pulse Width Modulation (PWM)

ST17H68T supports 6 channels of Pulse Width Modulation (PWM) outputs. PWM outputs generate waveforms with variable duty cycle or pulse width programmed by registers. And each of the 6 PWM outputs can be individually programmed. Their duty cycles are controlled by programming individual counters associated with each channel.

The master clock is 16MHz. For each PWM outputs, first there is a prescaler (pre-divider) with division ratio of 2 to 128 (only 2^N division ratios are supported), followed by another 16bit counter with programmable max count, denoted as top_count. When the 16bit counter counts from 0 to top_count, it resets back to 0. So the frequency of the PWM is given by:

Freq_PWM = 16MHz / (N_prescaler * N_top_count);

A threshold counter number can be programmed, when the 16bit counter reaches the threshold, PWM output toggles. So the duty cycle is:

Duty_cycle_PWM = N_threshold/N_top_count;

The polarity of the PWM can also be programmed, which indicates output 1 or 0 when counter is below/above the threshold. A PWM waveform vs counter values are illustrated in the following **Figure 11**, where the polarity is positive. Also in this case the counter ramps up and then resets, we call it “up mode”.

There is also a “up and down mode”, where the counter ramps up to count_top and then ramps down, instead of reset.

As discussed above, the key register bits for one PWM channel are: 16bit top_count, 16bit threshold count, 3bit prescaler count, PWM polarity, PWM mode (up or up/down), PWM enable, and PWM load enable (load new settings). All 6 PWM channels can be individually programmed by registers with addresses from 0x4000_E004 to 0x4000_E044. In addition, one should enable registers 0x4000_E000<0><4> to allow all PWM channels can be programmed.

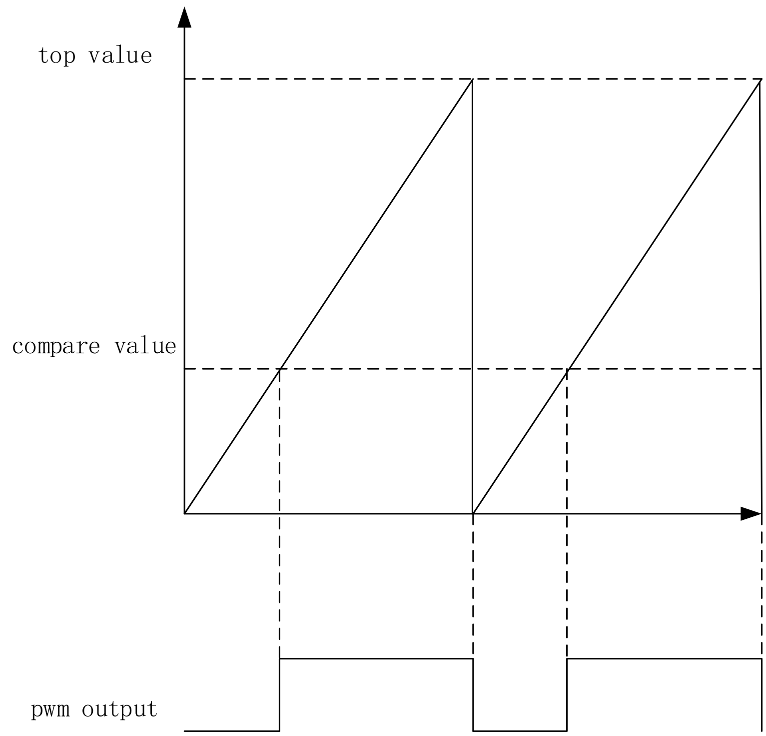


Figure 11: PWM operation

4.10 Quadrature Decoder (QDEC)

The quadrature decoder provides buffered decoding of quadrature-encoded sensor signals with input debounce filters. It is suitable for mechanical and optical sensors. The sample period and accumulation are configurable to match application requirements. The quadrature decoder has three-axis capability and index channel support. It can be programmed as 4x/2x/1x count mode.

4.11 Key Scan (KSCAN)

Keyscan supports key matrix with upto 16 rows by 18 columns. Each individual rows or columns can be enabled or disabled through register settings. GPIO pins can be configured to be used for key scan. A few key scan Parameters can be set through registers, including polarity (low or high indicating key pressed); support multi-key-press or only single-key-press; de-bounce time (the time duration a key press is deemed valid) from 0 to 128mS with 255us step.

A valid key press can trigger an interrupt when keyscan interrupt is enabled. After a keyscan interrupt is serviced, writing 1 to the interrupt state register bit can clear the state bit.

The keyscan has a manual mode and an auto mode. For manual mode, when a keyscan interrupt is received, it is upo the MCU/software to scan the keyscan output pins and check the input pins, to determine which keys have been pressed. Manual mode is relatively slow and need CPU to process. On the contrary, in automode keyscan will automatically scan the output/input pins, and store the row/column info corresponding to the key pressed into read only registers, then trigger an interrupt for software to retrieve key press information.

4.12 Analog to Digital Converter (ADC)

The 12bit SAR ADC has 1 input. Among them, there are two differential inputs for the on-chip temperature sensor. The other six inputs can be programmed to 4 pair differential inputs or six single-ended inputs. There is a manual mode with which the ADC can be configured to convert a specific input in single-ended or differential and with a specific ADC clock rate. There is also an auto sweep mode, namely all enabled input channels can be swept automatically in order by the ADC and the converted data will be stored at corresponding memory locations.

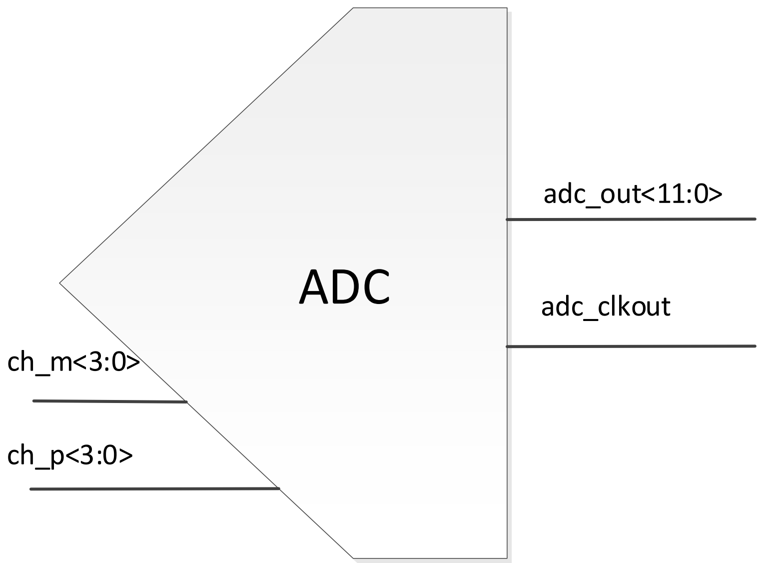


Figure 12: ADC

4.12.1 ADC Path

By default the ADC is configured in manual mode. In this mode, the ADC clock rate can be configured to 80k/160k/320k sample per second. Select the pair of inputs and configure it to differential or singled-ended (positive or negative). By default it is differential. After enabling, the ADC will take samples with the configured clock rate and store the data to a channel dependent memory location. For each channel a memory size of 128Byte is allocated, when it is full an interrupt bit will be flagged. Each sample of 12bits takes 2 Byte memory space.

ADC can also be configured into auto channel sweep mode by setting the “adc_ctrl_override” bit to 0, with which the enabled channels will be sampled in the configured order automatically. The ten ADC input channels can be configured by programming their corresponding registers. Their configurations include sampling time, enable/disable, differential/single-ended, and continuous sampling/single-shot, based on the following register table. The sampled data is stored in the corresponding memory locations as in manual mode.

Base address: 0x4000_F000

0x6C	ADC_CTL0	Register Description
[31:16]	auto mode config temp sense, differntial inputs	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

0x70	ADC_CTL1	Register Description
[31:16]	auto mode config input A, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x70	**ADC_CTL1**	**Register Description**
[15:0]	auto mode config input A positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x74	**ADC_CTL2**	**Register Description**
[31:16]	auto mode config input B, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	auto mode config input B positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
0x78	**ADC_CTL3**	**Register Description**
[31:16]	auto mode config input C, negative	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only
[15:0]	auto mode config input C positive or differential	channel config: [3:0] sample time, for max rate 320k: 2T to 62T, step 4T; for max rate 256k, 3T to 63T, step 4T, T is period of 1.28MHz; [4] channel enable; [5] differential 1 or single-ended 0; [6] continuous 0 or one shot 1. For auto channel sweep mode only

Table 11: ADC channel configurations

4.12.2 ADC Channel <3:0> Connectivity

ADC	Hardwired	Single	differential	note
aio<0>	gpio<11>	√	Input B negative	
aio<1>	gpio<23>	√	Input B positive	micphone bias reference voltage
aio<2>	gpio<24>	√	Input C negative	
aio<3>	gpio<14>	√	Input C positive	

ADC	Hardwired	Single	differential	note
aio<4>	gpio<15>	√	Input D negative	micphone bias
aio<5>	gpio<16>			32K XTAL input
aio<6>	gpio<17>			32K XTAL output
aio<8>	gpio<25>		Input A negative	

Table 12: ADC channel connectivity

Aio<9:7,4:0>can be selected through an analog Mux by programming aio_pass<7:0> and aio_attn<7:0>. For example, register 0x4000_F020<8><0> set to 01, then Aio<0> is connected to ADC input B negative.

0x4000_F020		Register Description
[15 : 8]	Attenuation ctrl	attn[7:0]. analogIO control for {aio<9>, aio<8>,aio<7>,aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass through 10 attenuate to 1/4 11 NC
[7 : 0]	pass ctrl	pass[7:0]. analogIO control for {aio<9>, aio<8>,aio<7>,aio<4>, aio<3>, aio<2>, aio<1>, aio<0>}. {attn[x], pass[x]}: 00 switch off 01 pass through 10 attenuate to 1/4 11 NC note: analog IO sharing gpio<11>/aio<0> gpio<23>/aio<1>/micphone bias reference voltage gpio<24>/aio<2> gpio<14>/aio<3> gpio<15>/aio<4>/micphone bias gpio<16>/aio<5>/32K XTAL input gpio<17>/aio<6>/32K XTAL output gpio<25>/aio<8>

Table 13: analog Mux

5 Absolute Maximum Ratings

Maximum ratings are the extreme limits to which ST17H68T can be exposed without permanently damaging it. Exposure to absolute maximum ratings for prolonged periods of time may affect the reliability of the ST17H68T. **Table 14** specifies the absolute maximum ratings for ST17H68T.

Symbol	Parameter	Min.	Max.	Unit
Supply voltages				
VDD3		-0.3	+3.6	V
VSS			0	V
I/O pin voltage				
VIO		-0.3	VDD + 0.3	V
Environmental				
Storage temperature		-40	+125	°C
MSL	Moisture Sensitivity Level		3	
ESD HBM	Human Body Model Class 2		2	kV
ESD CDMQF	Charged Device Model (SOP8 package)		500	V

Table 14: Absolute maximum ratings

6 Operating Conditions

The operating conditions are the physical Parameters that ST17H68T can operate within as defined in **Table 15**.

Symbol	Parameter	Min.	Typ.	Max.	Units
VDD3	Supply voltage, normal mode	1.8	3	3.6	V
tr_VDD	Supply rise time (0 V to 1.8 V)			100	ms
TA	Operating temperature	-40	27	125	°C

Table 15: Operating conditions

7 Radio Transceiver

7.1 Radio Current Consumption

Parameter	Description	MIN	TYP	MAX	UNIT
Tx only at 0dBm	@3V		10		mA
Rx Only	@3V		10		mA

Table 16: Radio current consumption

7.2 Transmitter Specification

Parameter	Description	MIN	TYP	MAX	UNIT
RF Max Output Power			6		dBm
RF Min Output Power			-20		dBm
OBW for BLE 1Mbps	20dB occupy-bandwidth for BLE modulation 1Mbps		1100		KHz
OBW for BLE 2Mbps	20dB occupy-bandwidth for BLE modulation 2Mbps		2300		KHz
FDEV for BLE 1Mbps	Frequency deviation for GFSK modulation 1Mbps	160		250	KHz
FDEV for BLE 2Mbps	Frequency deviation for GFSK modulation 2Mbps	320		500	KHz

Table 17: Transmitter specification

7.3 Receiver Specification

7.3.1 RX BLE 1Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 1Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-94		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		7		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		45		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		50		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm

Parameter	Description	MIN	TYP	MAX	UNIT
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 18: RX BLE 1Mbps GFSK

7.3.2 RX BLE 2Mbps GFSK

Parameter	Description	MIN	TYP	MAX	UNIT
Rx Sensitivity	Sensitivity test 2Mbps BLE ideal transmitter, 37 Byte BER=1E-3		-91		dBm
co-channel rejection	modulated interferer in channel, 37 Byte BER=1E-3		-6		I/C dB
Selectivity +-1MHz	Wanted signal at -67dBm, modulated interferer at +/- 1MHz, 37 Byte BER=1E-3		-5		I/C dB
Selectivity +-2MHz	Wanted signal at -67dBm, modulated interferer at +/- 2MHz, 37 Byte BER=1E-3		9		I/C dB
Selectivity +-3MHz	Wanted signal at -67dBm, modulated interferer at +/- 3MHz, 37 Byte BER=1E-3		30		I/C dB
Selectivity +-4MHz	Wanted signal at -67dBm, modulated interferer at +/- 4MHz, 37 Byte BER=1E-3		40		I/C dB
Selectivity +-5MHz or More	Wanted signal at -67dBm, modulated interferer at >=+/- 5MHz, 37 Byte BER=1E-3		55		I/C dB
Selectivity Imag frequency	Wanted signal at -67dBm, modulated interferer at imagefrequency, 37 Byte BER=1E-3		22		I/C dB
Intermodulation	Wanted signal at 2402MHz, -64dBm, Two interferers at 2405 and 2408 MHz respectively, at the given power level, 37 Byte BER=1E-3		-20		dBm
Carrier Frequency Offset Tolerance			+-350		KHz
Sample Clock Offset Tolerance			+-120		ppm

Table 19: RX BLE 2Mbps GFSK

7.4 RSSI Specifications

Parameter	Description	MIN	TYP	MAX	UNIT
RSSI Dynamic Range			70		dB
RSSI Accuracy	RSSI Accuracy Valid in range -100 to -30dBm		+/-2		dB
RSSI Resolution	Totally 7bit, from 0 to 127		1		dB
RSSI Period			8		us

Table 20: RSSI specifications

8 Glossary

Term	Description
AHB	Advanced High-performance Bus
AHB-AP	DAP AHB Port for debug component access thru AHB bus
AMBA	Advanced Microcontroller Bus Architecture
AON	Always-on power domain
APB	Advanced Peripheral Bus
APB-AP	DAP APB Port for debug component access thru APB bus
BROM	Boot ROM
DAP	Debug Access Port
ETM	Embedded trace module
FPU	Floating Point Unit
I2C	Inter-Integrated Circuit
I2S	Inter-IC Sound, Integrated Interchip Sound
ITM	Instrumentation Trace Macrocell Unit
JTAG	Joint Test Access Group (IEEE standard)
JTAG-AP	DAP's JTAG Access Port to access debug components
JTAG-DP	DAP's JTAG Debug Port used by external debugger
J&M	Jun and Marty LLC
MPU	Memory Protection Unit
NVIC	Nested vector Interrupt Controller
PCR	Power Clock Reset controller
POR	Power on reset, it is active low in this document
RFIF	APB peripheral to interface RF block
SoC	System on chip
SPI	Serial Peripheral Interface
SRAM	Static Random Access memory
TWI	Two-Wire Interface
UART	Universal Asynchronous Receiver and Transmitter
WDT	Watchdog Timer

Table 21: Glossary

9 Ordering Information

9.1 Order Code

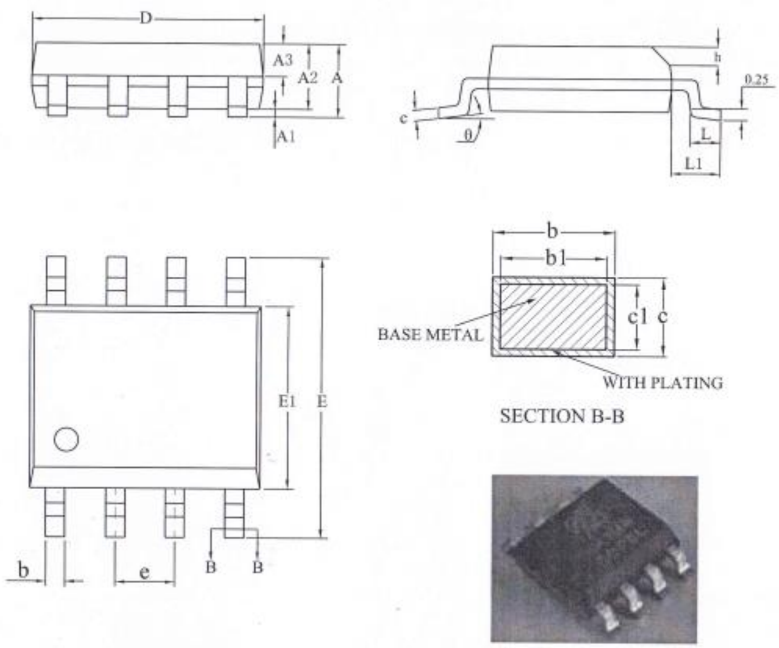
Part No.	Package	Supply Voltage	Operating Temp. (°C)	Packing	Quantity			
					ea /tube	tube /inner	inner /case	ea /case
ST17H68T	SOP8	1.8~3.6V	-40~125	Tube	100	100	10	100000

Table 22: Order Code

10 Package Dimensions

Note: dimensions are in mm, angels are in degree.

10.1.1 SOP8



SYMBOL	MILLIMETER		
	MIN	NOM	MAX
A	—	—	1.75
A1	0.10	—	0.225
A2	1.30	1.40	1.50
A3	0.60	0.65	0.70
b	0.39	—	0.47
b1	0.38	0.41	0.44
c	0.20	—	0.24
c1	0.19	0.20	0.21
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27BSC		
h	0.25	—	0.50
L	0.50	—	0.80
L1	1.05REF		
θ	0	—	8°

Figure 13: SOP8 Package Dimensions

11 Sample Application and Layout Guide

11.1 Sample Application

11.1.1 SOP8

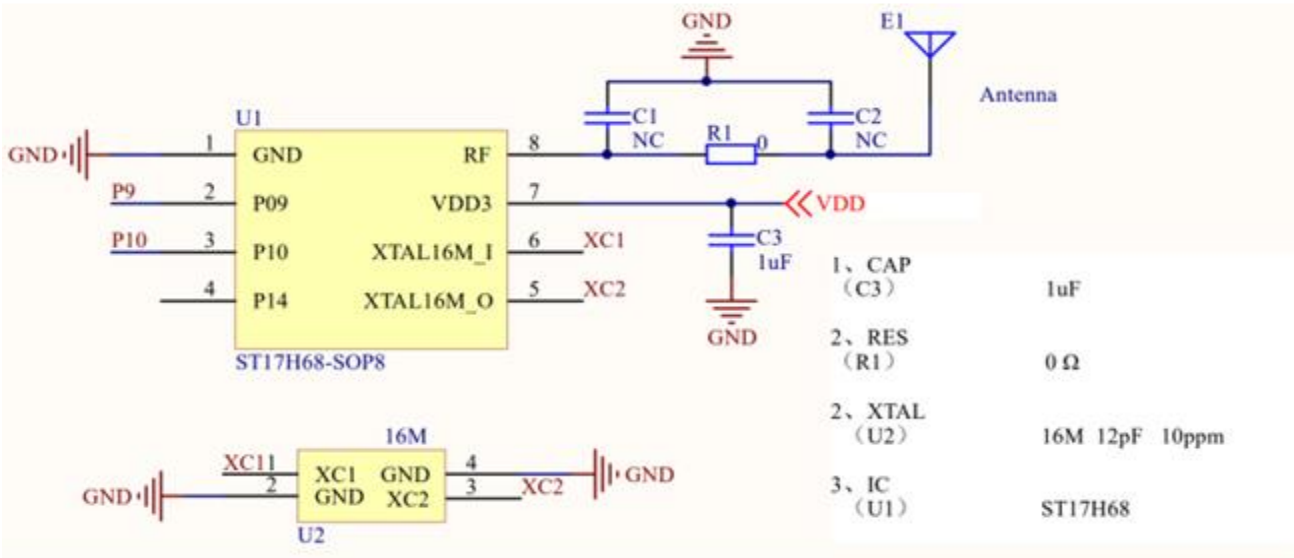


Figure 14: Sample Application of ST17H68T SOP8

11.2 Layout Guide

11.2.1 Placement

1. RF matching/Loop filter leading to antenna should be isolated from any other AC/DC signal as much as possible;
2. Xtal/OSC clock is a noise source to other circuits, keep clock trace as short as possible and away from any important area;
3. LDO’s are sensitive and could be easily contaminated, care should be taken for the environment;
4. Antenna is the main RF radiation point, other important blocks should be shielded or away from this area.

RF traces

1. Define RF line width with given dielectric thickness (thickness of PCB dielectric layer to ground plain) to achieve 50ohm impedance; this is mainly for the RF line connecting to matching/loop filter and antenna.
2. Differential traces should be kept in the same length and component should be placed symmetrically;
3. Certain length of RF trace should be treated as part of RF matching.

11.2.2 Bypass Capacitor

1. Each VDD pin needs a bypass capacitor to release chip internal noise and block noise from power supply.
2. For power traces, bypass capacitors should be placed as close as possible to VDD pins.
3. Use one large and one small capacitor when the pin needs two capacitors. Typically the capacitance of the larger capacitor is about 100 times of that of the smaller one. The smaller

capacitor usually has better quality factor than the larger one. Place the larger capacitor closer to the pin.

4. The capacitors of Loop filter need to have larger clearance to prevent EMC/EMI issue.
5. Ground via should be close to the Capacitor GND side, and away from strong signals.

11.2.3 Layer Definition

1. Normally 4 layer PCB is recommended.
2. RF trace must be on the surface layer, i.e. top layer or bottom.
3. The second layer of RF PCB must be "Ground " layer , for both signal ground and RF reference ground , DO NOT put any other trace or plane on second layer, otherwise "antenna effect" will complicate debug process.
4. Power plane generally is on the 3rd layer.
5. Bottom layer is for "signal " layer.
6. If two layer PCB is used, quality will degrade in general. More care needs to be taken. Try to maximize ground plane, avoid crossing of signal trace with other noise lines or VDD, shield critical signal line with ground plane, maximize bypass capacitor and number of ground vias.

11.2.4 Reference clock and trace

1. Oscillator signal trace is recommended to be on the 1st layer;
2. DO NOT have any trace around or across the reference clock (oscillator) trace.
3. Isolate the reference clock trace and oscillator by having more GND via around.
4. DO NOT have any other traces under the Oscillator.

11.2.5 Power line or plane

1. Whether to use power plain or power line depend on the required current, noise and layout condition. For RF chip, we generally suggest to use power line to bring power into IC pin. Line has parasitic inductance, which forms a low pass filter to reduce the noise traveling around PCB.
2. Add more conductive via on the current source, it will increase max current limit and reduce inductance of via.
3. Add some capacitor alone the power trace when power line travels a long distance.
4. DO NOT place power line or any plane under RF trace or oscillator and its clock trace , the strong clock or RF signal would travel with power line.

11.2.6 Ground Via

1. Ground Via must be as close to the ground pad of bypass capacitor as possible , too much distance between via and ground pad will reduce the effect of bypass capacitor.
2. Having as many ground via as possible.
3. Place ground via around RF trace, the RF trace should be shielded with via trail.