CSSE 332 – Operating Systems Rose-Hulman Institute of Technology Computer Science and Software Engineering Department

Page Table Structure B

Name:	 Box:
See next page	

(3 points) Consider a two level paging system. Assume that frames are 256 bytes.

Root Page Table Ptr		Main	Memory	Physical Address
0	Addresss	Valid	Frame	Frame # Offset
		bit	Number	
	0	1	104	
	4	1	334	
	8	0	45	
	12	1	1	
	16	1	115	
	20	1	713	
	24	1	2	
	28	0	228	
			• • •	
17:1 A JJ	256	1	900	
Virtual Address	$_{\neg}$ 260	1	1005	
Page # Offset	264	0	820	
Or Or	$_{\neg}$ 268	1	20	
$\boxed{ \text{Index}_1 \mid \text{Index}_2 \mid \text{Offset} }$	272	0	5	
	276	0	1005	
	280	0	220	
			• • •	
	512	1	303	
	516	1	689	
	520	0	446	
	524	1	848	
	528	0	666	
	532	1	111	Register
	536	1	229	Interrupt Indicator

For each of the following virtual addresses, determine whether or not a page fault occurs, if one occurs specify the level at which it occurs, and if a page fault does not occur, translate the virtual address to a physical address.

- 1. 2|2|105
- 2. 6|2|240
- 3. 3|3|120

(7 points) Consider a 32-bit addressing scheme with 6 bits for $Index_1$, 12 for $Index_2$, 14 for the offset and 4 GB of physical memory.

4.	How many entries are there in the root page table?
5.	How many entries are there in the second level page table?
6.	How many total entries are there in the page table structure?
7.	What is the minimum size of each page table entry?
8.	What is the size of each page?
9.	What are the advantages of using a two level page table?
10.	What are the disadvantages of using a two level page table?

(5 points) Consider an inverted page table system with hashing. Assume that frames are 1024 Bytes.

Virtual A	Address
Page #	Offset

	_ 02 02_ 0.0.0	
Page #	Offset	

Hash
Function

	Main Memory			
Addresss	Page	Frame	Valid	Rel.
	#	#	bit	Ptr
0	104	8	1	0
		• •	•	

0	104	8	1	0
			•	
256	33	0	0	0
260	81	1	1	0
264	807	2	1	0
268	19	3	1	0
272	41	4	1	-3
276	26	5	0	0
280	803	6	1	-3
284	404	7	0	0

Physical A	Address
Frame #	Offset

Page Table Ptr	
256	

Register Interrupt Indicator

For each of the following virtual addresses, determine whether or not a page fault occurs, and if a page fault does not occur, translate the virtual address to a physical address.

Assume the hash function is h(x) = 3 + (x%8)

Note that this system uses chained hashing, with the Rel Ptr indicating the page table elements to the next entry in the chain.

- 11. 81|105
- 12. 41|640
- 13. 25|320
- $14. \ 28|204$
- 15. 19|880