EEE334

Lab #7 (Honors Lab)

Design an Audio Amplifier using MOS transistor

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Vincent Li

Dr. Allee

## Introduction:

The goal of this experiment is to design a multistage audio amplifier with MOS transistors. The only equipment needed is LTSpice.

The design requirements are: overall voltage amplification $A_V \geq 300V/V$, total power consumption $P_{TOT} \leq 200mW$, load resistance $1k\Omega \leq R_L \leq 1M\Omega$, bandwidth is between $f_L \leq 20Hz$ and $f_H \leq 20kHz$, and source voltage $V_S \leq 5mV_{pp}$.

Voltage gain, MOS technology, transient analysis, and frequency response analysis will be researched.

## Equipment and Components:

Equipment:

| Name | Model | Quantity |
|---|---|---|
| LTSpice | | |

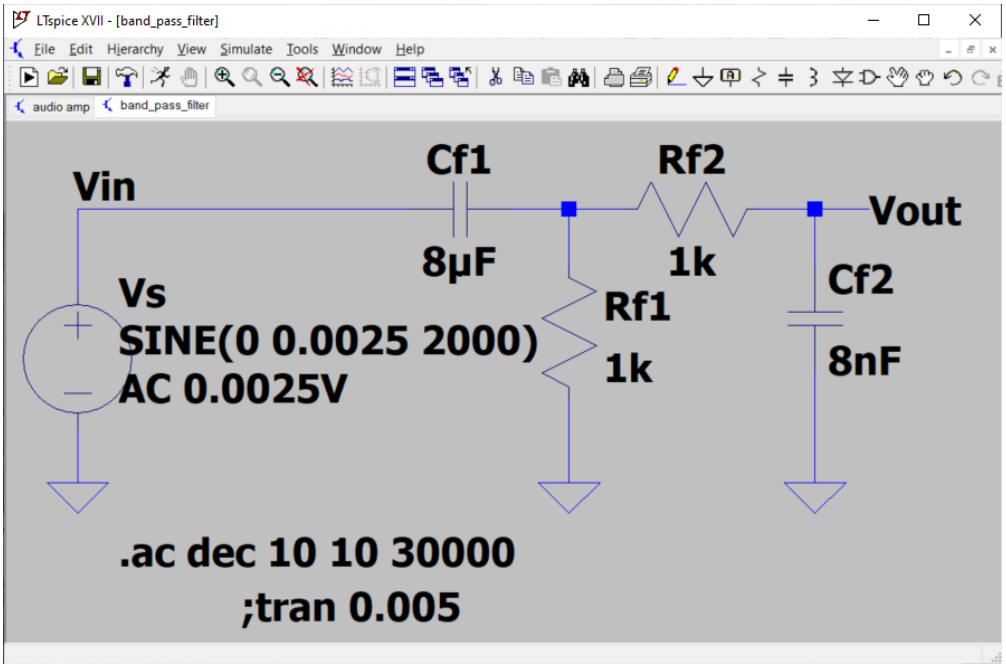
Components:

| Name | Value | Quantity |
|---|---|---|
| $v_s$ | sine $0.0025V_{amp}$ | 1 |
| $V_{DD}$ | $12V$ | 1 |
| NMOS transistor $0.8\mu m$ tech | $k_n = 0.127mA/V^2$<br>$V_t = 0.7V, \lambda = 0.001$<br>$\frac{W}{L} = 3$ | 4 |
| Capacitor $C_{f1}$ | $8\mu F$ | 1 |
| Capacitor $C_{f2}$ | $8nF$ | 1 |
| Resistor $R_{f1}$ | $1k\Omega$ | 1 |
| Resistor $R_{f2}$ | $1k\Omega$ | 1 |
| Resistor $R_{GA}$ | $2.6M\Omega$ | 4 |
| Resistor $R_{GB}$ | $1M\Omega$ | 4 |
| Resistor $R_{D1-3}$ | $6.6k\Omega$ | 3 |
| Resistor $R_{D4}$ | $5.3k\Omega$ | 1 |
| Resistor $R_S$ | $3\Omega$ | 3 |
| Capacitor $C_S$ | $50\mu F$ | 3 |
| Capacitor $C$ | $1\mu F$ | 5 |
| Resistor $R_L$ | $1M\Omega$ | 1 |

Procedure:

1. Design a band-pass filter for $v_S$ to fulfill the bandwidth requirement.

*Figure 1: Schematic of the band-pass filter*




Let $\boldsymbol{R_{f1} = R_{f2} = 1k\Omega}$

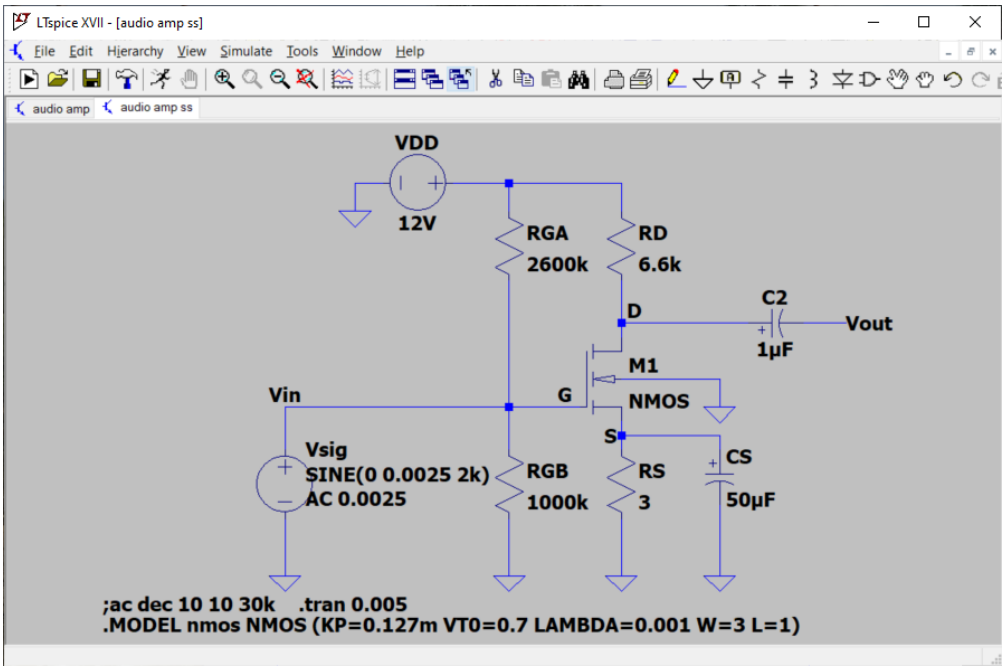
$$f_L = 20Hz, f_H = 20kHz$$

$$C_{f1} = \frac{1}{2\pi f_L R_{f1}} = \frac{1}{2\pi * 20 * 1000} = 7.958 * 10^{-6} \approx \boldsymbol{8\mu F}$$

$$C_{f2} = \frac{1}{2\pi f_H R_{f2}} = \frac{1}{2\pi * 20000 * 1000} = 7.958 * 10^{-9} \approx \boldsymbol{8nF}$$

2. Design a single-stage NMOS common-source amplifier.

*Figure 2: Schematic of NMOS amplifier for stages 1-3*




In saturation region: $V_{DS} \geq V_{GS} - V_t;\ V_D \geq V_G - 7;\ V_t = 0.7V$

To bias, let $V_G = 3.333V$

$$V_G = V_{DD} * \frac{R_{GB}}{R_{GA}+R_{GB}} = 3.333 = 12 * \frac{R_{GB}}{R_{GA}+R_{GB}}$$

$$3.333(R_{GA} + R_{GB}) = 12 * R_{GB}; 3.333R_{GA} + 3.333R_{GB} = 12R_{GB}$$

$$3.333R_{GA} = 8.667R_{GB}$$

$$R_{GA} = 2.600R_{GB};\ \frac{R_{GA}}{R_{GB}} = \frac{1}{2.600}$$

Have $\boldsymbol{R_{GA} = 1M\Omega, R_{GB} = 2.6M\Omega}$

Let $V_D = 3.279V$, just a bit less than $V_G$

Let $V_S = 0.004V$ which is very small

$$\frac{V_{DD}-V_D}{R_D} = \frac{V_S}{R_S};\ \frac{12-3.279}{R_D} = \frac{0.004}{R_S};\ \frac{8.721}{R_D} = \frac{0.004}{R_S};\ \frac{8.721}{0.004} = \frac{R_D}{R_S}$$

$\frac{R_D}{R_S} \approx \frac{6.6k}{3}$, choose 3 for practical purposes

$$\boldsymbol{R_D = 6.6k\Omega, R_S = 3\Omega}$$

Add a $\boldsymbol{50\mu F}$ capacitor at the source to further increase gain.

Add a $\boldsymbol{1\mu F}$ capacitor at the output to remove DC from it. The capacitance just needs to be large enough to block DC.

3. Cascade this single-stage amplifier 3 times to get triple the gain.
4. Design a fourth single-stage amplifier with a less gain compared to the previous. Otherwise, cascading the first single-stage amplifier 4 times will skew the output waveform severely and the overall voltage gain will be impractically high.

Have the same design as the previous single-stage amplifier, but without $R_S$ and $C_S$.

Let $V_G = 3.333V$, so $\boldsymbol{R_{GA} = 2.6M\Omega}$ and $\boldsymbol{R_{GB} = 1M\Omega}$

Let $V_D = 4.964V$, just under $5V$, which is the $V_{DD}$ of the NMOS

$R_D$ and $I_D$ can be $I_D * R_D = 5 - 4.964 = 0.036V$

$$1.328mA * 5.3k\Omega = 0.036V$$

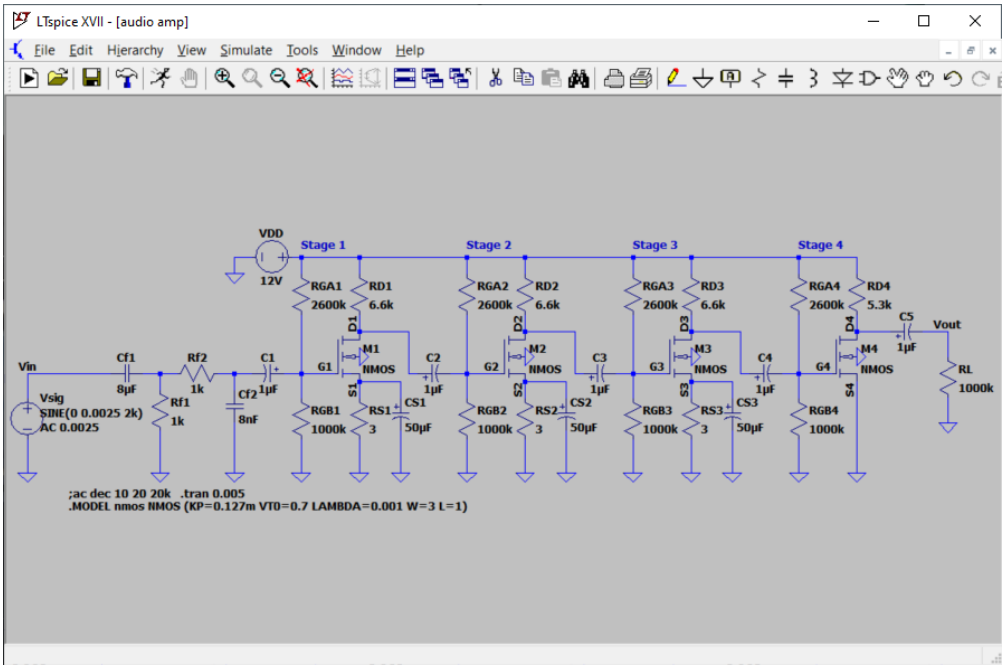
$$\boldsymbol{R_D = 5.3k\Omega}$$

Add a $\boldsymbol{1\mu F}$ capacitor at the output. The capacitance just needs to be large enough to block DC.

5. Let $\boldsymbol{R_L = 1M\Omega}$, which is the highest allowed value.

## Results:

*Figure 3: Schematic of the complete audio amplifier circuit*




Circuit parameters:

| | |
|---|---|
| $V_{DD}$ | $12V$ |
| $V_{SS}$ | $0V$ (ground) |
| NMOS $\frac{W}{L}$ | $3/1$ |
| NMOS technology | $0.8\mu m$ $\left(V_t = 0.7V, k_n = \frac{0.127mA}{V^2}\right)$ |
| NMOS $\lambda$ | $0.001$ |
| Load resistance | $1M\Omega$ |

*all MOSFETs used have the same parameters

*Figure 4: Transient analysis of the first stage*

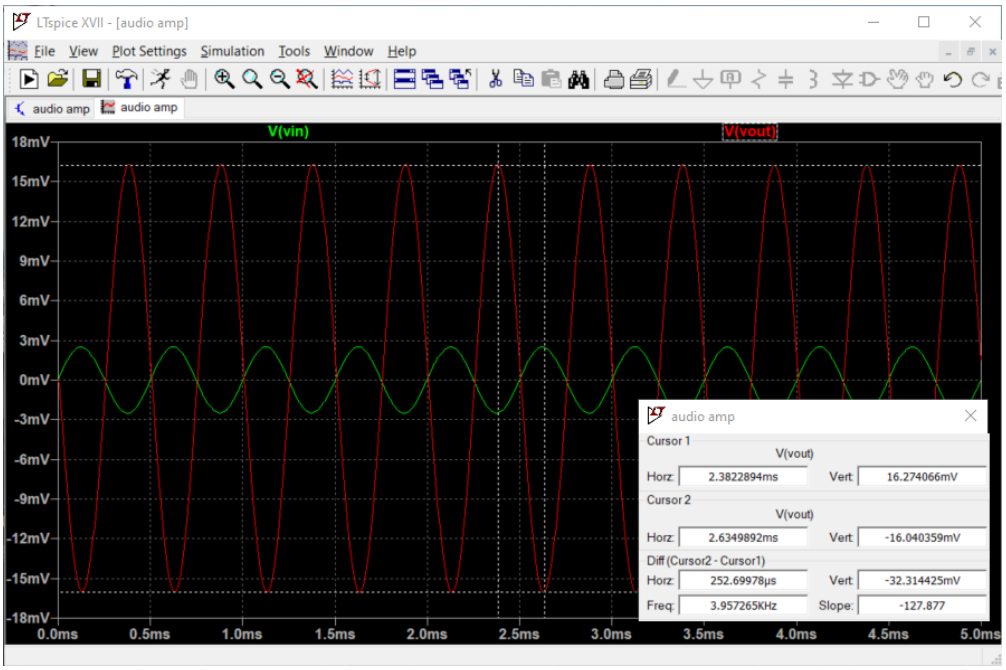



*Figure 5: Transient analysis for stage 4*

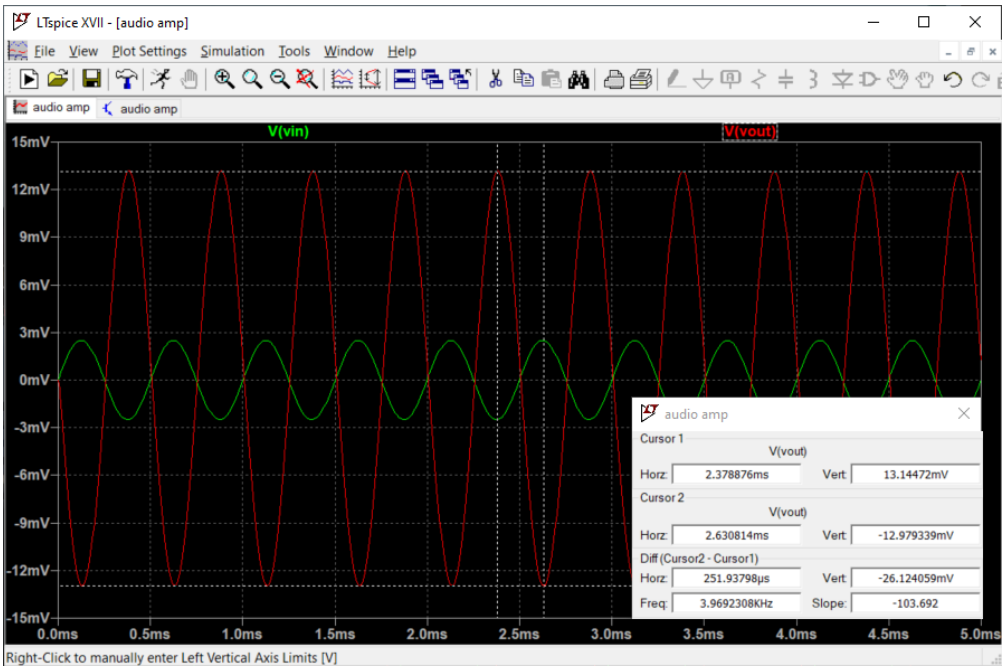
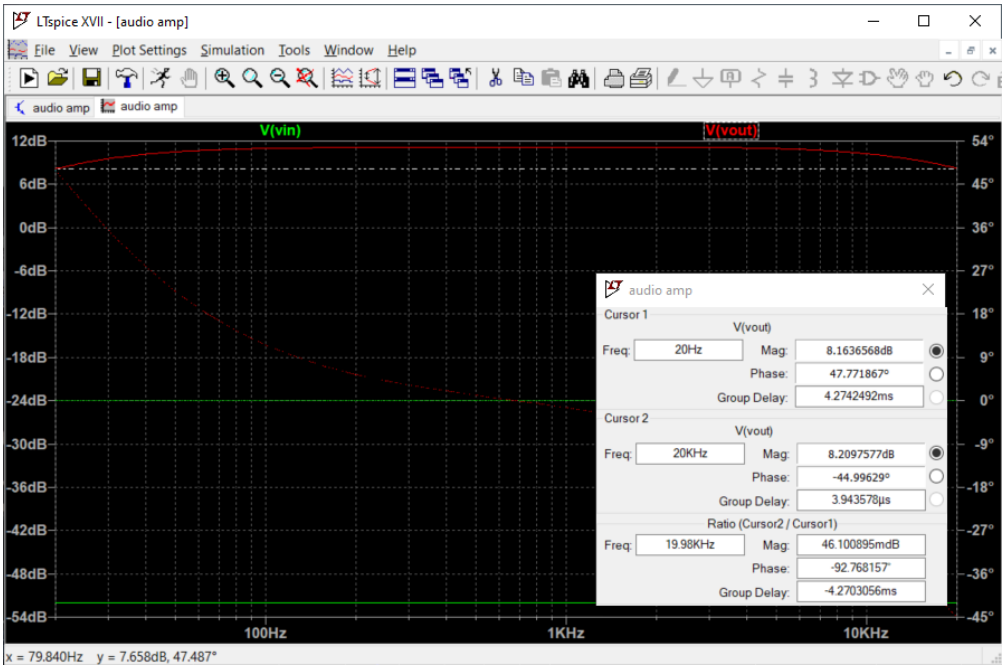


*Figure 6: Transient analysis of the entire circuit*


$$v_{out\ pp} = 5.869V$$

$$\boldsymbol{A_v} = \frac{v_{out\ pp}}{v_{in\ pp}} = \frac{5.869}{0.005} = \mathbf{1173.8V/V} \geq 300V/V$$

*Figure 7: Frequency analysis of the entire circuit*

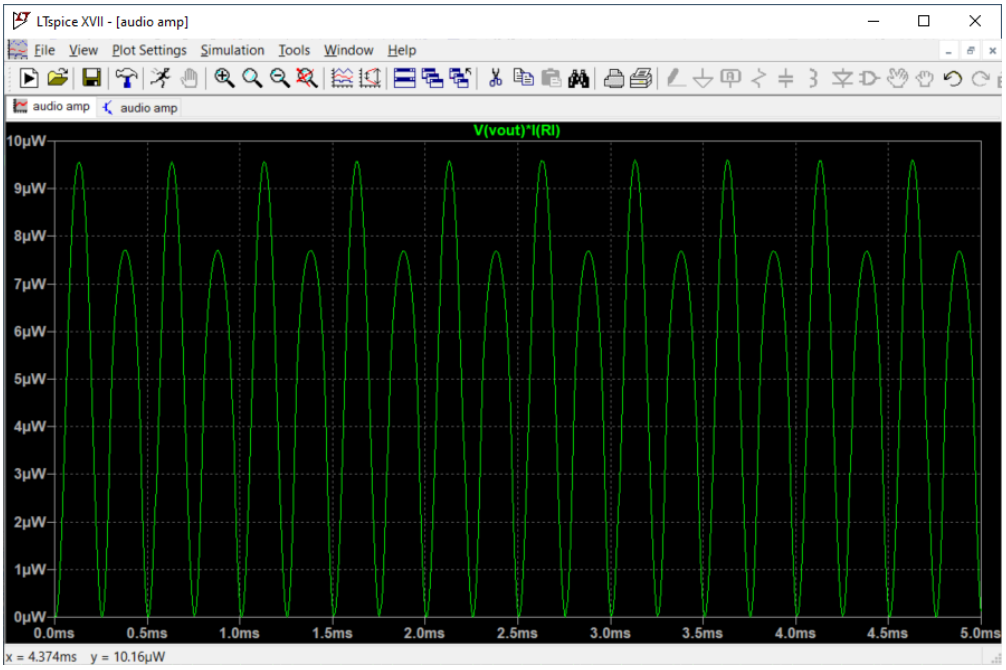


At $f_L = 20Hz, v_{out} = 8.164dB$

At $f_H = 20kHz, v_{out} = 8.210dB$

Highest magnitude $= 11.182dB$ at $1.255kHz$

*Figure 8: Total power consumption*




## Discussion:

The complete schematic of the audio amplifier is in Figure 3. In summary, it has a band-pass filter at the signal input, 3 of the same stages, a 4th different stage, and each stage is RC-coupled. All stages have the same specification NMOS ($0.8\mu m$ technology) and all are common source amplifiers. $V_{DD} = 12V$ and $V_{SS}$ is grounded $(0V)$. I chose lambda to be 0.001 and W/L to be 3. The load resistance is $1M\Omega$, which is the highest allowed value.

The input signal is $0.005V_{pp}$ and the output signal is $5.869V_{pp}$, so the amplifier yields an overall voltage gain of $1173.8V/V$ which is greater than the minimum required gain of $300V/V$. For the first, second, and third stages, the voltage gain is $6.463V/V$, and for the final stage, the voltage gain is $5.225V/V$. These values were calculated using the transient analysis from Figures 4-6.

From the frequency analysis (Figure 7), we learn that at $20Hz$, which is the required max $f_L$, the magnitude of the output voltage is 8.164dB. At $20kHz$, which is the required minimum $f_H$, the magnitude of the output signal is 8.210dB. Through a quick scan of the analysis graph, the highest magnitude is $11.182dB$. Since $11.182 - 8.164 = 3.022dB \approx 3dB$

and $11.182 - 8.210 = 2.982dB \leq 3dB$, then bandwidth is at least between $20Hz$ and $20kHz$. Although $3.022dB$ isn't exactly less than or equal to $3dB$, the difference is very small.

Finally, the total power consumption is less than $200mW$, as shown in Figure 8.

While designing the circuit, I had to deliberately choose $\lambda$ and $\frac{W}{L}$. Additionally, for each stage, I picked the desired $V_G, V_S, V_D$, and $I_D$ in order to get the correct resistor values. I found that having gate voltage and drain voltage very similar while staying in the saturation region provided a more ideal voltage gain. I also choose the values of $R_L$, $V_{DD}$, and $V_{SS}$. For the capacitors between the stages they simply had to be large enough to block DC voltage, but I noticed that for stages 1-3, adjusting the $C_S$ to $50\mu F$ increased voltage gain. I also decided to use only NMOS transistors because I read that they are quicker than PMOS ones.

## Conclusion:

In this experiment, I learned how to design a multi-stage MOSFET amplifier from scratch, which involved choosing the gate, source, drain voltages, and drain current to get an appropriate voltage gain from each stage, and then coupling them together to satisfy the voltage gain requirement. Difficulties included deciding the correct type of amplifier (common source), choosing the right layout of the stage (which components go where), choosing the best assumed values to start with, and tweaking capacitor values on LTSpice to see how the voltage gain responded from those changes. The goal of this lab was achieved.

## Post-lab Questions:

1. The advantages of using multistage amplifiers as opposed to single-stage amplifiers includes being able to achieve a very high gain, power efficiency, and being able to design properties like input and output resistance. The disadvantages are that they are more expensive and more complex to design.
2. If VDD and VSS were 10V, then the overall voltage gain would decrease. Additionally, gate and drain voltage will decrease.
3. If the overall voltage amplification was increased to 500V/V, this design would fulfill this new requirement.