NRZI recody: Activates the module stream: The bit stream out: The output strum out

Bit Statter Takes in a parallel 24 bit deput, and outjouts a bitstream that have been bit started . ready: Activate, module . parallel In: The 29-bit deput · out : Output - finished: Asserted when some processing the April wreset-n/ ones (0 -- t=0, index=0, finithed=0 Lecary Servin wheel & mes (mit !=6% ready e arthisted & Mde == 24/ oneslount==6/
oneslount=0,
out=0 ready anthrished k ready & ones Court!e 6/ afterished & sep Out, mor Index ~ house(Draw) & ans (mali = 2) ready & afairled & parallel Chilex J & signals orly (sunt =0 ent land in there aren't ilec Ones (see-t checities are l not asserted

CRCS realy: Actilotes module parallelly: 11 bit symt dre: done adjulting cpcs ont: Thirs
ont: Thirs GOLNG) D/STAGES MAIT 14dA==0) D Shu 4010 retu com Michael (%) Course المعصلي كم الراد المعمل reset_1 reset a D 5-th flyken MACK ری RG] paralle(In Ender) **@[**6] CijD Q[2] GC3] fledy R 5ti4 Ciny DC:3 D(3J D [47 P[0] [<]

Reverse

Reverses an injust.
Usage is changing MSB first to LSB tiest and vice-versa

[6:1-4101m] KI महि) मिक्र मिर्ड मिर्ड कार्ड के Caltio Caltio Caltio Caltio Caltio out[mbth-1:0]

Our Packet Datapath CRCnown address endport Reverse paralk(In mady rætu. paralli [15:11] [10:7] [6:2] BHJTCHER filished endpoint fuhished peruse | WREI_Ste urzz-redy ckc_in [10:4] [3-0] stream Brie Bri Newy Moth resetu NRZI NP21 mr 0 BS SEO out sudsto-NRZI_out bes CRC-in CRC-ready parallel In resetu pro [i] B] resetu CRC5 out ومدلماء CRC-out wres. DP whes. DM

Assume CRC. redy FSM nd NRZI mady on ~nsetu/ always asserted after enable =0 beay asserted. syrc_rdex = 4d15 WAIT s Yrc-dine = 160 StartOct SEO. must = 4/60 fonited act = 0 enazeo = o icle =0 START /CPC may /enable=1 NRZZruly & S perel NKSI SAM Send SYNC SYNLANIX ==1/ SEUCHAR) redy =1 2 mixed Pathisted/ mished out = (enable=0 send Data local RZI Pata SED-court < 1/finished & A Mor SEO_ court SEO-count < 2 IDLE send seo-1 send SFO SEC-GUMT >= 3