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| R | N | Function | Description | | | | | Alternative function | | | Description |
| 1 | 00 | ALU\_I0 | ALU Am2901 operand source selector | | | | | | | | |
| 01 | ALU\_I1 |
| 02 | ALU\_I2 |
| 03 | ALU\_I3 | ALU Am2901 function selector | | | | |  | | | |
| 04 | ALU\_I4 |
| 05 | ALU\_I5 | ALU\_nDE | Enable ALU\_D mux output (zero otherwise) | | |
| 06 | ALU\_I6 | ALU Am2901 shift/result selector | | | | |  | | | |
| 07 | ALU\_I7 |
| 2 | 08 | ALU\_I8 | XCSEL4 | Carry result bit selector | | |
| 09 | ALU\_C0 | Carry in LSB ALU | | | | | | | | |
| 10 | AMXR | Select Am2901 port A from PDP-11 instruction Rs/Rd fields | | | | | | | | |
| 11 | BMXR | Select Am2901 port B from PDP-11 instruction Rs/Rd fields | | | | | | | | |
| 12 | AMX0 | Am2901 Port A selection address | | | | |  | | | |
| 13 | AMX1 | ARS | PDP-11 opcode Rs field to Am2901 port A | | |
| 14 | AMX2 |  | | | |
| 15 | AMX3 |
| 3 | 16 | BMX0 | Am2901 Port B selection address | | | | |
| 17 | BMX1 | BRD | PDP-11 opcode Rd field to Am2901 port A | | |
| 18 | BMX2 |  | | | |
| 19 | BMX3 |
| 20 | MCI0 | Am29811 sequencer microinstruction | | | | | | | | |
| 21 | MCI1 |
| 22 | MCI2 |
| 23 | MCI3 |
| 4 | 24 | OR\_nEN | Am29811 OR conditions enable, target address is OR-ed with value selected by OMX mux | | | | | | | | |
| 25 | CC0 | Condition Code selector for Am29811 TST entry | | | | | | | | |
| 26 | CC1 |
| 27 | CC2 |
| 28 | CC3 | Inversion for Am29811 TST entry | | | | | | | | |
| 29 | RC0 | RC0=1 - PSW[3:0] strobe, RC0 & RC1 & RC2 - PSW[7:4] strobe | | | | | RC0=0 - register control | | | |
| 30 | RC1 | if RC0=1, NZVC selector | | | | | if RC0=0, microinstruction address register load | | | |
| 31 | RC2 | if RC0=1, NZVC selector | | | | | if RC0=0, PDP-11 instruction register load | | | |
| 5 | 32 | RC3 | if RC0=1, C selector | | | | | if RC0=0, TTL output strobe enable | | | |
| 33 | DMX0 | Am2901 D input mux selector | | | | | | | | |
| 34 | DMX1 |
| 35 | CLK\_nEN | Clock enable | | | | | | | | |
| 36 | IO\_nEN | Enable IO operation | | | | | | | | |
| 37 | DOUT | Q-Bus DOUT | | | | | | | | |
| 38 | ~SYNC | Q-Bus SYNC, low level sets SYNC active | | | | | | | | |
| 39 | WRPLY | Wait Q-Bus RPLY wait completion | | | | | | | | |
| 6 | 40 |  |  | D0 | ALU\_D  constant constant |  | | IAKO | I/O operation type | | |
| 41 | OMX0 | OR conditions Am29811 selector | D1 | DIN |
| 42 | OMX1 | D2 | ~RDIN |
| 43 | OMX2 | D3 | WTBT |
| 44 | NAF0 | Next address field | D4 | SMX0 | Shift in/out bit control | | |
| 45 | NAF1 | D5 | SMX1 | ASLB | RAMU | 0010 1X11 1001 |
| 46 | NAF2 | D6 | SMX2 | ROLB | RAMU | 0010 1X11 1011 |
| 47 | NAF3 | D7 | SMX3 | ASL | RAMU | 0011 1X10 1001 |
| 7 | 48 | NAF4 | D8 | SMX4 | ASHCL | RAMQU | 0011 1010 1010 |
| 49 | NAF5 | D9 | SMX5 | ROL | RAMU | 0011 1X10 1011 |
| 50 | NAF6 | D10 | XCQ0 | TTL control  register | SMX6 | RORB | RAMD | 0101 X1X1 11XX |
| 51 | NAF7 | D11 | XCQ1 | SMX7 | ASRB | RAMD | 0111 X1X1 0X?0 |
| 52 | NAF8 | D12 | XCQ2 | SMX8 | ROR | RAMD | 1001 X101 11XX |
| 53 | NAF9 | D13 |  | | SMX9 | ASR | RAMD | 1011 X101 0110 |
| 54 | NAF10 | D14 | SMX10 | ASHXR | RAMQD | 1111 0101 0101 |
| 55 | NAF11 | D15 | SMX11 | ASHCR | RAMQD | 1111 0101 0101 |

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| I[8:6] | RAM | | QREG | | Y |  | I[6:4] | Function |  | I[2:0] | R | S |  | OMX | Description |
| Dst | Shift | Load | Shift | Load | Function | Src |
| 0 | - | - | - | Fi | F |  | 0 | R + S |  | 0 | A | Q |  | 0 / MD | destination mode |
| 1 | - | - | - | - | F |  | 1 | S - R |  | 1 | A | B |  | 1 / MS | source mode |
| 2 | - | Fi | - | - | A |  | 2 | R - S |  | 2 | Z | Q |  | 2 / RR | 0, dst reg, src reg |
| 3 | - | Fi | - | - | F |  | 3 | R | S |  | 3 | Z | B |  | 3 / IV | interrupt vector |
| 4 | R | Fi+1 | R | Qi+1 | F |  | 4 | R & S |  | 4 | Z | A |  | 4 / LD | boot mode |
| 5 | R | Fi+1 | - | - | F |  | 5 | ~R & S |  | 5 | D | A |  | 5 / BT | 0, la0, byte |
| 6 | L | Fi-1 | L | Qi-1 | F |  | 6 | R ^ S |  | 6 | D | Q |  | 6 / TC |  |
| 7 | L | Fi-1 | - | - | F |  | 7 | ~R ^ S |  | 7 | D | Z |  | 7 / R67 | 0 if R6/R7 on A, 1 otherwise |

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| MC[3:0] | Name | Description | False | True |  | RC0 | RC[3:1] | Load registers |
| 0 | JZ | jump zero | D (must be zero) | |  | 0 | 0 | none |
| 1 | CJS | conditional call | PC | D, PUSH |  | 1 | pipeline = D |
| 2 | JMAP | jump map | D (map active) | |  | 2 | instruction = ALU\_D |
| 3 | CJP | conditional jump reg | PC | D |  | 3 | instruction = ALU\_D, pipeline = D |
| 4 | PUSH | push | PC, PUSH | PC, PUSH, LD CTR |  | 4 | TTL control |
| 5 | JSRP | conditional call reg | R, PUSH | D, PUSH |  | 5 | TTL control , pipeline = D |
| 6 | CJV | jump vector | PC | D |  | 6 | TTL control , instruction = ALU\_D |
| 7 | JRP | conditional jump reg | R | D |  | 7 | TTL control , instruction = ALU\_D, pipeline = D |
| 8 | RFCT | repeat ctr!=0 | F, CTR++ | PC, POP |  | 1 | 0 | N = F15, Z = ZH & (ZL | IR15), V = N ^ (PSW[0] / sh C), C = PSW[0] or sh C |
| 9 | RPCT | repeat reg ctr !=0 | D, CTR++ | PC |  | 1 | N = F15, Z = ZH & ZL, V = V16, C = C16 |
| A | CRTN | conditional return | PC | F, POP |  | 2 | N = F7, Z = ZL, V = V8, C = C8 |
| B | CJPP | cond jump reg / pop | PC | D, POP |  | 3 | PSW[7:0] = ALU\_F[7:0] |
| C | LDCT | load ctr | PC, CTR = ALU\_F | |  | 4 | N = F15, Z = ZH & (ZL | IR15), V = N ^ (PSW[0] / sh C) , C = PSW[0] or sh C |
| D | LOOP | loop ctr | F | PC, POP |  | 5 | N = F15, Z = ZH & ZL,V = V16, no C change |
| E | CONT | continue | PC | |  | 6 | N = F7, Z = ZL, V = V8, no C change |
| F | JP | jump | D | |  | 7 | PSW[7:0] = ALU\_F[7:0] |

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| CC[2:0] | Cond |  | XCQ[2:0] | TTL |  | DMX[1:0] | Value |
| 0 | C |  | 0 | - |  | 0 | CTR, PSW |
| 1 | V |  | 1 | INITC |  | 1 | Q-bus |
| 2 | N |  | 2 | REFC |  | 2 | Immed MCR[55:4] |
| 3 | Z |  | 3 | REFS |  | 3 | Swap |
| 4 | CTR 255 |  | 4 | INITS |  |  |  |
| 5 | nIRQ |  | 5 | - |  |  |  |
| 6 | BERR |  | 6 | ACLOC |  |  |  |
| 7 | ACLO |  | 7 | EVENTC |  |  |  |