西南交通大學

嵌入式系统及应用

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第5章 三星S5P6818 简介及编程实例

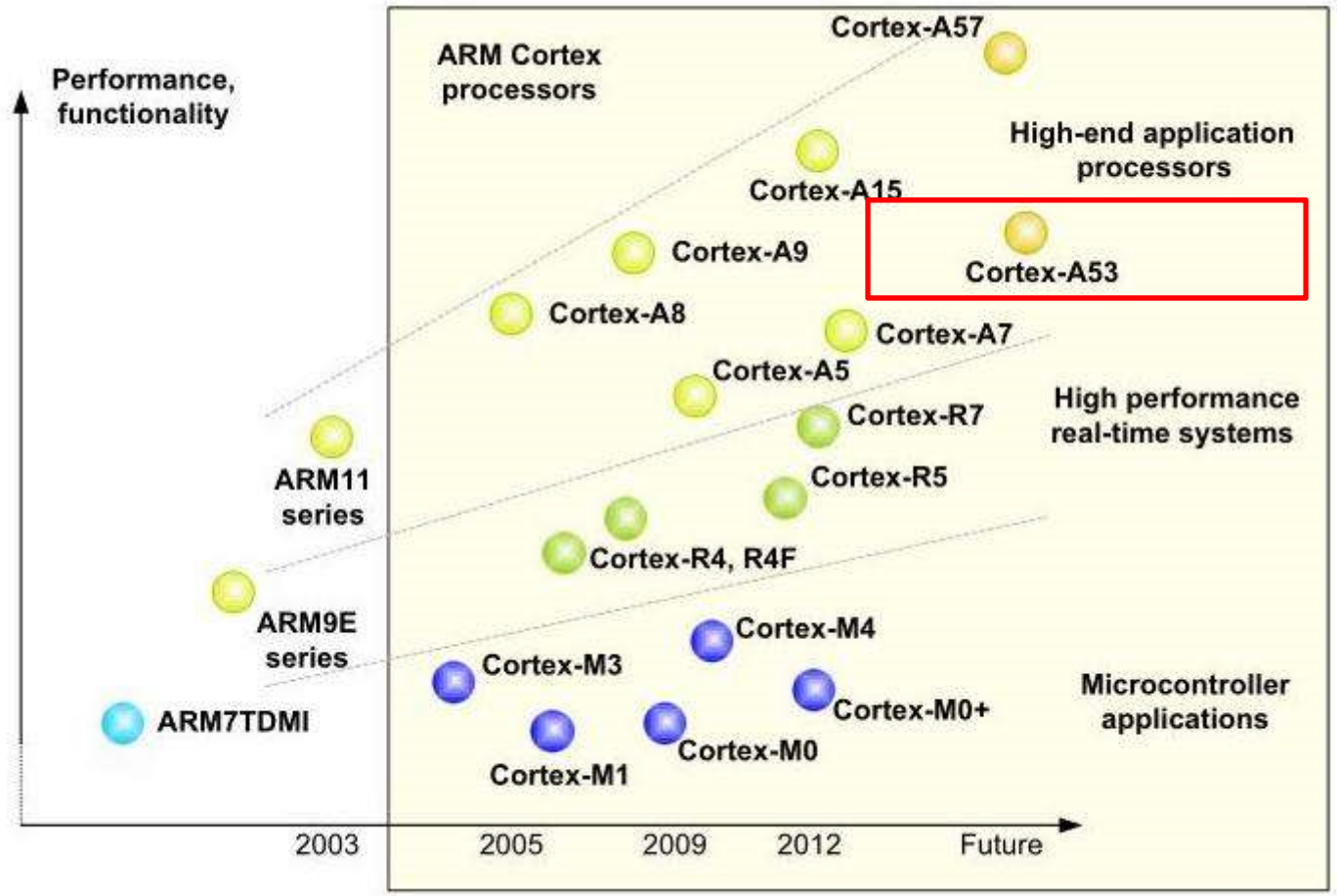
- 5.1三星S5P6818 SOC介绍
- 5.2 S5P6818 SOC编程实例
- 2学时

5.1 三星S5P6818 SOC介绍

- 5.1.1 S5P6818 SOC概述
- 5.1.2 S5P6818 SOC功能
- 5.1.3 S5P6818 SOC最小系统
- 5.1.4 S5P6818实验系统介绍

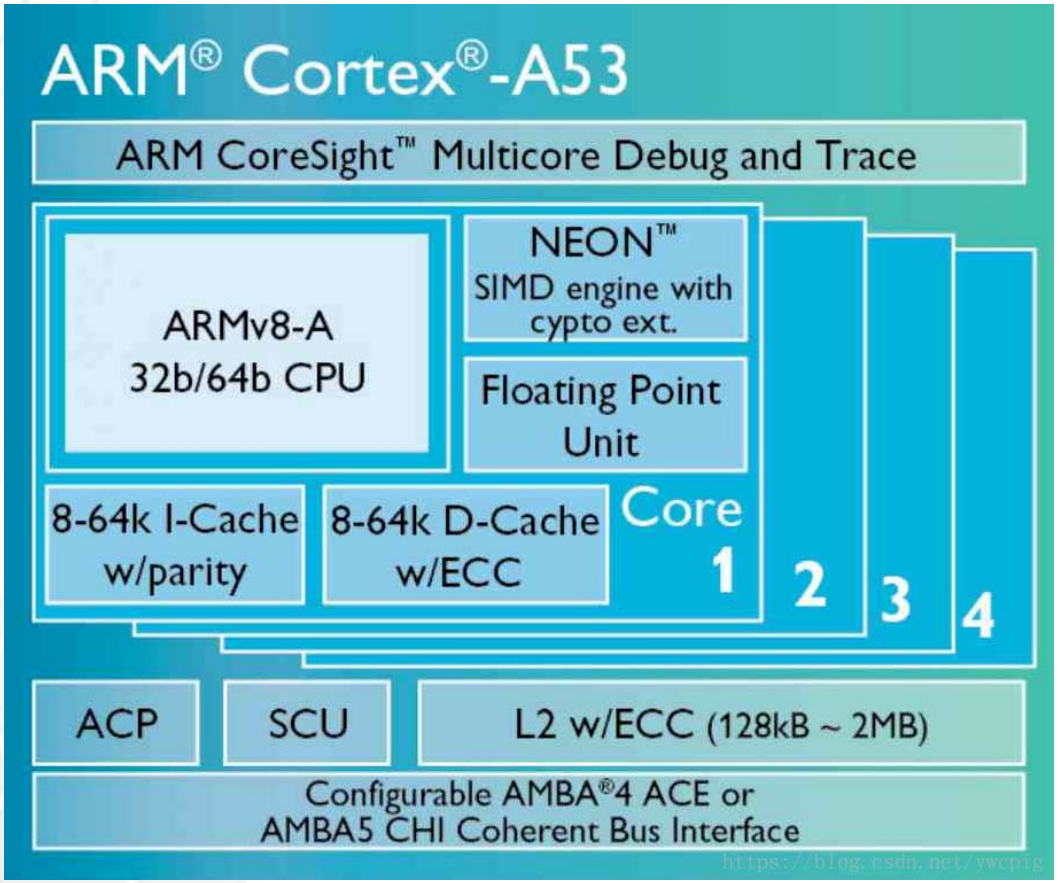
5.1.1 S5P6818 SOC概述

1、Cortex内核



5.1.1 S5P6818 SOC概述

2、Cortex-A53应用系统架构



- Cortex-A53是采取了ARMv8-A架构、支持多核
- 支持32位的ARMv7代码和64位代码的AArch64执行状态。
- 每个核心都必须使用DSP和NEON SIMD扩展
- 板载VFPv4浮点单元（每个核心）
- 功耗降低

5.1.1 S5P6818 SOC概述

3、Cortex-A53处理器特点

- Cortex-A53处理器，在高性能与低功耗领域的领先地位
- Cortex-A53是全球最小的64位处理器。可独立运作或整合为ARM big.LITTLE处理器架构。能够针对智能手机、高性能服务器等需求开发系统级芯片（SoC）。

5.1.1 S5P6818 SOC概述

3、 S5P6818 SOC概述

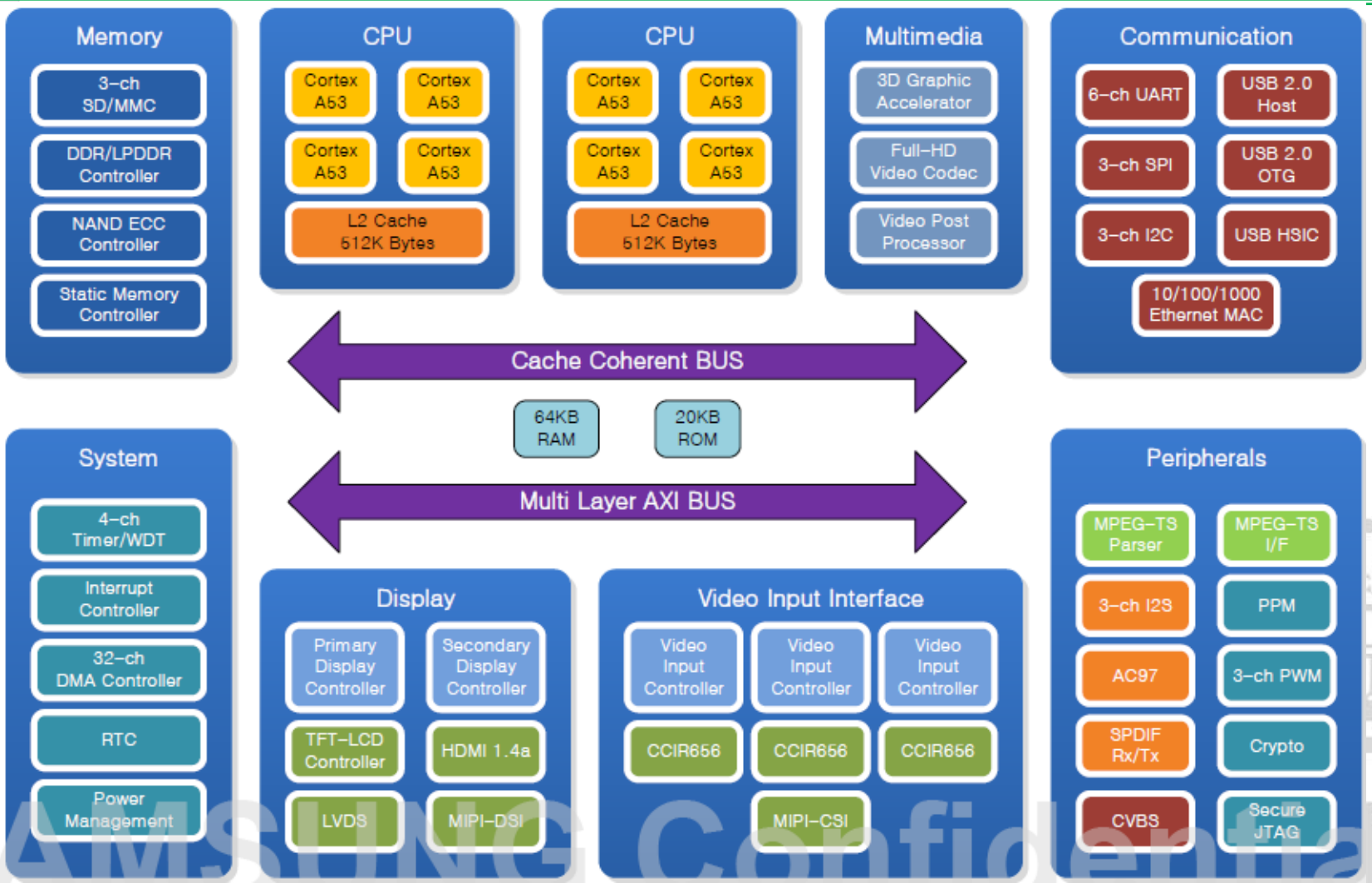
- 内核
  - 64位 ARM Cortex A53 8核处理器，32Kbyte I-Cache, 32Kbyte D-Cache per core，CPU频率为1.4Ghz，
  - 1MByte L2 Cache
  - VFP(Vector float-point Processor), Neon Processor per core
- 存储器
  - 支持LPDDR2/3 and DDR2/3 up to 4Gbytes
  - 支持SRAM, ROM and NOR flash，SLC/MLC NAND Flash，SD/MMC/eMMC
- 外设
  - 6x UART, 3x SPI, PPM, 3x I2C, 3x PWM, 2x MPEG-TS
  - 8x 12bit general purpose ADC等

5.1.1 S5P6818 SOC概述

- 多媒体
  - Multi-format video decoder
  - H.264 video encoder
- 3D Graphic
  - Enhanced 3D graphic processor
  - Supports OpenGL|ES 1.1/2.0, Open VG
- Security
  - ARM TrustZone : TZPC, TZASC and TZMA
  - Hardware crypto accelerator
  - Supports Secure boot and Secure JTAG

5.1.2 S5P6818 SOC功能

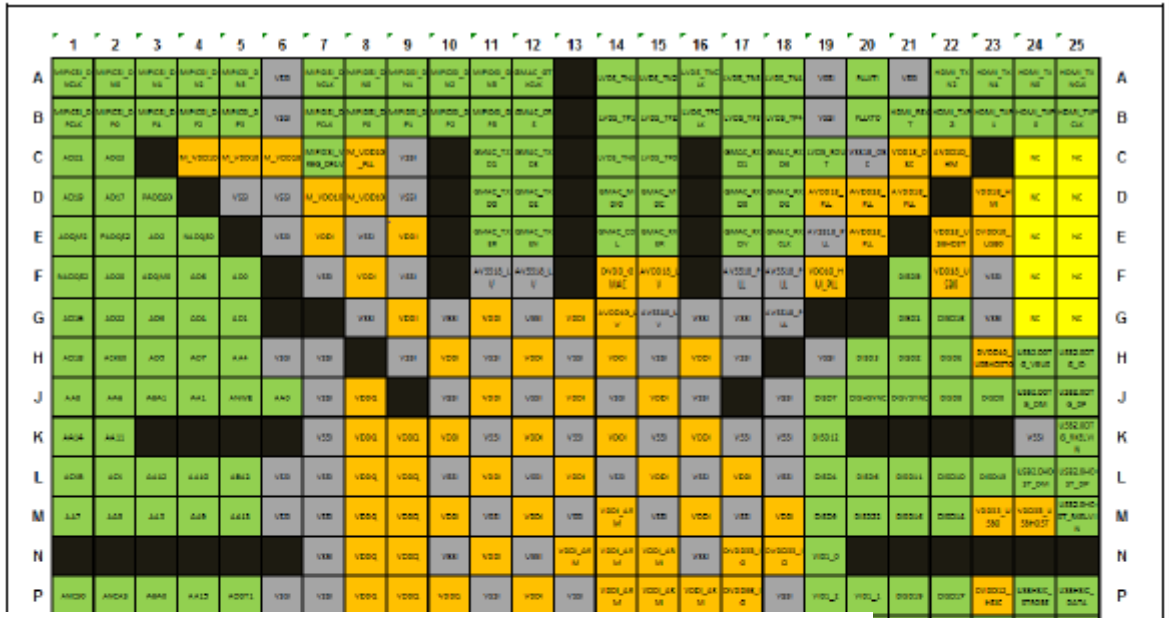
1、 S5P6818 SOC功能框图



5.1.2 S5P6818 SOC功能

❖3、S5P6818引脚图(FCBGA封装)

- 有的一个引脚定义多个功能



2.3 I/O Function Description

2.3.1 Ball List Table

Table 2-1 Ball Function Table

Ball	Name	Type	I/O	PU /PD	Alternate Function 0	Alternate Function 1	Alternate Function 2	Alternate Function 3
A1	MIPICSI_DNCLK	S	IO	N	MIPICSI_DNCLK			
A2	MIPICSI_DN0	S	IO	N	MIPICSI_DN0			
A3	MIPICSI_DN1	S	IO	N	MIPICSI_DN1			
A4	MIPICSI_DN2	S	IO	N	MIPICSI_DN2			
A5	MIPICSI_DN3	S	IO	N	MIPICSI_DN3			

5.1.2 S5P6818 SOC功能

1、自举配置

- 外部静态存储器自举
- 内部ROM自举
  - NAND自举(具有)
  - SD/MMC/SDFS自举
  - SPI串行EEPROM自举
  - UART自举
  - USB自举

Name	Pin	RST_CFG	Note	
BootMode[2:0]	SD[2:0]	RST_CFG[2:0]	Boot Mode Select	0 = Static Memory 1 = SDFS 3 = UART 4 = SPI 5 = SDMMC 6 = USB 7 = NAND

5.1.2 S5P6818 SOC功能

❖ 1）外部静态存储器自举配置

Pin Name	Function Name	Description
RST_CFG[2:0]	BOOTMODE[2:0]	Pull-down
RST_CFG[7:3]		Don't care
RST_CFG8	CfgSTLATADD	Static Latched Address (user select) 0 = None 1 = Latched
RST_CFG9	CfgSTBUSWidth	Static Bus Width (user select) 0 = 8-bit 1 = 16-bit
RST_CFG[24:10]		Don't care

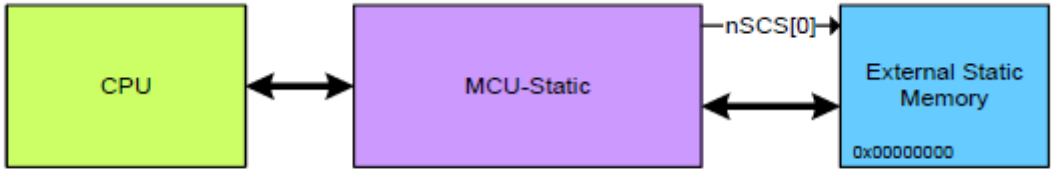


Figure 3-1 External Static Memory Boot

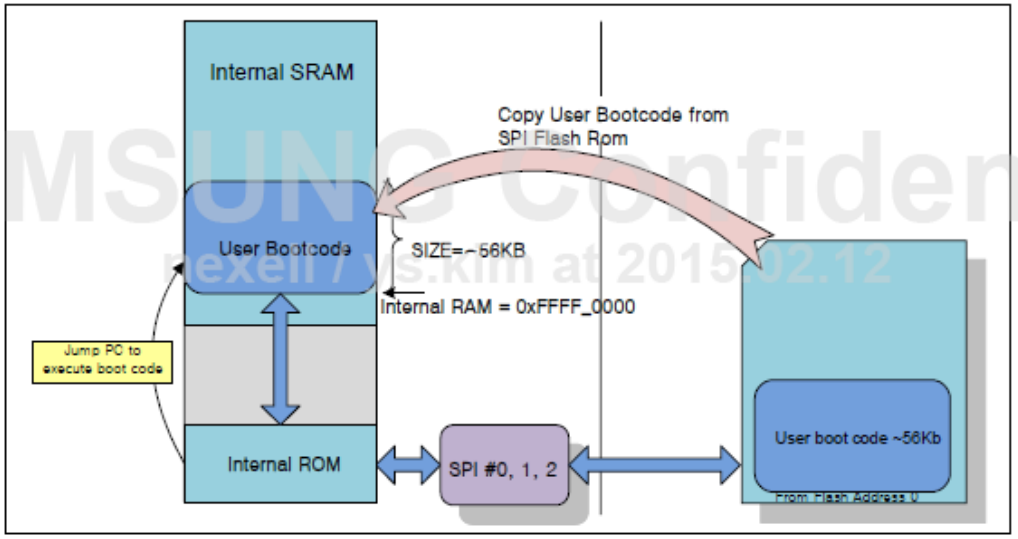
5.1.2 S5P6818 SOC功能

❖ 2）内部ROM自举自举配置

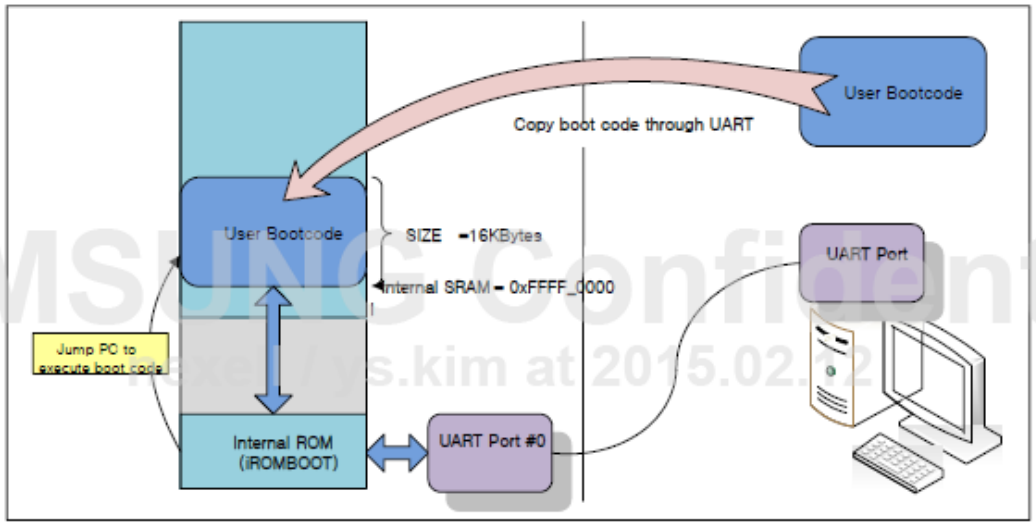
Pins	iROMBOOT					
	SDFS	UART	SPI Serial Flash	SDMMC	USB Device	NANDBOOT with Error Correction
RST_CFG[2:0]	BOOTMODE=1	BOOTMODE=3	BOOTMODE=4	BOOTMODE=5	BOOTMODE=6	BOOTMODE=7
RST_CFG[12:11]	Don't care					NANDTYPE[1:0]
RST_CFG[13, 10]						PAGESIZE[1:0]
RST_CFG[3]						SELCS
RST_CFG[17]	Don't care				OTG Session Check	Don't care
RST_CFG[6]	Don't care	Baud Rate	Speed	Should be Zero	Don't care	
RST_CFG[5:4]	Don't care		ADDRWIDTH[1:0]		Don't care	
RST_CFG[19, 3]	Port Number					
RST_CFG[14]	DECRYPT					
RST_CFG[15]	I-CACHE					
RST_CFG[8]	LATADDR					
RST_CFG[9]	Should be Zero (BUSWIDTH)					

5.1.2 S5P6818 SOC功能

SPIBOOT

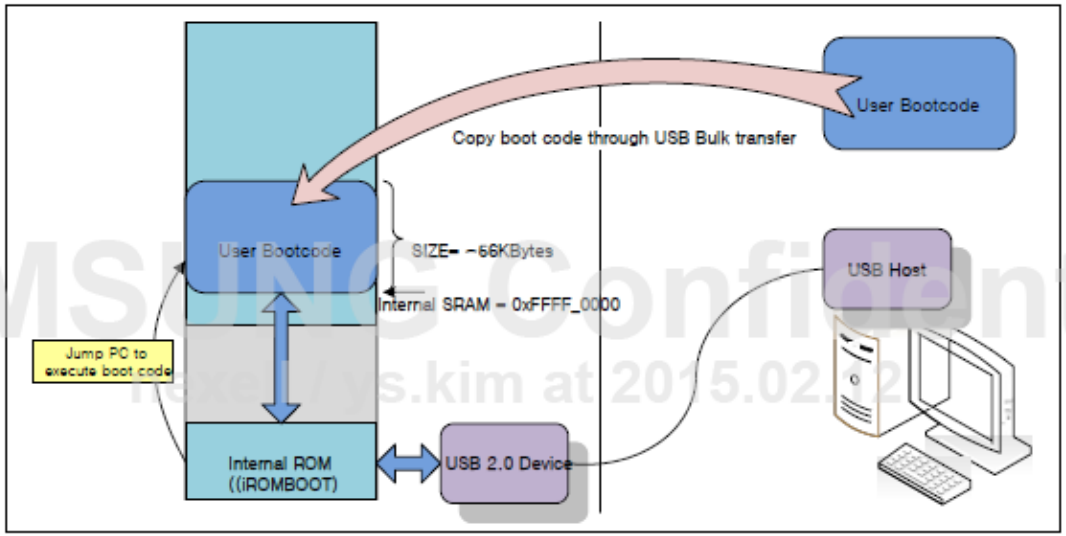


UARTBOOT

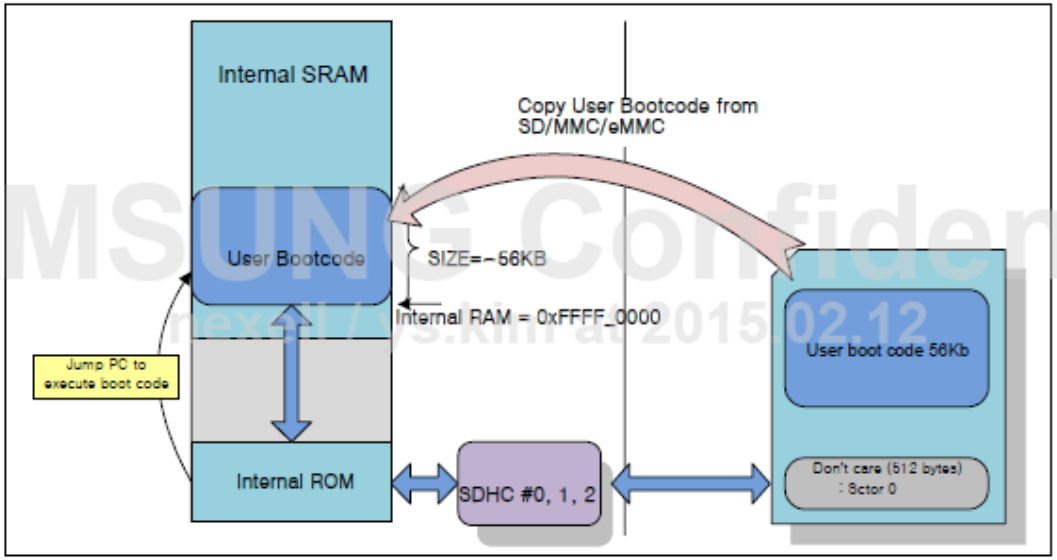


5.1.2 S5P6818 SOC功能

USB Boot

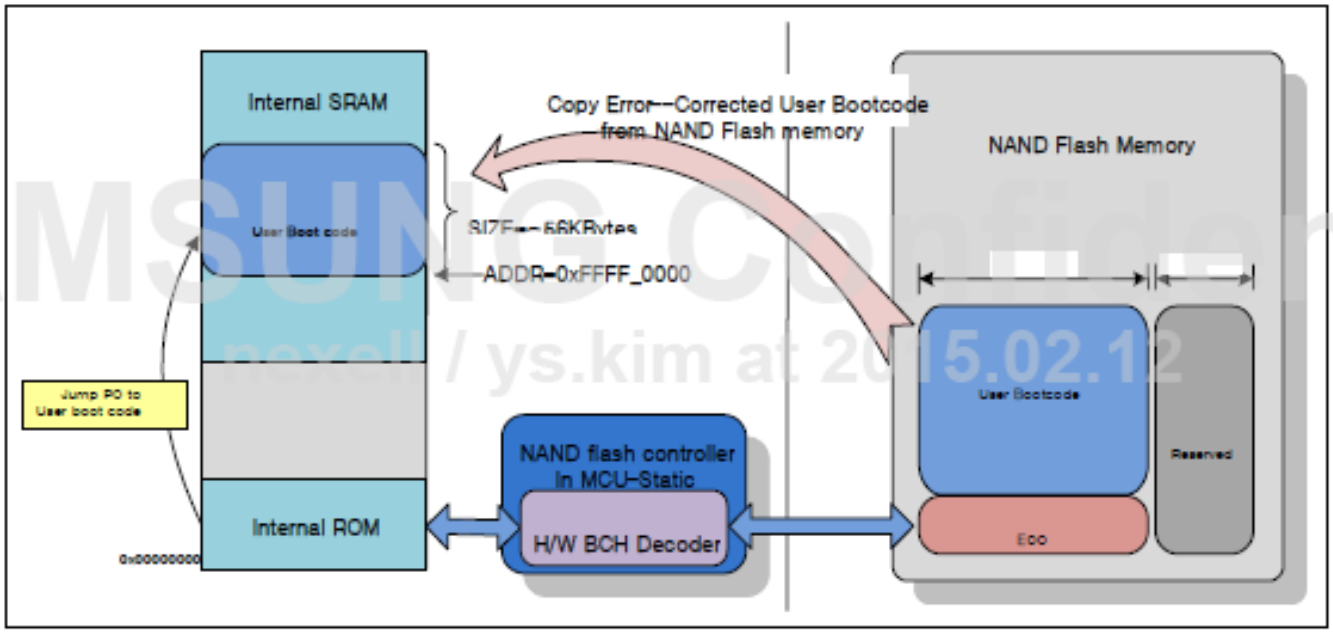


SDHC Boot



5.1.2 S5P6818 SOC功能

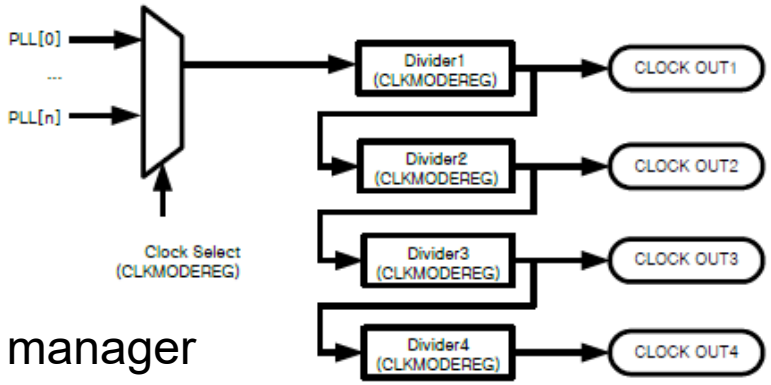
NANDBOOT with Error Correction



5.1.2 S5P6818 SOC功能

2、主时钟

- 5种时钟
  - FCLK——CPU， HCLK——CPU BUS,
  - MCLK—— Memory
  - BCLK—— SYSTEM BUS
  - PCLK—— PERIPHERAL BUS CLOCK

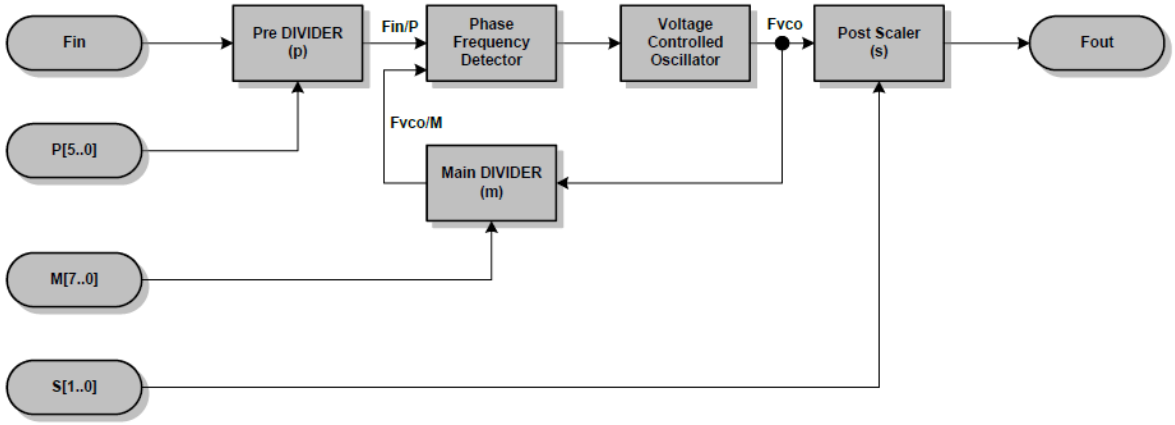


the clock manager

5.1.2 S5P6818 SOC功能

- 4个PLLs(X-TAL input of 24MHz)
  - PLL0—— 40 to 2500 MHz
  - PLL1—— 40 to 2500 MHz
  - PLL2 ——35 to 2200 MHz
  - PLL3—— 35 to 2200 MHz

Block Diagram of PLL



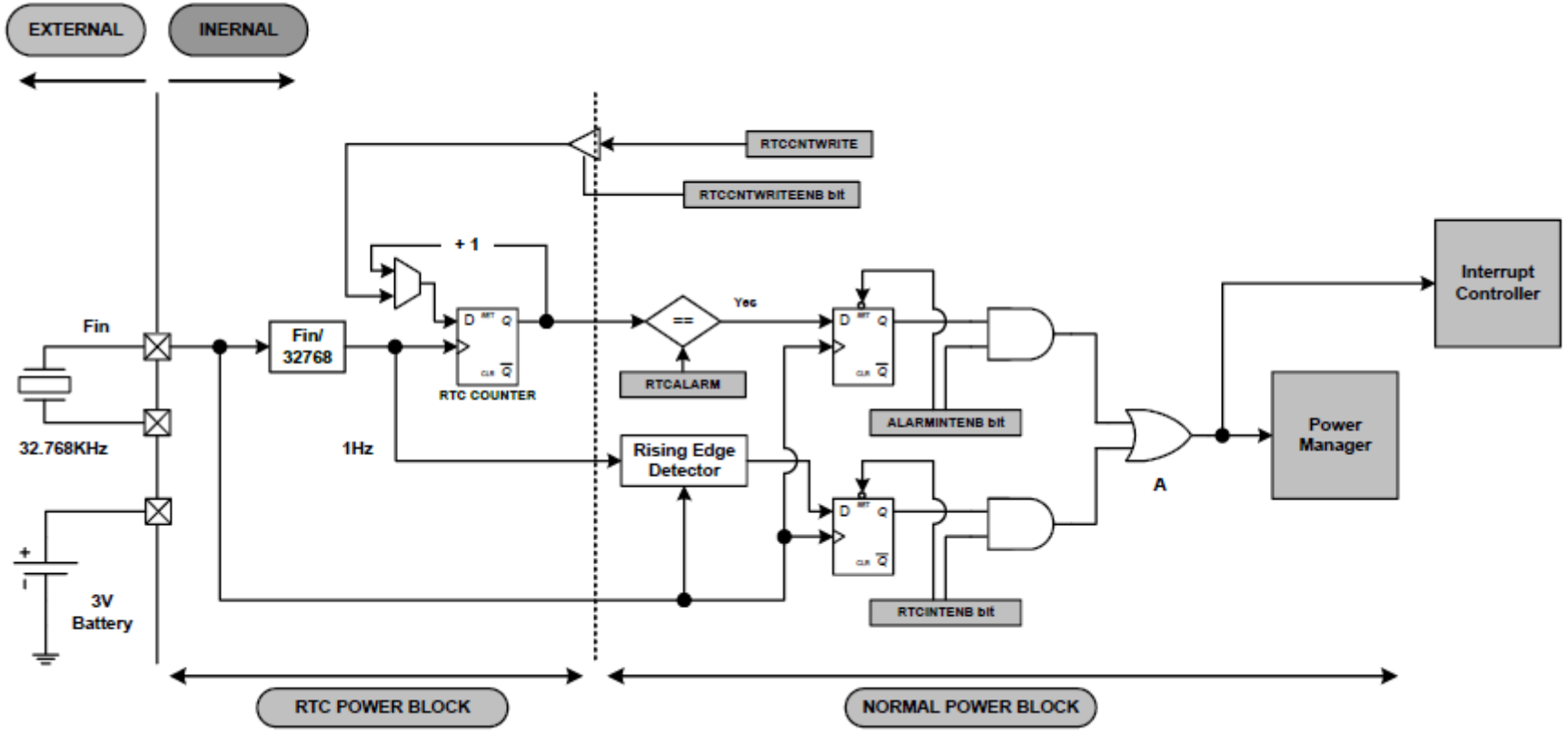
5.1.2 S5P6818 SOC功能

3、实时时钟（RTC）

❖特点：

- 使用external 32.768 kHz Crystal
- 32-bit Counter
- Alarm Function: Alarm Interrupt or Wake Up from Power Down Mode
- Independent power pin (VDD_RTC)
- Supports 1 Hz Time interrupt for Power Down Mode
- Generates Power Management Reset signal

5.1.2 S5P6818 SOC功能



RTC 框图

5.1.2 S5P6818 SOC功能

4、复位

- 4种复位
  - Power on Reset
  - Watchdog Reset
  - Software Reset(GPIO Reset)
  - Wake up(Idle, Stop)

5.1.2 S5P6818 SOC功能

5、中断控制器 (GIC)

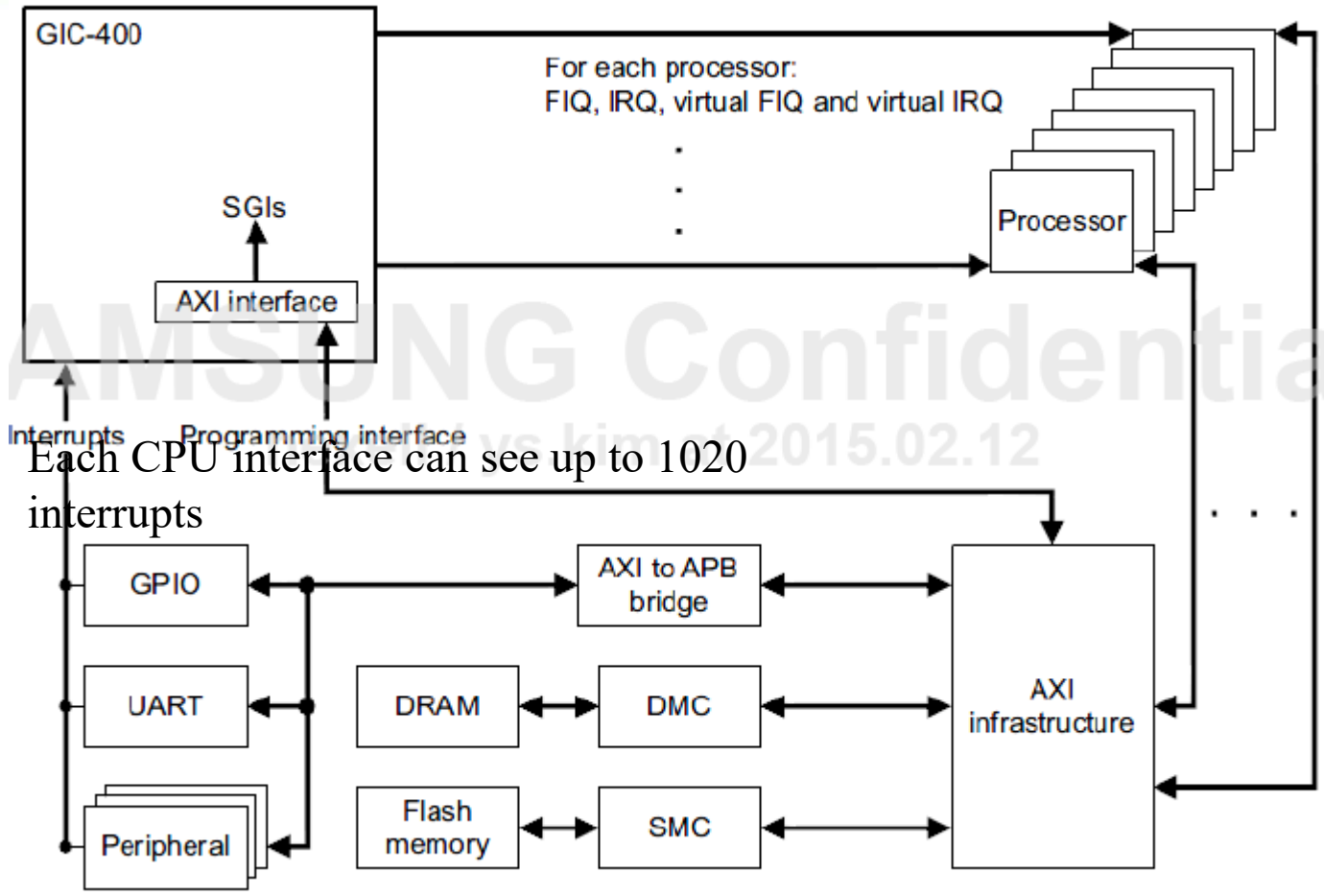
GIC支持中断类型

- 16 Software Generated Interrupt (SGIs)
- 6 external Private Peripheral Interrupt (PPIs) for each processor
- 1 internal PPI for each processor
- 128 Shared Peripheral Interrupt (SPIs)

中断处理模式

- SGIs 使用N-N模式
- 硬件中断使用1-N模式

5.1.2 S5P6818 SOC功能



GIC 功能框图

每个**CUP**可以看到**1020**个中断，

5.1.2 S5P6818 SOC功能

6、存储器控制器

- 统一存储体系结构（**UMA**）
  - MCU-A: DDR3/LVDDR3 (Low Voltage DDR3)/LPDDR3/LPDDR2
  - MCU-S: Static Memory

- MCU-A特点
  - 支持8/16/32-bit SDRAM of 2 Gbyte
  - Single Bank of Memory (32-bit data bus width)
  - 支持 Power down mode
  - 支持 Self Refresh mode

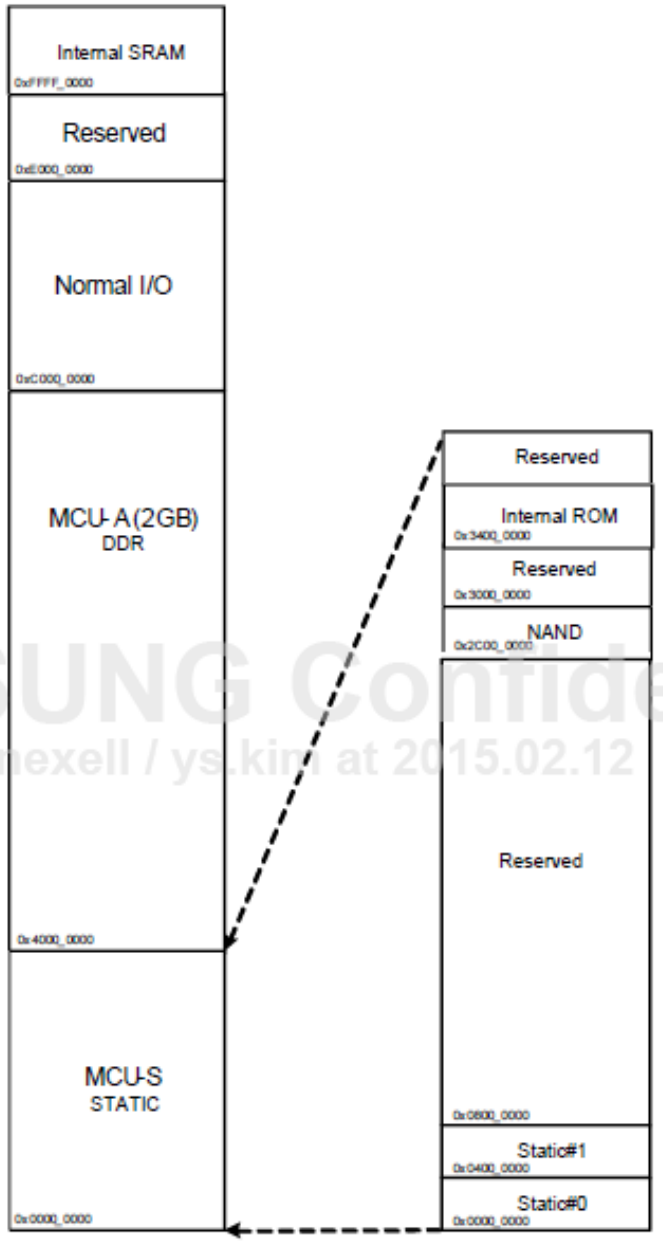
5.1.2 S5P6818 SOC功能

- MCU-S特点
  - Two Static Memory Chip Selects
  - NAND Flash Interface
  - 23-bit address supports using latch address
  - SLC NAND, MLC NAND with ECC (Supports BCH-algorithm)
  - Static Memory Map Shadow

5.1.2 S5P6818 SOC功能

存储器映射

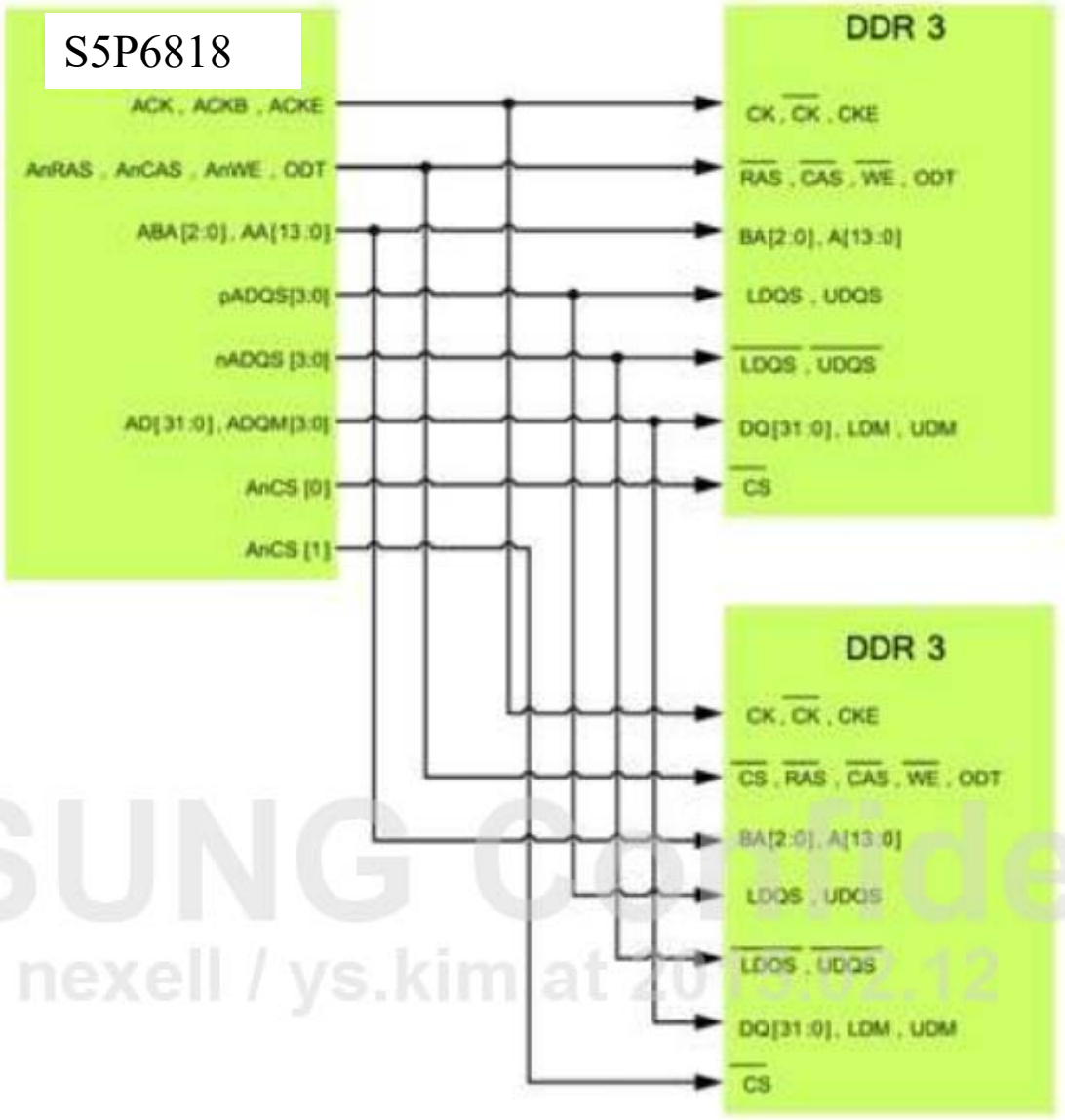
- 存储器分为SDRAM库（MCU-A）和static 库（MCU-S）



5.1.2 S5P6818 SOC功能

例： 32位SDRAM

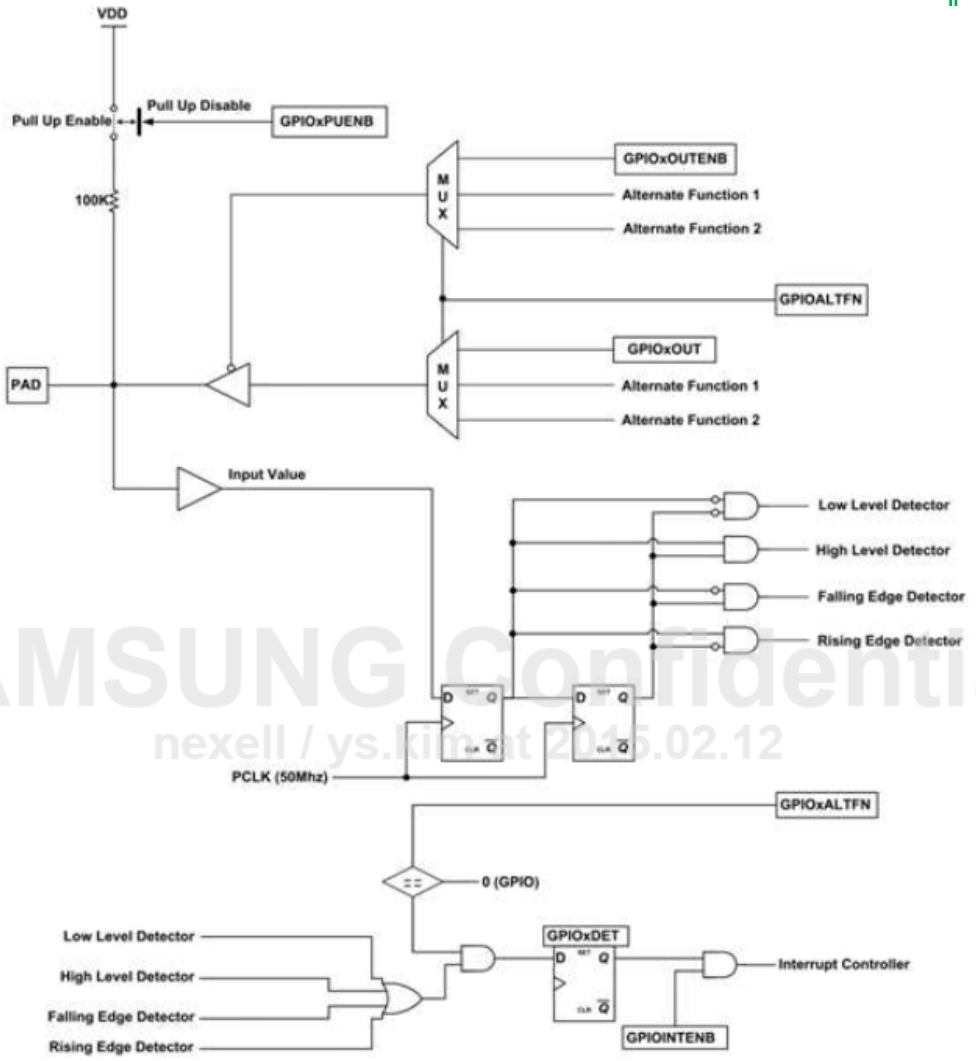
与MCU-A库接口



5.1.2 S5P6818 SOC功能

7、GPIO

- 特征
  - 可编程上拉
  - 边缘/电平检测
  - 160个GPIOs

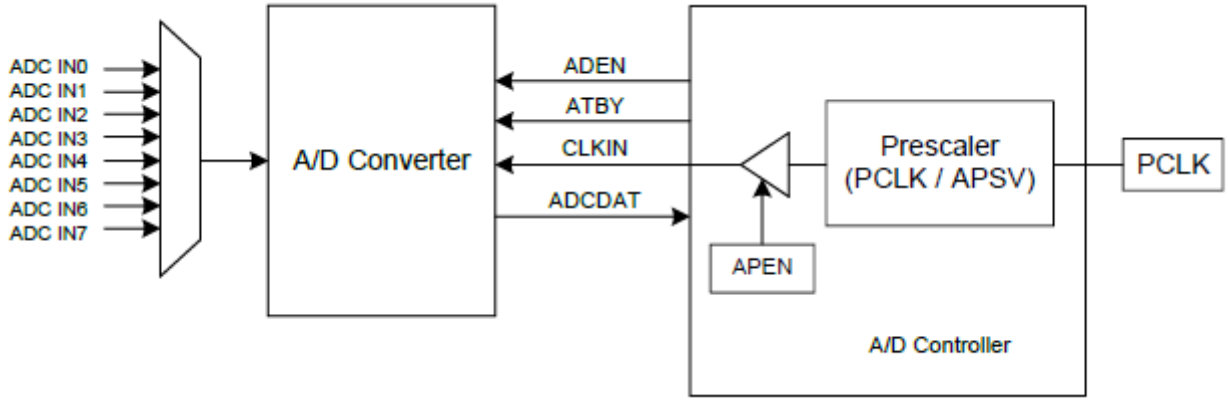


5.1.2 S5P6818 SOC功能

8、GPIO

特征

- 12位分辨率
- 1M最大采用率
- 0~1.8V模拟输入、DC~100kHz的输入频率
- 8个输入通道



5.1.2 S5P6818 SOC功能

A/D转换表

Index	ADC Input (V)	Digital Output	
0	~ 1 x LSB	0000_0000_0000	
1	1 x LSB ~ 2 x LSB	0000_0000_0001	
2	2 x LSB ~ 3 x LSB	0000_0000_0010	
~	~	~	1LSB = (VREF – AGND)/4096
2047	2047 x LSB ~ 2048 x LSB	0111_1111_1111	≒ 0.43945 mV
2048	2048 x LSB ~ 2049 x LSB	1000_0000_0000	
2049	2049 x LSB ~ 2050 x LSB	1000_0000_0001	VREF = 1.8 V (Typ.)
~	~	~	AGND = 0.0 V (Typ.)
4093	4093 x LSB ~ 4094 x LSB	1111_1111_1101	
4094	4094 x LSB ~ 4095 x LSB	1111_1111_1110	
4095	4095 x LSB ~ 4096 x LSB	1111_1111_1111	

5.1.2 S5P6818 SOC功能

9、 串口(UART)

- 特点：
  - 6个独立串口（Channel 0 to 5）
  - 所有串口支持基于中断操作
  - 串口1~串口5支持基于DMA的操作
  - 除串口2外，其他串口支持自动流控
  - 支持硬件握手操作

5.1.2 S5P6818 SOC功能

- 10、其他通信接口

- 网口（10/100/1000 Mbps）
- SD/MMC接口
- I2C接口、I2S接口
- SPI/SSP接口
- USB2.0 OTG/ USB2.0 host

- 其他外设：DMA、PWM、AC97、HDMI等请见数据手册和参考手册

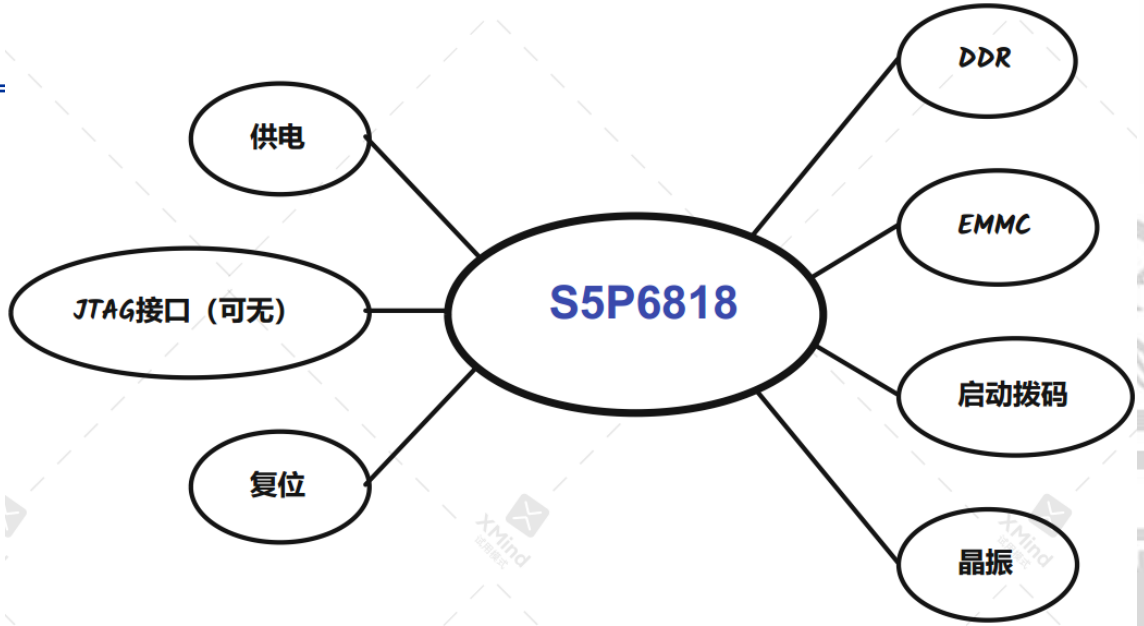
5.1.2 S5P6818 SOC功能

- **11、S5P6818典型应用**
  - 平板电脑
  - 智能手机

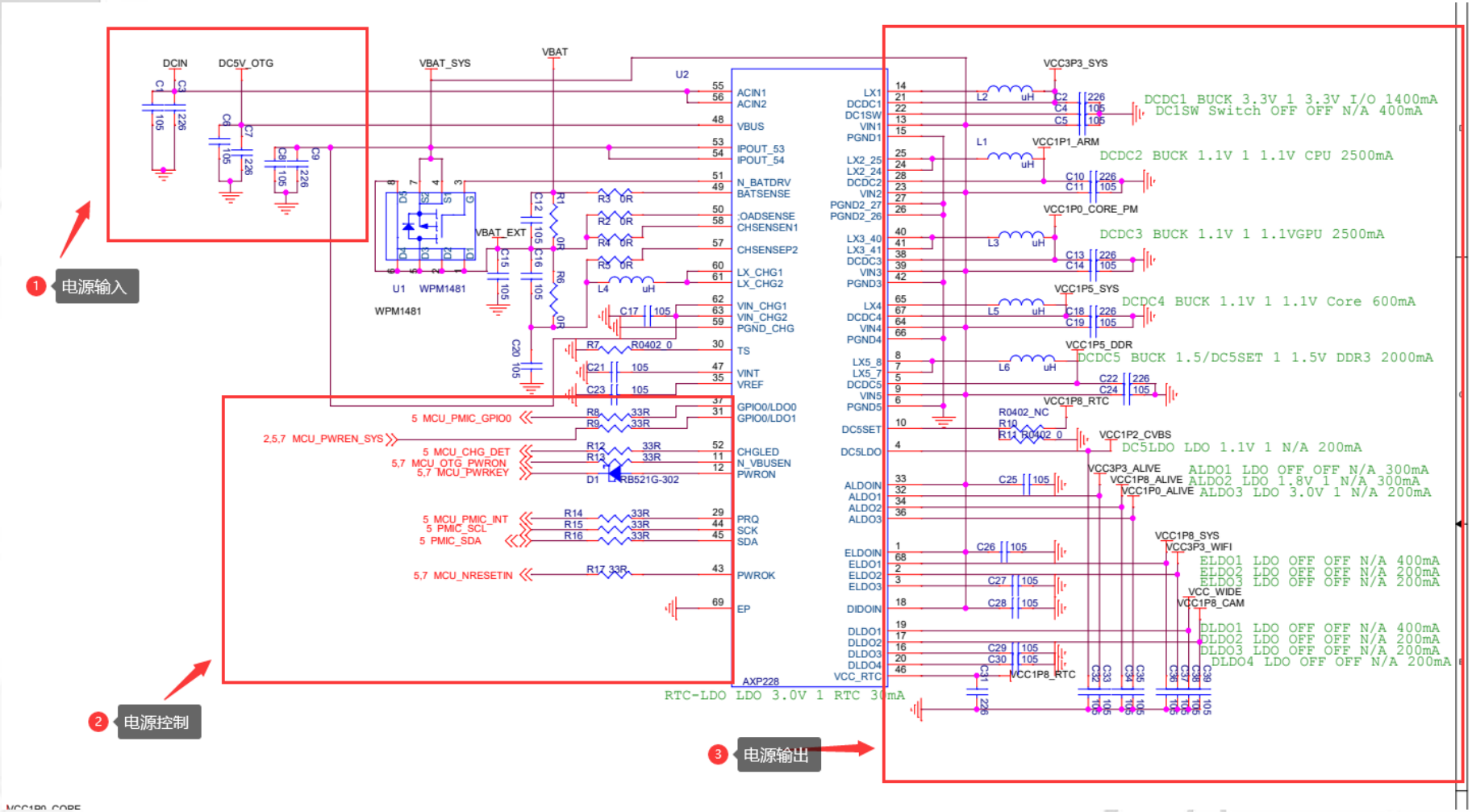
5.1.3 S5P6818 SOC最小系统

- **S5P6818最小系统**

- 电源
- 复位电路
- 存储器
- 时钟电路（外部晶振）
- Boot启动模式选择电路

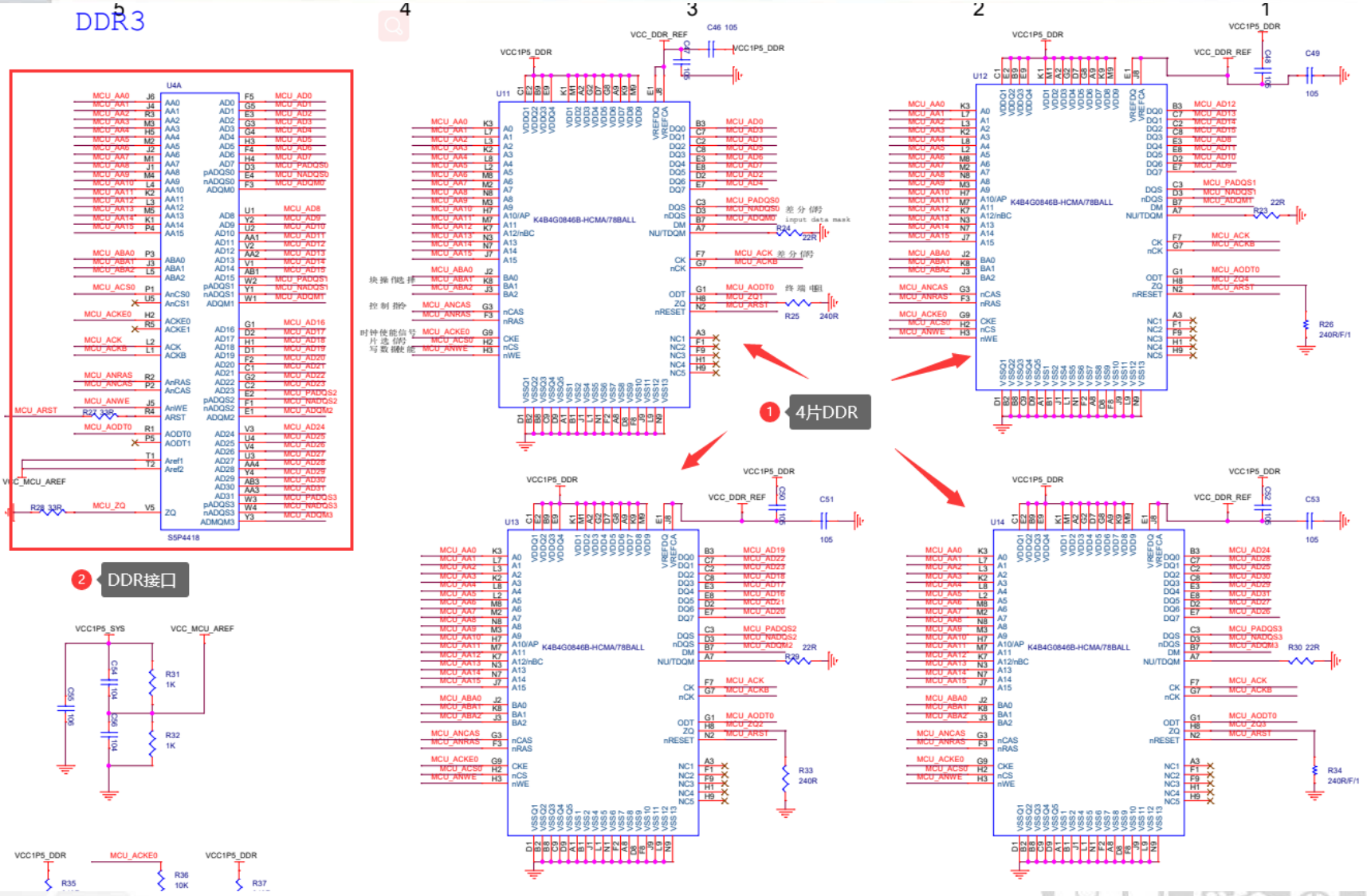


5.1.3 S5P6818 SOC最小系统

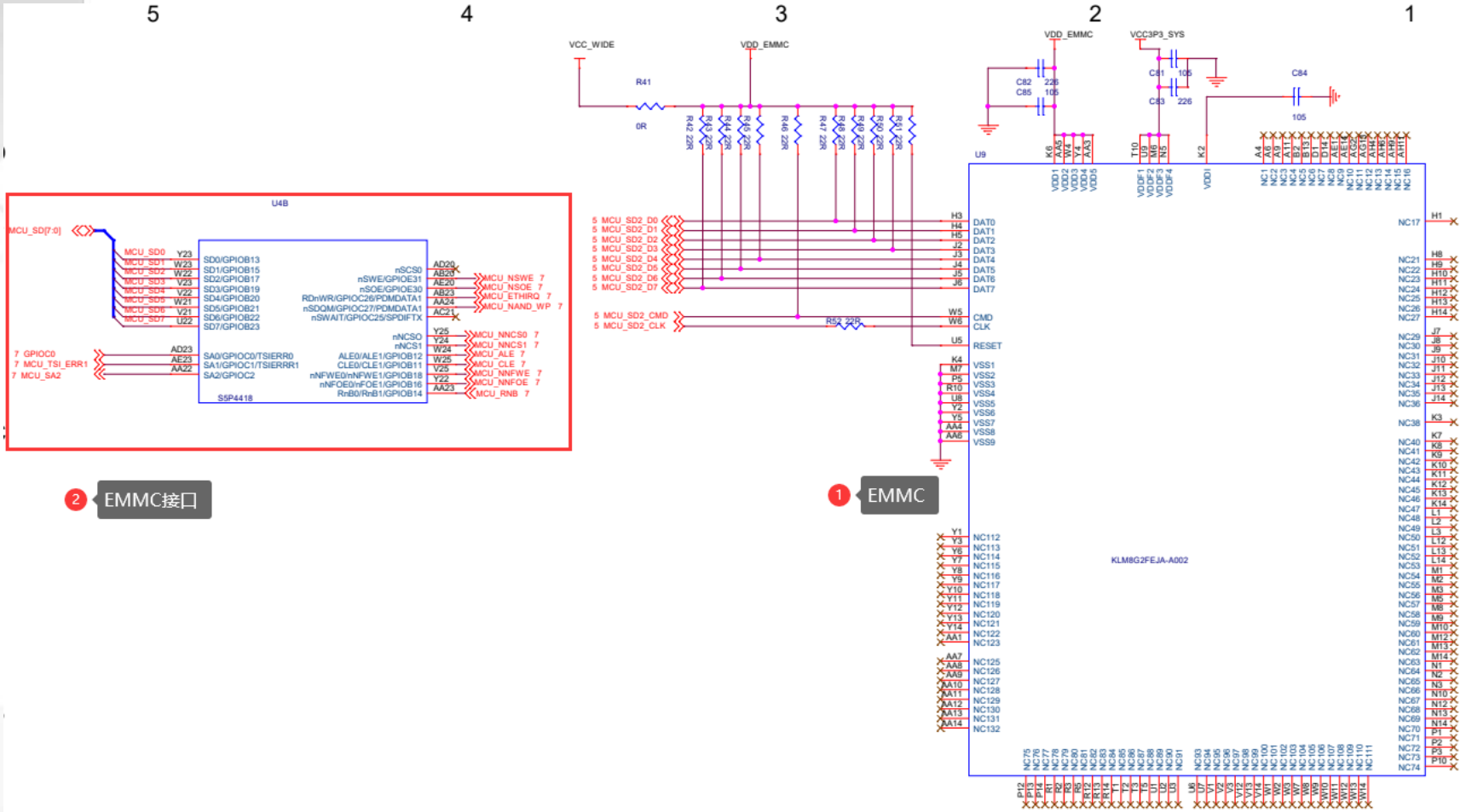


电源电路

5.1.3 S5P6818 SOC最小系统

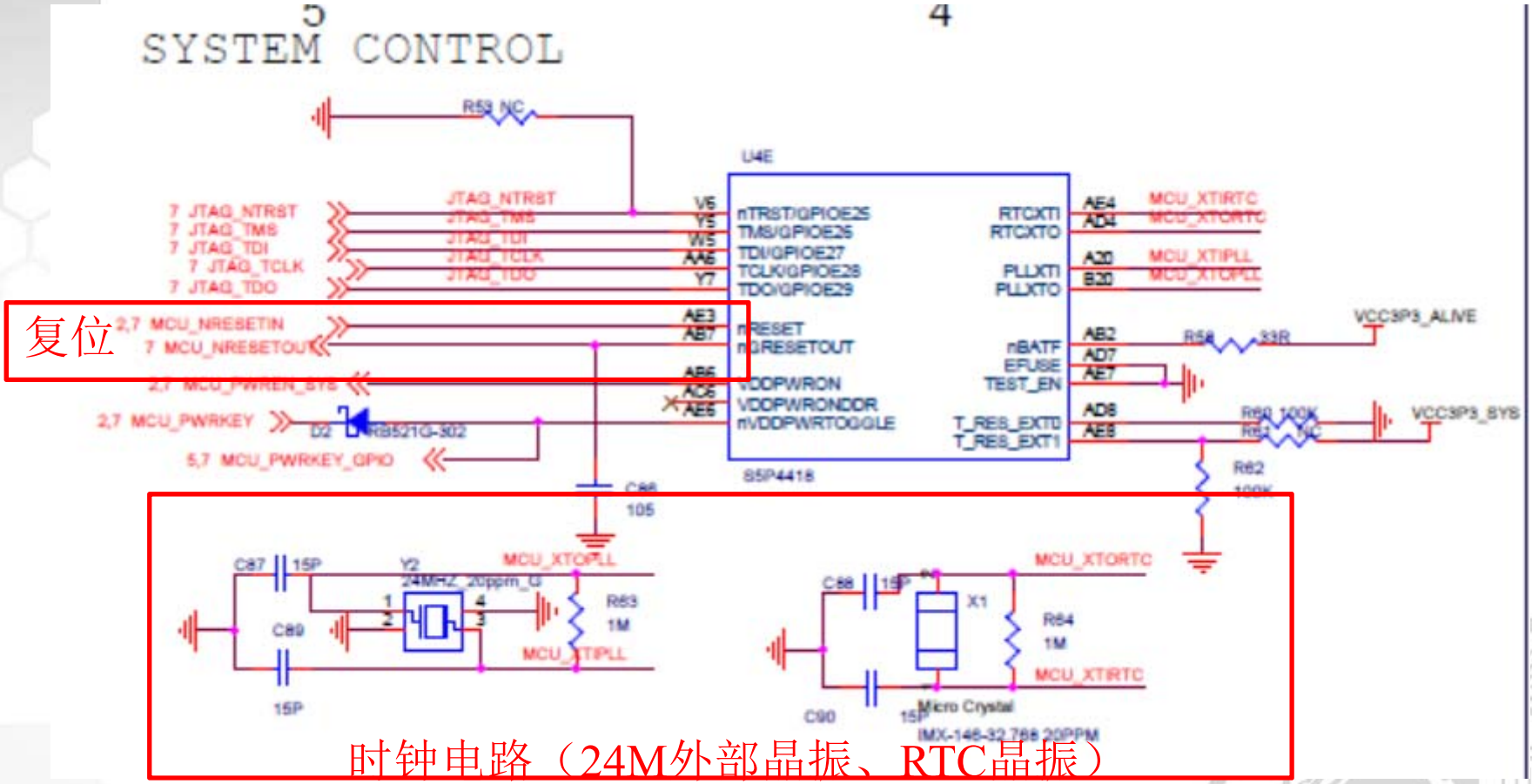


5.1.3 S5P6818 SOC最小系统

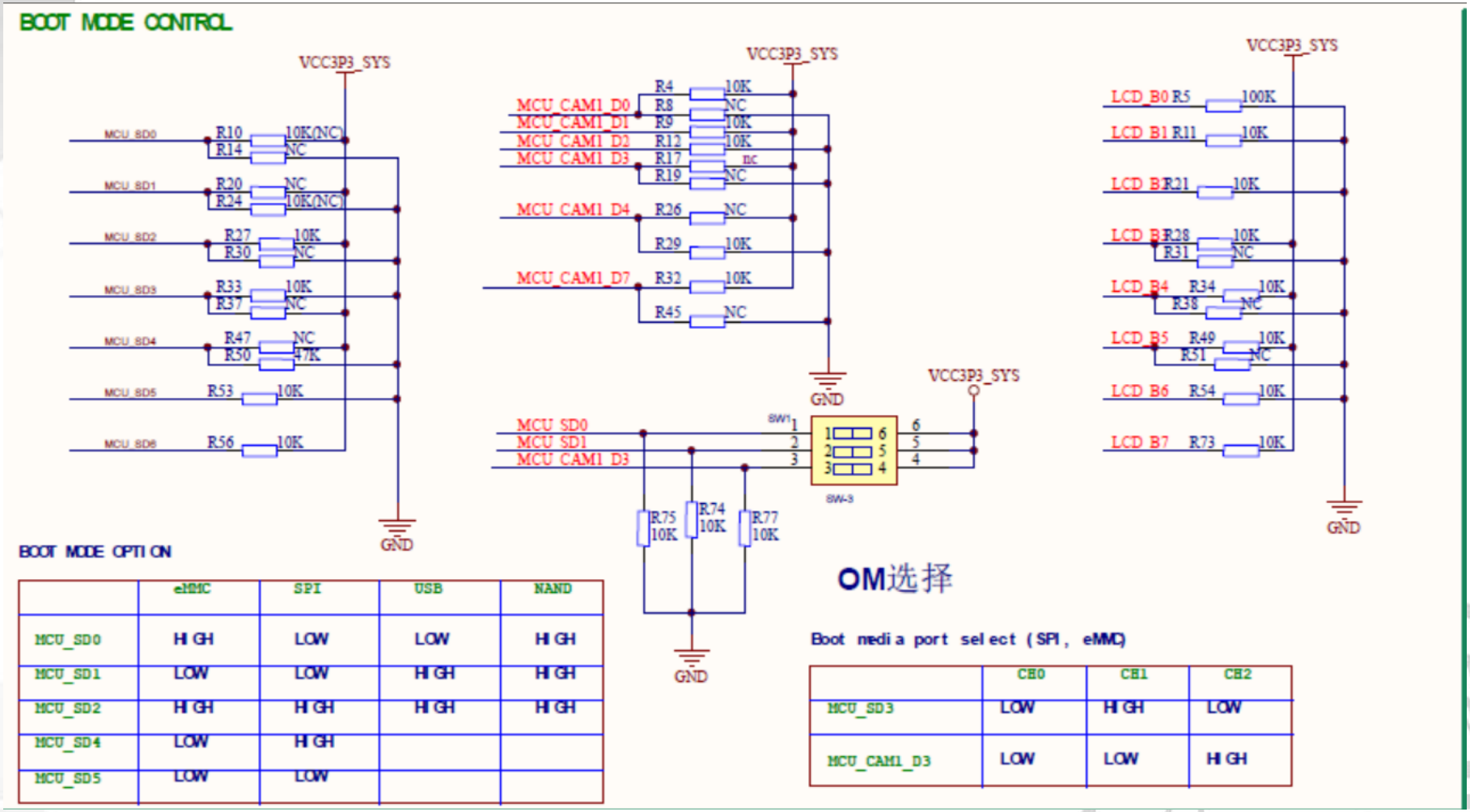


存储器电路（SD/MMC）

5.1.3 S5P6818 SOC最小系统



5.1.3 S5P6818 SOC最小系统



Boot启动模式选择电路

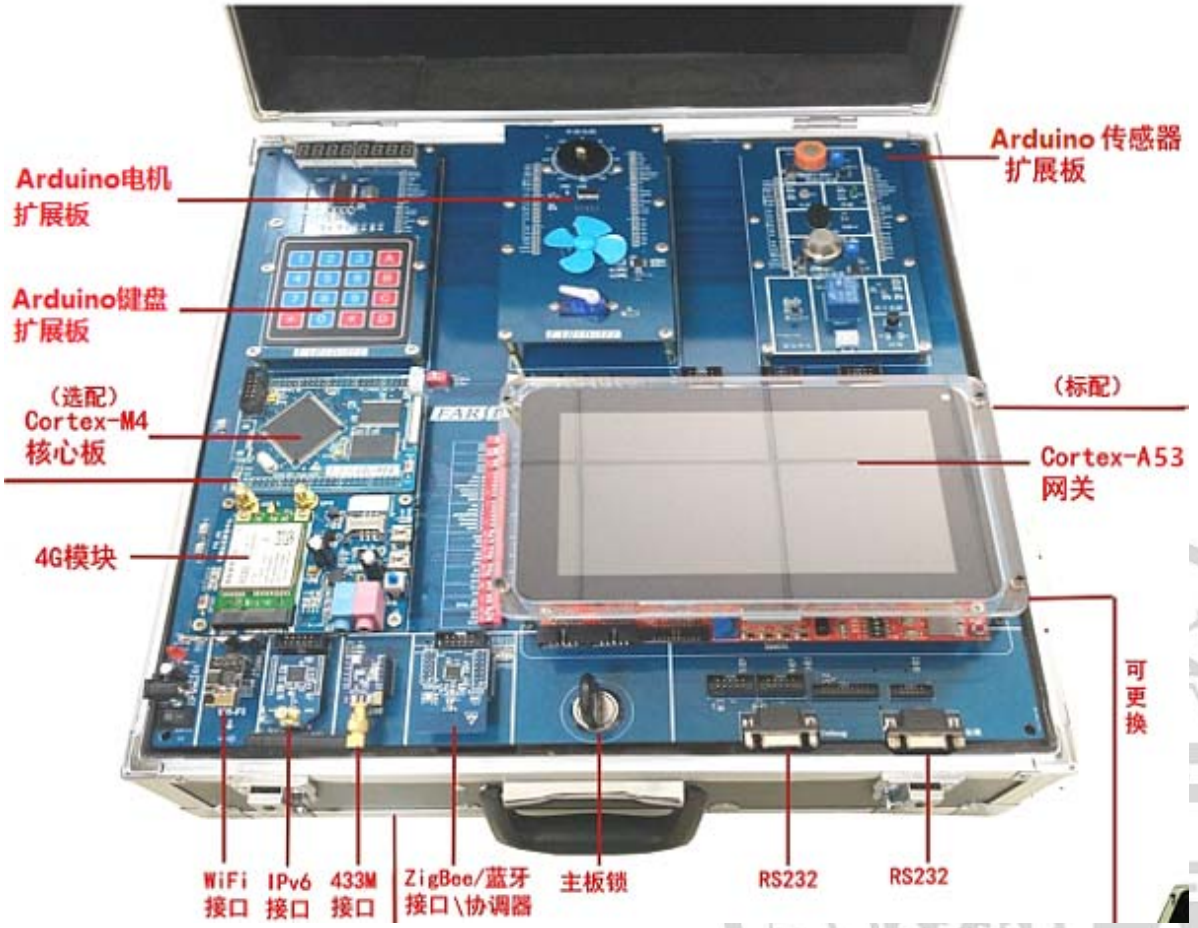
5.1.3 S5P6818 SOC最小系统

S5P6818核心板（最小系统）

5.1.4 S5P6818实验系统介绍

1、实验系统组成

- 微处理器标配ARM Cortex-A53(S5P6818)



5.1.4 S5P6818实验系统介绍

1、实验系统组成

	功能部件	型号参数
Cortex-A53 核心配置	CPU	- Samsung s5p6818（八核处理器） - 28nm HKMG - 1.4GHz+
	GPU	- Mali-400 MP4
	屏幕	- RGB 40 Pin 显示接口 - 7 寸 1024 x 600 IPS 高分辨率显示屏 - 多点电容触摸屏
	RAM容量	- 2GB DDR3
	ROM容量	- 8GB eMMC
	多启动方式	- eMMC 启动、 MicroSD(TF)/SD 卡启动 - 通过控制拨码开关切换启动方式 – 可以实现双系统启动

5.1.4 S5P6818实验系统介绍

	功能部件	型号参数
Cortex-A53 板载接口	存储卡接口	- 1 个 MicroSD(TF)卡接口 - 1 个 SD 卡接口 - 最高可扩展至 64GB
	摄像头接口	- 20Pin接口，支持OV5460 500万像素自动对焦摄像头
	HDMI接口	HDMI A 型接口 HDMI v1.4a 最高 1080p@60fps 高清数字输出
	JTAG接口	- 20 Pin 标准 JTAG 接口 独家支持详尽的 ARM 裸机程序
	ROM容量	- 8GB eMMC
	USB接口	- 1 路 USB OTG - 3 路 USB HOST 2.0（可扩展 USB-HUB）

5.1.4 S5P6818实验系统介绍

	功能部件	型号参数
Cortex-A53 板载接口	音频接口	- 1 路 Mic 接口 - 1 路 Speaker 耳机输出 - 1 路 Speaker 立体声功放输出（外置扬声器）
	网卡接口	- DM9000 10M/100M/1000M 网卡
	总线接口	- 1 路 RS485 总线接口 - 1 路 CAN 总线接口
	串口接口	- 3 路 5 线 RS232 串口
	扩展接口	- 2路 扩展10PinGPIO接口

第5章 三星S5P6818 简介及编程实例

- 5.1三星S5P6818 SOC介绍
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5.2 S5P6818 SOC编程实例

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5.2.1 RGB彩灯编程实例

- GPIO端口输出模式配置寄存器

（1）GPIOxALTFN0\ GPIOxALTFN1　开启/关闭复用

（2）GPIOxOUTENB　端口输出使能

（3） GPIOxOUT　　端口输出高/低电平

5.2.1 RGB彩灯编程实例

❖ GPIOxALTFN0 端口复用寄存器(pin0~pin15)

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A020h, B020h, C020h, D020h, E020h, Reset Value = 0x0000_0000

该寄存器共32位宽,每一个pin的复用状态由两个位控制，所以可以控制pin0~pin15端口，以pin2为例，如下如所示

Name	Bit	Type	Description	Reset Value
GPIOXALTFN0_2	[5:4]	RW	GPIOx[2]: Selects the function of GPIOx 2pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b0

5.2.1 RGB彩灯编程实例

❖ GPIOxALTFN1 端口复用寄存器(pin16~pin31)

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A024h, B024h, C024h, D024h, E024h, Reset Value = 0x0000_0000

该寄存器共32位宽,每一个pin的复用状态由两个位控制，所以可以控制pin16~pin31端口，以pin31为例，如下如所示

Name	Bit	Type	Description	Reset Value
GPIOXALTFN1_31	[31:30]	RW	GPIOx[31]: Selects the function of GPIOx 31pin. 00 = ALT Function0 01 = ALT Function1 10 = ALT Function2 11 = ALT Function3	2'b0

5.2.1 RGB彩灯编程实例

❖ GPIOxOUTENB　端口输出使能寄存器

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A004h, B004h, C004h, D004h, E004h, Reset Value = 0x0000_0000

Name	Bit	Type	Description	Reset Value
GPIOXOUTENB	[31:0]	RW	GPIOx[31:0]: Specifies GPIOx In/Out mode. The Open drain pins are operated in Input/Output mode by the GPIOxOUTPUT register (GPIOxOUT) and not by this bit. 0 = Input Mode 1 = Output Mode	32'h0

5.2.1 RGB彩灯编程实例

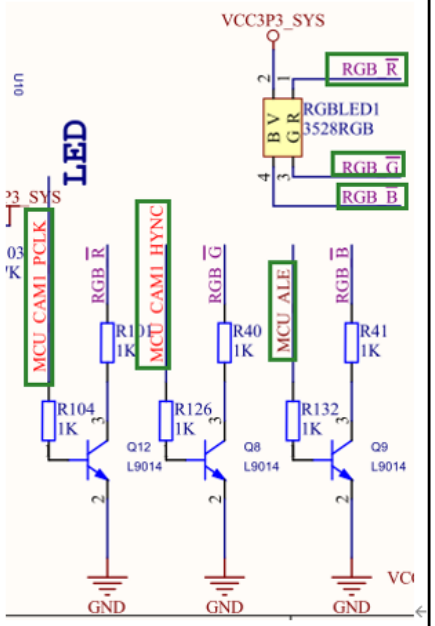
❖ GPIOxOUT　　端口输出寄存器

- Base Address: C001_A000h (GPIOA)
- Base Address: C001_B000h (GPIOB)
- Base Address: C001_C000h (GPIOC)
- Base Address: C001_D000h (GPIOD)
- Base Address: C001_E000h (GPIOE)
- Address = Base Address + A000h, B000h, C000h, D000h, E000h, Reset Value = 0x0000_0000

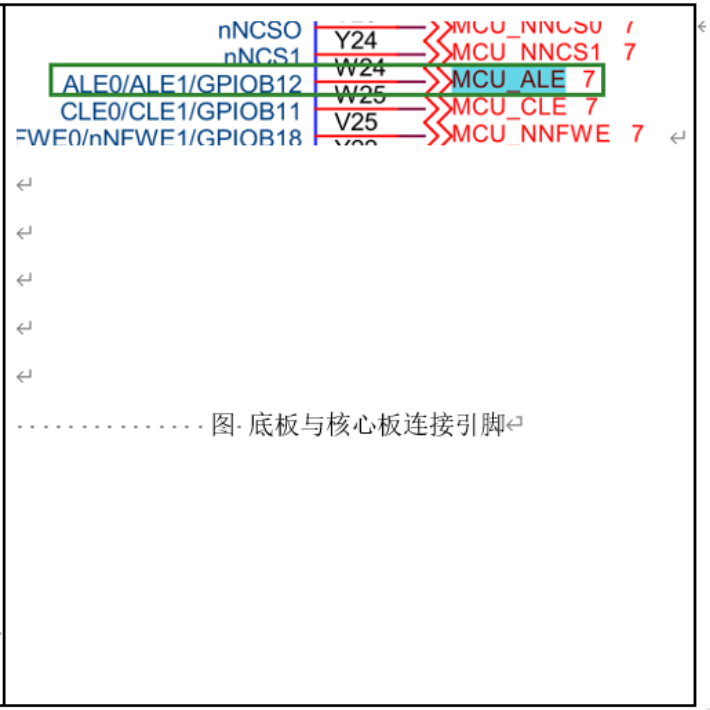
Name	Bit	Type	Description	Reset Value
GPIOXOUT	[31:0]	RW	GPIOx[31:0]: Specifies the output value in GPIOx output mode. This bit should be set as "1" (Input mode) or "0" (Output mode) to use the Open drain pins in Input/Output mode. 0 = Low Level 1 = High Level	32'h0

5.2.1 RGB彩灯编程实例

❖ 硬件连接



图· 底板 RGB 连接



图· 底板与核心板连接引脚

name	pin
LED_R	GPIOA28
LED_G	GPIOE13
LED_B	GPIOB_12

5.2.1 RGB彩灯编程实例

❖代码讲解

（1）定义各寄存器起始地址

```
#define   GPIOA28ALTFN1    (*(volatile unsigned int*)0xC001A024)
#define   GPIOA28OUTENB    (*(volatile unsigned int*)0xC001A004)
#define   GPIOA28OUT       (*(volatile unsigned int*)0xC001A000)

#define   GPIOE13ALTFN0    (*(volatile unsigned int*)0xC001E020)
#define   GPIOE13OUTENB    (*(volatile unsigned int*)0xC001E04)
#define   GPIOE13OUT       (*(volatile unsigned int*)0xC001E000)

#define   GPIOB12ALTFN0    (*(volatile unsigned int*)0xC001B020)
#define   GPIOB12OUTENB    (*(volatile unsigned int*)0xC001B004)
#define   GPIOB12OUT       (*(volatile unsigned int*)0xC001B000)
```

定义GPIOAxALTFN1寄存器起始地址

定义GPIOAxOUTENB寄存器起始地址

定义APIOAxOUT寄存器起始地址

5.2.1 RGB彩灯编程实例

❖代码讲解

（2）初始化各IO端口

```
void rgb_init(void)
{
        unsigned int reg = 0;

        /* r */
        reg = GPIOA28ALTFN1;
        reg &= ~(0x3 << 28);
        GPIOA28ALTFN1 = reg;

        reg = GPIOA28OUTENB;
        reg &= ~(0x1 << 28);
        reg |= (0x1 << 28);
        GPIOA28OUTENB = reg;

        /* g */
        reg = GPIOE13ALTFN0;
        reg &= ~(0x3 << 26);
        GPIOE13ALTFN0 = reg;

        reg = GPIOE13OUTENB;
        reg &= ~(0x1 << 13);
        reg |= (0x1 << 13);
        GPIOE13OUTENB = reg;
```

禁止复用

配置为输出模式

5.2.1 RGB彩灯编程实例

❖代码讲解

(3) 输出高低电平控制灯的亮灭

```
void main(void)
{
        unsigned int reg = 0;
        int i = 0, j = 0;

        rgb_init();

        while (1) {
                reg = GPIOA28OUT;
                reg &= ~(0x1 << 28);
                reg |= (0x1 << 28);
                GPIOA28OUT = reg;

                for (i = 0; i < 5000; i++)
                        for (j = 0; j < 1500; j++);

                reg = GPIOA28OUT;
                reg &= ~(0x1 << 28);
                GPIOA28OUT = reg;

                /****************************************/
```

输出高电平

输出低电平

作业

- 简述下S5P6818 SOC最小系统组成
- 设计编写一个4×4按键按轮询读取按键状态的原理图，并编写相应的程序(不限定具体芯片型号)。