GT9764BA

±100mA Current Output 10-Bit, I2C® DAC

1. Features

- ±100mA current output
- 2-wire (I2C-compatible) 1.8 V serial interface
- 10-bit resolution
- Available in 3×2 array WLCSP package
- Advanced Actuator Control (AAC) technology
- Integrated current sense resistor
- 2.3 V to 4.8 V power supply
- Guaranteed monotonic over all codes
- Thermal Shutdown
- Power-down to 0.5μA typical
- Internal reference
- Ultralow noise preamplifier
- Power-on reset

2. General Description

The GT9764BA is a single 10-bit digital-to-analog converter with ± 100mA output current capability. Current generation can be selected via I2C register. GT9764BA can produce bi-direction and uni-direction drive current. The DAC is controlled via a 2-wire (I2C-compatible) serial interface that operates at clock rate up to 1MHz. It features an internal reference and operates from a single 2.3V to 4.8V supply. GT9764BA integrated Advanced Actuator Control (AAC) technology. AAC is a fast autofocus and image quality enhancing technology developed by Giantec Semiconductor, and integrated into VCM driver GT9764BA.

The GT9764BA incorporates a power-on reset circuit that ensures that the DAC output current is 0mA and remains there until a valid write takes place. It has a power-down feature that reduces the current consumption of the device to 1μA maximum.

The GT9764BA is designed for autofocus, image stabilization, and optical zoom applications in camera phones, digital still cameras, and camcorders.

The GT9764BA also has many industrial applications, such as controlling temperature, light, and movement, over the range of -35°C to +85°C without derating.

The I2C address for the GT9764BA is 0x18, and can be selected to 0x1C by different part number

3. Applications

CONSUMER APPLICATIONS

- Lens autofocus
- Image stabilization
- Optical zoom
- Shutters
- Iris/exposure
- Neutral density (ND) filters
- Lens covers
- Camera phones
- Digital still cameras
- Camera modules
- Digital video cameras/camcorders
- Camera-enabled devices
- Security cameras
- Web/PC cameras

INDUSTRIAL APPLICATIONS

- Heater controls
- Fan controls
- Cooler (Peltier) controls
- Solenoid controls
- Valve controls
- Linear actuator controls
- Light controls
- Current loop controls

4. Application Diagram

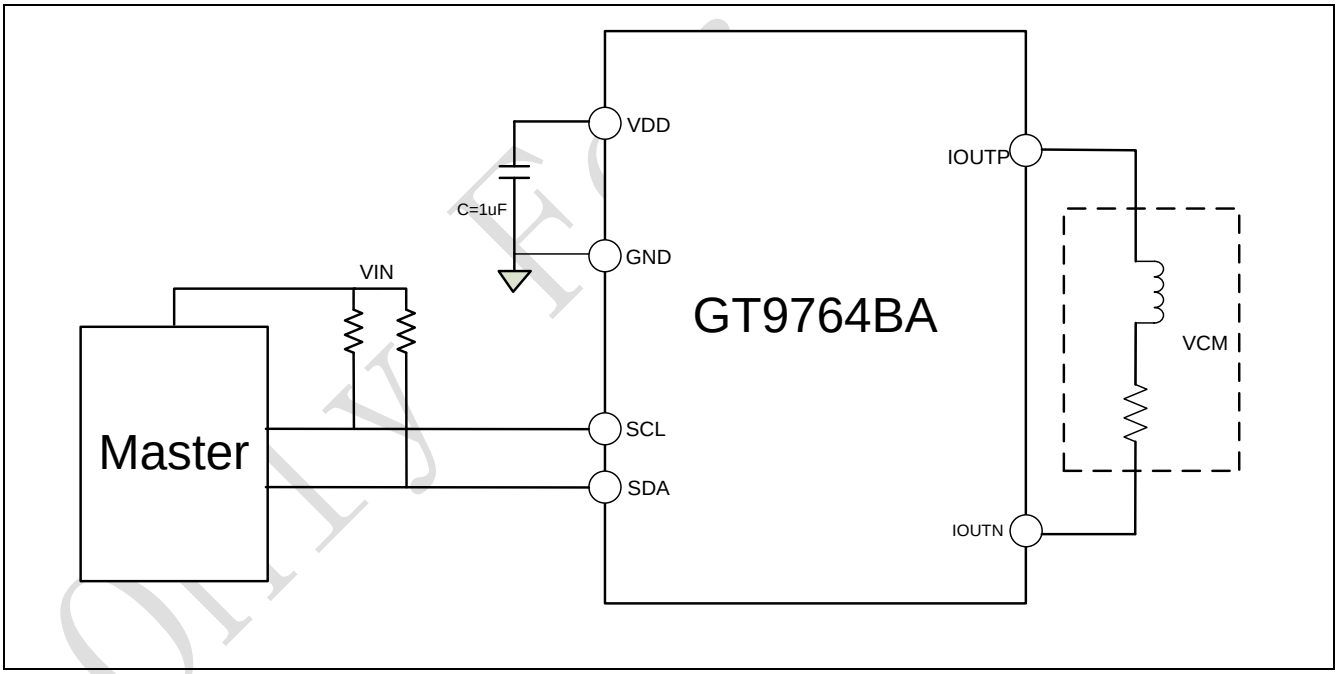


Figure1. Application Diagram 1 --- Bi-direction

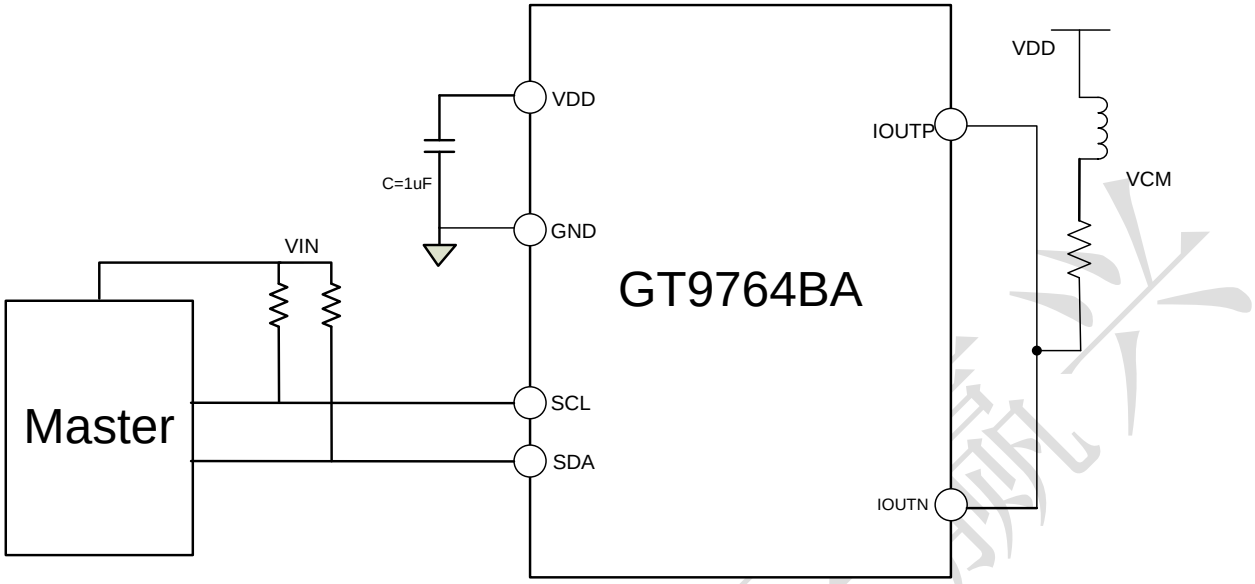


Figure2. Application Diagram 2 --- Uni-direction

5. Pin Configuration

5.1 Pin Assignment Top View

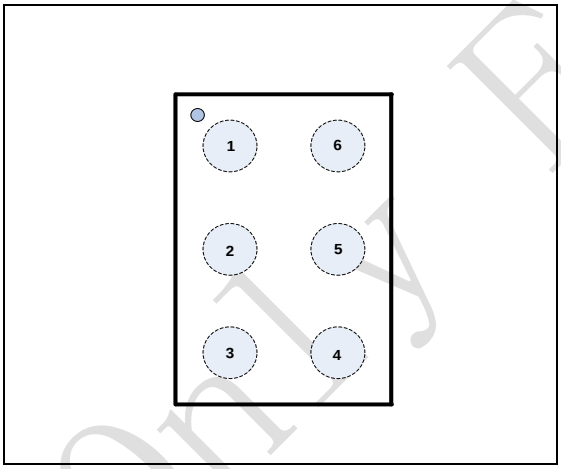


Figure3. 6 Ball WLCSP Pin Configurations

Note: Please see section "**Part Markings**" for detailed Marking Information

5.2 Pin Descriptions

Pin Number	Pin Name	Pin functions
1	VSS	Ground Pin
2	IOUTN	Output current source
3	SDA	I2C Interface Signal
4	SCL	I2C Interface Signal
5	IOUTP	Output current source
6	VDD	Power supply

6. Terminology

Relative Accuracy

For the DAC, relative accuracy or integral nonlinearity is a measurement of the maximum deviation, in LSB, from a straight line passing through the endpoints of the DAC transfer function.

Differential Nonlinearity (DNL)

Differential nonlinearity is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design.

Zero-Code Error

Zero-code error is a measurement of the output error when zero code (0x0000) is loaded to the DAC register. Ideally, the output is 0mA. The zero-code error is always positive in the GT9764BA because the output of the DAC cannot go below 0mA. This is due to a combination of the offset errors in the DAC and output amplifier. Zero-code error is expressed in mini amperes (mA).

Gain Error

Gain error is a measurement of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from the ideal, expressed as a percent of the full-scale range.

Gain Error Drift

Gain error drift is a measurement of the change in gain error with changes in temperature. It is expressed in LSB/°C.

Digital-to-Analog Glitch Impulse

This is the impulse injected into the analog output when the input code in the DAC register changes state. It is normally specified as the area of the glitch in nano amperes per second (nA-s) and is measured when the digital input code is changed by 1 LSB at the major carry transition.

Digital Feed through

Digital feed through is a measurement of the impulse injected into the analog output of the DAC from the digital inputs of the DAC, but it is measured when the DAC output is not updated. It is specified in nano amperes per second (nA-s) and measured with a full-scale code change on the data bus, that is, from all 0s to all 1s and vice versa.

Offset Error

Offset error is a measurement of the difference between SENSE (actual) and IOUT (ideal) in the linear region of the transfer function, expressed in mini amperes (mA). Offset error is measured on the GT9764BA with Code 1 loaded into the DAC register.

Offset Error Drift

Offset error drift is a measurement of the change in offset error with a change in temperature. It is expressed in microvolt per degree Celsius (μV/°C).

7. Theory of Operation

The GT9764BA is a fully integrated, 10-bit digital-to-analog converter (DAC) with ±100mA output current capability. It is intended for bi-direction driving voice coil actuators in applications such as lens autofocus, image stabilization, and optical zoom. The circuit diagram is shown in Figure 3.

VCM current can be controlled via an I2C interface and VCM_CURRENT register. The output current of GT9764BA can be chosen in bi-direction or uni-direction through OTP. In uni-direction the output current range can be chosen 0~100mA or 0~120mA. And in bi-direction the output current can be chosen ±100mA or ±60mA.

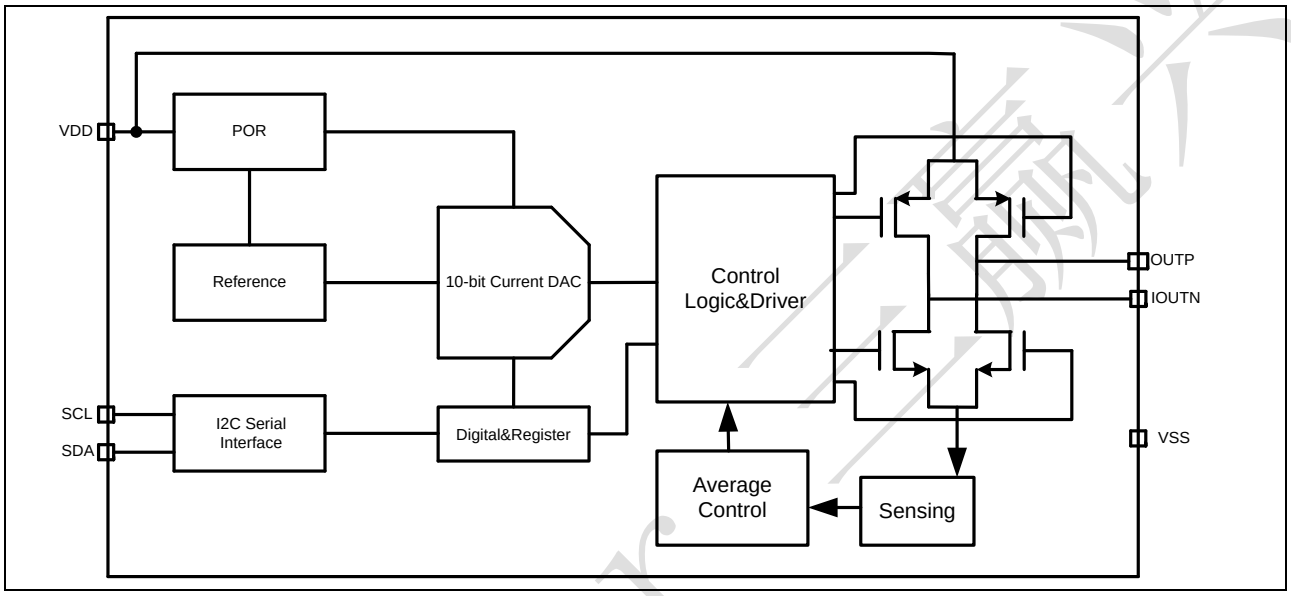


Figure4. Functional Block Diagram

Serial Interface

The GT9764BA is controlled using the industry-standard I2C 2-wire serial protocol. Data can be written to or read from the Register at data rates of up to 1MHz. After a power-on reset, the contents of the input register are reset to default value. For details, view the Register table.

I2C Slave Address selection

VCM driver has different slave address which is controlled by different part number.

Part Number	VCM slave address
GT9764BA-CLI_TR	0x18
GT9764BAH-CLI_TR	0x1C

I2C Bus Operation

An I2C bus operates with one or more master devices that generate the serial clock (SCL) and read and write data on the serial data line (SDA) to and from slave devices such as the GT9764BA. All devices on an I2C bus have their SDA pin connected to the SDA line and their SCL pin connected to the SCL line of the master device. I2C devices can only pull the bus lines low; pulling high is achieved by pull-up resistors, RP. The value of RP depends on the data rate, bus capacitance, and the maximum load current that the I2C device can sink (3mA for a standard device).

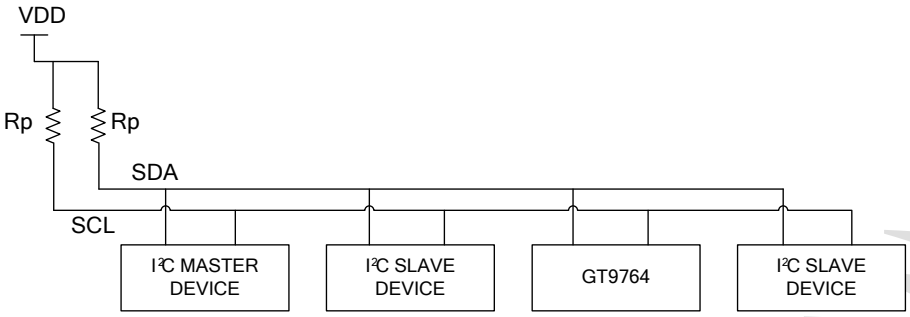


Figure5. Typical I2C Bus

When the bus is idle, SCL and SDA are both high. The master device initiates a serial bus operation by generating a start condition, which is defined as a high-to-low transition on the SDA low while SCL is high. The slave device connected to the bus responds to the start condition and shifts in the next eight data bits under control of the serial clock. These eight data bits consist of a 7-bit address, plus a read/write (R/W) bit that is 0 if data is to be written to a device, and 1 if data is to be read from a device. Each slave device on an I2C bus must have a unique address. The address of the GT9764BA is 0001100;Because the address plus the R/W bit always equals eight bits of data, the write address of the GT9764BA is 00011000 (0x18) and the read address is 00011001 (0x19) (see Figure 7 and Figure8). The slave address in GT9764BA also can be changed to 0x1C and 0x1D if necessary.

At the end of the address data, after the R/W bit, the slave device that recognizes its own address responds by generating an acknowledge (ACK) condition. This is defined as the slave device pulling SDA low while SCL is low before the ninth clock pulse and keeping it low during the ninth clock pulse. Upon receiving ACK, the master device can clock data into the GT9764BA in a write operation, or it can clock it out in a read operation. Data must change either during the low period of the clock (because SDA transitions during the high period define a start condition, as described previously), or during a stop condition, as described in the IIC Format section.

GT9764BA supports three write and two read operation: one Byte write, two byte write, three byte write and one byte read and sequential byte read. Figure 7 shows the format of write; Figure 8 shows the format of read.

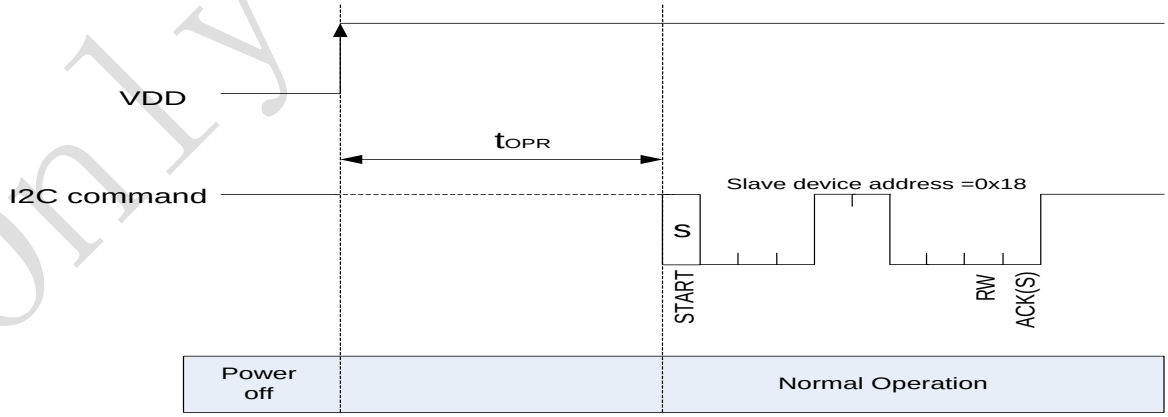
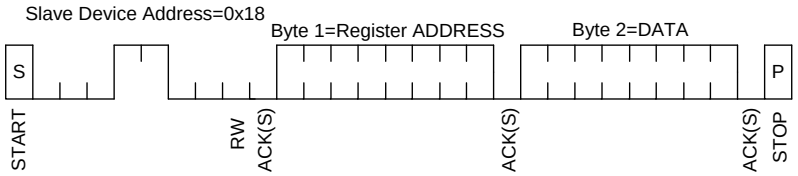


Figure6. Power on Sequence

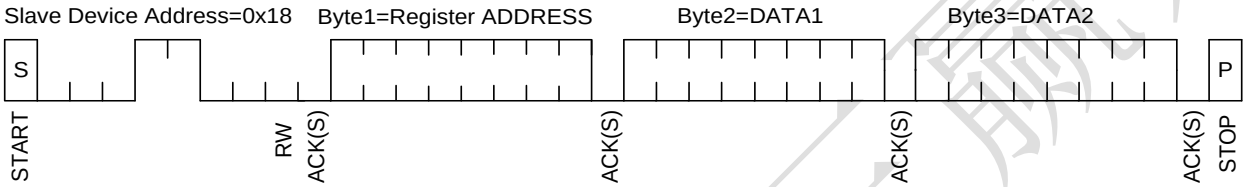
※ GT9764BA required waiting time of tOPR after power on

I2C Format

Write Opertion – Byte Write



Write Opertion – Sequential Write(two byte)



Write Operation-Sequential Write(three byte)

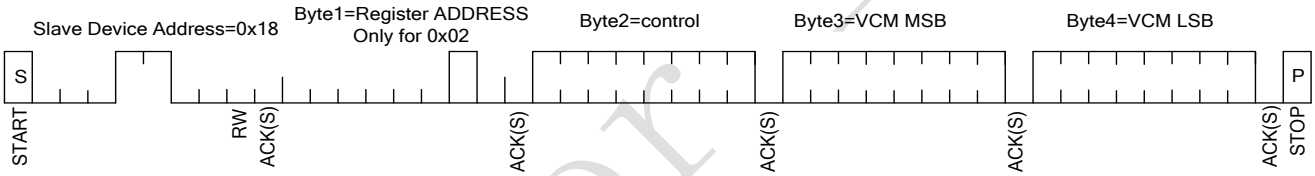
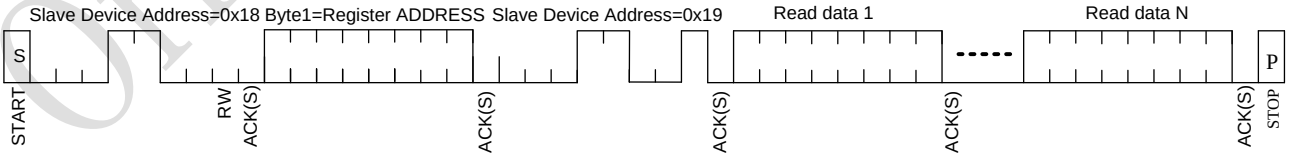


Figure7. Write Operation

Read Operation - Selective read(one byte)

Read Operation – Selective sequential read



- In I2C format, Master must check the ACK bit before sending the next data.

Figure8. Read Operation

Register table

Table1. Register table

NAME	Addr	Default	R/W	Data							
IC Info	0x00	0x00	R	IC Manufacture ID				IC Model			
IC Ver	0x01	-	R					Design Round			
CONTROL	0x02	0x00	R/W							RING	PD
VCM_MSB	0x03	0x02	R/W							D9	D8
VCM_LSB	0x04	0x00	R/W	D7	D6	D5	D4	D3	D2	D1	D0
Status	0x05	0x00	R				TSD				BUSY
Mode	0x06	0x00	R/W	Ring Mode							DIV2
				AAC1	AAC0						
Resonance	0x07	0x60	R/W	Resonance Frequency							
				DIV1	DIV0	AACT5	AACT4	AACT3	AACT2	AACT1	AACT0
TRANSLATION	0x08	0x00	R/W								TRANS
KAVL	0x09	0x00	R/W				KAVL4	KVAL3	KVAL2	KVAL1	KVAL0

XXXX = Default value is 'H'

Register description

Table2. IC information

NAME	Addr	Default	R/W	Data	
IC Info	0x00	0x00	R	IC Manufacture ID	IC Model

Table3. IC version

NAME	Addr	Default	R/W	Data	
IC Ver	0x01	-	R		Design Round

Design Round: Revision history.

Table4. Control

NAME	Addr	Default	R/W	Data							
CONTROL	0x02	0x00	R/W							RING	PD

RING

0: Direct mode

1: AAC mode

PD

0: normal operation

1: Power down chip（PD=1）

Table5. VCM current register

NAME	Addr	Default	R/W	Data							
VCM_MSB	0x03	0x02	R/W							D9	D8
VCM_LSB	0x04	0x00	R/W	D7	D6	D5	D4	D3	D2	D1	D0

D[9]: DAC direction bit

0 : negative direction

1 : positive direction

D[8:0]: DAC current input data

Positive current = D[8:0] x 100/511 [mA]

Negative current= -(512 - D[8:0]) x 100/511 [mA]

※ Zero current code = 512code

※ Zero current code can be changed 0 code to 512 code by Factory trimming

Table6. D[9:0] code and output current

D[9:0]	Current(mA)	D[9:0]	Current(mA)
00_0000_0000	-100.19mA	10_0000_0000	0.00mA
00_0000_0001	-100.00mA	10_0000_0001	0.19mA
00_0000_0010	-99.80mA	10_0000_0010	0.39mA
…	…	…	…
0 1_1111_1110	-0.39mA	11_1111_1110	99.80mA
0 1_1111_1111	-0.19mA	11_1111_1111	100.00mA

Table7. TSD register

NAME	Addr	Default	R/W	Data							
Status	0x05	0x00	R				TSD				BUSY

TSD: thermal shutdown state monitor

0: normal operation

1: TSD mode

BUSY: BUSY bit must be ”L” during ”VCM MSB and LSB” registers are being written.

During Ringing control operation, BUSY bit keeps ”H”. While BUSY=”H”**,** the I2C command is ignored except “PD” register

Table8. AAC register

NAME	Addr	Default	R/W	Data							
Status	0x06	0x00	R/W	AAC1	AAC0						DIV2

AAC[1:0]: AAC(Advance Actual Control) mode selection

Table9. AAC mode

RING	AAC[1:0]	Mode
0	0x	Direct mode
0	1x	LSC mode
1	00	AAC1
1	01	AAC2
1	10	AAC3
1	11	AAC4

Table10. DIV and AACT register

NAME	Addr	Default	R/W	Data							
Resonance	0x07	0x60	R/W	DIV1	DIV0	AACT5	AACT4	AACT3	AACT2	AACT1	AACT0

DIV[2:0]: Divider

Table11. DIV code and Motor Period

DIV[2:0]	Period
000	Tvib x 2(double)
001	Tvib x 1(default)
010	Tvib x 1/2(half)
011	Tvib x 1/4(quarter)
100	Tvib x 8
101	Tvib x 4
110	Reserved
110	Reserved

AACT[5:0]: AAC Tvib

Tvib = (252us+AACT[5:0]*4us)*25*Dividing Rate = (6.3ms+ AACT[5:0]*0.1ms)*Dividing Rate

TLSC(1-step period) = (252us+AACT[5:0]*4us)*Dividing Rate

Table12. Translation

NAME	Addr	Default	R/W	Data							
TRANSLATION	0x08	0x00	R/W								TRANS

TRANS: Translating motor period in AAC control

0: no translating

1: translating

Table13. KVAL

NAME	Addr	Default	R/W	Data							
KVAL	0x09	0x00	R/W				KAVL4	KVAL3	KVAL2	KVAL1	KVAL0

KVAL[4:0]

K factor is set by KVAL[4:0] .KVAL[4:0] default value is 5'b=00000.

Table14. KVAL and K factor

KVAL[4:0]	K factor
00001	0.9921875
00010	0.984375
00011	0.9765625
00100	0.96875
00101	0.9609375
00110	0.953125
00111	0.9453125
01000(default)	0.9375
01001	0.9296875
01010	0.921875
01011	0.9140625
01100	0.90625
01101	0.8984375
01110	0.890625
01111	0.8828125
10000	0.875
10001	0.8671875
10010	0.859375
10011	0.8515625
10100	0.84375
10101	0.8359375
10110	0.828125
10111	0.8203125
11000	0.8125
11001	0.8046875
11010	0.796875
11011	0.7890625
11100	0.78125
11101	0.7734375
11110	0.765625
11111	0.7578125

Power Supply Bypassing and Grounding

When accuracy is important in an application, it is beneficial to consider power supply and ground return layout on the PCB. The PCB for the GT9764BA should have separate analog and digital power supply sections. Where shared GND is necessary, the connection of grounds should be made at only one point, as close as possible to the GT9764BA.

Special attention should be paid to the layout of the GND return path, and it should be tracked between the voice coil motor and IOUT to minimize any series resistance. Figure 8 shows the output current sink of the GT9764BA and illustrates the importance of reducing the effective series impedance of GND and the track resistance between the motor and IOUT. The voice coil is modeled as Inductor LC and Resistor RC. The current through the voice coil is effectively a dc current that results in a voltage drop, V_{COIL}, when the GT9764BA supply current. The effect of any series inductance is minimal.

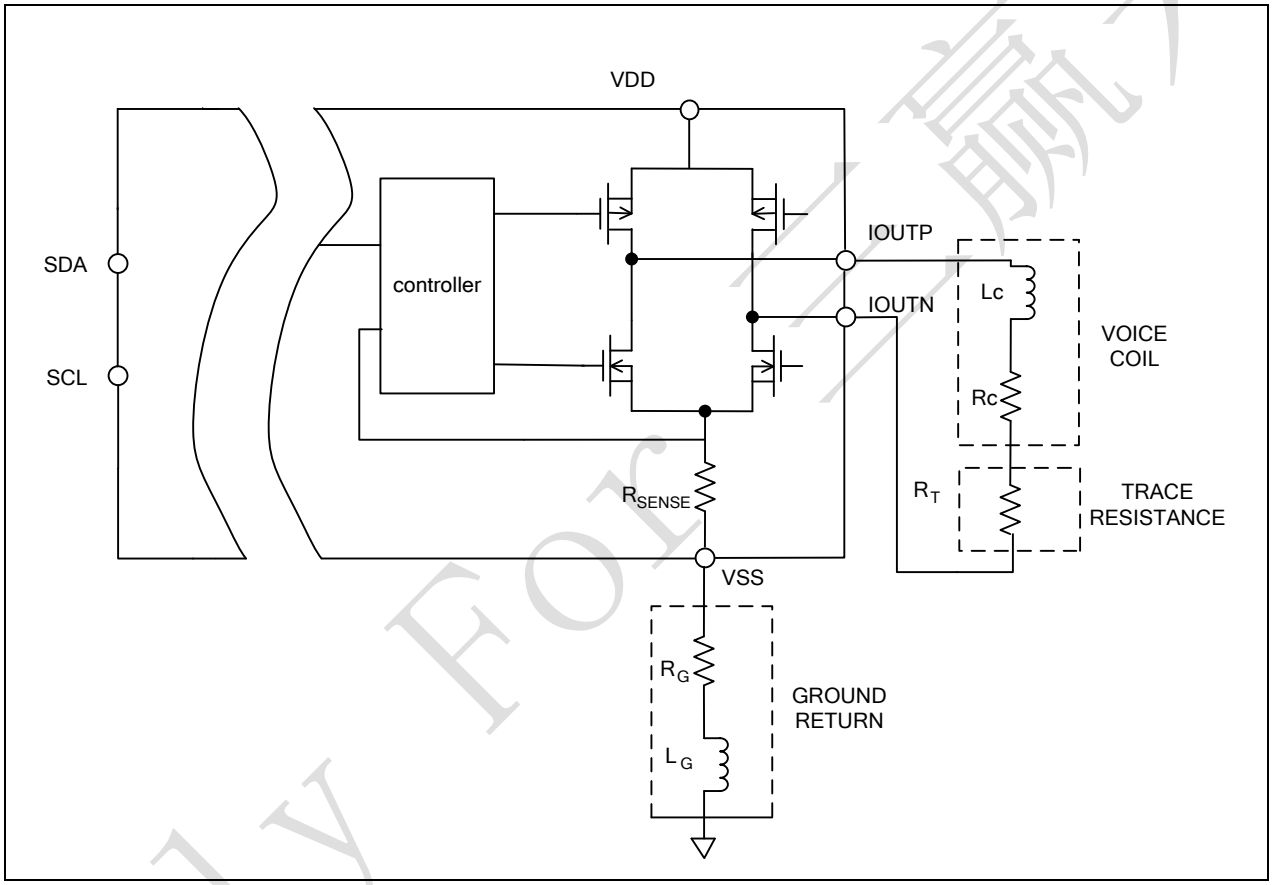


Figure9. Effect of PCB Trace Resistance and Inductance

The ground return path is modeled by the components RG and LG. The track resistance between the voice coil and the GT9764BA is modeled as RT. The inductive effects of LG influence RSENSE and RC equally, and because the current is maintained as a constant, it is not as critical as the purely resistive component of the ground return path. When the maximum sink current is flowing through the motor, the resistive elements, RT and RG, may have an impact on the voltage headroom of Q1 and could, in turn, limit the maximum value of RC because of voltage compliance.

For this reason, it is important to minimize any series impedance on both the ground return path and interconnect between the GT9764BA and the motor. It is also important to note that for lower values of IOUT, the compliance voltage of the output stage also decreases. This decrease allows the user to either use voice coil motors with high resistance values or decrease

the power supply voltage on the voice coil motor. The compliance voltage decreases as the IOUT current decreases.

The power supply of the GT9764BA, or the regulator used to supply the GT9764BA, should be decoupled. Best practice power supply decoupling recommends that the power supply be decoupled with a 10μF capacitor. Ideally, this 10μF capacitor should be of a tantalum bead type. However, if the power supply or regulator supply is well regulated and clean, such decoupling may not be required. The GT9764BA should be decoupled locally with a 0.1μF ceramic capacitor, and this 0.1μF capacitor should be located as close as possible to the VDD pin. The 0.1μF capacitor should be ceramic with a low effective series resistance and effective series inductance. The 0.1μF capacitor provides a low impedance path to ground for high transient currents.

The power supply line should have as large a trace as possible to provide a low impedance path and reduce glitch effects on the supply line. Clocks and other fast switching digital signals should be shielded from other parts of the board by digital ground. Avoid crossover of digital and analog signals, if possible. When traces cross on opposite sides of the board, they should run at right angles to each other to reduce feed through effects through the board. The best technique is to use a multilayer board with ground and power planes, where the component side of the board is dedicated to the ground plane only and the signal traces are placed on the solder side. However, this is not always possible with a 2-layer board.

Ringing Control

Ringing control is enabled or disabled on the GT9764BA using the Ring and AAC[1:0]. When Ring=0,AAC[1:0] =0x, direct load mode is used. In direct load mode, the output increments or decrements to the target code in a single step. No ringing control is used in direct load mode.

When Ring=0, AAC[1:0]=1x, LSC(linear slope control) mode is used. In LSC mode, the output increase and decrease to the target in smallest step. It will take Tvib to get target current.

When Ring=1, ringing control is enabled (by setting AAC[1:0]), the GT9764BA allow the user to overcome the mechanical limitations associated with reductions in VCM form factor. The GT9764BA VCM drivers can operate in one of four different ringing control modes:

- 00: AAC1
- 01: AAC2
- 10: AAC3
- 11: AAC4

When AAC mode is used (by setting the AAC[1:0]), the user decides the required move time. In AAC mode, the output increments or decrements to the target code in single code steps in the required actuation time. When one of the AAC modes is used, the AACT[5:0] register should be loaded with a value equivalent to the VCM mechanical resonance period. The mechanical resonance period of a VCM can be found by applying a step current to the VCM and measuring the time taken for one complete oscillation. T_{vib} is shown in Figure 10.

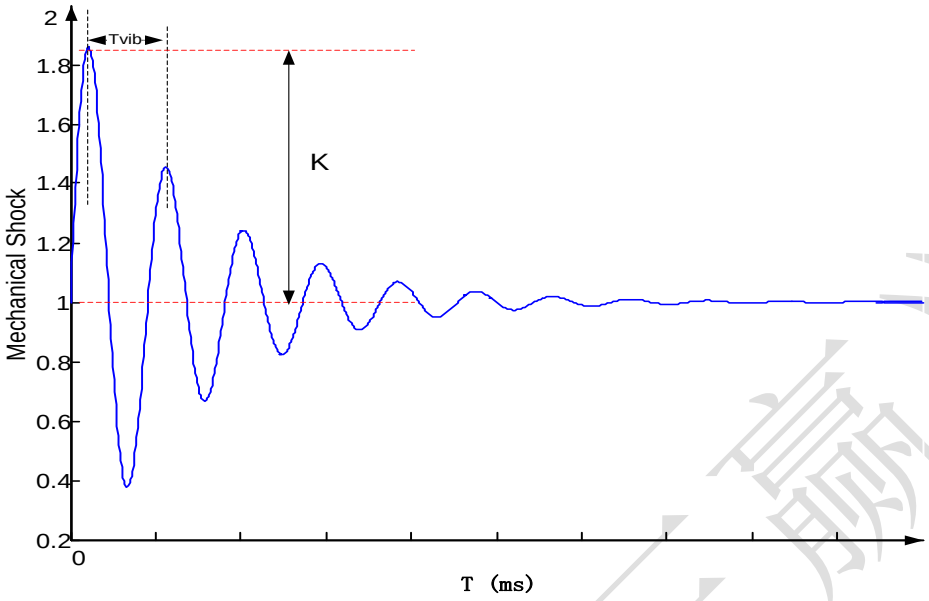


Figure10. VCM Mechanical Response to a Step Current Input

The output increments or decrements to the target code using AAC technology.

Advanced Actuator Control (AAC) Technology

Mechanical ringing is an inherent problem in voice coil motors. It is an artifact of an underdamped system and is dependent on many factors, but primarily on the integrity of the mechanical springs employed in the actuator assembly.

AAC is a revolutionary autofocus response time and image quality enhancing technology, which has been developed by Giantec and integrated into the GT9764BA VCM drivers. AAC circuitry applies specialized, patented wave form and application technology to underdamped voice coil motors to reduce mechanical ringing. This technology enables the user to achieve very fast mechanical settling times and, as a result, greatly enhances autofocus response times, image quality, and user experience. This technology is completely proprietary to Giantec and patents are pending.

AAC technology incorporates a wide band of tolerance around the resonant period of the VCM to compensate for manufacturing variability in the mechanical resonance period of the VCM. AAC technology can allow for variations of ±64% (for example, manufacturing variations and variations over time and temperature) in the VCM resonant period while still greatly enhancing autofocus response times and image quality. This band of tolerance varies, depending on the AAC option used.
Each of the four AAC options achieves a different actuation time. A faster actuation time leads to a narrower resonant period tolerance band (see Figure 11 and Table 4).

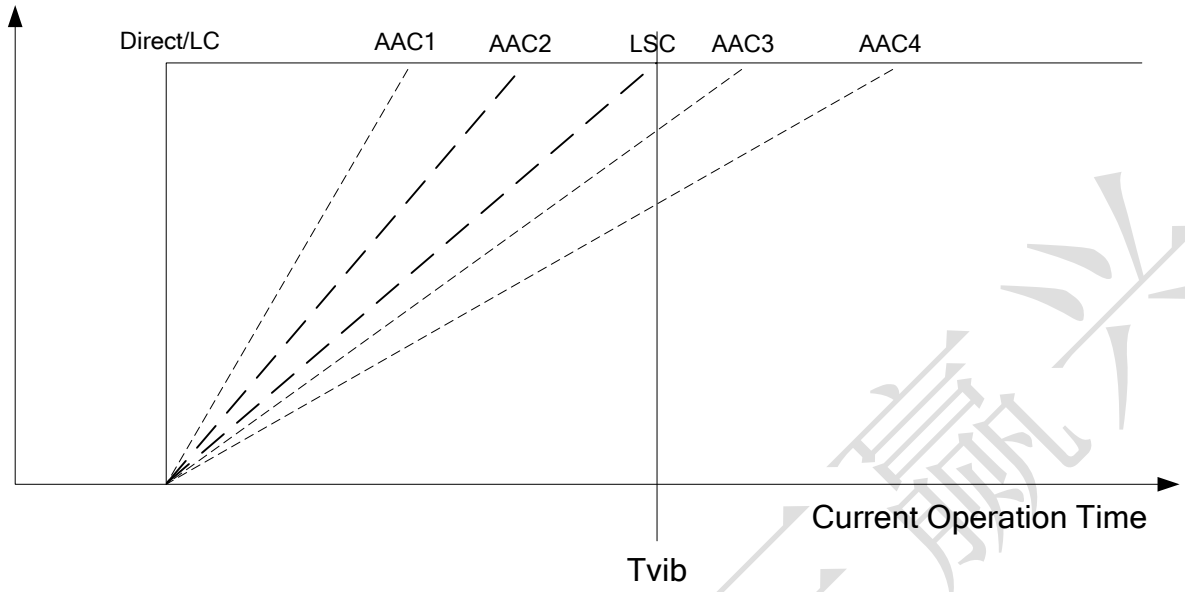


Figure11. AAC Current Operation Time

Table 15. Current Operation Times and Tolerances of AAC Options

AAC Option	Current Operation Time(1)	Frequency Tolerance(2)
AAC1 mode	0.50 Tvib	±6.5%
AAC2 mode	0.72 Tvib	±20%
AAC3 mode	1.21 Tvib	±40%
AAC4 mode	1.50 Tvib	±45%

(1) Operation time: Driver's current moving time

(2) This is a design spec. Frequency Tolerance can be variable according to mechanical characteristics of each VCM

(3) Tvib = vibration period of VCM

Figure 12 illustrates all the output modes of the GT9764BA and clearly shows the significant impact that Linear and AAC technology has on the settling time and the amount of mechanical ringing and overshoot in a sample VCM.

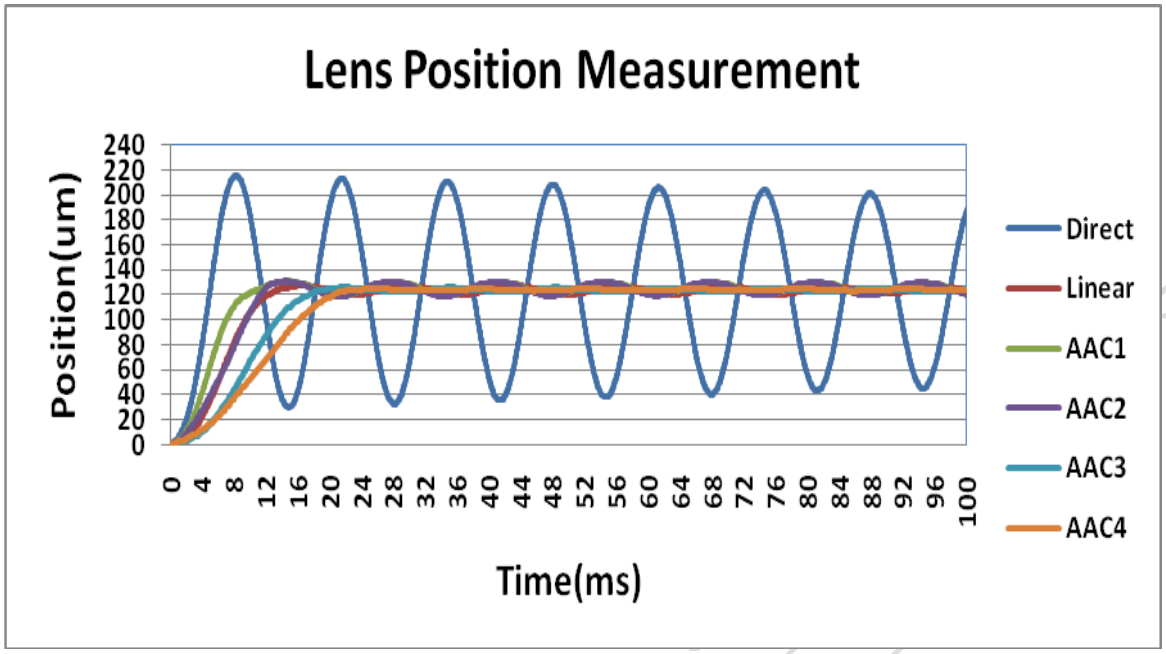


Figure12. Comparing Direct, Linear, and AAC Modes Using a Sample VCM

8. Slew Rate Control Set up Method

8.1. Driving Mode – Direct, Linear Slope Control, AAC1, AAC2, AAC3, and AAC4.

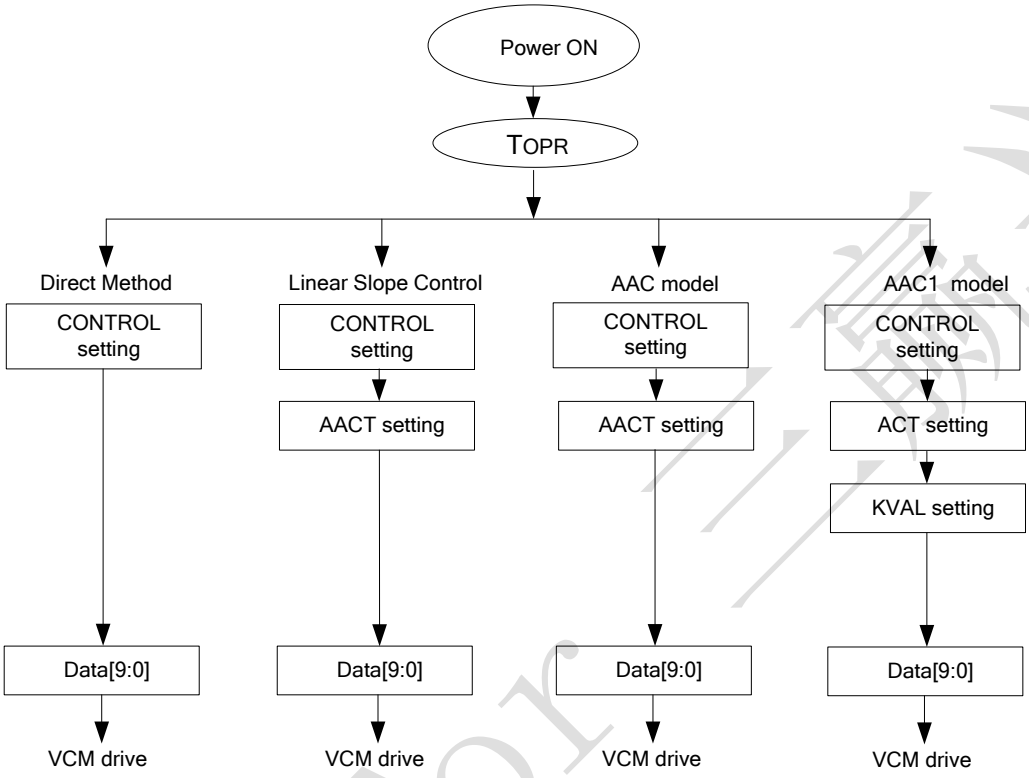


Figure13. Driving Mode

Linear Slope Control Scheme

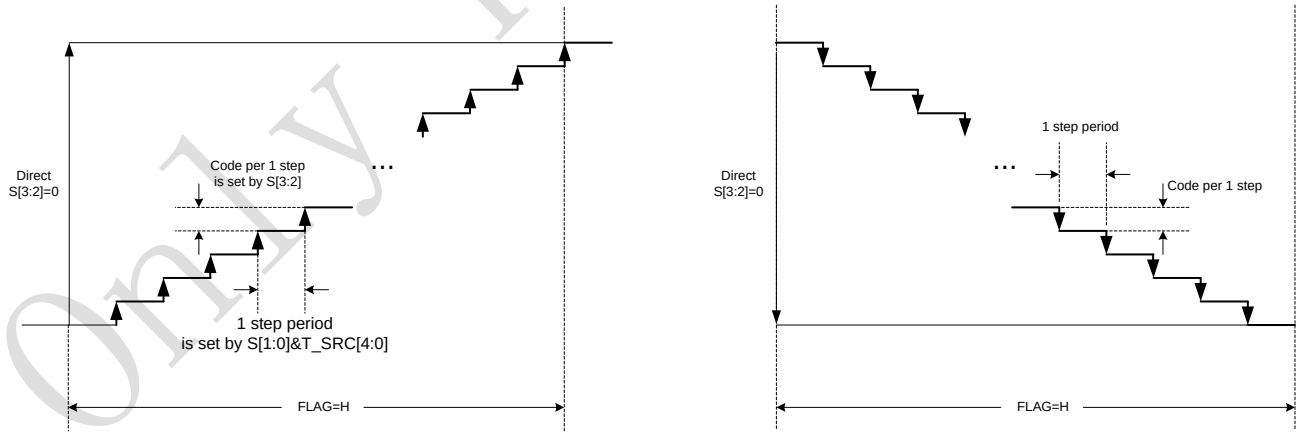


Figure14. Linear Slope Control Scheme

9. Application Information

The GT9764BA is designed to drive both bi-direction and uni-direction motors used in applications such as lens auto-focus, image stabilization, or optical zoom.

The GT9764BA is designed to sink up to ±100mA, which is more than adequate for available commercial linear motors or voice coils. Another factor that makes the GT9764BA the ideal solution for these applications is the monotonicity of the device, ensuring that lens positioning is repeatable for the application of a given digital word.

Figure 15 shows a typical application circuit for the GT9764BA.

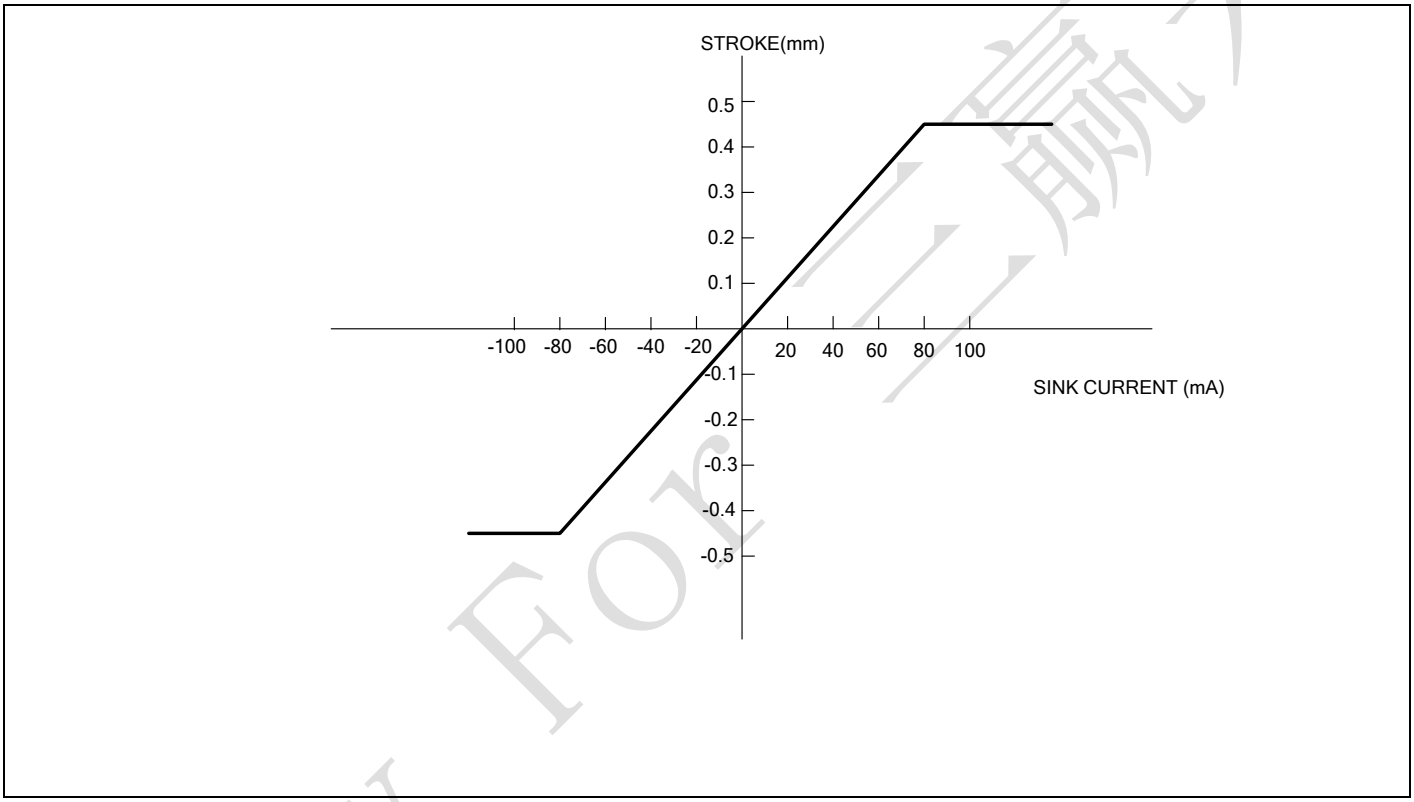


Figure15. Spring-Preloaded Voice Coil Stroke vs. Sink Current

The requirement to reduce optical module form factors has led to a reduction in the size of VCM actuators. When large current transitions occur, the momentum of the lens can often lead to overshoot and VCM can take some time to settle to its final position. This phenomenon, often described as mechanical ringing, varies with output current step size and for large lens displacements can lead to unacceptably long auto focus times. The GT9764BA unique and proprietary output slew rate control design allows the user to overcome the mechanical limitations associated with reductions in VCM form factor.

The GT9764BA uses an innovative and proprietary scheme to provide the user with the option of four slew rate control modes. The slew rate control mode feature of the GT9764BA allows the user to customize output transition times and where mechanical ringing is an issue the GT9764BA output can be programmed to effectively decelerate the lens movement as it approaches its target position; thereby reducing the overshoot and minimizing mechanical ringing.

10. Electrical Characteristics

10.1 Absolute Maximum Ratings

Condition	Min	Max
VDD to VSS	–0.3 V	+5.5 V
SCL, SDA to VSS	–0.3 V	VDD + 0.3 V
IOUT to VSS	–0.3 V	VDD + 0.3 V
Operating Temperature Range Industrial (B Version)	−35°C	+85°C
Storage Temperature Range	−65°C	+150°C
Junction Temperature (TJ MAX)	+150°C`	
WLFCSP Power Dissipation	(TJ MAX – TA)/θJA	
θJA Thermal Impedance1 Mounted on 4-Layer Board	95°C/W	
Lead Temperature, Soldering Maximum Peak Reflow Temperature2	260°C (±5°C)	

Note: Stress greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions outside those indicated in the operational sections of this specification are not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

10.2 DC Electrical Characteristics

VDD = 2.8 V, VSS = 0 V, all specifications TMIN to TMAX, unless otherwise noted.

Parameter	Conditions	Min.	Typ.	Max.	Units
DC PERFORMANCE	V_{DD} = 2.3 V to 4.8 V				
Resolution	0.195 mA/LSB	-	10		Bits
Relative Accuracy[2]		-	±1.5	±4	LSB
Differential Nonlinearity[2, 3]	Guaranteed monotonic over all codes	-	-	±1	LSB
Zero-Code Error[2, 4]	All 0s loaded to DAC	0	0	0.2	mA
Offset Error @ Code 1[2]			0.2		mA
Gain Error[2]	@ 25°C			±0.6	% of FSR
Offset Error Drift[4, 5]			10		µA/°C
Gain Error Drift[2, 5]			±0.2	±0.5	LSB/°C
OUTPUT CHARACTERISTICS					
Maximum output Current		97	100	103	mA
Total Resistance value of the Output[5] (Sensing Resistor + Tr On Resistance)	Output Current = 100mA		2.5		Ω
Thermal shutdown					
Thermal shutdown			140		°C
LOGIC INPUTS (SCL, SDA)[5]					
Input Low Voltage, V_{INL}	V_{DD} = 2.3V to 4.8 V			0.54	V
Input High Voltage, V_{INH}	V_{DD} = 2.3 V to 4.8 V	1.26			V
Input Current, I_{IN}	V_{IO} =V_{DD} =4.8V			±8	µA
Delay time for POR/PD5		100			µs
Digital Input Capacitance, C_{IN}			6		pF
Glitch Rejection[6]				50	ns
Leakage Current[8]		-1		1	µA
POWER REQUIREMENTS					
V_{DD}		2.3		4.8	V
I_{DD} (Normal Mode)	I_{DD} specification is valid for all DAC codes		0.35		mA
I_{PD} (power down Mode)		-1		1	µA
Power On Time[7]		200			us

Note:

1 Temperature range is as follows －35°C to +85°C.

2 See the Terminology section.

3 Linearity is tested using a reduced code range: Code 1 to Code 1023.

4 To achieve near zero output current, use the power-down feature.

5 Guaranteed by design and characterization; not production tested. SDA and SCL pull-up resistors are tied to 1.8 V.

6 Input filtering on both the SCL and the SDA inputs suppresses noise spikes that are less than 50 ns.

7 Power on time is required for the auto-calibration of the error amplifier input offset.

8 When test SDA leakage current, we put SDA High/SCL Low, test the current of SDA to Ground; When test SCL leakage current, we put SCL High/SDA Low, test the current of SCL to Ground.

10.3 Timing Specifications

VDD = 2.3V to 3.6V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Parameter[1]	Limit at T_{MIN},T_{MAX}	Unit	Description
f_{SCL}	1000	MHz max	SCL clock frequency
t_1	1	us min	SCL cycle time
t_2	0.26	us min	t_{HIGH}, SCL high time
t_3	0.5	us min	t_{LOW}, SCL low time
t_4	0.26	us min	$t_{HD, STA}$, start/repeated start condition hold time
t_5	50	ns min	$t_{SU, DAT,}$ data setup time
t_6[2]		us max	$t_{HD, DAT}$, data hold time
	0	us min	
t_7	0.26	us min	$t_{SU, STA}$, setup time for repeated start
t_8	0.26	us min	$t_{SU, STO}$, stop condition setup time
t_9	0.5	us min	t_{BUF}, bus free time between a stop condition and a start condition
t_{10}	120	ns max	t_R, rise time of both SCL and SDA when receiving
	0	ns min	May be CMOS driven
t_{11}	120	ns max	t_F, fall time of SDA when receiving
	300	ns max	t_F, fall time of both SCL and SDA when transmitting
	20+0.1 C_b[3]	ns min	
C_b	400	pF max	Capacitive load for each bus line

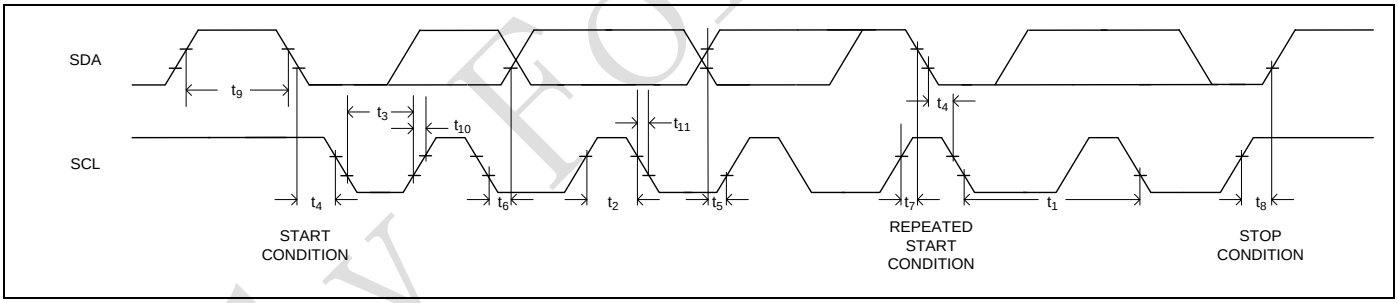


Figure16. Wire Serial Interface Timing Diagram

Note:

1 Guaranteed by design and characterization; not production tested.

2 A master device must provide a hold time of at least 300ns for the SDA signal (referred to the VINH MIN of the SCL signal) to bridge the undefined region of the SCL falling edge.

3 PCB is the total capacitance of one bus line in pF. t_R and t_F are measured between 0.3 VDD and 0.7 VDD.

11. Typical Performance Characteristics

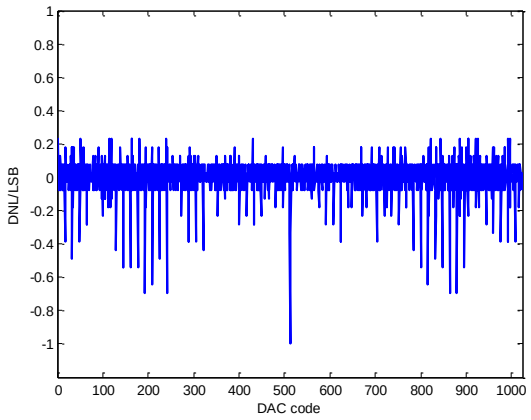


Figure17. DNL of 1023 code

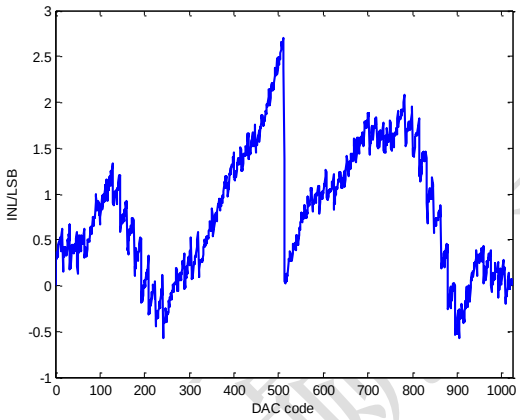


Figure18. INL of 1023 code

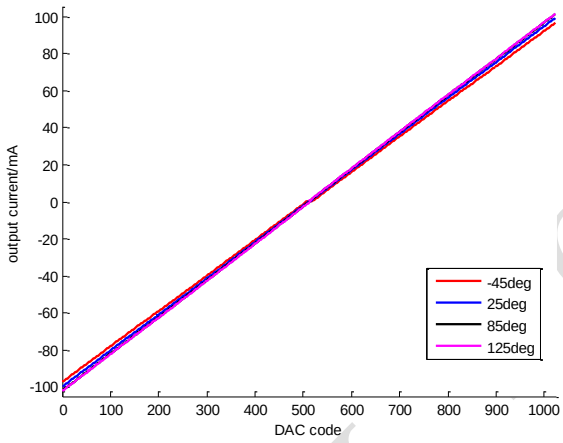


Figure 19. Output current in different temperature

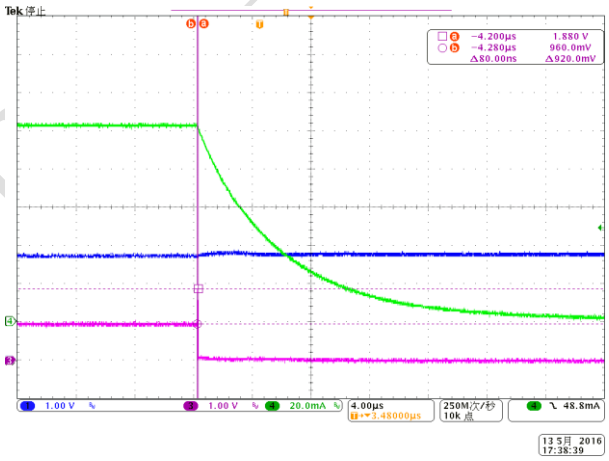


Figure20. Isink Power-down (VDD=3.6V)

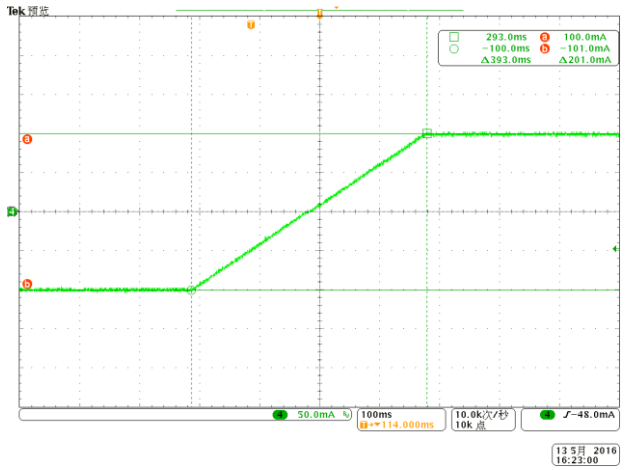


Figure21. linear control code 0- 1023 (VDD=2.8V)

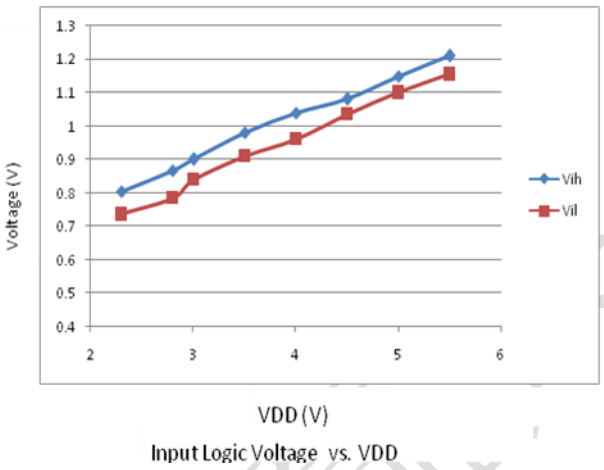


Figure22 input logic voltage vs VDD

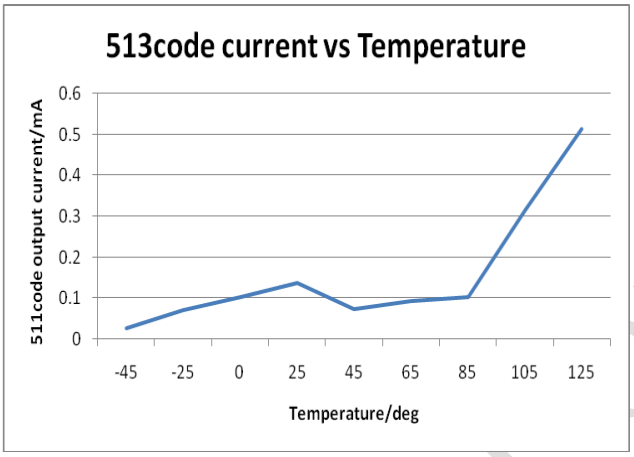


Figure23. 513code current vs temperature

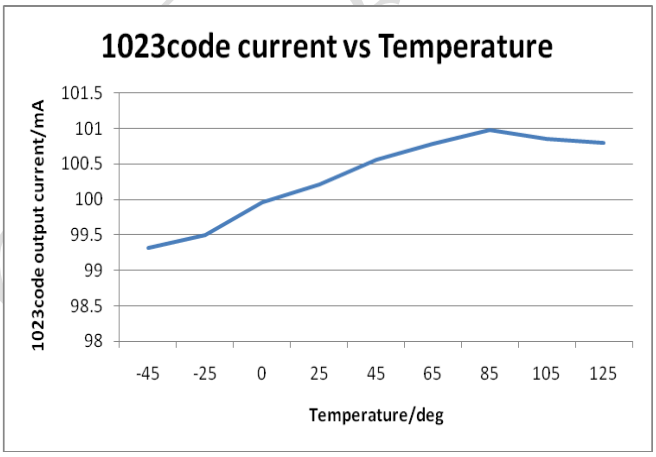


Figure24. 1023code current vs temperature

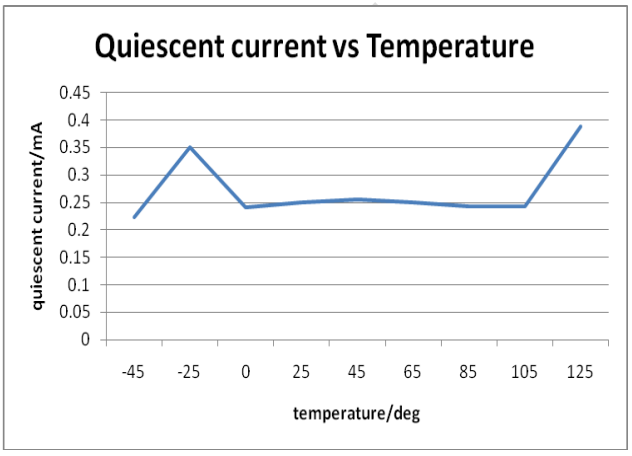


Figure25. Quiescent current vs temperature

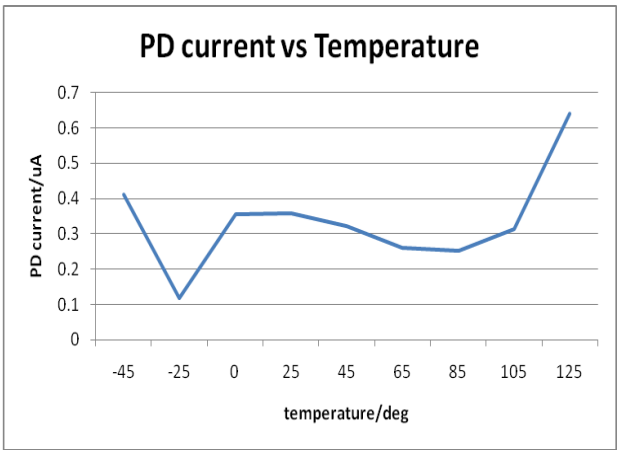
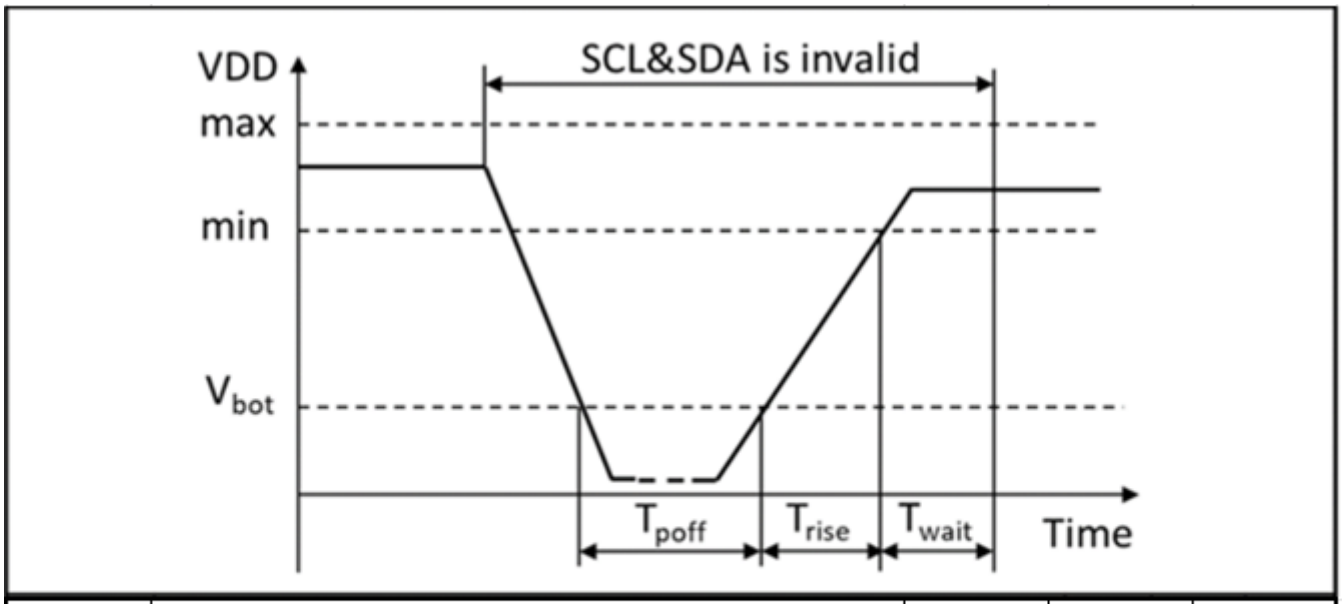


Figure26. PD current vs temperature

12. Power Up/Down Timing Requirement



Symbol	Parameter	min	max	unit
Vbot	VDD at power off		0.2	V
Tpoff	VDD at power off time	2		ms
Trise	Vbot to VDD min time		5	ms
Twait	The delay time before the device can be access	2		ms

13. Top Markings

- **GT9764BA-CLI-TR**

Marking: 64BA=GT9764BA

YWW: date code, Y=Year, WW=Week

- **GT9764BAH-CLI-TR**

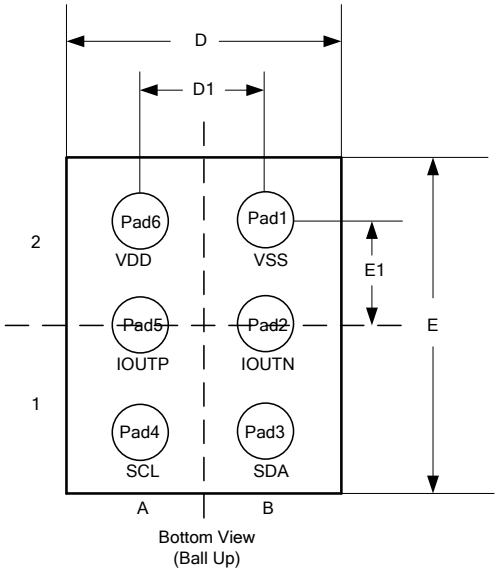
Marking: 64AH=GT9764BAH

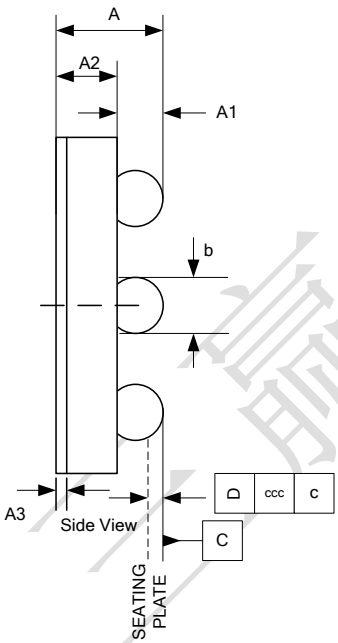
YWW: date code, Y=Year, WW=Week

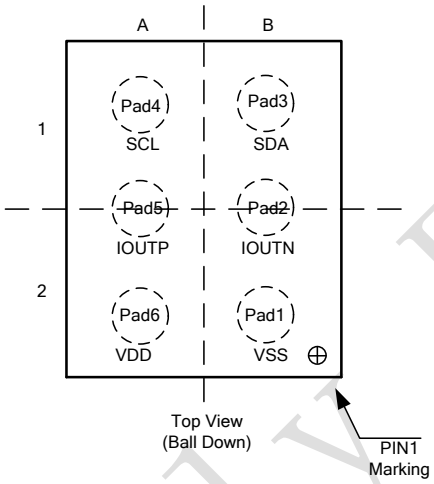
13. Ordering Information

Order Number	Marking	Package Option	Operating Temperature	Quantity	Note
GT9764BA-CLI-TR	64BA	WLCSP 6-Pin	-35ºC ~ 85ºC	Reel 4000	Bi-direction +-100mA
GT9764BAH-CLI-TR	64AH	WLCSP 6-Pin	-35ºC ~ 85ºC	Reel 4000	Bi-direction +-100mA

14. Part Markings -6 Ball WLCSP







SYMBOLS	DIMENSIONS IN MILLIMETERS			DIMENSIONS IN INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.260	0.280	0.300	0.0102	0.0110	0.0118
A1	0.045	0.055	0.065	0.0018	0.0022	0.0026
A2	0.200	0.225	0.250	0.0079	0.0089	0.0098
A3	0.020	0.025	0.030	0.0008	0.0010	0.0012
b	0.170	0.200	0.230	0.0067	0.0079	0.0091
D	0.700	0.720	0.760	0.0276	0.0283	0.0299
D1	--	0.400	--	--	0.0157	--
E	1.100	1.120	1.160	0.0433	0.0441	0.0457
E1	--	0.400	--	--	0.0157	--
ccc	--	--	0.010	--	--	0.0004

Note:
1. Controlled dimensions are in millimeter
2. Drawing is not in scale

15. Revision History

Revision	Date	Descriptions
A0	Aug.,2015	Initial Version
A1	Dec.2017	Version A1
A2	Feb.,2019	Update 'Total Resistance value of the Output'
A3	Sept.2020	Update IIC speed to 1MHz
A4	Nov.2021	Add timing requirements for power up/down
A5	Jun.2023	Typo Fixed
A6	Nov.2023	Trise spec update
A7	Nov. 2023	Tpoff spec update