Note: All differential pairs are routed as impedance controlled 100 ohm pairs (50 ohms individual impedance).

NOTE: ADC is initially in Power Down mode (PD/PDQ pulled high) and calibration delayed (ADC_CAL pulled high). When the FPGA is ready, it can begin the ADC power and calibration process.

U1G$1

ADC08D500

U2

XC6SLX9-3TQG144C

MOSI not used but it toggles during initialization.

M1 pulled down for Master Serial Mode.

M0 pulled up for Master Serial Mode.

Note: Unused Q input is connected to VCMO (datasheet p.34). Using buffered signal for safety.

NOTE: Resistors listed as NA are assumed to not be needed. They should all be 0603, placed on the back of the board, and not populated.

Note: HSWAPEN is pulled up to VCCO_0 (1.8V). During FPGA Configuration, if HSWAPEN is high, all IO are floating.

GROUND PAD

ADC and FPGA Connections

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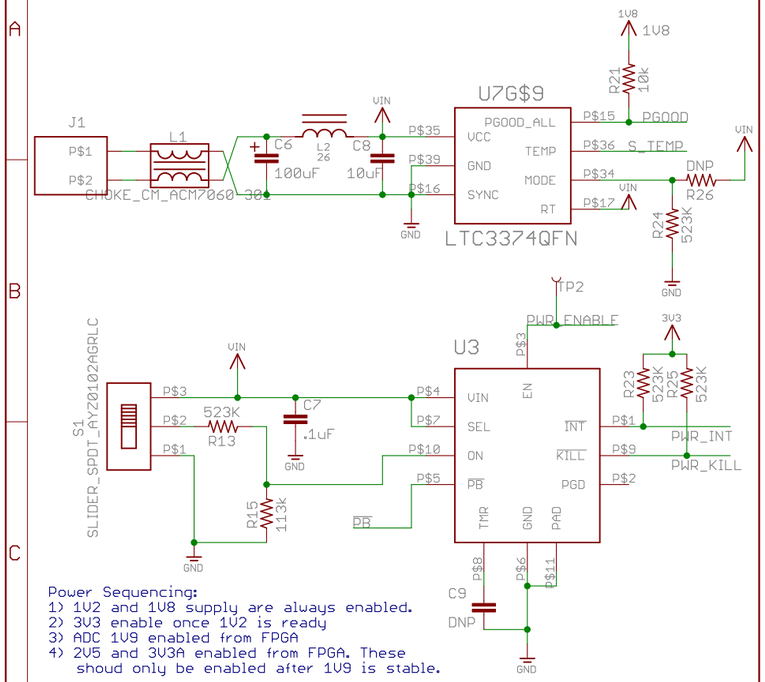
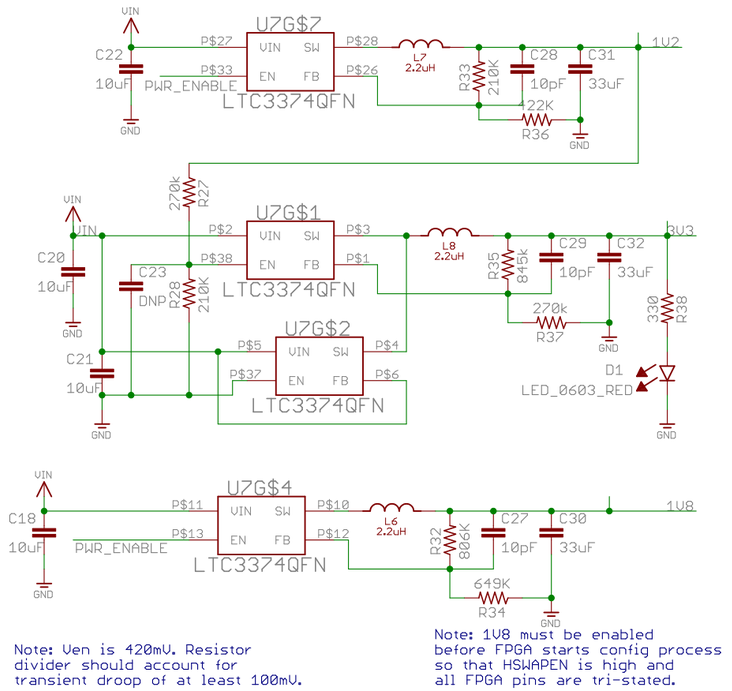
Power Regulation



Power Sequencing:
1) 1V2 and 1V8 supply are always enabled.
2) 3V3 enable once 1V2 is ready
3) ADC 1V9 enabled from FPGA
4) 2V5 and 3V3A enabled from FPGA. These shoud only be enabled after 1V9 is stable.

FPGA & Digital Power

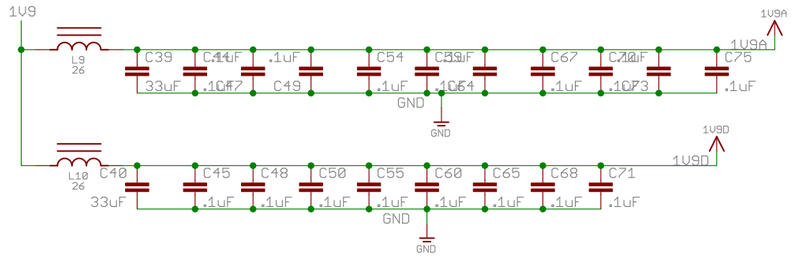


Note: Ven is 420mV. Resistor divider should account for transient droop of at least 100mV.

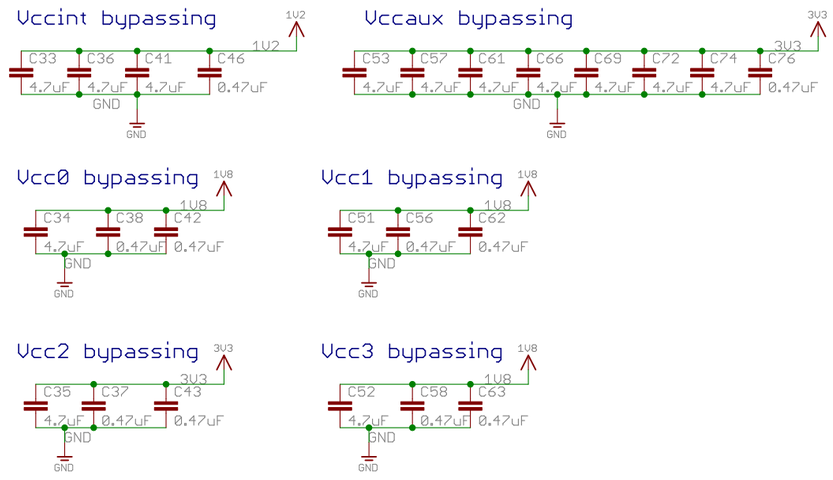
Note: 1V8 must be enabled before FPGA starts config process so that HSWAPEN is high and all FPGA pins are tri-stated.

ADC Bypassing

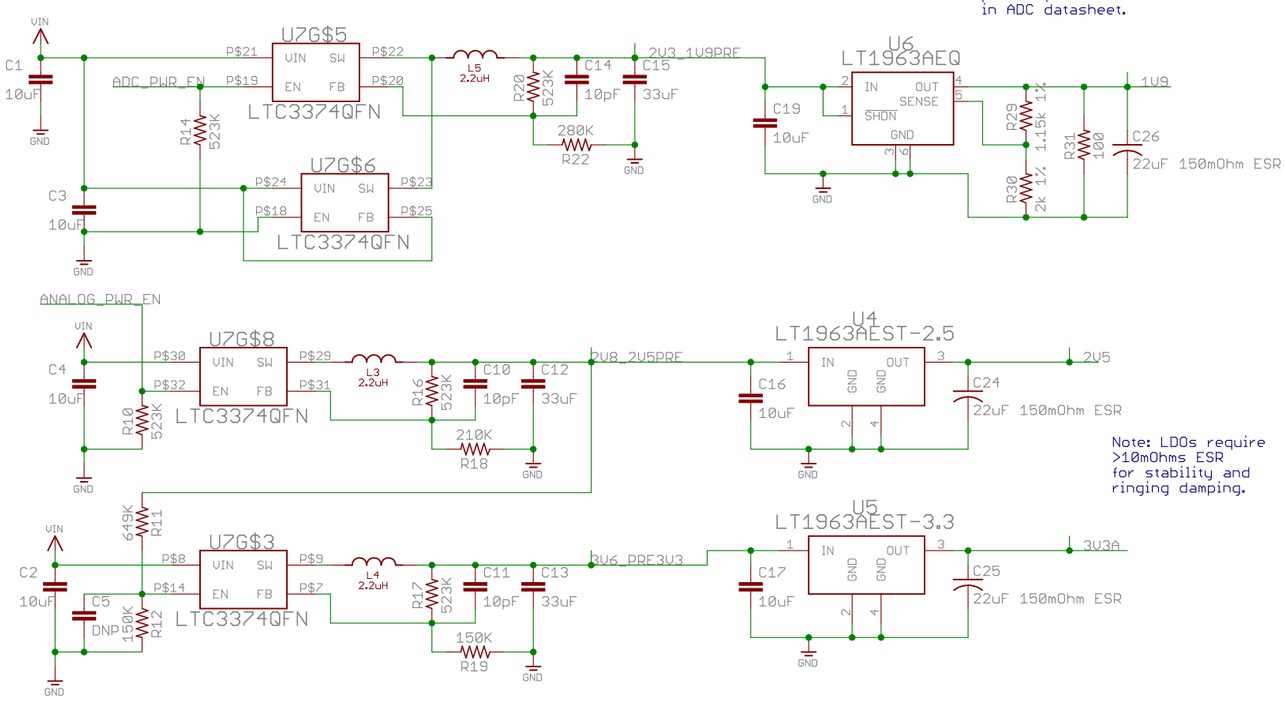
Each analog and digital supply pin is bypassed with a 0.1 uF capacitor. A 33uF capacitor is also placed within 1" of pins. Ferrite chokes isolate each supply from each other.



FPGA Bypassing



ADC and Analog Power



Note: LDOs require >10mOhms ESR for stability and ringing damping.

Power Supply and Bypassing

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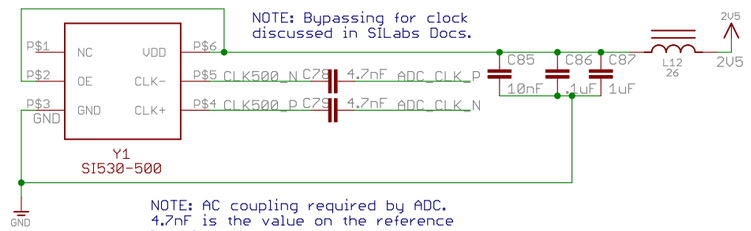
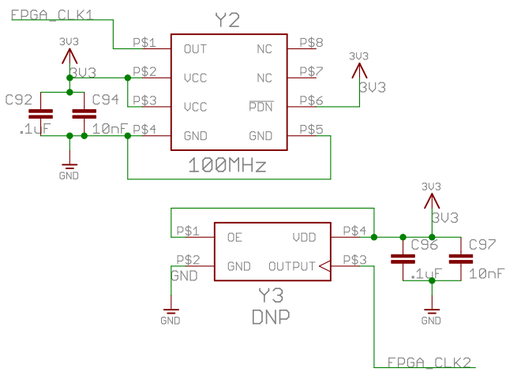
ADC Clock

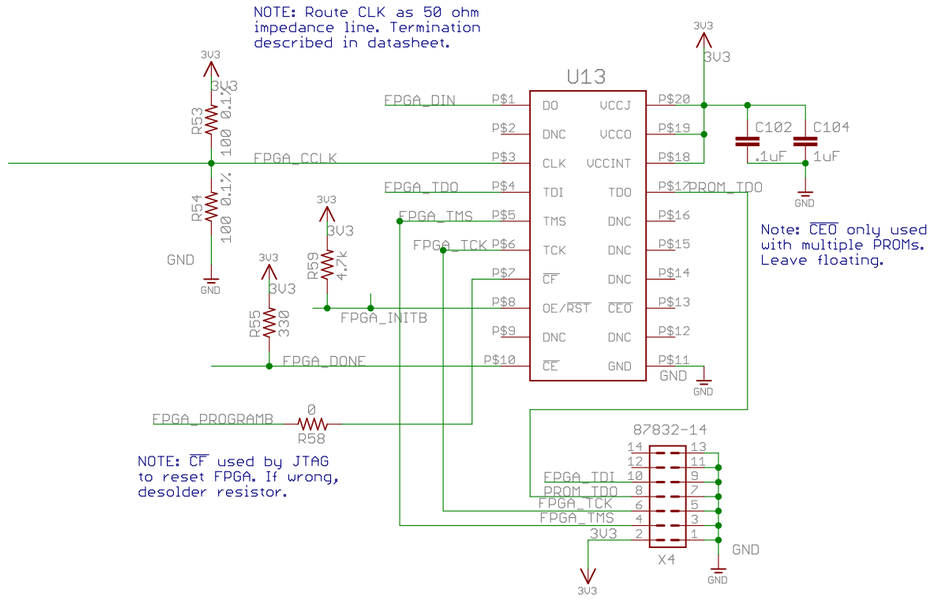


FPGA Clock

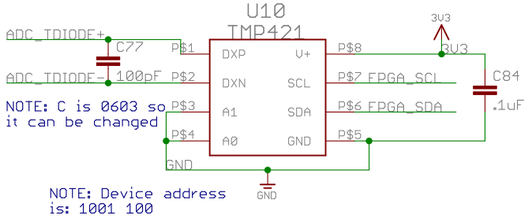
NOTE: Y3 is the primary clock. Y2 is a backup but should not be populated



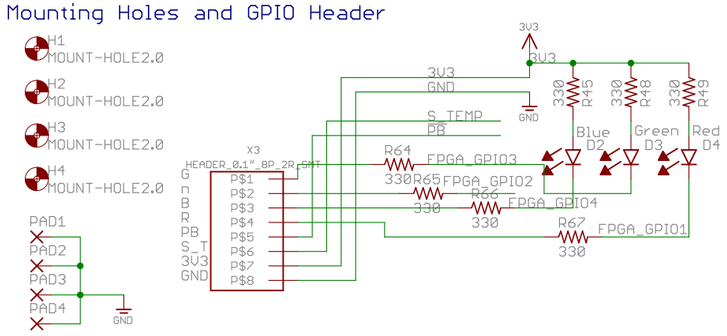
FPGA Programmable ROM (XILINX Platform Flash)



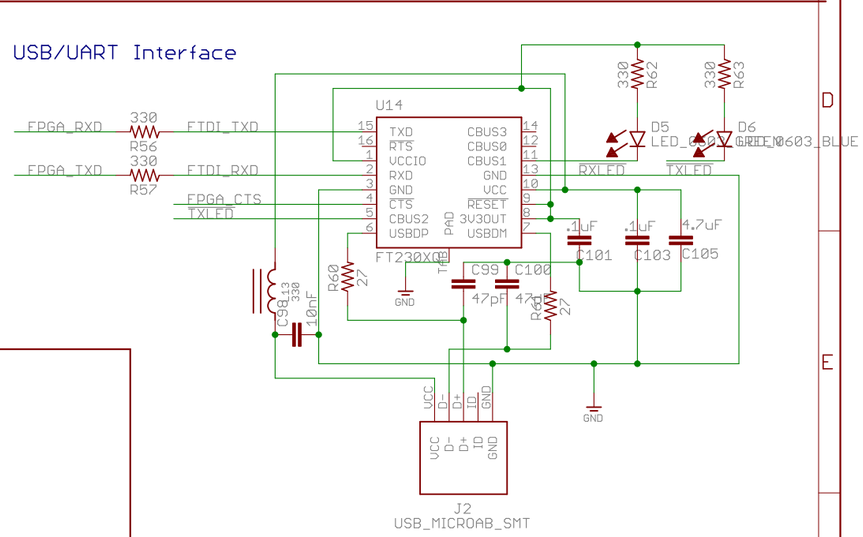
Temperature Sensor



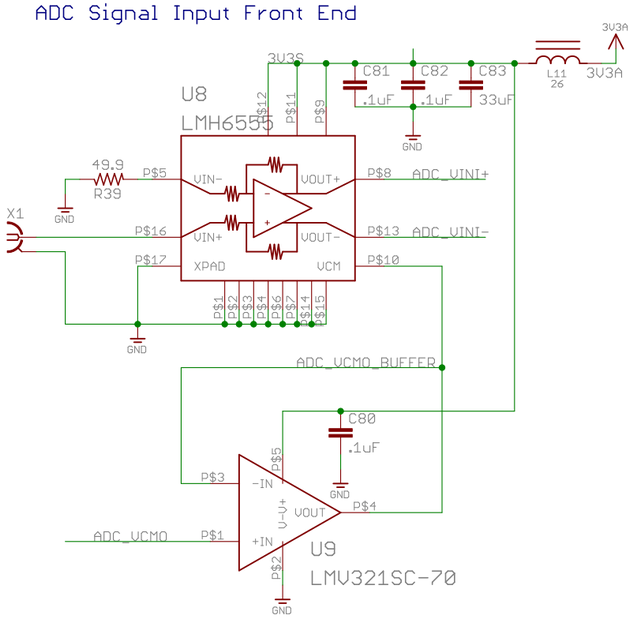
Mounting Holes and GPIO Header



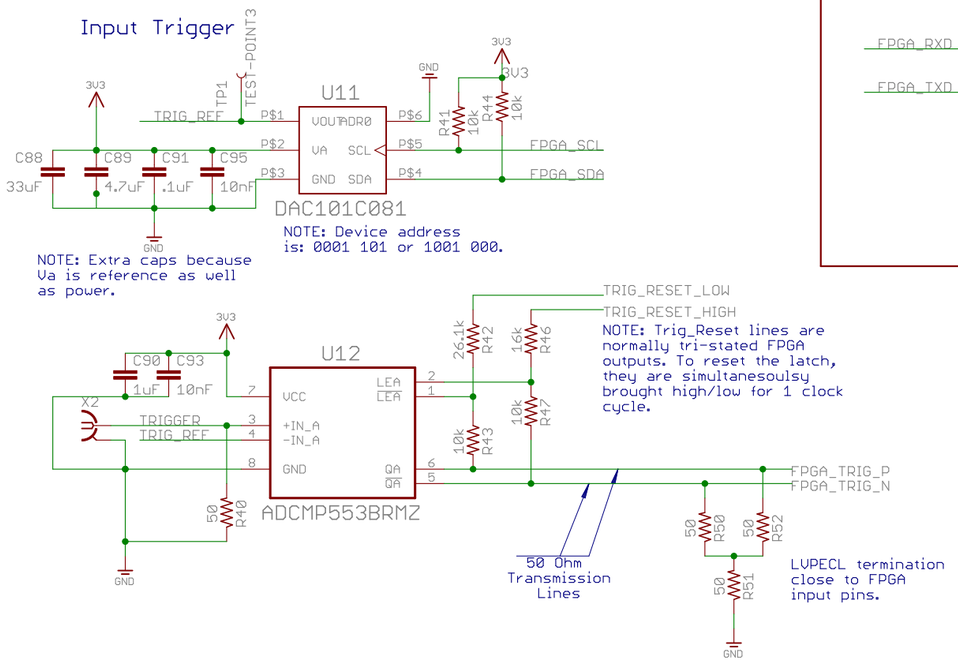
USB/UART Interface



ADC Signal Input Front End



Input Trigger



Additional Support ICs

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