Note: All differential pairs are routed as impedance controlled 100 ohm pairs (50 ohms individual impedance).

NOTE: ADC is initially in Power Down mode (PD/PDQ pulled high) and calibration delayed (ADC_CAL pulled high). When the FPGA is ready, it can begin the ADC power and calibration process.

M0 pulled up for Master Serial Mode.

MOSI not used but it toggles during initialization.

M1 pulled down for Master Serial Mode.

U$1

ADC08D500

U$2

XC6SLX9-3TQG144C

Note: Unused Q input is connected to VCMO (datasheet p.34). Using buffered signal for safety.

NOTE: Resistors listed as NA are assumed to not be needed. They should all be 0603, placed on the back of the board, and not populated.

Note: HSWAPEN is pulled up to VCCO_0 (1.8V). During FPGA Configuration, if HSWAPEN is high, all IO are floating.

ADC and FGPA Connections

TITLE: FastDataAcq

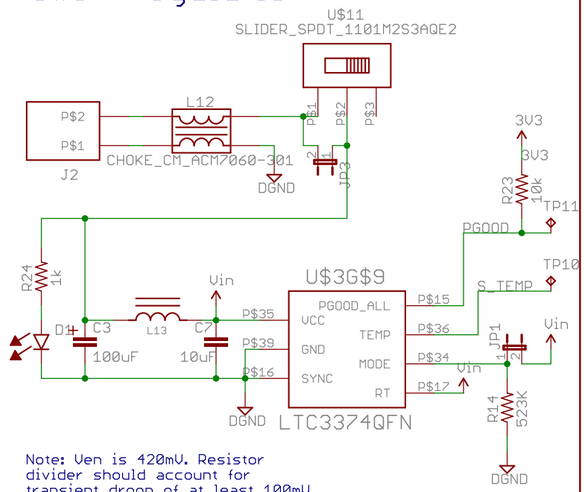
Document Number:

REV:

Date: 9/25/2013 6:07:57 PM

Sheet: 1/3

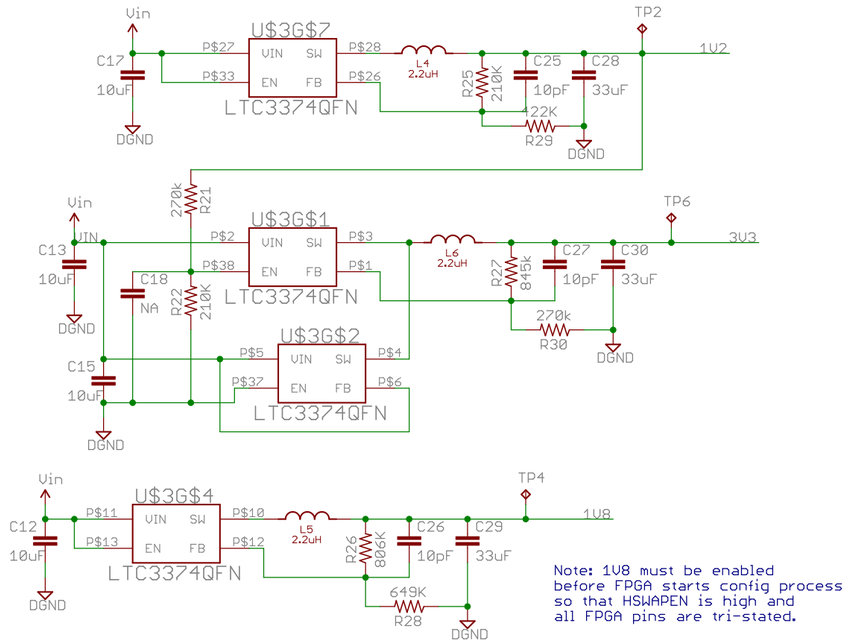
Power Regulation



Note: Ven is 420mV. Resistor divider should account for transient droop of at least 100mV.

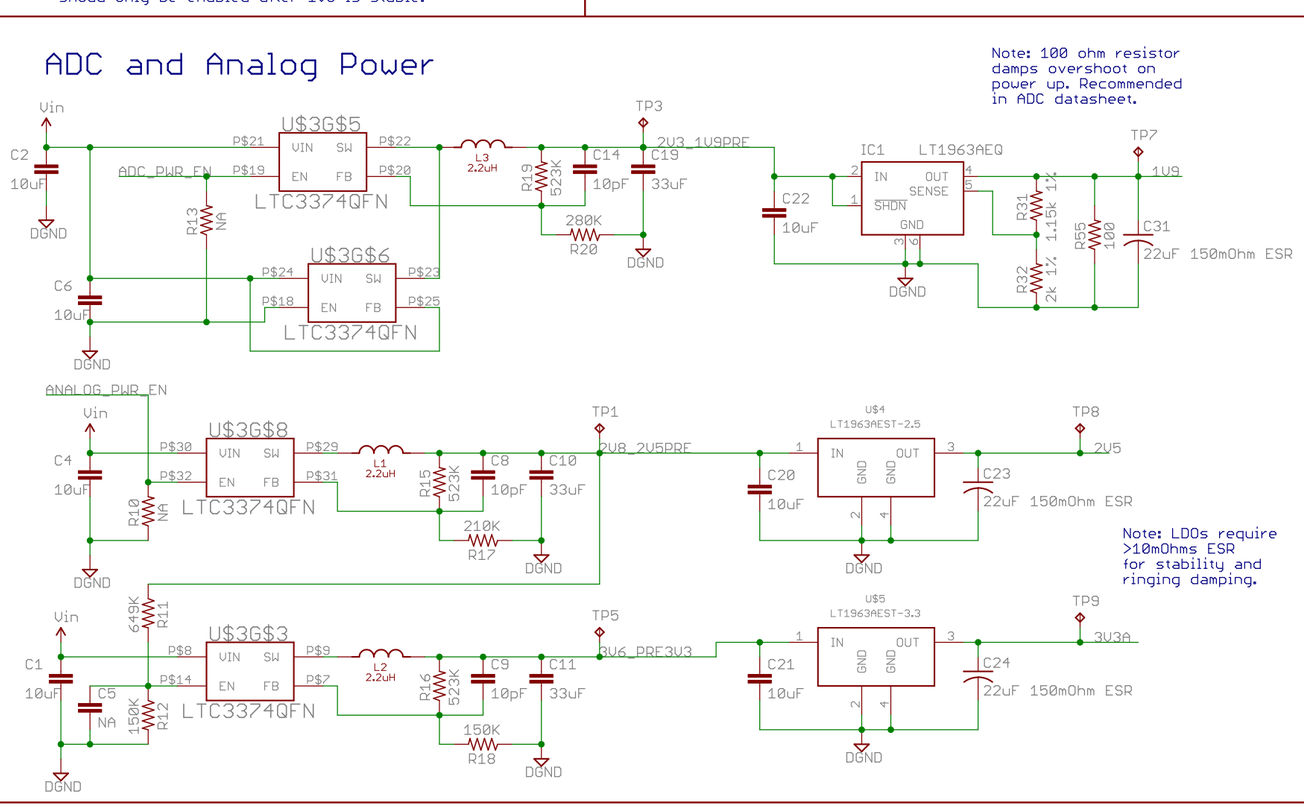
Power Sequencing:
1) 1V2 and 1V8 supply are always enabled.
2) 3V3 enable once 1V2 is ready
3) ADC 1V9 enabled from FPGA
4) 2V5 and 3V3A enabled from FPGA. These shoud only be enabled after 1V9 is stable.

FPGA & Digital Power



Note: 1V8 must be enabled before FPGA starts config process so that HSWAPEN is high and all FPGA pins are tri-stated.

ADC and Analog Power



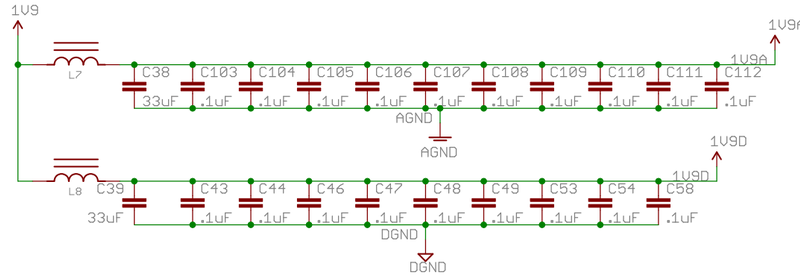
Note: 100 ohm resistor damps overshoot on power up. Recommended in ADC datasheet.

Note: LDOs require >10mOhms ESR for stability and ringing damping.

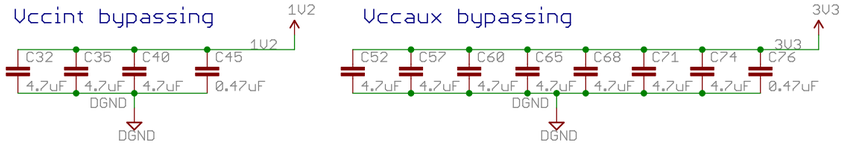
ADC Bypassing

Each analog and digital supply pin is bypassed with a 0.1 uF capacitor. A 33uF capacitor is also placed within 1" of pins. Ferrite chokes isolate each supply from each other.

TODO: Change 0.1uF 4V capacitors to 6V



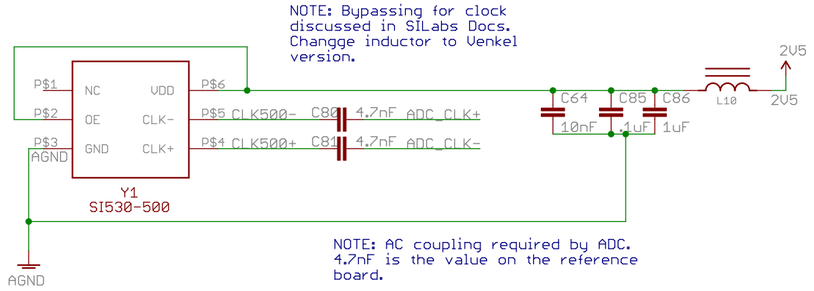
FPGA Bypassing



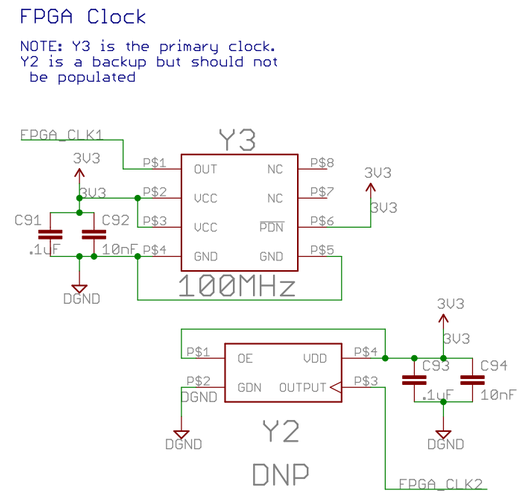
Power Supply and Bypassing

TITLE: FastDataAcq	
Document Number:	REV:
Date: 9/25/2013 6:07:57 PM	Sheet: 2/3

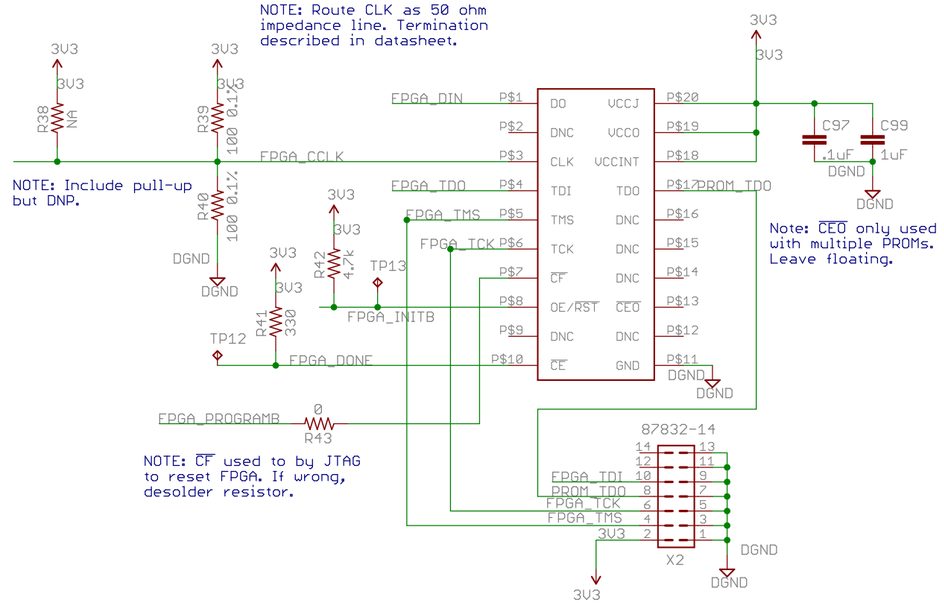
ADC Clock



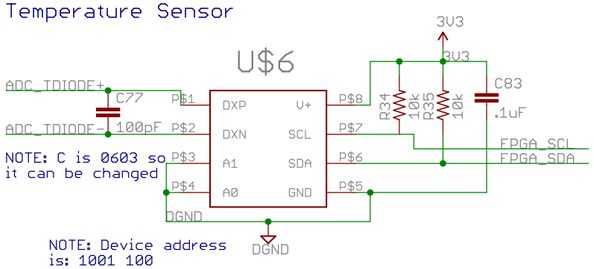
FPGA Clock



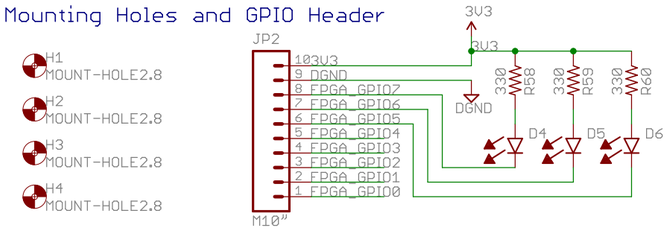
FPGA Programmable ROM (XILINX Platform Flash)



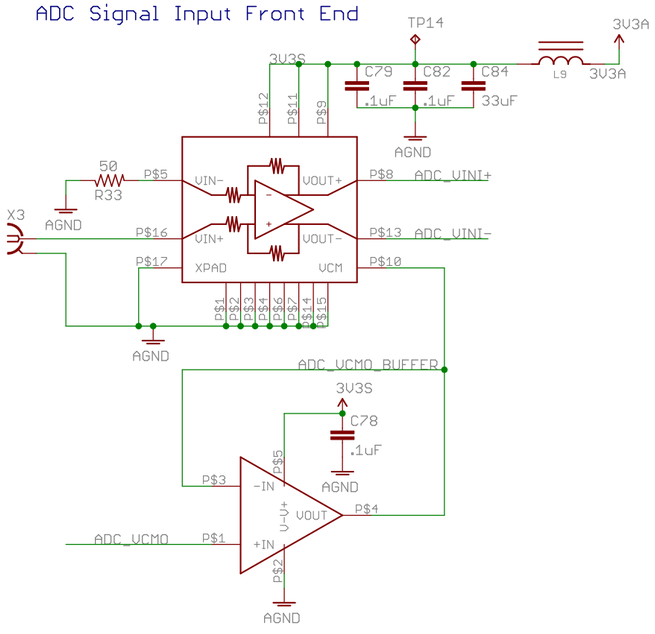
Temperature Sensor



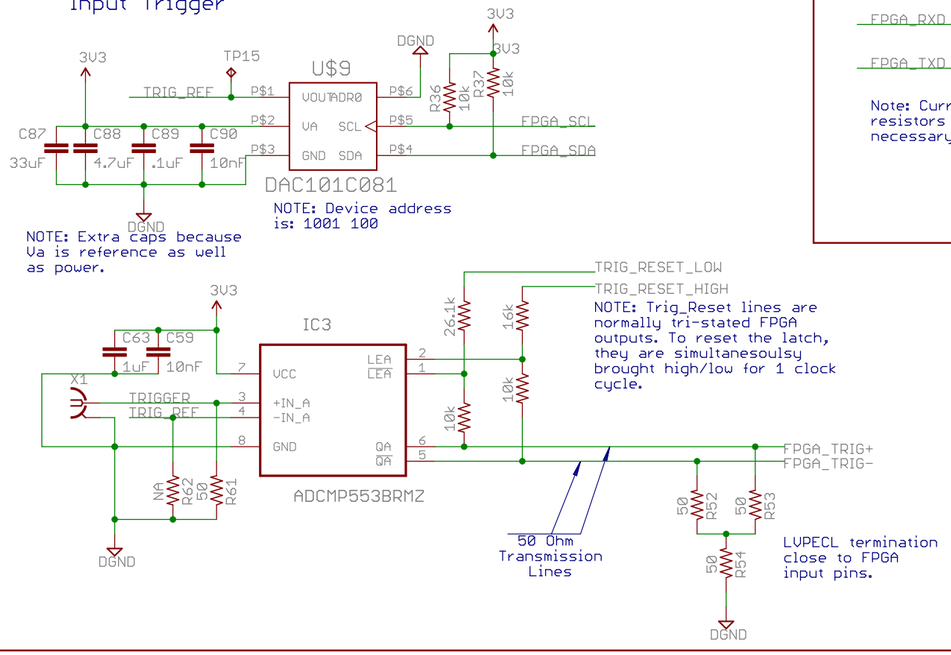
Mounting Holes and GPIO Header



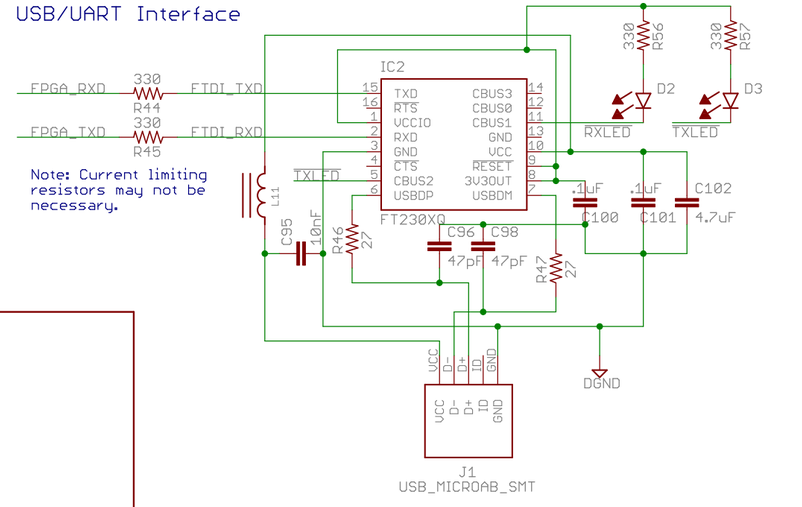
ADC Signal Input Front End



Input Trigger



USB/UART Interface



Additional Support ICs

TITLE: FastDataAcq	
Document Number:	REV:
Date: 9/25/2013 6:07:57 PM	Sheet: 3/3