High speed DAQ system with EDA and EKG extension

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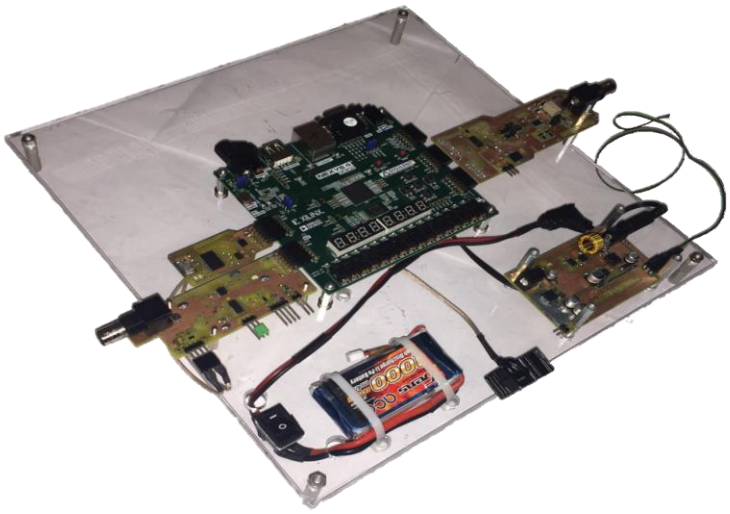

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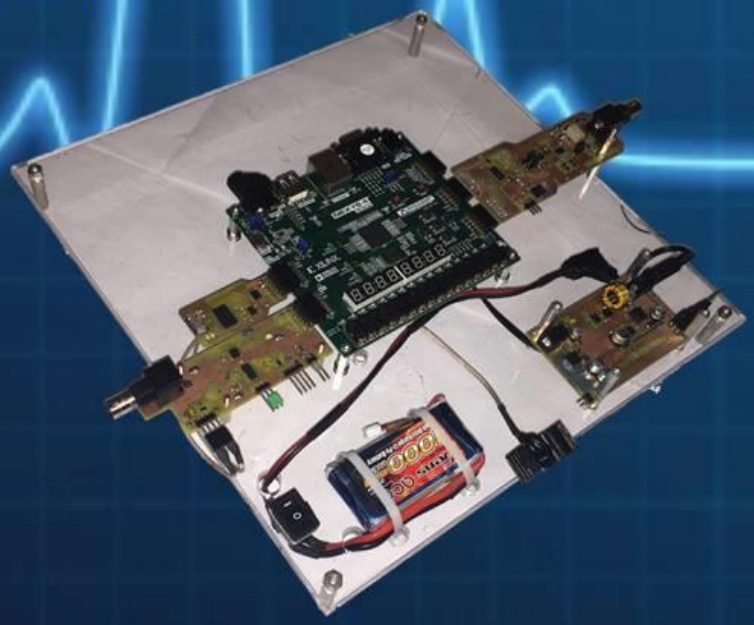
Product Marketing Sheet

Custom High Speed DAQ System with FPGA

Includes the following:

- High speed low cost digital oscilloscope with the following features:
  - 100 MSPS max sampling rate;
  - ± 30V max amplitude of the signal under test accepted;
  - PGA included with 4 stages of amplification/attenuation;
  - Fast Fourier Transform (FFT) included;
  - Bandwidth is 20MHz;
  - Low signal/noise ratio;
  - Very compact design.;
- Heart rate measurement based on non invasive method;
- Galvanic skin response (GSR) measurement;
- The device is fully galvanic isolated from main socket supply;
- LabVIEW GUI.



Introduction

Abstract

This project, **Custom High Speed DAQ with FPGA**, integrates 3 different features in a single system: an oscilloscope with FFT capabilities and a maximum sampling rate of 100 MSPS, a heart rate measurement module (based on **plethysmograph** method) and a galvanic skin response (**GSR**) module. Besides of this features, the entire project is powered from a Li-Po battery which provides galvanic isolation of the entire system with the main socket supply. The entire project is controlled by an **ARTIX-7 FPGA** based board, **NEXYS 4 DDR**, which communicates with the user through a GUI (Graphic User Interface) developed in LabVIEW. In this environment, the user can see the waveforms, and can also set all of the adjustments, which are converted in commands, and finally sent to FPGA.

Objectives

The main motivation of this project was the need to build something “unusual” that can be used by a lot of passionate persons (most of them, students with minimum knowledge in electronics), for their personal projects or applications which require this kind of device .

The main target is to design:

- Low cost oscilloscope with high resolution and high sampling rate, 100 MSPS and optional FFT;
- Possibility of heart rate measurement based on a non-invasive method, with optional visualization of the waveform;
- Possibility of galvanic skin response (GSR) measurement;
- Portable;
- Fully galvanic isolation with PC and the main socket supply.

Project Summary

The main idea of this project is to create something that encapsulates some measuring tools in a DIY DAQ system. In this way, a wide range of users can benefit from this, because, having a FPGA board and reproducing some modules, they could create their own tool. The features are:

- High speed oscilloscope with FFT (Fast Fourier Transform);
- Heart rate monitoring by using a non invasive method (Plethysmograph);
- Galvanic skin response (GSR), by measuring the voltage across 2 electrodes, placed in specific parts of the human body;
- Full galvanic isolation by using a battery for power supply board and galvanic isolated communication with PC.

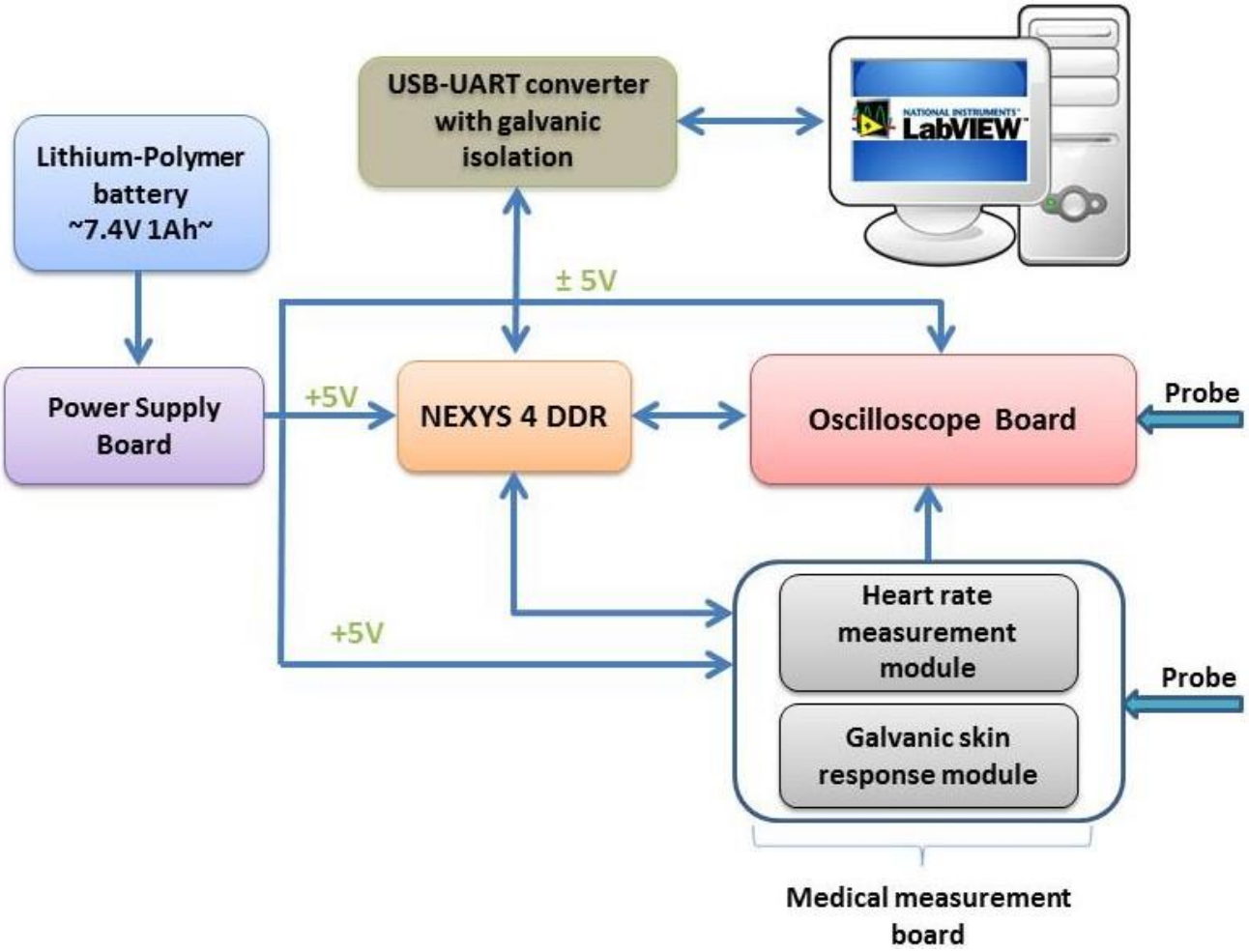


Fig.1 Entire project presented by a schematic block

The oscilloscope board use a 10 bit high speed ADC with parallel interface which can reach about **100 MSPS**. For processing the signal under test before it goes in ADC, an analogic part was developed, and it performs operations like:

- Buffering;
- Dividing;
- Amplification/attenuation control.

As the ADC has differential inputs and the analogic part used for processing the signal was single-ended, a differential driver was included to realize the conversion.

This module is capable of waveform analysis and it can also compute the FFT for the signal under test.

The medical measurement board contains two sub-modules on the same board. First module is used to measure the galvanic skin response (GSR) of a human subject by measuring the skin conductance (G), the value of GSR is measured with the oscilloscope board and it can be used in medical applications and also in psychological experiments. The second module is used to monitor the heart rate of a human by measuring the alteration of blood volume pumped by the heart. This feature uses an IR diode which sends IR light to the human tissue and a photo-transistor as main sensor receives the transmitted IR light, but it will be modified by the alteration of the blood volume. That is how is obtained the heart rate.

The USB-UART converter uses a dedicated USB-UART bridge which can emulate a virtual serial port, used for the communication with the NEXYS 4 DDR board. In order to achieve galvanic isolation, a dedicated IC was used in this purpose.

The power supply board contains 4 independent power supplies which give the voltages, referred to the ground like:

- +5V with capability of 1A used for powering NEXYS 4 DDR board;
- ±5V with capability of 1A used for powering the analogic part of the project.

The input of the power supply board ranges from 7V to 15V, but in our case a Li-Po battery is used in order to achieve galvanic isolation from main socket supply.

All the incoming and outcoming data to NEXYS 4 DDR board is managed by a GUI (Graphic User Interface) developed using LabVIEW.

Tools Required

For the electronic boards we used the following resources:

- Altium Designer for PCB design;
- 3 axis CNC milling machine for manufacturing the boards;
- Hot air station and solder iron for soldering the components;
- Power supply, signal generator, digital oscilloscope;
- Components (ICs, transistors, resistors, capacitors, inductors, connectors).

For the software part, we used the following resources:

- Windows7 and Windows 10;
- Digilent Adept software;
- ISE design compiler for writing the configuration file for FPGA;
- LabVIEW software from National Instruments.

Design Status

We are in time with the project and we shall be ready for the final presentations and demonstrations in the front of the jury. During the contest period we have encountered a lot of minor problems with the hardware part and software (especially with the configuration file for FPGA), but finally we managed to solve them all. Almost all the requirements of the project were archived.

Background

Why This Project?

The main reason for choosing this subject, was to approach a domain that appealed to us, to try to build something as advanced as possible, and also to build something that can be used by a other keen persons. Of course, there are many products on the market that can be more efficient and

also can have small dimensions than our device, but we cannot find a product on the market which has all 3 features embedded in one device.

Reference Material

We are everyday surrounded by a lot of types of waveforms and stray signals which need to be analysed and processed in order to find out the source and all the information that are carry out with them. The most simple waveform analyser is the oscilloscope. With this tool, almost any diagnosis can be done for the systems which don't work properly. The first versions of oscilloscopes were manufactured with tube lamps and then with cathode tubes, but those are analogic oscilloscopes. In this new era of technology, a new version of oscilloscope has been introduced on the market, the digital oscilloscopes. They can do a lot of more functions and mathematical operations like FFT (Fast Fourier Transform), which is the best way to analyse a signal in the frequency domain. The FFT was pioneered in 1973 for analysis of cosmic ray data.

Also based on waveform analysis, other devices were invented, like **polygraphs** with applications in medical field and not only. Parts of a polygraph system are heart rate measurement (based on plethysmography method) and galvanic skin response (GSR) which will be implemented in our project.

The plethysmography is used to measure different changes in volume, from fluctuations in the amount of the blood or how much air it contains. In our case, the method will be used to detect the heart rate of a human subject by measuring the amount of oxygen pumped in blood. The measurement test point will be chosen to be a finger.

The galvanic skin response is a phenomenon that can be influenced by several factors. Simplified, the term of galvanic skin response refers to the capability of the skin to lead the electricity, when an external voltage source is applied. Usually the galvanic skin response is measured in microSiemens (μS) and is the inverse of electrical resistance.

In the galvanic skin response measurement techniques, there were used DC sources and also sources of alternative current (AC). Thus, DC sources based measurements, in where the voltage at the skin contact is kept constant, is called skin conductance measurement, and the one when the current at the level of the skin contact remains constant is called skin resistance measurement. The AC measurement, in which the effective value of the voltage at the level of the skin contact remains constant is called skin admittance measurement. Similar, when the current is maintained constant using alternative power sources, the process is called skin impedance measurement.

The most practical method is to measure the skin conductance within the experiments for interpretation the psychological states, because the constant voltage source are easy to be achieved and used. The most complex device in this range, currently used to detect the emotional states, is the polygraph which, besides the skin conductance, also measures the pulse, the blood pressure, the body temperature and the respiratory rhythm. The first polygraph was the polygraph of John A. Larson from the University of California, which measured both the skin conductance and the blood pressure.

In our case the galvanic skin response will be measured in DC and will be with the voltage kept constant at the skin contact.

Fig.2 One of first versions of the polygraph around 1921

Design

Features and Specifications

This sytem is capable of the following features and specifications:

- Low cost digital oscilloscope is capable of measuring any type of signal with an input swing of maximum ±30V and it has the standard input impedance of 1MΩ||10pF;
- Measures the heart rate of the human heart and also plot the waveform;
- Measures the galvanic skin response and plot the value;
- It is fully galvanic isolated.

Design Overview

The NEXYS 4 DDR board features 4 standard PMOD I/O connectors which are connected to the electronic boards that we have designed, but not to all of them. Also, the board is powered from

an external 5V source and is no longer supplied from a USB cable. The configuration file will be burned in a memory located on the motherboard.

All the electronic boards were designed using Altium Designer software and finally, the boards were manufactured using a 3 axis CNC milling machine with GERBER files generated by Altium Designer. In this way 0.1 mm tracks were archived and boards look very professional. Each board was designed on 2 layers.

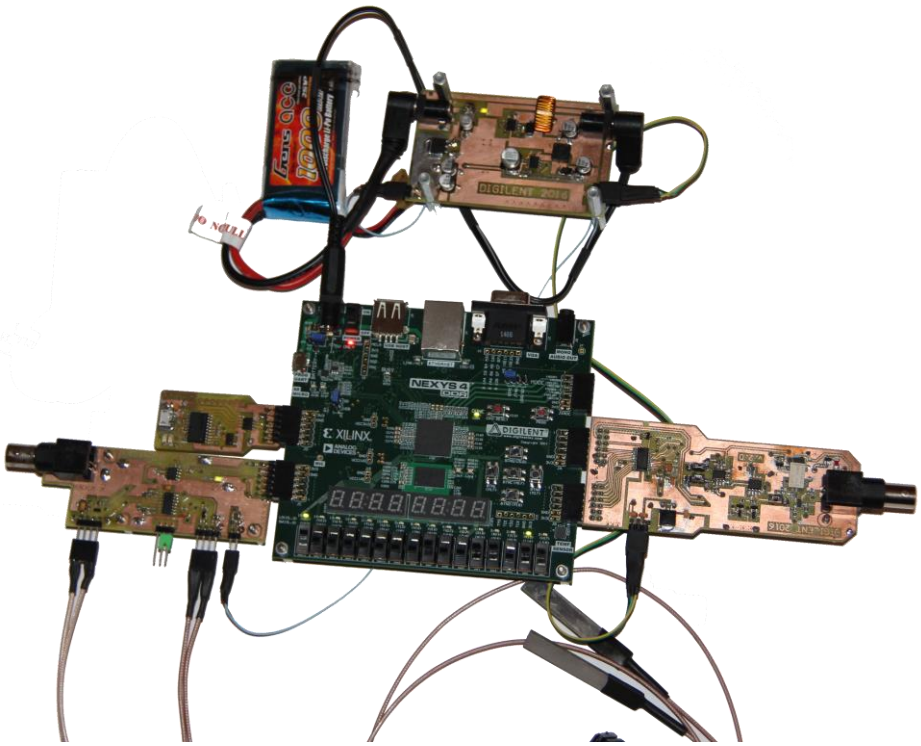


Fig.3 Hardware overview of the project

The FPGA board is the brain of the entire system, being the control unit. Besides the NEXYS 4 DDR board, the oscilloscope also includes an external hardware module, which is attached to the board via two PMOD connectors. Because working with high voltages is quite dangerous, an external isolated serial module was also included.

The main function of this system, is to provide the waveform of an analog signal, and also its Fast Fourier Transform. All of the computation part for the FFT is done in FPGA, so the only purpose of the GUI is to indicate the adjustments and to display the waveform, without any other tasks.

The ADC converter on the plugin board is an AD9215. It is designed to work on 10bits, and its maximum sampling rate is 105MSPS. In this project, we didn't exceed 100 MSPS, because there can appear harmonic distortion near the upper limit. Taking all of those into consideration, it is obvious why a FPGA is the best choice for this project. Otherwise is would be complicated to process a 10bit parallel bus.

This oscilloscope keeps the principles of any other one, and it displays the waveform frame by frame. When it comes to this part of instrumentation, any oscilloscope has three states in the measuring process: The PRERIG state, the TRIGGERING state, and the PROCESSING one. This is just at level of concept, because any of these states can also include more states.

As the waveform has to be displayed synchronized, this means that every time, the sampling process has to start from the same value of signal (and also the same slope). This value can be adjusted by the user and is called the TRIGGER LEVEL.

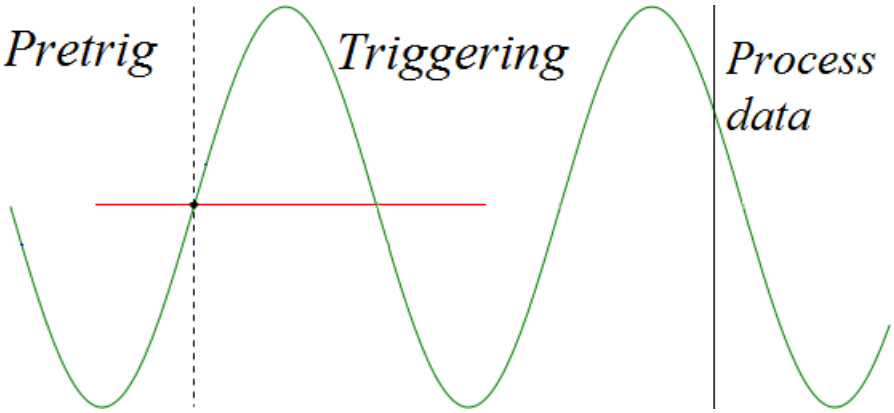


Fig.4 General states for oscilloscopes

As it can be seen, first time an oscilloscope is found in the Pretrig state, waiting a certain time period for the trigger level. When the trigger level is reached, the sampling state is started for a fixed number of samples (in our case 2048). In the process state, the waveform is taken from the buffer, processed and sent to display. After this, the entire process is restarted.

The most important adjustments are represented by the vertical and horizontal scale. The vertical one is easy to set, and it was presented in the analogic part. With the horizontal adjustment is more difficult. In theory, this setting is imposed by the sampling rate. That is the principle of the time base. The higher the sampling rate is, the smaller will be the time of acquisition, which involves a better capability of capturing high frequency signals. Because the high speed ADC's can't deal with low frequency clock signal, it will not be as easy as expected to modify the sampling rate. For instance, our ADC is guaranteed to be precise in the [1 MHz, 105 MHz] range of input clock signals.

In order to solve this problem, an "in code solution" was adopted. So, in this way the buffer of the FPGA won't store a sample on each clock cycle and it will ignore a number of samples according to the desired value for the time base. For instance, if a division by two is required, the system will store the current sample, and it will throw away the following one.

NEXYS 4 DDR boards, presents a 200 ohm resistor in series with every PMOD pin. So, taking into account that the parasite capacitance of the ADC's clock pin is very small, almost 5pF, it will appear in parallel with the input capacitance of the ADC clock pin (which is 3pf). In this way, it was obtained a RC low pass filter.

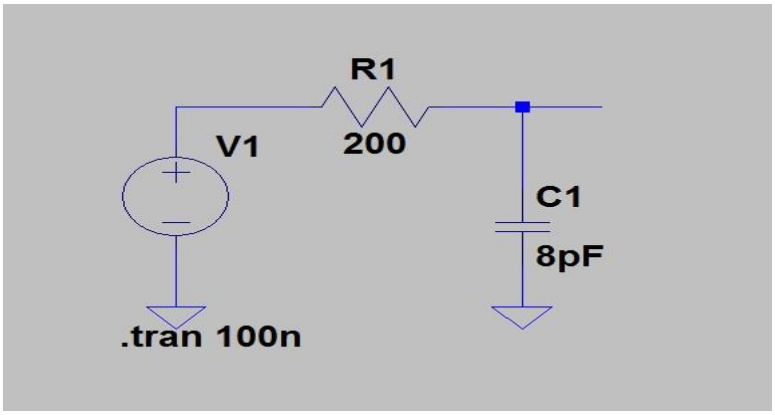


Fig.5 Equivalent RC filter

In order to simulate its behavior, a 100 Mhz square signal was applied on the RC's input. The result is visible in Fig. 6.

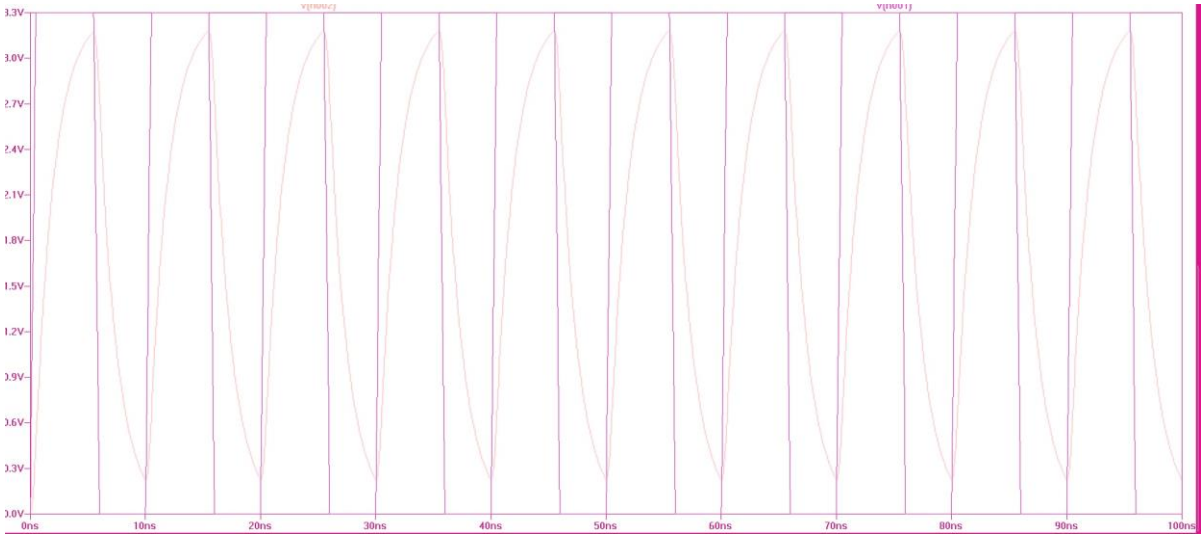


Fig.6 The output of the RC filter, with a square signal at input

The output signal appears to be very filtered, so the only solution to solve this problem is to replace the 200 ohm resistor with a short circuit. In this way, the system is able to provide a 100 MHz clock signal for the ADC.

Detailed Design Description for Hardware

The power supply board

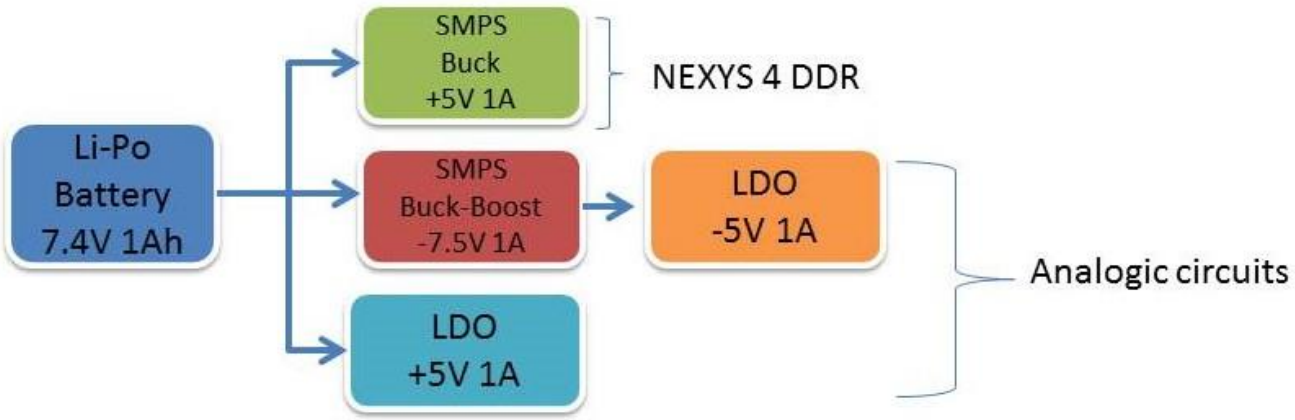


Fig.7 Block diagram of the power supply board

The power supply board is designed to meet the supply requirements of our project and also to provide a cleaner supply voltage with very low ripple value, about 50mV. It contains 2 Low drop out linear regulators (LDO) and 2 switching mode power supplies.

The first switching mode power supply used to power up the NEXYS 4 DDR board is made around MAX5035B which is a buck regulator IC capable of operation with input voltages from 7.5V to 76V and the output voltage is internally stabilized at 5V. This power supply can deliver up cu 1A, is more than enough for NEXYS to operate properly.

The second switching mode power supply is made around same IC family, MAX5035D, but operate in another configuration, buck-boost, in order to deliver a negative voltage referrer to ground. The output voltage is established via a feedback resistor network at -7.5V, and is used to get -5V using an LDO.

Linear regulators were used in order to have a good ripple rejection and a good stabilized voltage for the analogic part of the oscilloscope.

For safety measures a 2A fuse is put between the battery and power supply board.

This power supply was designed to be powered from a Li-Po battery, but can work very fine with an input voltage from 7V to 15V.

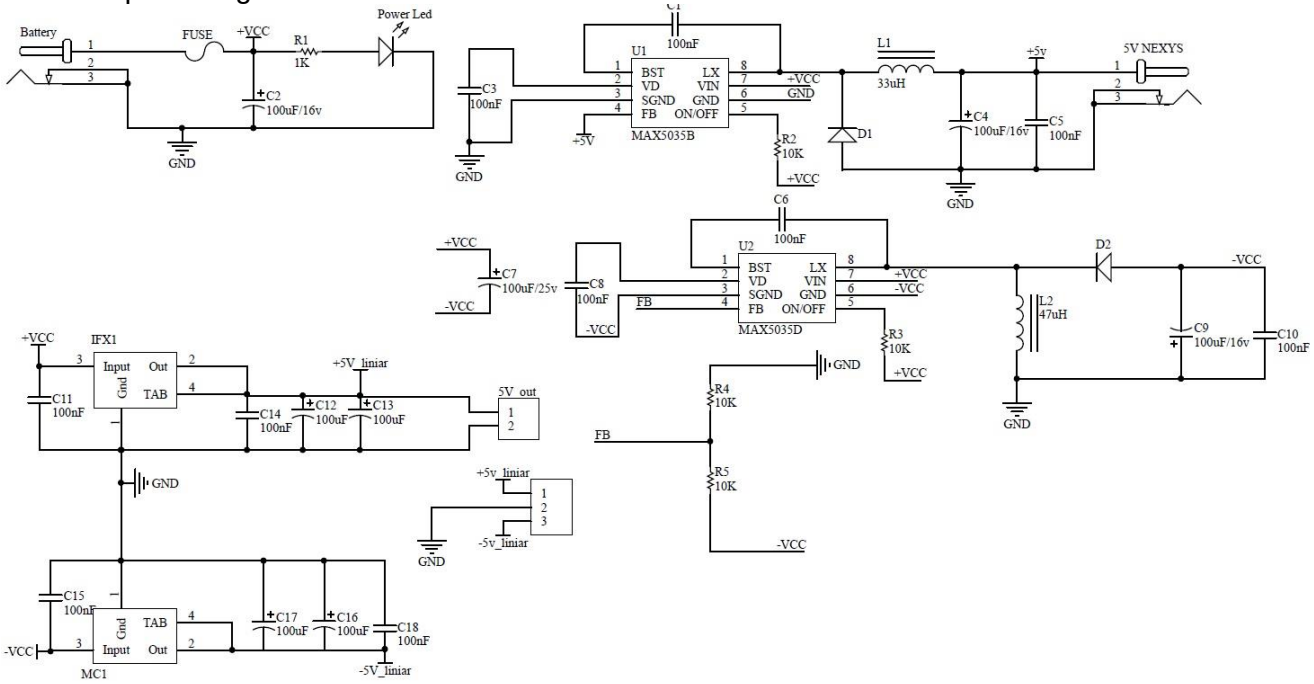


Fig.8 Electric schematic of power supply board

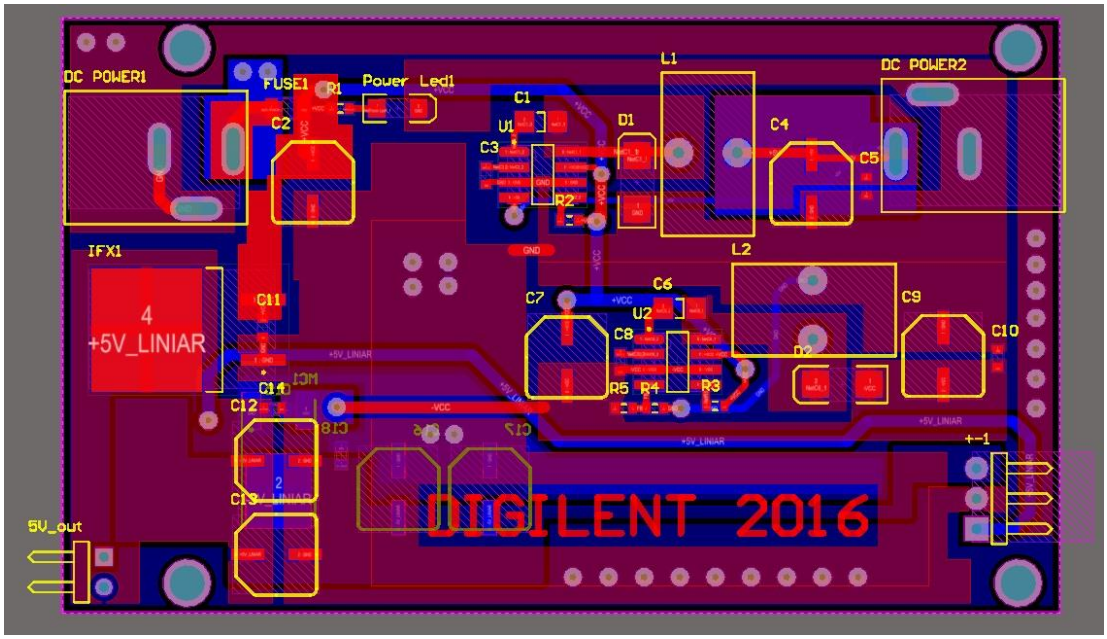


Fig.6 PCB Design of power supply board

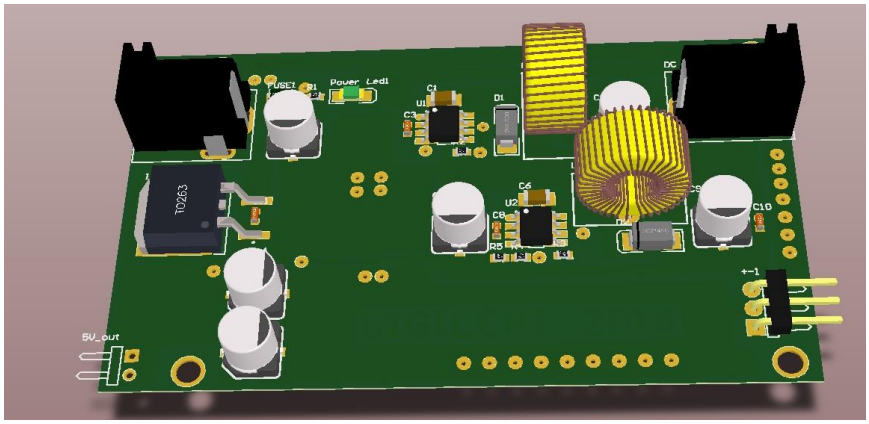


Fig.9 3D design of power supply board

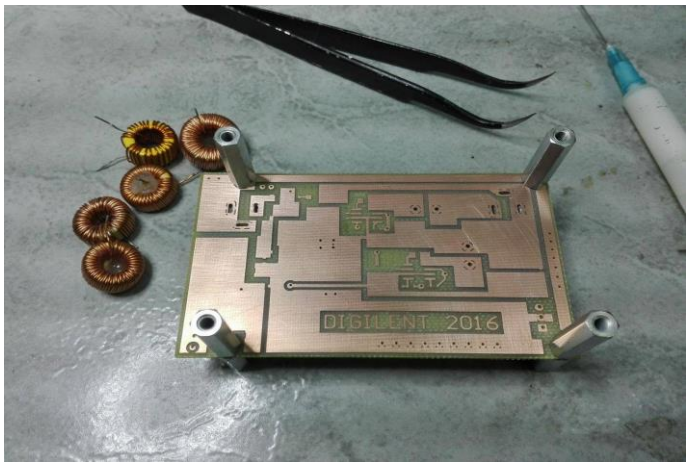


Fig.10 PCB after was manufactured by CNC

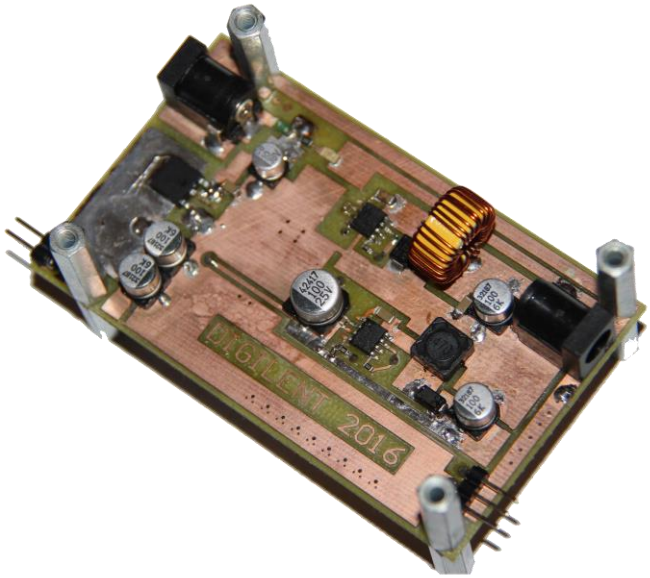


Fig.11 Power supply board fully assembled and tested

The oscilloscope board

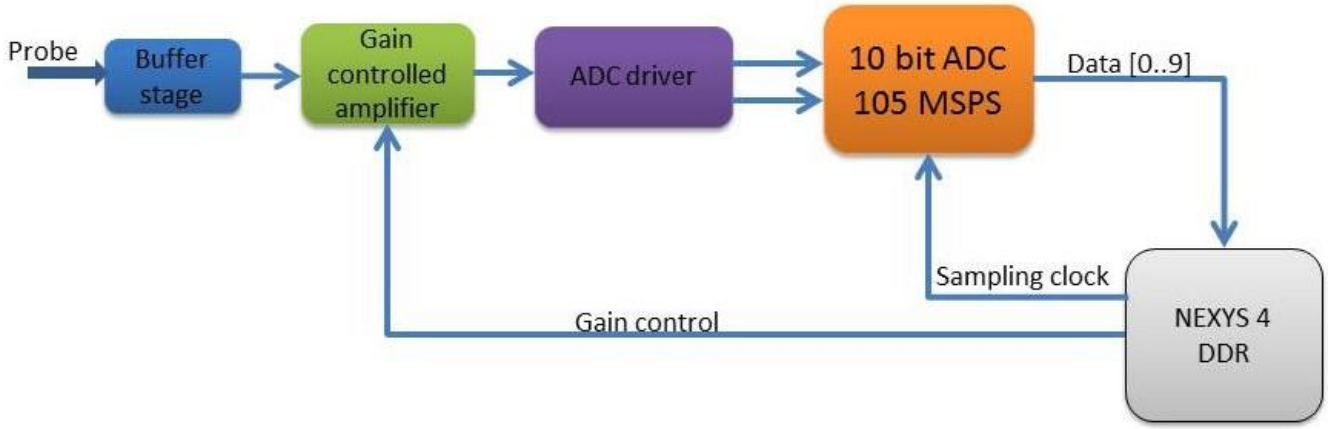


Fig.12 Block diagram representing the oscilloscope board

At first, the signal has to go through the **buffer stage**, which is actually a JFET input op-amp, OPA659. Then, the signal is injected into a compensated attenuator with the possibility of adjusting the attenuation with a signal relay, when is needed. The voltage divider has on each resistor a parallel capacitor in order to present equal values for the time constants.

The next stage is the amplification stage designed with a **gain controlled amplifier,** commanded by FPGA according to the needs of the user. This stage has a wide band op-amp, **ADA4857,** with the feedback network controlled by FPGA via 4 N-channel MOSFET transistors placed in anti-series configuration, which switches between 2 resistors in to the feedback network of the op-amp. The values of gain can be 1, 3 and 5, and are all configurable.

After the signal passes through these 2 blocks, it is directed by ADC driver, **AD8138**, to the differential inputs of the ADC. In this way a single-ended to differential conversion is achieved. Consequently, this configuration is a much more noiseless than a single-ended one.

The ADC, AD9215, is a high speed 10 bit ADC with parallel interface and has a maximum sampling rate of 105 MSPS. The maximum input admissible voltage on his differential inputs is ±1V.

Also, for safety reasons it has a dedicated pin which enters in a specific state when the signal is over range. Another useful feature of this ADC is the dedicated input pin which enable/disable the ADC.

In order to measure signals with higher amplitude the user can use a probe with 10x or 100x attenuation placed before the buffer stage.

For the analogic and digital part where used 2 separate grounds in PCB design which are united in one single point. This method is used to minimize the noise and to obtain a good noise/signal ratio.

The clock track provided by FPGA to drive the ADC, is placed between grounds planes in order to minimize the crosstalk effects.

The input impedance of the oscilloscope is 1MΩ and a capacitance of 10pF. Also the bandwidth is around 20MHz.

The entire board is supplied with ±5v from linear regulator and also a 3.3V linear regulator was placed on the board in order to supply the ADC and other circuits. In this case we didn't want to use the 3.3V from FPGA PMODs because it is noisy (all the voltages from NEXYS 4 DDR board are obtained from switching mode power supplies).

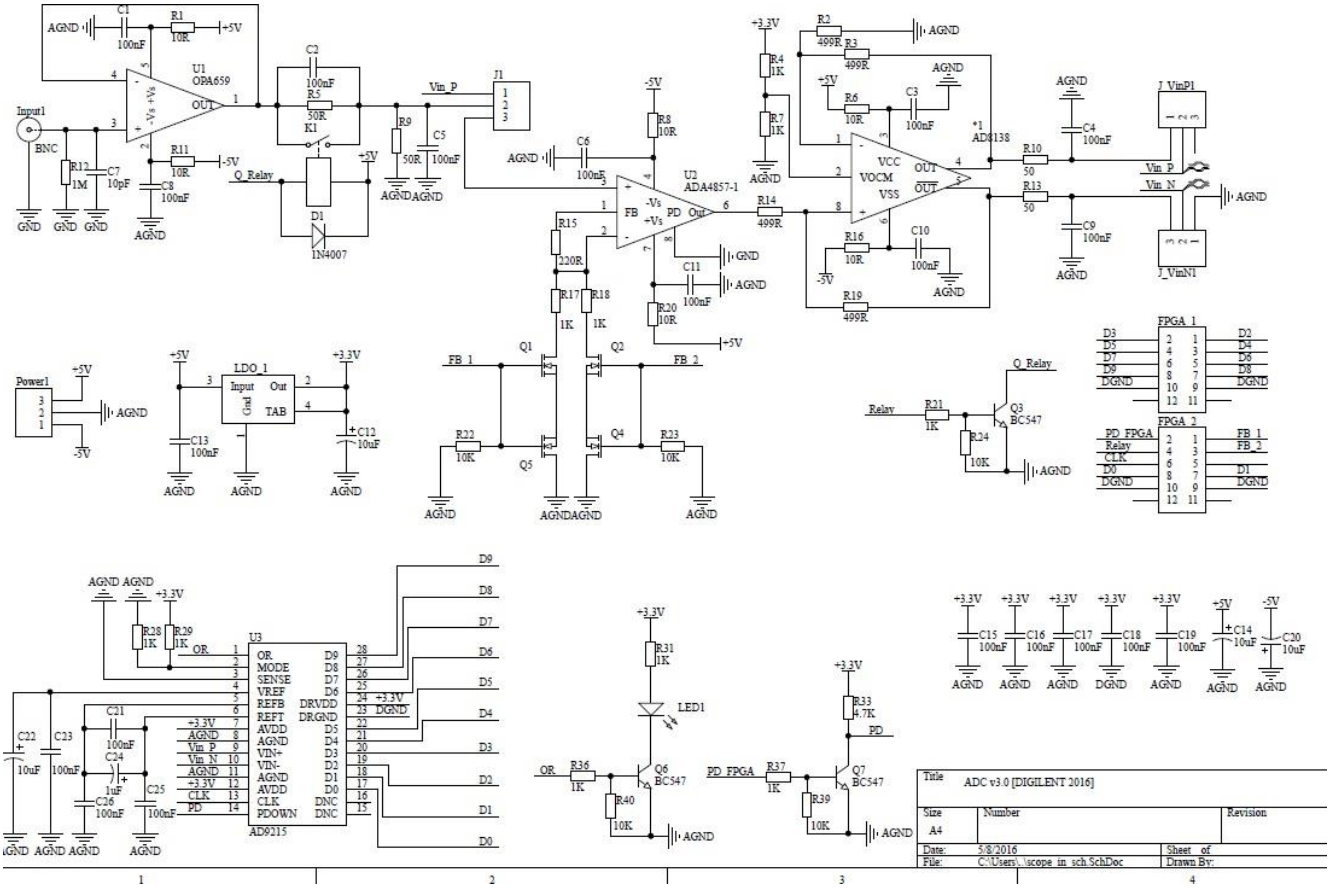


Fig.13 Electrical schematic of the oscilloscope board

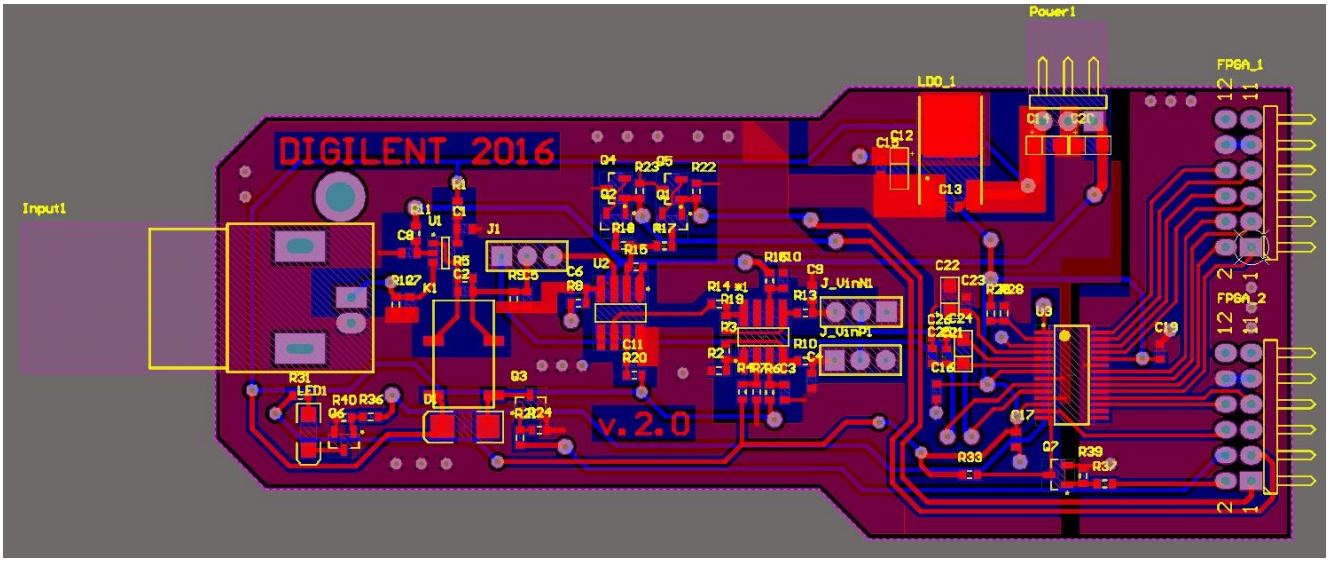


Fig.14 PCB design of the oscilloscope board

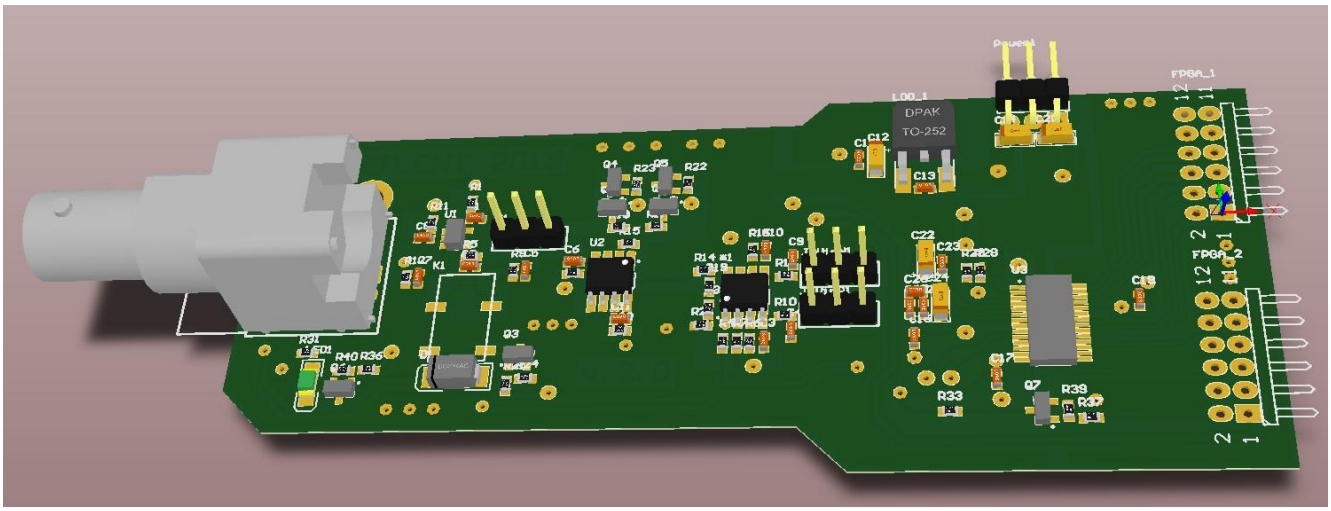


Fig.15 3D design of the oscilloscope board

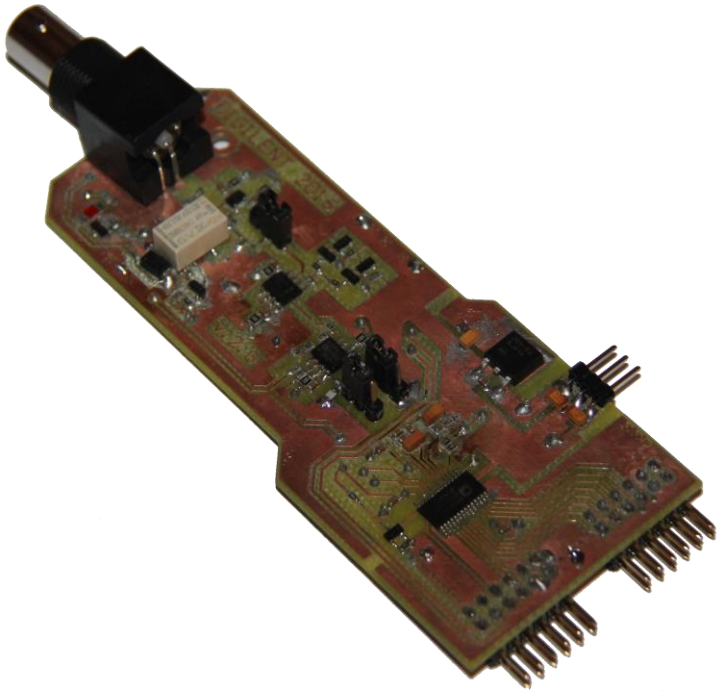


Fig.16 The oscilloscope board fully assembled

The USB-UART converter board

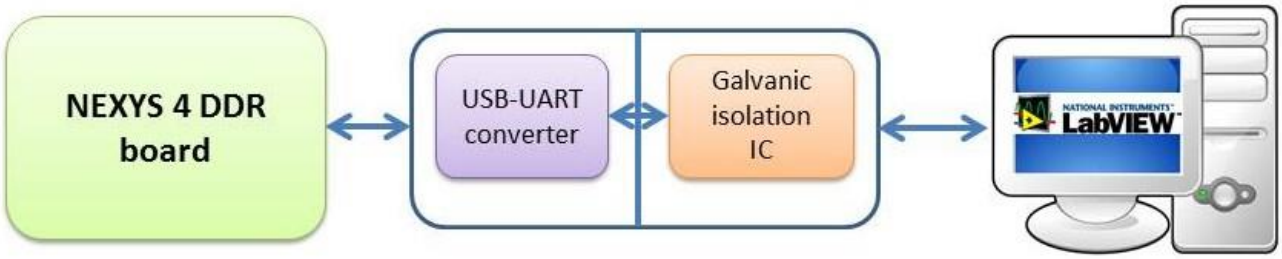


Fig.17 Block diagram of the USB-UART converter

This module is made around MCP2200 from Microchip, which is an USB-UART bridge with capabilities of 1Mbaud maximum speed. The galvanic isolation is made with a specific IC, ADUM1201, from Analog devices, which also integrates a Schmidt trigger circuit at his output terminals.

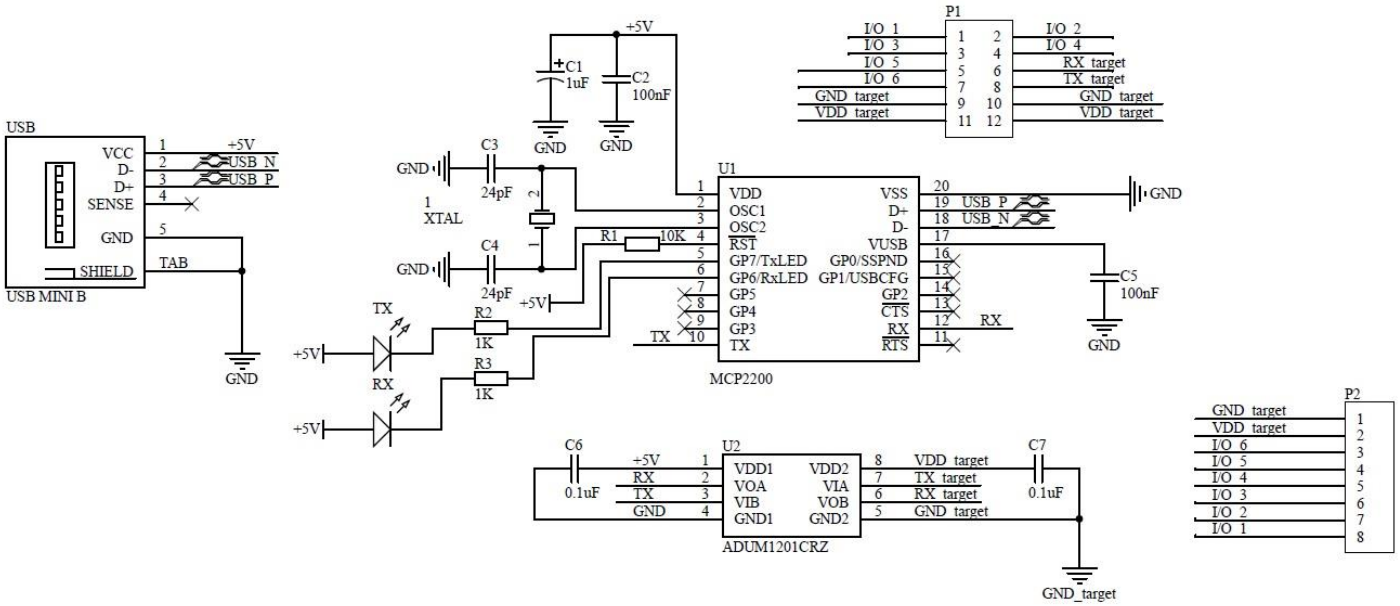


Fig.18 Electrical diagram of the USB-UART converter

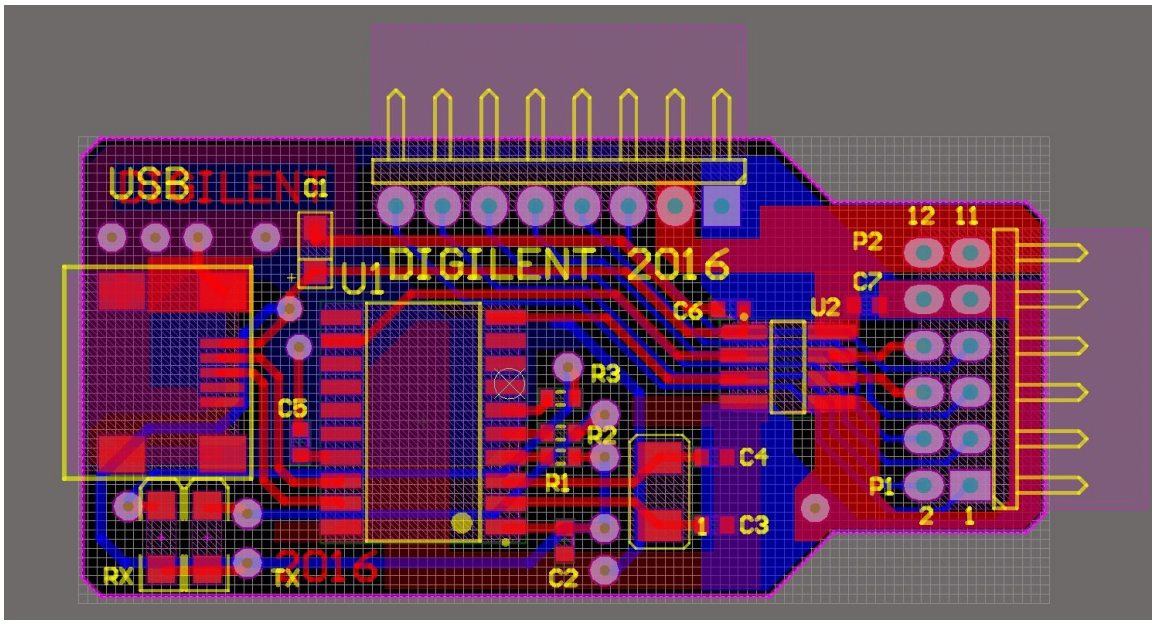


Fig.19 PCB design of the USB-UART converter

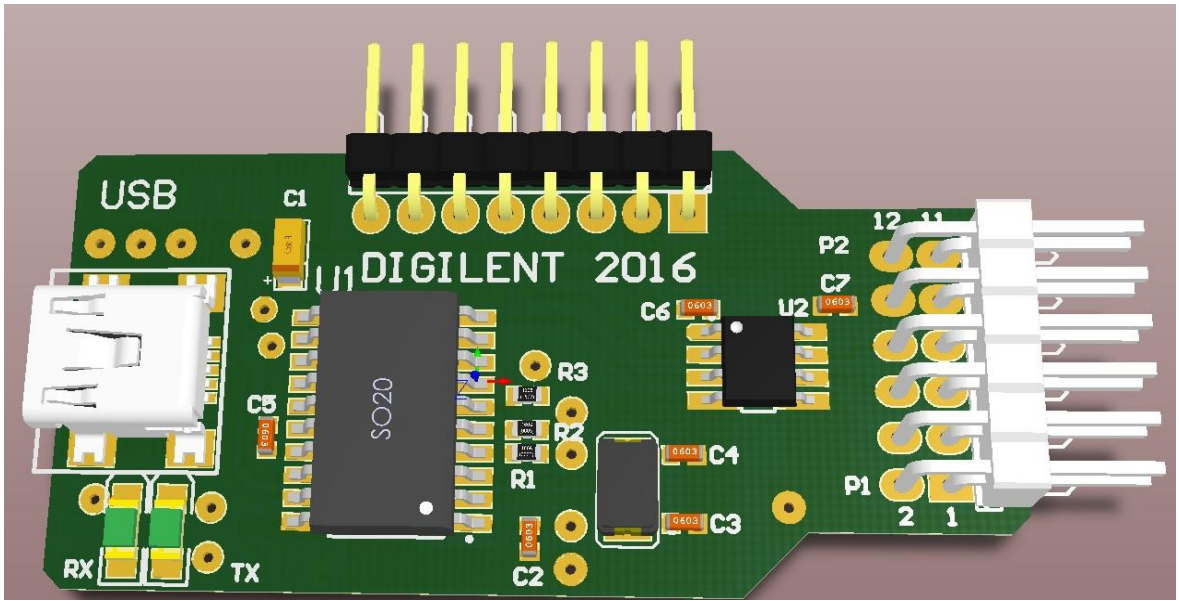


Fig.20 3D Design of the USB-UART converter

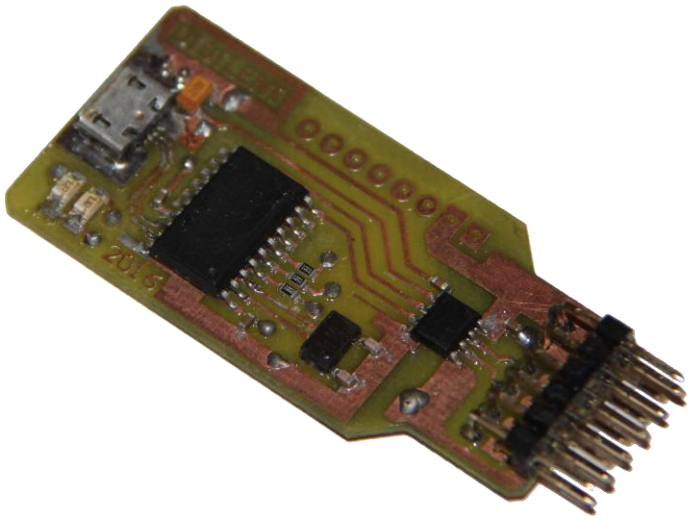


Fig.21 USB-UART converter module fully assembled and plugged in to NEXYS board

The medical measurement board

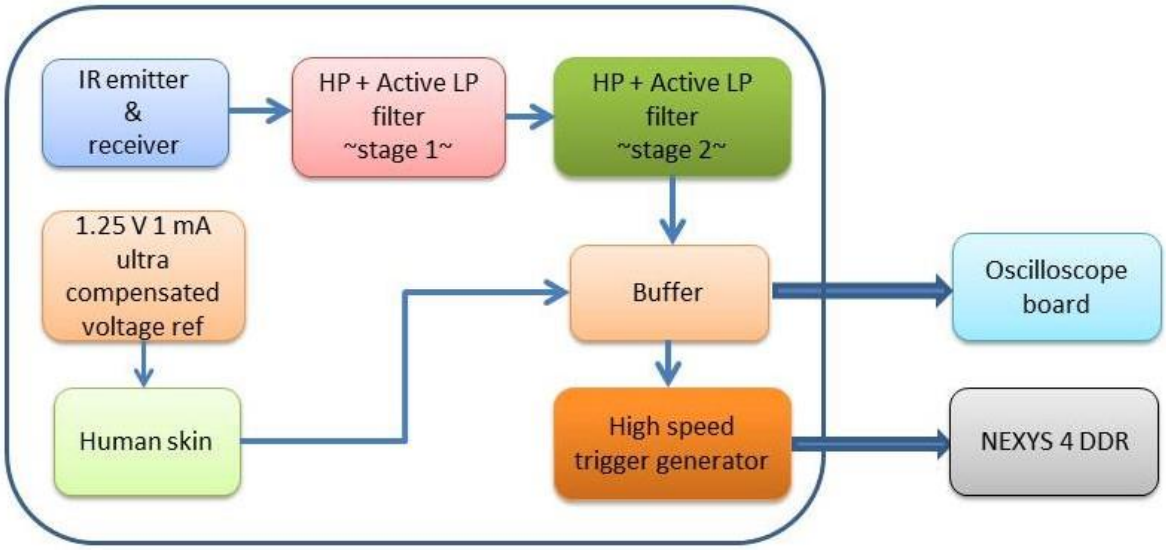


Fig.23 Block diagram which illustrates the medical measurement board

This board is used to measure some data from the human body like:

- Heart rate;
- Galvanic skin response.

For heart rate measurement, a non invasive method was proposed, based on IR emitter& receiver sensor. This sensor injects IR light in to the human tissue and reads the reflection of this light. TCRT1000 was chose as sensor for this purpose, and it has embedded both parts of the sensor.

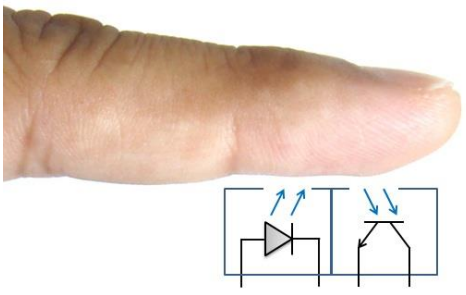


Fig.24 Base principle of heart rate measurement

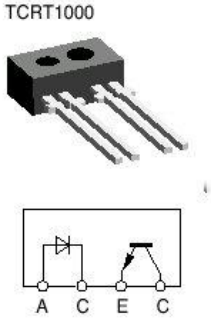


Fig.25 TCRT1000 sensor

TCRT1000 was embedded in a custom socket for finger and it is wired to the board via an 40cm high quality coaxial cable.

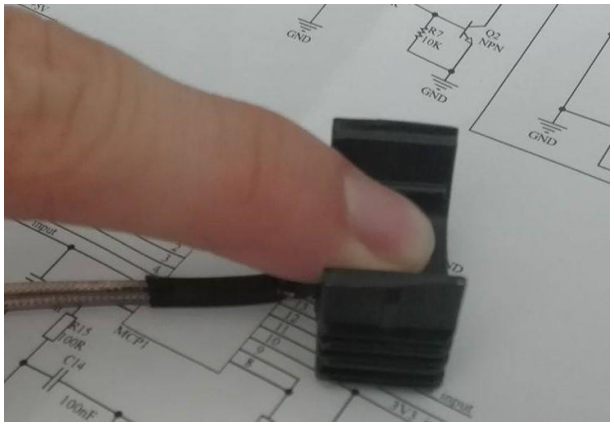


Fig.26 TCRT1000 embedded in a custom socket

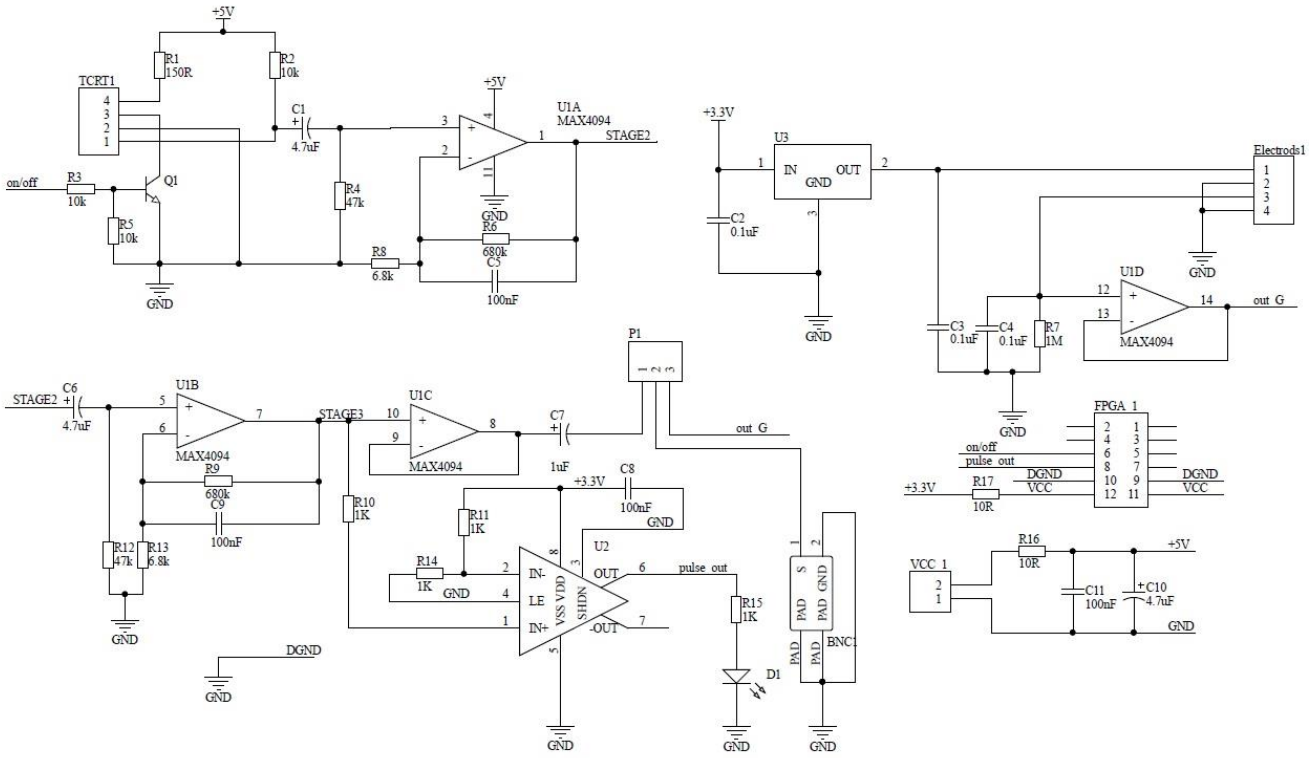


Fig.27 Electrical schematic of the medical measurement board

The output signal from the TCRT1000 is a periodical physiological waveform, attributed to small variations in the reflected IR light, which is caused by the pulsatile tissue blood volume inside the finger. The waveform is, therefore, synchronous with the heart beat. In the first stage is passed through an HPF (High Pass Filter) and a LPF (Low Pass Filter) with an op-amp in order to suppress the large DC component and boost the weak AC pulsatile component, which carries the golden information. The output of the first stage is passed to a similar stage in order to rise the magnitude of the signal to a value that can be used. After this 2 stage is goes in a buffer stage in order to assure an

impedance matching with the oscilloscope board via BNC connector. Also the same signal from stage 2 is injected in an ultra high speed comparator, MAX961, in order to generate synchronous triggers with the heart rate. The triggers are sent to the FPGA pin in order to be counted.

For the galvanic skin response an ultra compensated voltage reference, MAX6061, of 1.25V and 1mA was used in order to inject a constant voltage in to skin voltage and measure its response in volts. The voltage response from skin is buffered through op amp based buffer and with a jumper is set to be the signal source for the BNC connector in order to be measured with the oscilloscope. The waveform is sent after from FPGA to LabVIEW GUI in order to be processed. For the human contact 2 custom electrodes were made and wire via 1m high quality coaxial cable to the board.

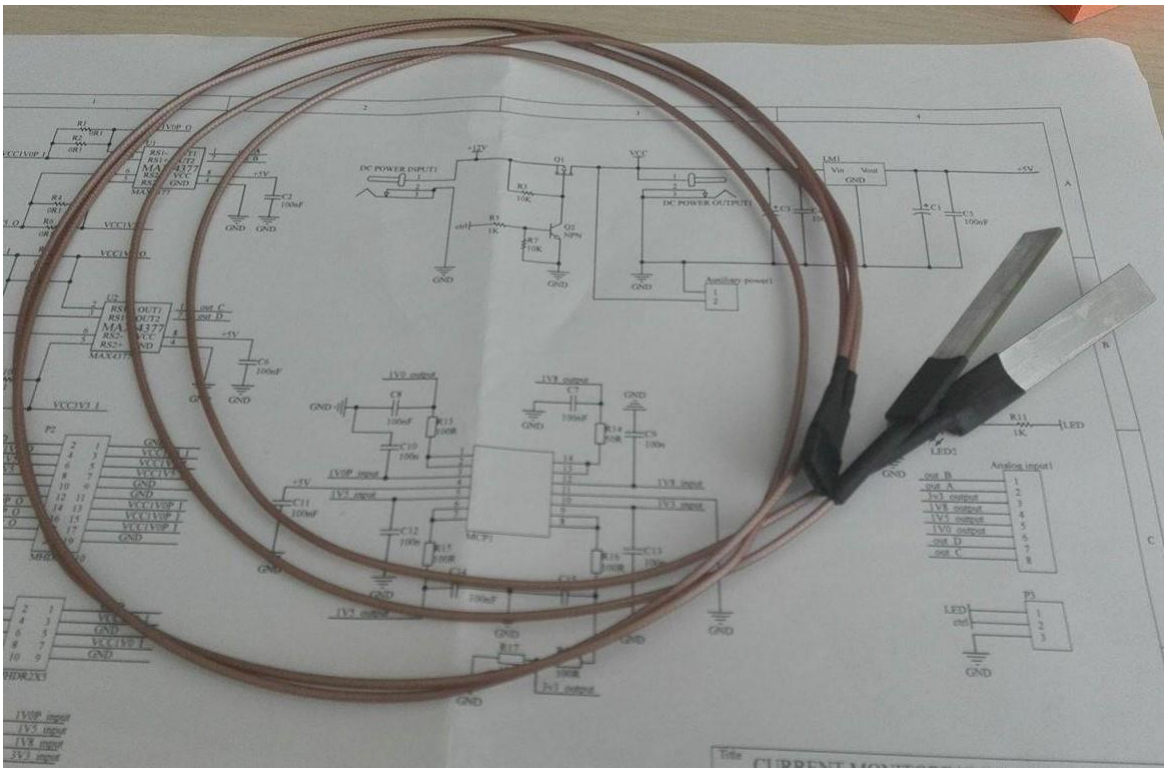


Fig.28 The custom electrodes used to measure the galvanic skin response

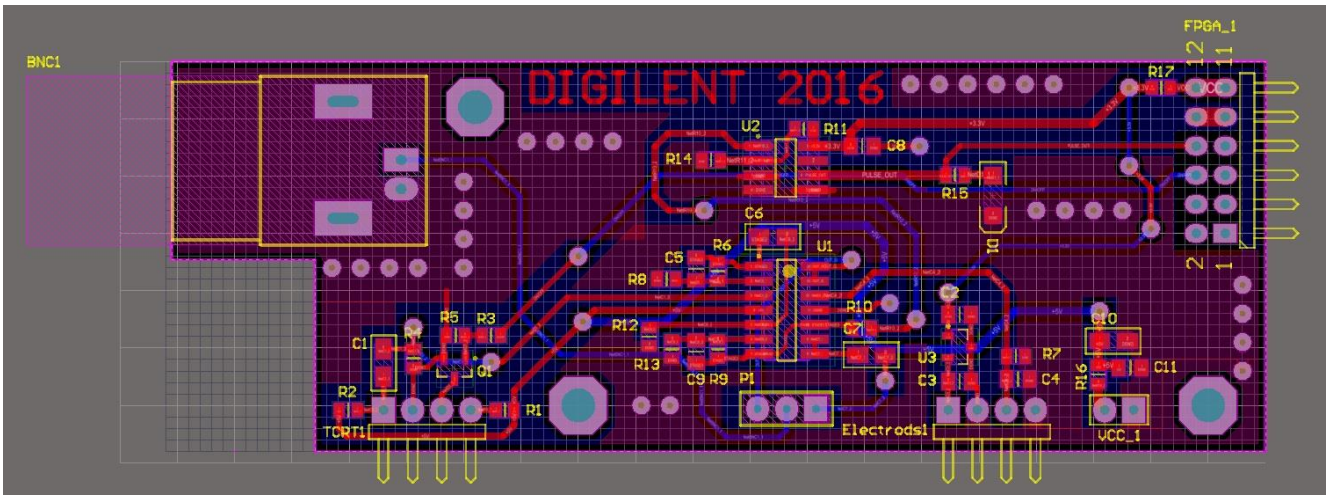


Fig.29 PCB Design of the medical measurement board

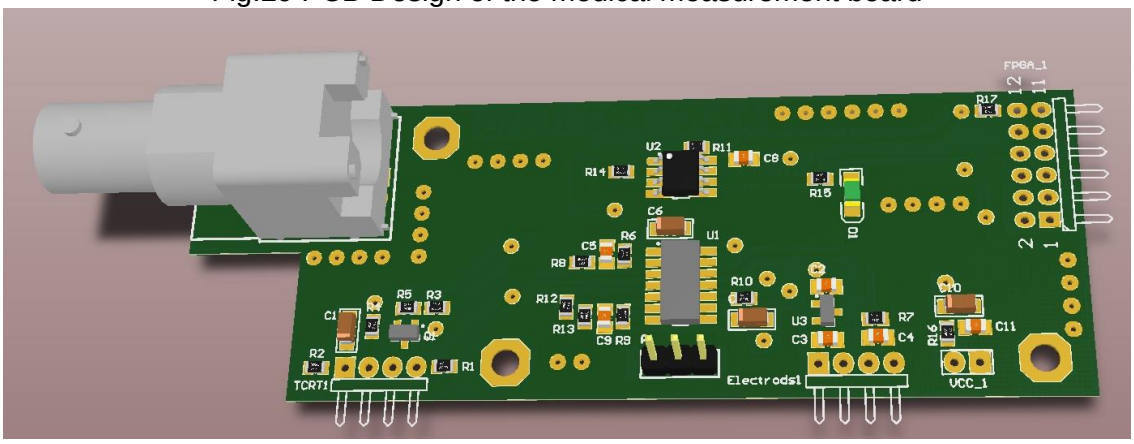


Fig.29 3D Design of the medical measurement board

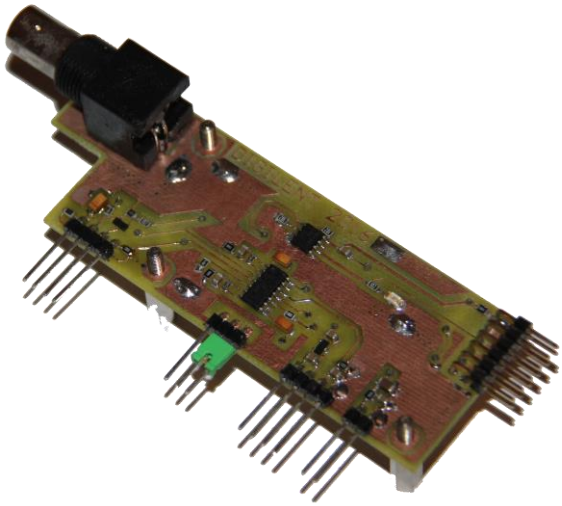


Fig.30 The board fully assembled and ready for tests

Detailed Design Description for the configuration file of the FPGA

The TOP level block diagram

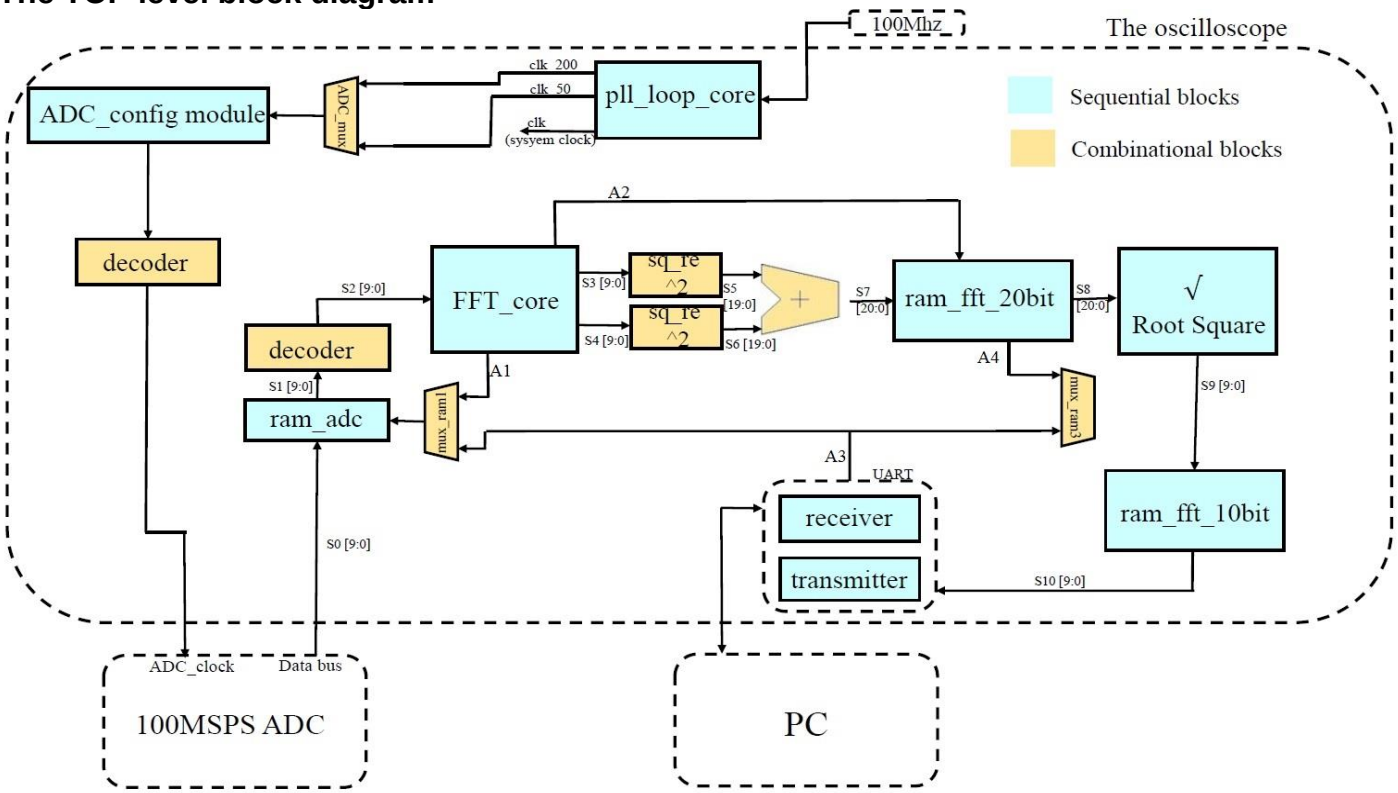


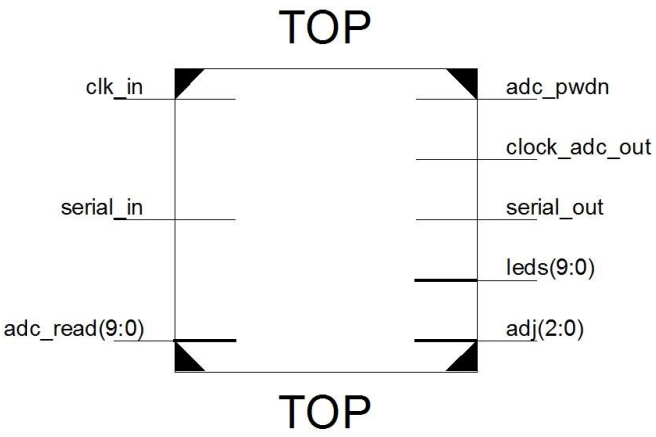
Fig.31 The block diagram of top module

Name	Description
S0	Data bus of the ADC
S1	Output bus of the RAM which keeps the signal's samples. It outputs data for a binary offset to two's complement decoder
S2	Input bus for the FFT Core
S3	Real part of FFT Core's output
S4	Imaginary part of FFT Core's output
S5	First input of the adder
S6	Second input of the adder
S7	The partial result for the absolute value of the FFT core's output. It still Needs to go through rot square module
S8	Input in the root square module
S9	The final result of the FFT
S10	The input of the UART module.

The HDL Modules

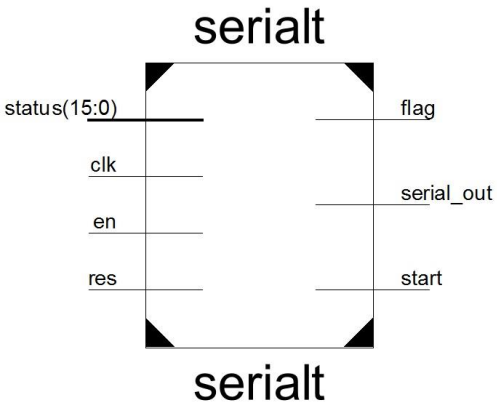
The TOP Module:

The TOP module includes all of the modules, and it has the I/O ports directly linked to the board. Apart from the modules instantiations, the entire logic is implemented in this module as a double state machine. A second state machine was required, because the system uses two important clock signals: the system clock and the other one for ADC. Some processes are driven by the system clock, but others are synchronized only with the one of converter. In its structure, this module encapsulates seventeen modules on the first level.

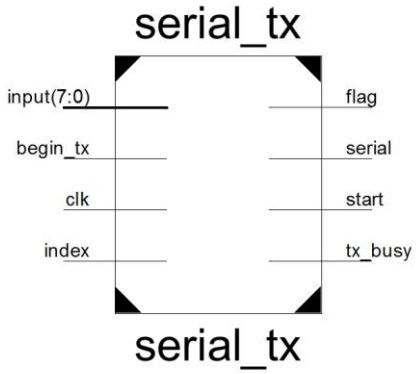


Name	Width	Pin type	Function
clk_in	1	Input	The 100 MHz clock of the NEXYS 4 board
serial_in	1	Input	UART receive pin
adc_read	10	Input	Connects the ADC's data bus with the system
adc_pwdn	1	Output	The power down pin of the ADC (active HIGH)
clk_adc_out	1	Output	The ADC's clock input
leds	10	Output	Led bar for debugging
adj	3	Output	The adjustments register. Commands the amplification/attenuation of the analogic circuit
serial_out	1	Output	The UART's transmitter

The Serial Transmitter module: serial



Name	Width	Pin type	Function
status	16	Input	Input buffer. Data for sending is loaded here
clk	1	Input	Input clock. By division is obtained the baud rate
en	1	Input	Enable bit. Active HIGH
res	1	Input	Reset the index*
flag	1	Output	Debugging pin
serial_out	1	Output	The out of the UART
start	1	Output	Signals whenever a sample was sent.



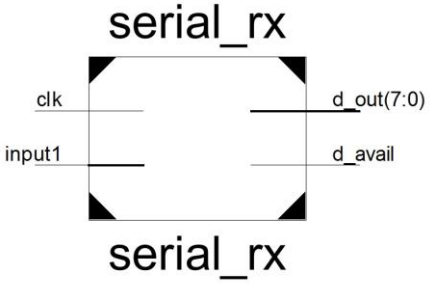
*this is a 16 bit module, but any UART module works on 8bit. In its structure, this module has another 8bit UART module, which splits the 16 bit value in two bytes. It keeps the evidence of these using an index.

Name	Width	Pin type	Function

input	8	Input	Input buffer
clk	1	Input	Input clock. By division is obtained the baudrate
begin_tx	1	Input	Flag for validation
index	1	Input	Keeps the number of the byte(can be 0 or 1)
flag	1	Output	Debugging pin
serial	1	Output	Data output pin
start	1	Output	Signals whenever a sample was sent.
tx_busy	1	Output	Signals if transmission is in progress

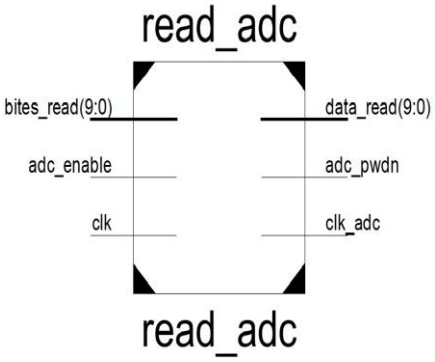
The receiver module: serial_rx

Name	Width	Pin type	Function
clk	1	Input	Clock input Baudrate=clk/16/M*
input1	1	Input	Input clock
d_out	8	Input	Controls the power down pin
d_avail	1	Output	//Unused. Present for future developments



*M is an adjustable constant

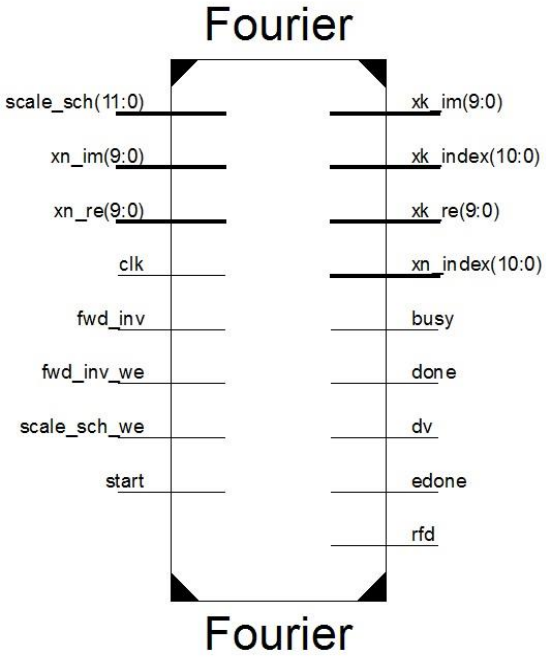
The ADC module: read_adc



Name	Width	Pin type	Function
bites_read	10	Input	Linked to the ADC data bus(but doesn't store anything
clk	1	Input	Input clock
adc_enable	1	Input	Controls the power down pin
data_read	10	Output	//Unused. Present for future developments
adc_pwdn	1	Output	Power down pin
clk_adc	1	Output	Outputs the clock signal for ADC

The FFT Module: Fourier

The Fast Fourier Transform module uses a pipelined processing, and it is applied for the entire frame of the signal(Length 2048 samples). The data representation type is a fixed point one, and a scaling mechanism was chosen, because we wanted to reduce the width of the output data (to optimize the communication). In order to calculate the FFT, the module loads the samples from a RAM, by addressing it with its index, and, in final, it loads the results in another RAM. The module works with a clock of 100 MHz.
The latency of this block is 62.510us and it requires resources as it follows:

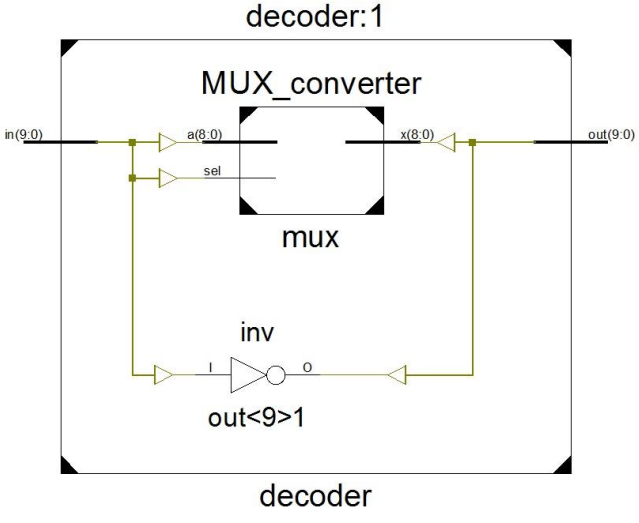


Transform size	Output data width	Xtreme DSP Slices	18K Block RAMs
2048	10	20	12

Name	Width	Pin type	Function
scale_sch	12	Input	Scales the result to need less bits
xn_im	10	Input	Input real part
xn_re	10	Input	Input imaginary part. Set to 0 as we work with real values
clk	1	Input	Clock of the module
Fwd_inv	1	Input	Set the transform type: forward/inverse
fwd_inv_we	1	Input	Write enable for the previous pin
scale_sch_we	1	Input	Write enable for scaling input
start	1	Input	Triggers the start of the transform
xk_im	10	Output	Imaginary part of the output
xk_index	11	Output	Index for the output
xk_re	10	Output	Real part of the output
xn_index	11	Output	Index for the input
busy	1	Output	Flag that signals: computing in progress
done	1	Output	Signals when the transform is done
dv	1	Output	Data valid
edone	1	Output	Signals that computing is done with one clock before this
rfd	1	Output	Ready for data

The decoder module: decoder

As the FFT module works with numbers in two's complement representation, and the ADC outputs data in binary offset, an intermediary conversion is necessary. That is the purpose of this module. Binary offset means that, if the MSB equals 1, the number is positive, otherwise it is negative. So, if the MSB on the input is 1, the output negates it, and lets the other bits as they are. If the MSB



equals 0, the input is a negative value, so the other bits are complemented and the result is incremented by one.

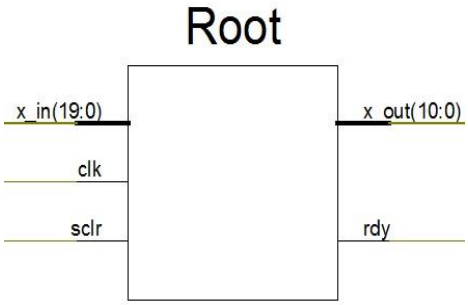
A comparison between the two data representation types is highlighted below:

Digital Output Offset Binary (D9••••••D0)	Digital Output Twos Complement (D9••••••D0)
11 1111 1111	01 1111 1111
10 0000 0000	00 0000 0000
01 1111 1111	11 1111 1111
00 0000 0000	10 0000 0000

Name	Width	Pin type	Function
bites_read	10	Input	Linked to the ADC data bus(but doesn't store anything
clk	1	Input	Input clock
adc_enable	1	Input	Controls the power down pin
data_read	10	Output	//Unused. Present for future developments
adc_pwdn	1	Output	Power down pin
clk_adc	1	Output	Outputs the clock signal for ADC

The square root module: Root

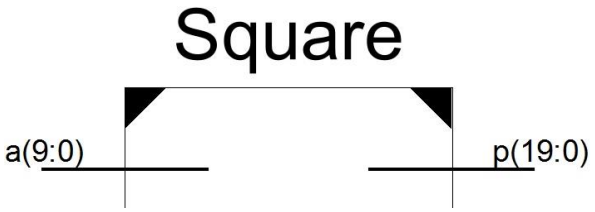
Name	Width	Pin type	Function
x_in	20	Input	Input
clk	1	Input	Clock
sclr	1	Input	Reset
x_out	11	Output	Output
rdy	1	Output	Data ready at output



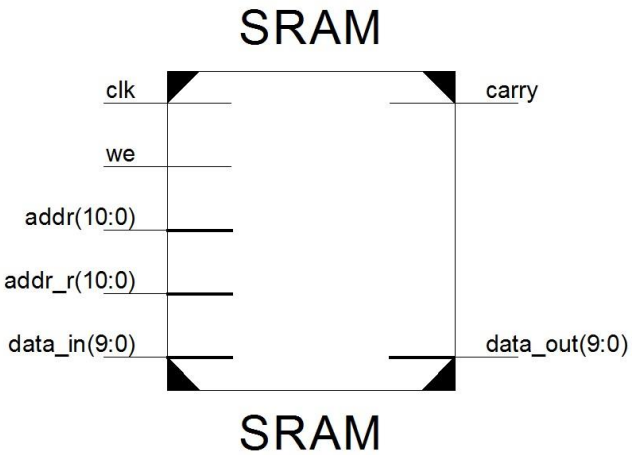
Operation: x_out=sqrt(x_in)

The square module: Square

Name	Width	Pin type
a	10	Input
b	10	Input
p	20	output

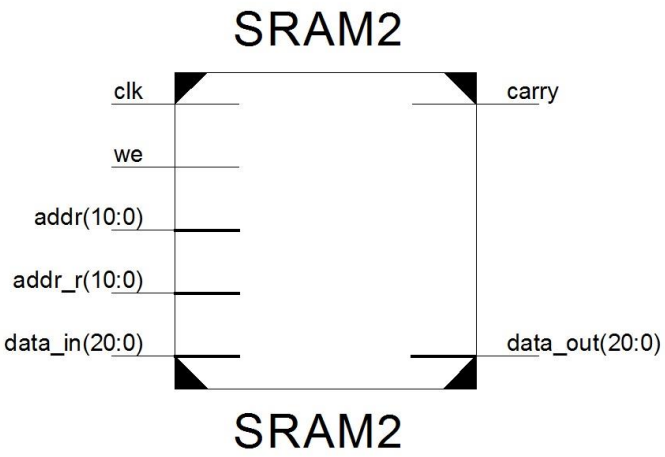


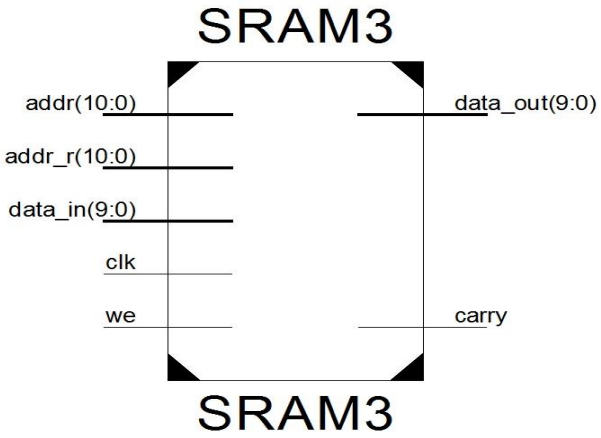
It computes the mathematical expression p=a*b



The SRAM modules:

Name	Width	Pin type	Function
clk	1	Input	Memory clock
we	1	Input	Write Enable pin
addr	11	Input	The write address
addr_r	11	Input	The read address
data_in	10	Input	Input bus: from ADC
carry	1	Output	Goes HIGH whenever the address is at maximum
data_out	10	Output	Output bus, and the input source for FFT

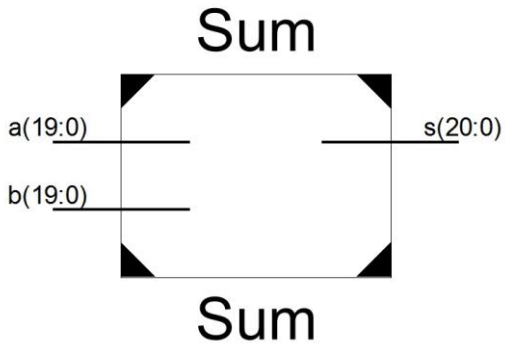




The adder module: Sum

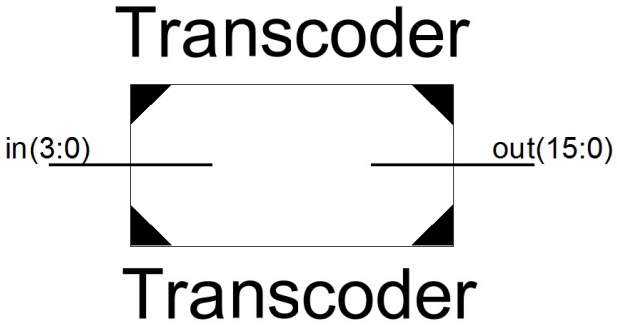
Name	Width	Pin type
a	20	Input
b	20	Input
s	21	Output

Computes the following operation:
s=a+b;



The transcoder module

Name	Width	Pin type
in	4	Input



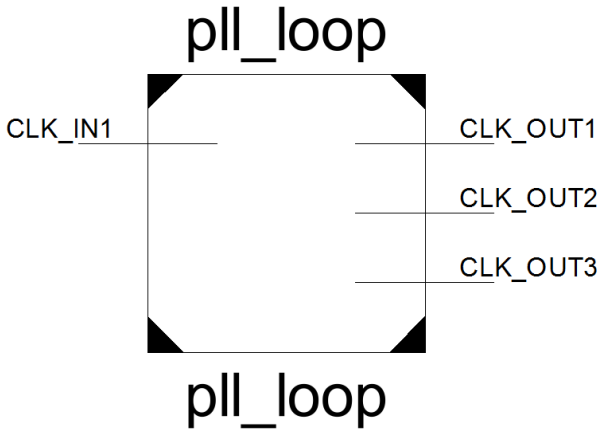
out	16	Output

For the time base adjustment, it is required a 16 bit value, to obtain a very low frequency signal, divided from 25 MHz. As the computer transmits this value, it is easier to send a 4bit number instead a 16bit one. This module assigns a 16 bit number, for a 4bit input.

Out = 2^in + 1;

The PLL module: PLL loop

Name	Width	Pin type
CLK_IN1	1	Input
CLK_OUT1	1	Output
CLK_OUT2	1	Output
CLK_OUT3	1	Output



This module has an input of 100 MHz, and outputs three other signals with the frequency of: 50MHz, 100MHz, 200MHz;

The algorithm

The entire system is commanded by three state machines. Two of those three are controlled by a clock signal (not the same clock), and the last one is controlled by a certain bit.

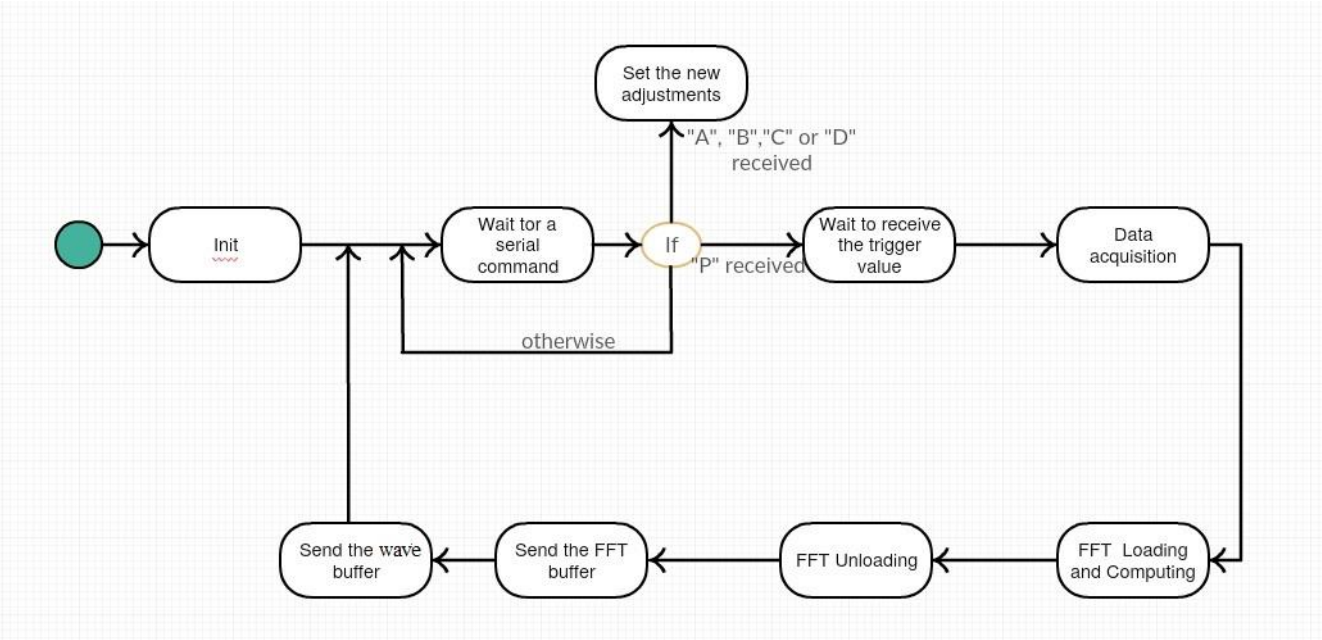


Fig.32 State machine: FSM_1

The steps:

- Wait_state: Waits for a serial command. If the command is A, B, C or D, it sets the adjustments, and stays in the same state. So, if one of those four letters is received, it allocates the next serial value for a specific adjustment.

The current byte	A	B	C	D
The next byte will command:	Time base	Trigger level	Slope	Amplification/ Attenuation

- ***Wait_state***: If the serial command is P, it goes on in the acquisition state
- ***Trig_state***:In this state, the FSM waits for the signal to equal the trigger level value, and also to has the corresponding slope. The slope is evaluated by the second FSM, which runs in parallel with this. When trigger condition is met, the automaton goes in the next state
- ***Acq_state***: In this state, a buffer of 2048 samples provided by ADC is stored into ram_adc(the first SRAM). In this state, this FSM only check if the memory is full. The addressing is done by the second FSM, which is triggered by the ADC clock.
- ***Fft_state***: When the samples buffer is full, the system comes in this state, where he FF algorithm is started. Using the index address bus, the ram_adc memory is completely read by the FFT core. After this, the processing starts, until edone signals that the transform is done.
- ***Fft_write_state***: Now, data is unloaded from FFT block into ram_fft_20bit (the second SRAM); on every clock, a sample is unloaded. Between the two modules, there were introduced two square modules and an adder, so as to, if the FFT outputs a real part and an imaginary one, at the ram input it will be real^2+imag^2. These modules are combinational circuits, so they present a 0 latency.
- ***Square_state***: In this state, a square root operation is applied for every sample from ram_fft_20bit, and stored in the third ram(ram_fft_10bit). The square root value is not a zero latency one, and it lasts a few clock cycles. When sqr_rdy is high, the module outputted the data, and it is stored, and memory location is incremented, to process a new sample. These operations are made during other four similar states(Square_state2, Square_state3, Square_state4, Square_state5)
- As soon as the data has been processed, and a correct samples set for the spectral analyses was stored in the last ram(ram_fft_10bit), the send state can begin

- In this state, the array with FFT is sent at first, then three control characters (‘F’, ‘F’, ‘T’). After those, the waveform buffer (from ram_adc) is also sent. The data sending process is controlled by a third state machine.
- In final, the system goes in the first state

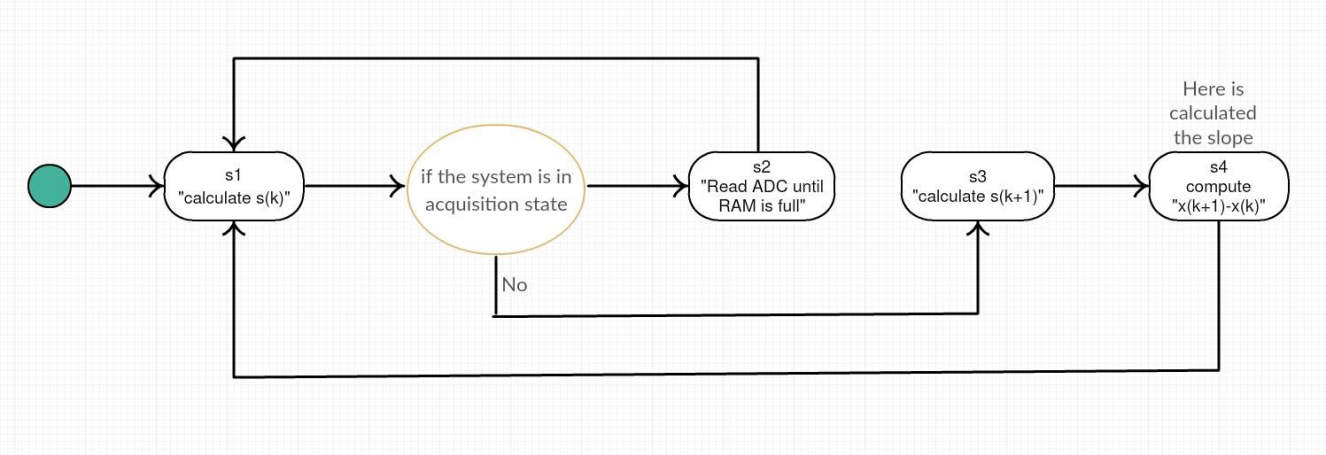


Fig.33 State machine: FSM_2

This FSM is controlled by the ADC’s clock. The second state machine controls the ram_adc filling with samples from ADC. It checks if the main state machine is in the acquisition state (acq_state), and in this case it starts to fill the ram. Otherwise, is calculate the value for two consecutive samples (in s1 and s3), and its compute its difference to evaluate the slope(in s4).

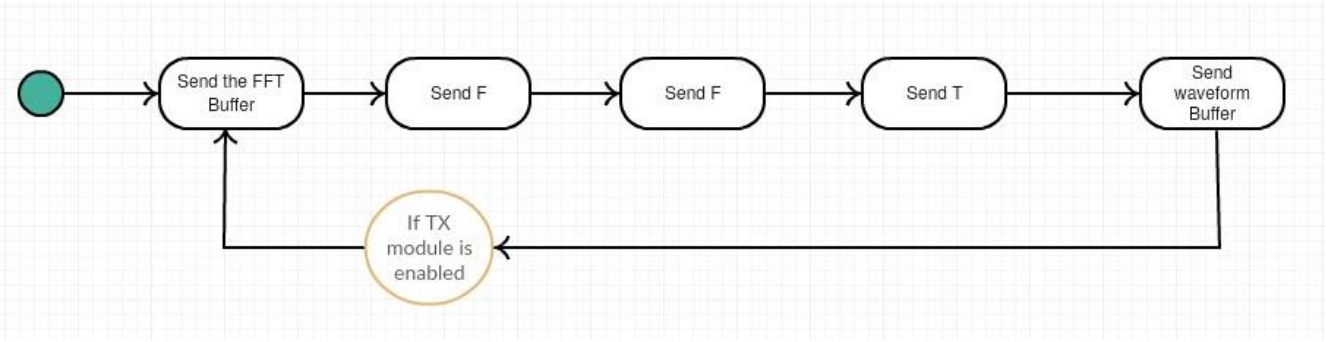


Fig.34 State machine: FSM_3

The third state machine controls the data transmission process. The state value is checked every time a sample has been sent to PC. The “start: bit of the UART module signals this thing. When the enable bit of UART is deactivated, the global communication stops, consequently the FSM 3 stops (because start bit won’t change its value anymore).

Detailed Design Description for the GUI

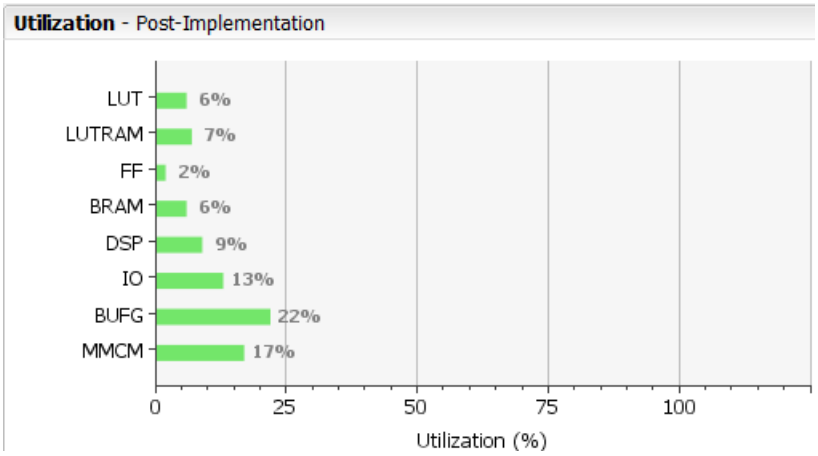
LabVIEW stand for Laboratory Virtual Instrument Engineering WorkBench, is a system-design platform and development environment for a visual programming language from National Instruments.

We chose to develop a GUI in LabVIEW because is more powerful and reliable and it is used by a large scale of customers.

Our virtual instruments instantiates a RS232 communication with NEXYS 4 DDR with the following parameters:

- 1562500 Baud rate;
- 8 bits;
- No parity;
- 1 stop bit;

- Timeout configurable from 0.3ms to 10s;
- No termination char.



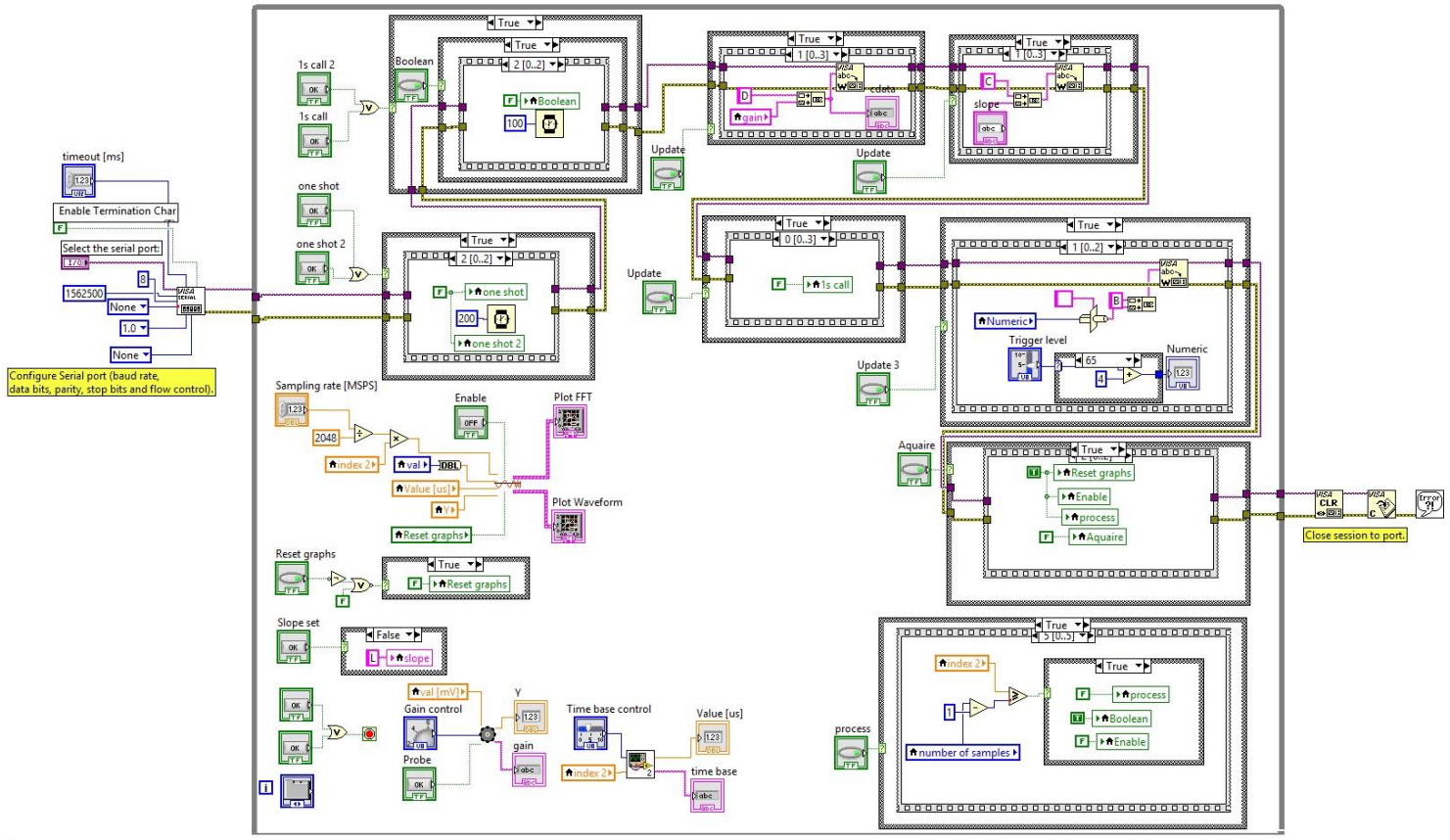


Fig.35 LabVIEW Graphical User Interface block diagram

A single while loop is running this **VI**. Outside of the loop, in the left side, the serial port is instantiated and configured via **VISA Configure** block; in the right the port is cleared and closed using **VISA CLEAR** and **VISA CLOSE** blocks; when the VI is stopped, this operation leaves the serial port in a known state.

In order to start the acquisition, an ASCII character "**P**" is sent to FPGA using **VISA WRITE** block and after transmission, the received state is instantly activated and waits to read 8197 bytes using **VISA READ** block. This 8197 bytes contains 2048 samples, each of them being consisted of 2 data bytes for the standard waveform data, 6 control bytes with ASCII characters "**FFT**" and another 2048 samples of 2 bytes for FFT data.

After the separation phase done with **Search/Split String** block, all the data is decoded and displayed using **XY Graph block**.

For better redundancy and clearness of the code, 3 sub-vis were created. All sub-vis perform operation like time base and vertical scale calculation.

Settings like: **slope controls**, **gain calculation**, **trigger level settings** and **time base control** are performed are sent to FPGA using char characters and HEX values.

Discussion

Problems Encountered

On our way to the finals we have encountered some problems, most of them with the hardware part, and also with the configuration file of the FPGA. One of the first problems was the noise in the analogic board, which was solved by designing a dual layer PCB which isolated the analogic ground and digital ground, by joining them in one point. Also the power supply played a role in this problem. At the first phase we had some problems with the signals synchronization, but we managed to solve all of those problems recently.

Engineering Resources Used

We have worked a lot in order to succeed in finishing this project, and we have dedicated a lot of time, and also have benefited from the help and experience of our advisor, which helped us to solve some issues in LabVIEW GUI. The number of hours dedicated for this project is enormous and we are glad that in the final we have managed to get all the stuff working.

Marketability

As we are in the Internet of things era, the number of people eager to work with electronics is increasing. At this moment, everybody encounter with the need of having a debugging tool, especially an oscilloscope. Because a professional one is very expensive, they will focus on the idea of buying a portable one, because in a wide range of applications a very high performance will not be necessary. That is the strong part of our project. If you already have a FPGA board, all that you need is to get the plugin module, and you have your own 100 MSPS digital oscilloscope.

Community Feedback

The project was presented to some keen students and also to teachers, and after this, they have expressed very favorable opinions regarding this idea. As the students don't need very expensive tools, some teachers were interested to manufacture some samples in order to introduce them in the laboratory classes, in order to study how well the students will get accustomed with the system.

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