1 Digital Interface

| Pin	Direction	Function
SCK	in	SCK for SPI communication/SCK for PLL communication
MOSI	in	MOSI for SPI communication/MOSI for PLL communication
MISO	out	MISO for SPI communication/MUX for PLL communication
NSS	in	Chip Select for SPI communication/LE for PLL communication
INTR	out	Active high interrupt indicator
RESET	in	FPGA reset
AUX1	in	Selector for direct communication with Source PLL
AUX2	in	Selector for direct communication with LO PLL
AUX3	in	Active low sweep enable. Has to be high when changing settings

Depending on the voltage on AUX1/AUX2 the SPI port controls either the FPGA or one of the MAX2871 PLLs:

AUX1	AUX2	Function
low	low	SPI communication with FPGA
high	low	Direct feedthrough of SCK, MOSI, MISO and NSS to Source PLL
low	high	Direct feedthrough of SCK, MOSI, MISO and NSS to LO PLL
high	high	Invalid

When communicating with a PLL, the MUX output of the MAX2871 is forwarded to MISO and the NSS signal is forwarded to the LE pin. As the LE pin should stay low until after a valid register has been shifted in (see MAX2871 datasheet), set NSS low before switching to PLL communication mode.
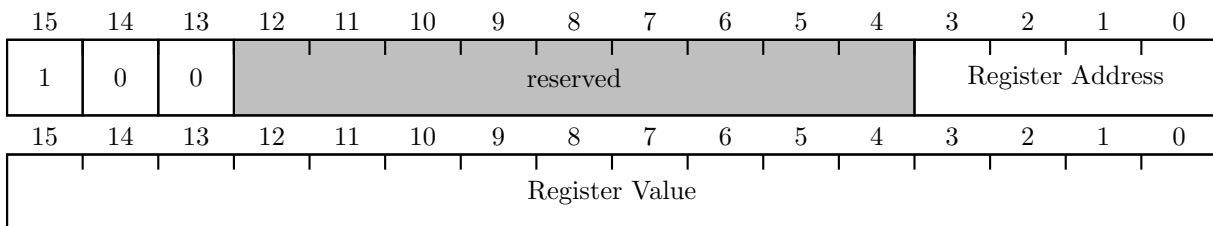
2 SPI Protocol

Each SPI transfer starts with pulling NSS low and ends with NSS returning to high level. SPI communication is done in words of 16 bits. The first word after NSS is pulled low is the command word and determines the amount and meaning of the following words. The word received while transmitting the command word is the interrupt status register:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					reserved						SH	OR	ND	SU	LU
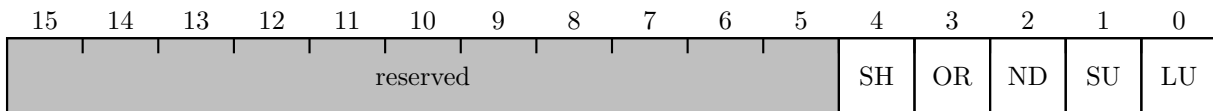
- **SH:** Sweep halted due to halt bit set. Sweep will be resumed once the resume command is issued.

- **OR:** Data overrun occured (only cleared by resetting the FPGA)

- **ND:** New data available

- **SU:** Source unlocked

- **LU:** LO unlocked

2.1 Writing a register

Writing a register requires the transfer of two words: First the control word selecting the destination address and a second word containing the new register value:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	0	0				reserved							Register Address		

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						Register Value									

2.2   Writing SweepConfig

Initiate the sweep config transfer by sending the command word:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	0						Sweep point							
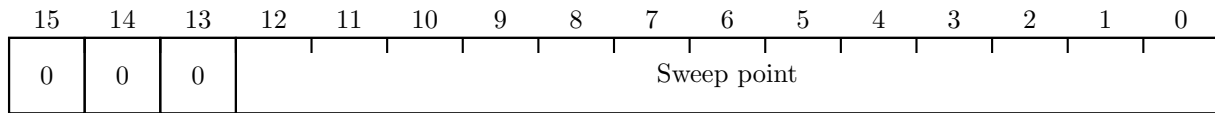
The maximum number of points per sweep is 4501, thus the highest valid value for "Sweep point" is 4500. After the control word, send the six words of the sweep config (see section 4) while keeping NSS low. The sweep config is transmitted MSB first.

2.3   Reading a sampling result

Whenever the ND bit in the interrupt status register is set, new sampling data is available and can be read via SPI. It has to be read before the next sampling data arrives otherwise the old data will be overwritten.

Initiate the reading of sampling data by sending the command word:

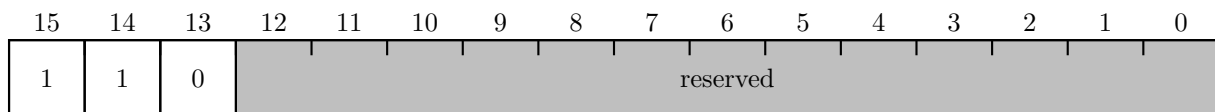| 15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	0						reserved							

Afterwards, read 18 words before setting NSS high. These 18 words will contain the sampling result (see section 5), transmitted with the least significant word first.

2.4   Resuming a halted sweep

When the halt bit is set in the SweepConfig, the FPGA will configure the Source and LO as requested but will not start the settling timer (and subsequently the sampling process) until this resume command is issued. The halted sweep is indicated by the sweep halted bit in the status register.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	0	1						reserved							
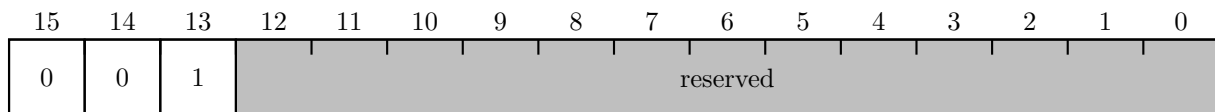
2.5   Reading ADC limits

The FPGA keeps track of the highest and lowest sample of each ADC to detect saturation and verify signal levels.

Initiate the reading of ADC limit data by sending the command word:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
1	1	1						reserved							
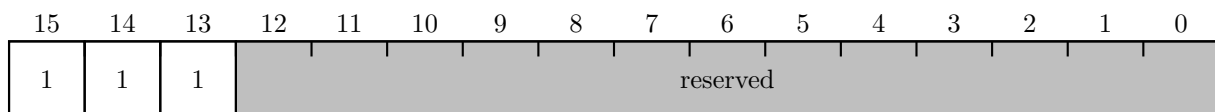
Afterwards, read 6 words before setting NSS high. These 6 words will contain the sampling result:

95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
							Port 1 minimum								

79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
							Port 1 maximum								

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
							Port 2 minimum								

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
							Port 2 maximum								

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
							Reference minimum								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							Reference maximum								
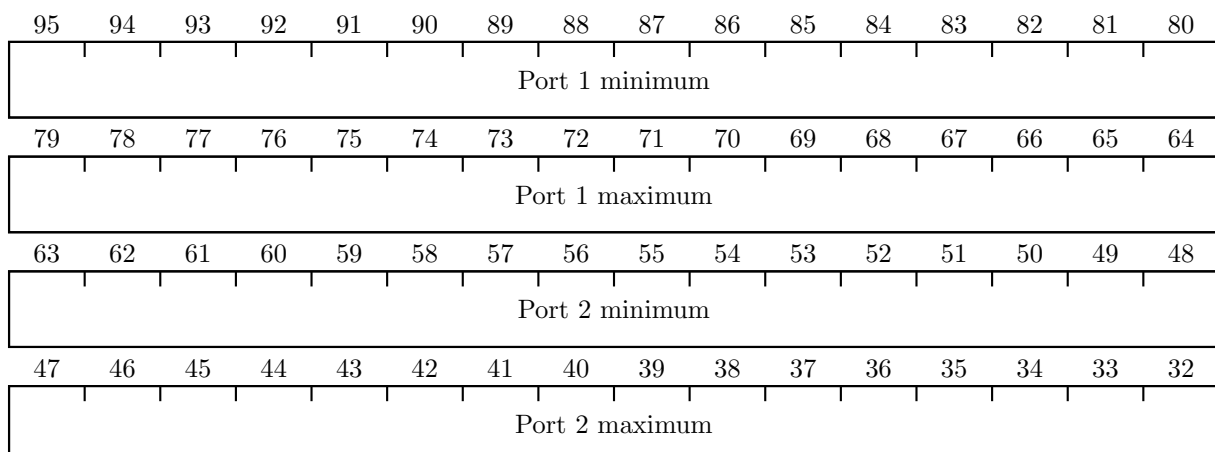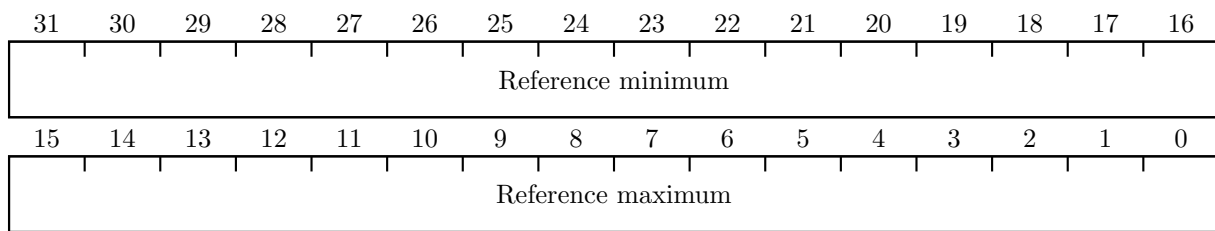
2.6 Resetting the ADC limit

Issuing this command result in all minimum values set to 32767 and all maximum values set to -32768.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0	1	1						reserved							
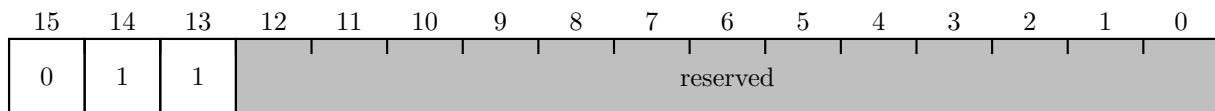
3 Registers

3.1 Interrupt Mask Register: 0x00

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
					reserved						SHIE	ORIE	NDIE	SUIE	LUIE
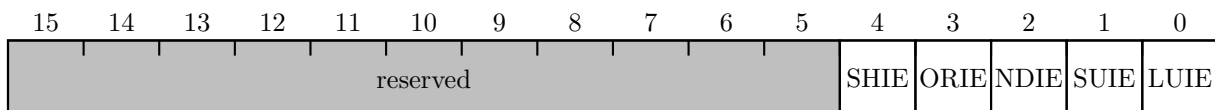
- **SHIE:** Sweep halted interrupt enable

- **ORIE:** Data overrun interrupt enable

- **NDIE:** New data interrupt enable

- **SUIE:** Source unlocked interrupt enable

- **LUIE:** LO unlocked interrupt enable

3.2 Sweep Points Register: 0x01

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
						Number of points per sweep - 1									
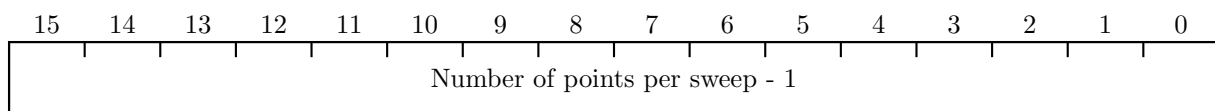
The register contains the number of points per sweep negative one, e.g. set to 11b if the sweep contains four points.

3.3 Samples Per Point Register: 0x02

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
		reserved				SPP[9:0]									
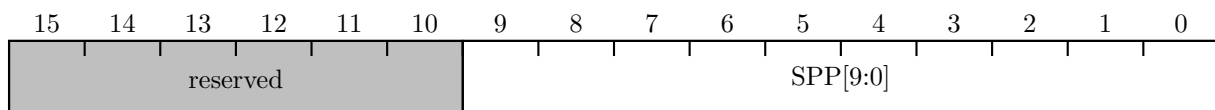
- **SPP[9:0]:** The register contains the number of samples per point in increments of 128 samples (e.g. SPP=0b0000001000=0x08 uses 1024 samples per point). The value of this register is only used if Sweep-Config[92:90] is set to 000. Otherwise it is overwritten for the sweep point with one of seven preselected values.

3.4 System Control Register: 0x03

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
P1EN	P2EN	REN	AMEN	SOEN	LOEN	RLED	LED6	LED7	Window[1:0]		SCEN	LCEN	EXP2	EXP1	PSEN
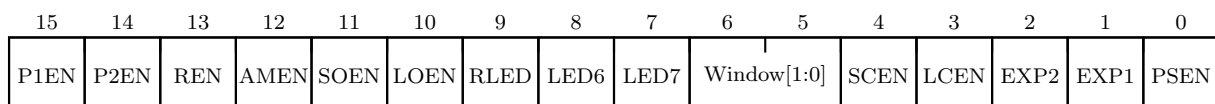
- **P1EN:** Port 1 Mixers/Amplifier enable

- **P2EN:** Port 2 Mixers/Amplifier enable

- **REN:** Reference Mixers/Amplifier enable

- **AMEN:** Source amplifier enable

- **SOEN:** Source enable

- **LOEN:** LO enable

- **RLED:** External frequency LED control

- **LED6:** User LED 6 control

- **LED7:** User LED 7 control

- **Window[1:0]:** Type of window to be used in calculation of real/imag of the sampling result

Setting	Window type
00	Rectangular (no window)
01	Kaiser
10	Hann
11	Flat Top

- **SCEN:** Source chip enable

- **LCEN:** LO chip enable

- **EXP1:** Excite Port1 during sweep

- **EXP2:** Excite Port2 during sweep

- **PSEN:** Port switch enable

3.5   ADC Prescaler register: 0x04

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			reserved								Presc[7:0]				
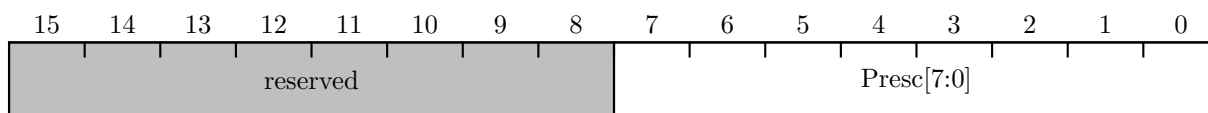
- **Presc[7:0]:** Amount of FPGA clock cycles between ADC samples.

$$SR_{ADC} = \frac{102.4\,\text{MHz}}{Presc}$$

The minimum value for this register is 111, which results in a samplerate of roughly 922.5 kHz. If Presc is set to a lower value, the data acquisition from the ADC is not done when the next sample starts and samples will be skipped.

3.6   Phase Increment: 0x05

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	reserved							Phase Increment[11:0]							
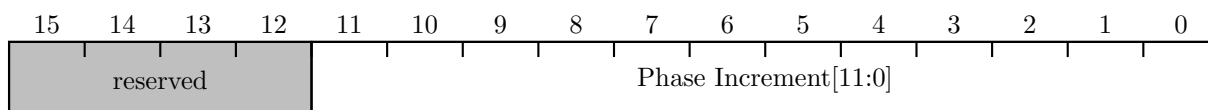
- **Phase Increment[7:0]:** Phase angle between ADC samples for DFT bin calculation in $\frac{2\pi}{4096}$ rad. For a given ADC samplerate SR_{ADC} and final IF frequency f_{IF2} set this value to

$$PhaseInc = \frac{4096 * f_{IF2}}{SR_{ADC}}$$

For the the default IF frequency of $f_{IF2} = 250\,\text{kHz}$ this evaluates to 10*Presc (see ADC prescaler register).

3.7 MAX2871 Default Values Registers: 0x08-0x0F

See datasheet of MAX2871 for bit descriptions. Bits for the fields N, FRAC, M, VCO and DIV_A are "don't care" as they will be overwritten by the SweepConfig setting.

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX2871 Register 0[15:0]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX2871 Register 0[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX2871 Register 1[15:0]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX2871 Register 1[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX2871 Register 3[15:0]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX2871 Register 3[31:16]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX2871 Register 4[15:0]															

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
MAX2871 Register 4[31:16]															

4 SweepConfig

The SweepConfig contains data for the source and LO1 PLL as well as the attenuator and source filter. Each point in the sweep, needs a valid SweepConfig before the sweep is started.

95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
HS	SettlingTime		Samples			SourceFilter		LO M[11:4]							

79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
LO M[3:0]				LO FRAC[11:0]											

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
LO DIV_A[2:0]			LO VCO[5:0]						LO N[6:0]						

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
BS	Attenuator[6:0]							Source M[11:4]							

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
Source M[3:0]				Source FRAC[11:0]											

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Source DIV_A[2:0]			Source VCO[5:0]						Source N[6:0]						

- **HS: Halt sweep.** If set, settling and sampling of this sweep point will be postponed until the sweep resume command is issued.

- **SettlingTime:** Amount of time between locking of PLLs and beginning of ADC sampling

Setting	Time
00	20 μs
01	60 μs
10	180 μs
11	540 μs

- **Samples:** Number of ADC samples to take

Setting	Samples	Equivalent IF bandwidth
000	Defined by SPP register	914 kHz/SPP
001	128	10 kHz
010	384	3 kHz
011	896	1 kHz
100	3072	300 Hz
101	9088	100 Hz
110	30464	30 Hz
111	91392	10 Hz

- **SourceFilter:** Low pass filter selection for source signal

Setting	Selected Band
00	0 MHz to 900 MHz
01	900 MHz to 1800 MHz
10	1800 MHz to 3500 MHz
11	3500 MHz to 6000 MHz

- **BS: Band select.** Set to 0 for highband, set to 1 for lowband.

- **Attenuator:** Attenuation of source signal in 0.25 dB.

5 Sampling Result

Each point in the sweep generates two sampling results. The first one contains the measurement when the source was routed to Port 1, the second sampling result was taken when the source was routed to Port 2. The sampling result does not indicate which point in the sweep it belongs to, that information is implicitly given by the order of transmitted sampling results.

287	286	285	284	283	282	281	280	279	278	277	276	275	274	273	272
							Port 1 I[47:32]								

271	270	269	268	267	266	265	264	263	262	261	260	259	258	257	256
							Port 1 I[31:16]								

255	254	253	252	251	250	249	248	247	246	245	244	243	242	241	240
							Port 1 I[15:0]								

239	238	237	236	235	234	233	232	231	230	229	228	227	226	225	224
							Port 1 Q[47:32]								

223	222	221	220	219	218	217	216	215	214	213	212	211	210	209	208
							Port 1 Q[31:16]								

207	206	205	204	203	202	201	200	199	198	197	196	195	194	193	192
							Port 1 Q[15:0]								

191	190	189	188	187	186	185	184	183	182	181	180	179	178	177	176
							Port 2 I[47:32]								

175	174	173	172	171	170	169	168	167	166	165	164	163	162	161	160
							Port 2 I[31:16]								

159	158	157	156	155	154	153	152	151	150	149	148	147	146	145	144
							Port 2 I[15:0]								

143	142	141	140	139	138	137	136	135	134	133	132	131	130	129	128
							Port 2 Q[47:32]								

127	126	125	124	123	122	121	120	119	118	117	116	115	114	113	112
							Port 2 Q[31:16]								

111	110	109	108	107	106	105	104	103	102	101	100	99	98	97	96
							Port 2 Q[15:0]								

95	94	93	92	91	90	89	88	87	86	85	84	83	82	81	80
							Reference Signal I[47:32]								

79	78	77	76	75	74	73	72	71	70	69	68	67	66	65	64
							Reference Signal I[31:16]								

63	62	61	60	59	58	57	56	55	54	53	52	51	50	49	48
							Reference Signal I[15:0]								

47	46	45	44	43	42	41	40	39	38	37	36	35	34	33	32
							Reference Signal Q[47:32]								

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
							Reference Signal Q[31:16]								

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
							Reference Signal Q[15:0]								