

1. THIS DRAWING SPECIFIES THE REQUIREMENTS FOR A PRINTED WIRING BOARD IN ACCORDANCE WITH SPECIFICATION IPC-A-600 CLASS 2 (LATEST REVISION).
2. THE PWB MUST BE LEAD FREE ASSEMBLY PROCESS COMPATIBLE AND MUST BE ABLE TO HANDLE A MINIMUM OF 5 CYCLES AT 240 DEGREES CELSIUS FOR 10 SECONDS.
3. BASE MATERIAL - LAMINATE AND PREPREG SHALL MEET IPC-4101B-26, B3 or 98
Tg - MUST BE GREATER THAN OR EQUAL TO 150 DEGREES CELSIUS.
Td - MUST BE GREATER THAN OR EQUAL TO 330 DEGREES CELSIUS.
4. COPPER FOIL WEIGHT - SEE STACKUP DETAIL "A"
5. CHARACTERISTIC IMPEDANCE - SEE DETAIL "B"
6. MINIMUM CONDUCTIVE WIDTH/SPACING TO BE .004"/.004"
7. PLATING FINISH: a. BOTH SIDES ENIG (ELECTROLESS NICKEL IMMERSION GOLD):
.050@ ±32 MICRON (.8 MICRONS) OF GOLD OVER
2.540-6.350 MICRON (100-250 MICRONS) OF NICKEL.

8. ALL THROUGH HOLE VIAS MAY BE PLATED SHUT.

9. SOLDERMASK - RED COLOR (TAIYO OR EQUIVALENT)
MODIFICATION OF SOLDERMASK IS NOT ALLOWED

10. SILKSCREEN - WHITE EPOXY INK, BOTH SIDES. NO SILK ON PADS.

11. ELECTRICAL TEST - 100% IPCD356.

12. PRINTED WIRING BOARD IS TO BE INDIVIDUALLY BAGGED.

13. DRC'S MUST BE RUN ON THE GERBER BEFORE BUILDING BOARDS.
UNLESS PRIOR APPROVAL IS GIVEN IN WRITING BY FREESCALE.

14. TEARDROPS MAYBE ADDED AT THE FAB HOUSE TO ALL SIGNAL LAYERS.

15. TWO SOLDER SAMPLES TO BE PROVIDED.

17. SUPPLIER MARKINGS - ON SOLDER SIDE ONLY, WHERE SHOWN.

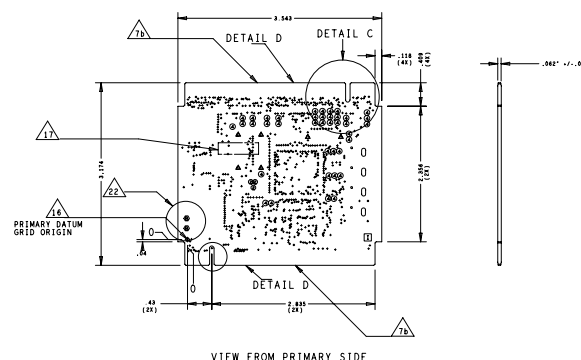
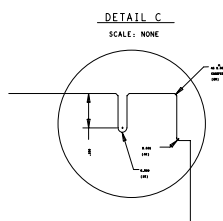
MUST BE UL RECOGNIZED AND MUST HAVE AN ID THAT CONFORMS TO UL94V-0

19. THE PWB WILL BE MARKED AS LEAD FREE PROCESS COMPATIBLE BY USE OF AN INK STAMP (260°C)

20. ALL PLATED AND NON-PLATED THROUGH HOLES ARE TO BE DRILLED AT PRIMARY DRILL STEP.
ALL HOLE LOCATION TOLERANCES ARE TO BE $\pm .002$ IN REFERENCE TO THE PRIMARY DATUM.

21. FINISHED PCB MUST BE PANELIZED FOR ASSEMBLY ACCORDING TO CONTRACT MANUFACTURERS REQUIREMENTS.
THE ADDITION OF RAILS AND .125" NON-PLATED TOOLING HOLES ARE AT THE DISCRETION OF
CONTRACT MANUFACTURER. PANELIZATION MUST BE APPROVED BY CONTRACT MANUFACTURER.









22. ALLOW SHAVING OF COPPER FOR COMPONENTS THAT ARE CLOSE TO THE BOARD EDGES.



DETAIL B
IMPEDANCE REQUIREMENTS
IMPEDANCE TOLERANCE IS 10%

Layers	Single Ended		Differential		
	Trace Width (Mils)	Impedance (Ohms)	Trace Width (Mils)	Trace Spacing (Mils)	Impedance (Ohms)
L1_PS	9.00	50	5.00	4.00	90
L2_INT.1	4.50	50			
L4_INT.2	4.50	50			
L5_INT.3	6.50	50			
L7_INT.4	4.50	50	5.00	7.00	90
L8_SS	9.00	50	5.00	4.00	90

DRILL CHART: TOP to BOTTOM				
ALL UNITS ARE IN MILS				
FIGURE	SIZE	TOLERANCE	PLATED	QTY
•	8.0	+0.0/-0.8	PLATED	816
•	12.0	+0.0/-12.0	PLATED	4
•	28.0	+3.0/-3.0	PLATED	3
⊙	40.0	+3.0/-3.0	PLATED	39
•	25.0	+2.0/-2.0	NON-PLATED	1
•	36.0	+2.0/-2.0	NON-PLATED	2
▲	53.0	+3.0/-0.0	NON-PLATED	6
□	125.0	+3.0/-3.0	NON-PLATED	1
0	140.0x70.0	+2.0/-2.0	NON-PLATED	4

	LAYER 1 TOP	1/2 to 1 oz.
	LAYER 2 L2_INT_1	1/2 oz.
	LAYER 3 L3_GND	1 oz.
	LAYER 4 L4_INT_2	1/2 oz.
	LAYER 5 L5_INT_3	1/2 oz.
	LAYER 6 L6_PWR	1 oz.
	LAYER 7 L7_INT_4	1/2 oz.
	LAYER 8 BOTTOM	1/2 to 1 oz.

DETAIL A
LAYER STACKUP
SCALE: NONE

PART NO. 170-27167		FREESCALE SEMICONDUCTOR	
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TITLE PRINTED WIRING BOARD		TWR-K60F120M	
DSN 11-18-11		DATE 11-18-11	
ORIGIN K MANUFACTURING (LNT)		APPROVALS 11-18-11	
DESIGN K MANUFACTURING (LNT)		DATE 11-18-11	
SCALE DO NOT SCALE DRAWING		SHEET 1 OF 1	