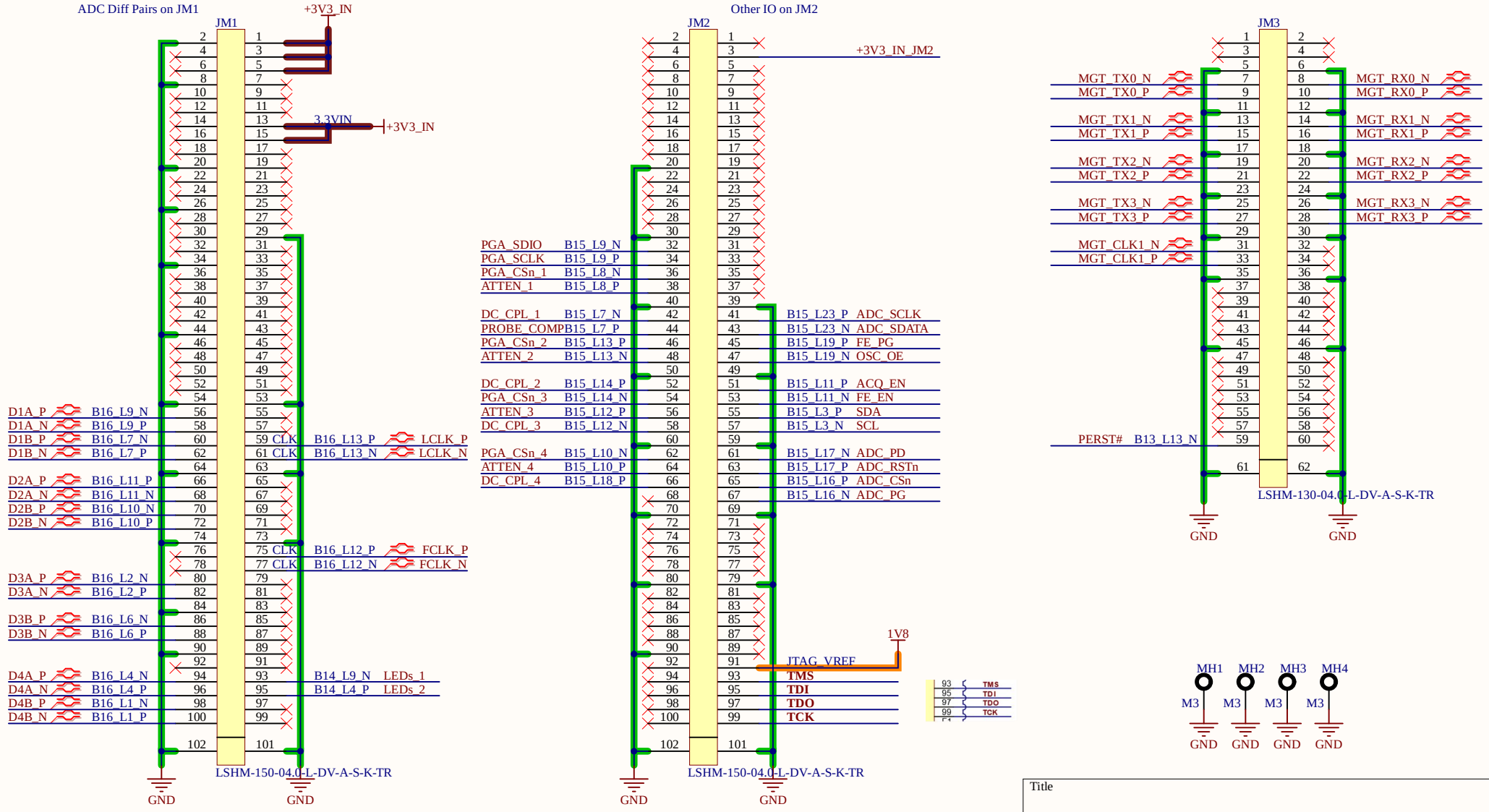
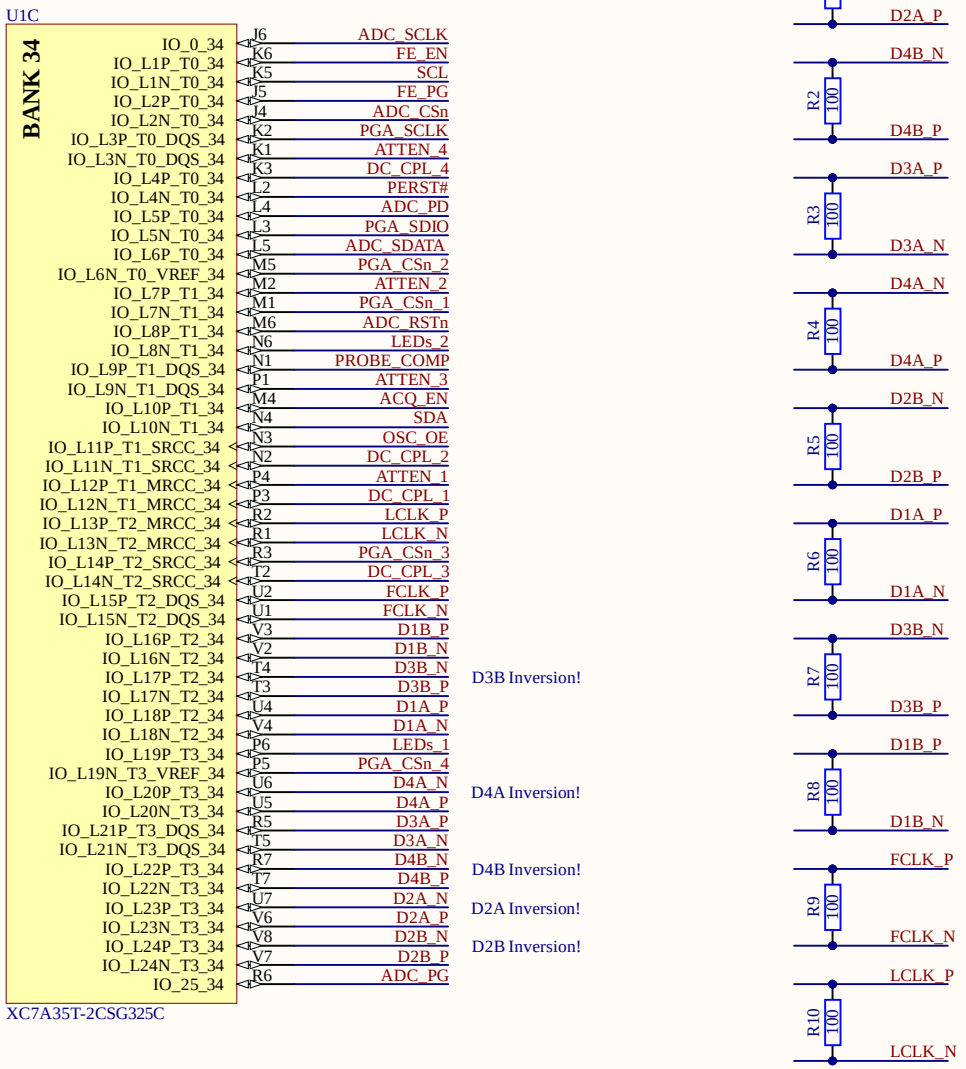
These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.



Title		
Size: A4	Number	Revision
Date: 2-15-2022		Sheet of
File: C:\Users\..\Connectors.SchDoc		Drawn By:



Title		
Size A4	Number	Revision
Date: 2-15-2022		Sheet of
File: C:\Users\..\FPGA_Bank_IO.SchDoc		Drawn By:

Pull-Up During Configuration (bar)

Active-Low PUDC_B input enables internal pull-up resistors on the SelectIO pins after power-up and during configuration.

- When PUDC_B is Low, internal pull-up resistors are enabled on each SelectIO pin.
- When PUDC_B is High, internal pull-up resistors are disabled on each SelectIO pin.

PUDC_B must be tied either directly, or via a ≤ 1 kΩ to V_{CCO_14} or GND. When PUDC_B is tied to GND, the activation of internal pull-ups during power-on depends on the power sequence because the PUDC_B control signal is forwarded through an input buffer in bank 14 and internal paths to the enables of internal pull-ups at applicable pins in their respective I/O banks. An external pull-up resistor is recommended between a pin and the pin's V_{CCO} power supply when it is critical for the pin to be pulled High immediately as the pin's V_{CCO} power ramps up.

Caution! Do not allow this pin to float before and during configuration.

U1A

BANK 14

IO_0_14	L14	
IO_L1P_T0_D00_MOSI_14	K16	SPI_DQ0_1V35
IO_L1N_T0_D01_DIN_14	L17	SPI_DQ1_1V35
IO_L2P_T0_D02_14	J15	SPI_DQ2_1V35
IO_L2N_T0_D03_14	J16	SPI_DQ3_1V35
IO_L3P_T0_DQS_PUDC_B_14	J18	PUDC
IO_L3N_T0_DQS_EMCCLK_14	K18	DDR3_CAS
IO_L4P_T0_D04_14	K17	DDR3_ODT
IO_L4N_T0_D05_14	L18	DDR3_CKE
IO_L5P_T0_D06_14	J14	
IO_L5N_T0_D07_14	K15	DDR3_RAS
IO_L6P_T0_FCS_B_14	L15	SPI_CS_1V35
IO_L6N_T0_D08_VREF_14	M15	DDR3_S0
IO_L7P_T1_D09_14	M16	DDR3_WE
IO_L7N_T1_D10_14	M17	DDR3_A10
IO_L8P_T1_D11_14	M14	
IO_L8N_T1_D12_14	N14	
IO_L9P_T1_DQS_14	N16	
IO_L9N_T1_DQS_D13_14	N17	DDR3_BA0
IO_L10P_T1_D14_14	N18	DDR3_BA2
IO_L10N_T1_D15_14	P18	
IO_L11P_T1_SRCC_14	P15	
IO_L11N_T1_SRCC_14	P16	
IO_L12P_T1_MRCC_14	P14	
IO_L12N_T1_MRCC_14	R15	
IO_L13P_T2_MRCC_14	T14	DDR3_A8
IO_L13N_T2_MRCC_14	T15	DDR3_A7
IO_L14P_T2_SRCC_14	R16	
IO_L14N_T2_SRCC_14	R17	
IO_L15P_T2_DQS_RDWR_B_14	R18	DDR3_A9
IO_L15N_T2_DQS_DOUT_CSO_B_14	T18	DDR3_A11
IO_L16P_T2_CSI_B_14	T17	DDR3_A1
IO_L16N_T2_A15_D31_14	U17	
IO_L17P_T2_A14_D30_14	U15	
IO_L17N_T2_A13_D29_14	U16	
IO_L18P_T2_A12_D28_14	V16	DDR3_A3
IO_L18N_T2_A11_D27_14	V17	DDR3_A12
IO_L19P_T3_A10_D26_14	R13	
IO_L19N_T3_A09_D25_VREF_14	T13	DDR3_A6
IO_L20P_T3_A08_D24_14	U14	
IO_L20N_T3_A07_D23_14	V14	DDR3_A0
IO_L21P_T3_DQS_14	V12	DDR3_A2
IO_L21N_T3_DQS_A06_D22_14	V13	DDR3_A4
IO_L22P_T3_A05_D21_14	T12	DDR3_BA1
IO_L22N_T3_A04_D20_14	U12	
IO_L23P_T3_A03_D19_14	U11	DDR3_RESET
IO_L23N_T3_A02_D18_14	V11	DDR3_A5
IO_L24P_T3_A01_D17_14	U9	DDR3_CLK_P
IO_L24N_T3_A00_D16_14	V9	DDR3_CLK_N
IO_25_14	U10	

XC7A35T-2CSG325C

1V35

R58 100

R59 100

GND

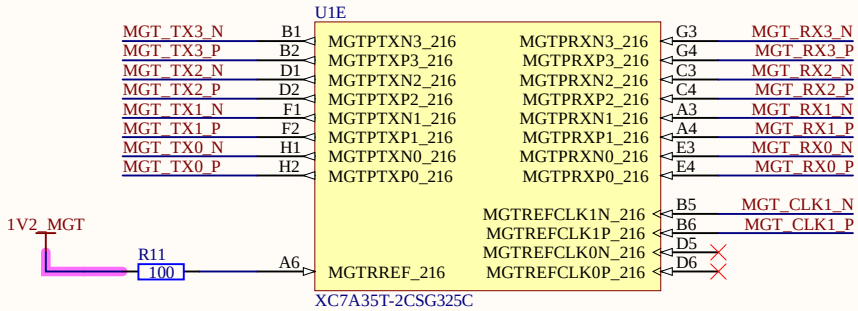
U1B

BANK 15

IO_0_15	D10	
IO_L1P_T0_AD0P_15	D8	DDR3_D10
IO_L1N_T0_AD0N_15	C8	DDR3_D12
IO_L2P_T0_AD8P_15	D9	DDR3_D14
IO_L2N_T0_AD8N_15	C9	DDR3_D9
IO_L3P_T0_DQS_AD1P_15	B9	DDR3_DQS1_P
IO_L3N_T0_DQS_AD1N_15	A9	DDR3_DQS1_N
IO_L4P_T0_15	C11	DDR3_D13
IO_L4N_T0_15	B11	DDR3_D15
IO_L5P_T0_AD9P_15	B10	DDR3_DM1
IO_L5N_T0_AD9N_15	A10	DDR3_D8
IO_L6P_T0_15	D11	DDR3_D11
IO_L6N_T0_VREF_15	C12	VTTREF
IO_L7P_T1_AD2P_15	B12	DDR3_DM0
IO_L7N_T1_AD2N_15	A12	DDR3_D1
IO_L8P_T1_AD10P_15	A13	DDR3_D5
IO_L8N_T1_AD10N_15	A14	DDR3_D4
IO_L9P_T1_DQS_AD3P_15	C14	DDR3_DQS0_P
IO_L9N_T1_DQS_AD3N_15	B15	DDR3_DQS0_N
IO_L10P_T1_AD11P_15	B14	DDR3_D7
IO_L10N_T1_AD11N_15	A15	DDR3_D2
IO_L11P_T1_SRCC_15	D13	DDR3_D6
IO_L11N_T1_SRCC_15	C13	DDR3_D3
IO_L12P_T1_MRCC_15	E13	
IO_L12N_T1_MRCC_15	D14	DDR3_D0
IO_L13P_T2_MRCC_15	E15	
IO_L13N_T2_MRCC_15	D15	DDR3_D22
IO_L14P_T2_SRCC_15	E16	DDR3_D18
IO_L14N_T2_SRCC_15	D16	DDR3_D17
IO_L15P_T2_DQS_15	B16	DDR3_DQS2_P
IO_L15N_T2_DQS_ADV_B_15	A17	DDR3_DQS2_N
IO_L16P_T2_A28_15	C16	DDR3_D20
IO_L16N_T2_A27_15	B17	DDR3_D16
IO_L17P_T2_A26_15	E17	DDR3_D19
IO_L17N_T2_A25_15	D18	DDR3_DM2
IO_L18P_T2_A24_15	C17	DDR3_D23
IO_L18N_T2_A23_15	C18	DDR3_D21
IO_L19P_T3_A22_15	G17	DDR3_D24
IO_L19N_T3_A21_VREF_15	F18	VTTREF
IO_L20P_T3_A20_15	H16	DDR3_D28
IO_L20N_T3_A19_15	G16	DDR3_DM3
IO_L21P_T3_DQS_15	G15	DDR3_DQS3_P
IO_L21N_T3_DQS_A18_15	F15	DDR3_DQS3_N
IO_L22P_T3_A17_15	G14	DDR3_D31
IO_L22N_T3_A16_15	F14	DDR3_D29
IO_L23P_T3_FOE_B_15	H17	DDR3_D26
IO_L23N_T3_FWE_B_15	H18	DDR3_D30
IO_L24P_T3_RS1_15	F17	DDR3_D25
IO_L24N_T3_RS0_15	E18	DDR3_D27
IO_25_15	H14	

XC7A35T-2CSG325C

Title		
Size: A4	Number	Revision
Date: 2-15-2022	Sheet of	
File: C:\Users\..\FPGA_Banks_DDR3.SchDoc	Drawn By:	



Title		
Size: A4	Number	Revision
Date: 2-15-2022		Sheet of
File: C:\Users\..\FPGA_MGT.SchDoc		Drawn By:

Table 2-1: **7 Series FPGA Configuration Modes**

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

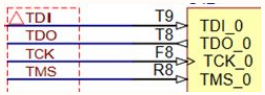
M[2:0] = 001

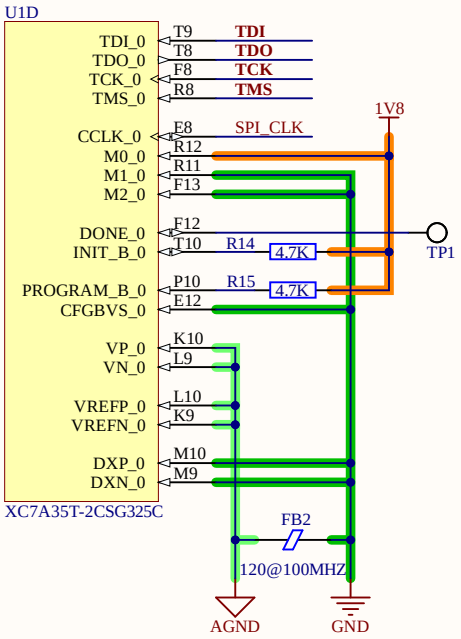
A High signal on the DONE pin indicates completion of the configuration sequence. The DONE output is an open-drain output by default.

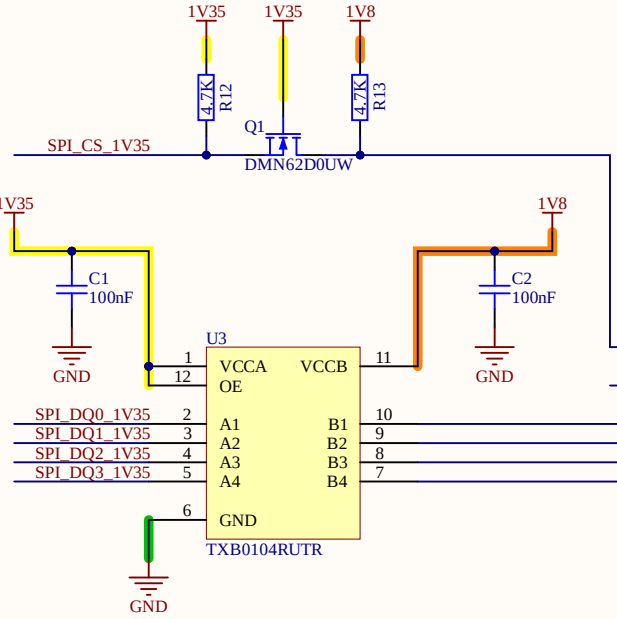
Note: DONE has an internal pull-up resistor of approximately 10 kΩ. There is no setup/hold requirement for the DONE register. These changes, along with the DonePipe register software default, eliminate the need for the DriveDONE driver-option. External 330Ω resistor circuits are not required but can be used as they have been in previous generations.

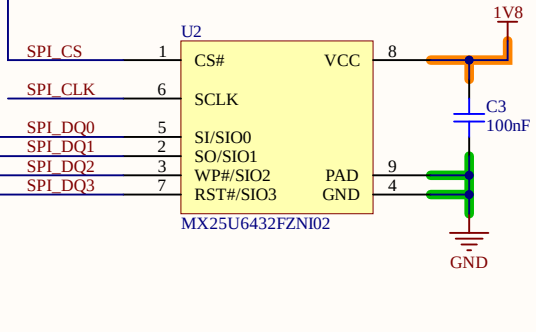
Connect INIT_B to a ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure clean Low-to-High transitions.

Connect PROGRAM_B to an external ≤ 4.7 kΩ pull-up resistor to V_{CCO_0} to ensure a stable High input, and









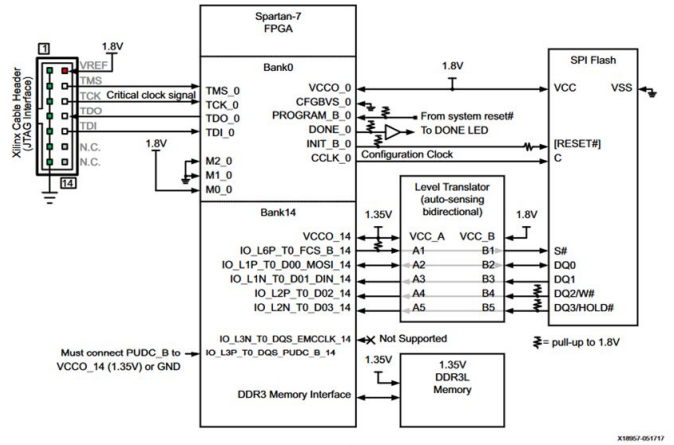
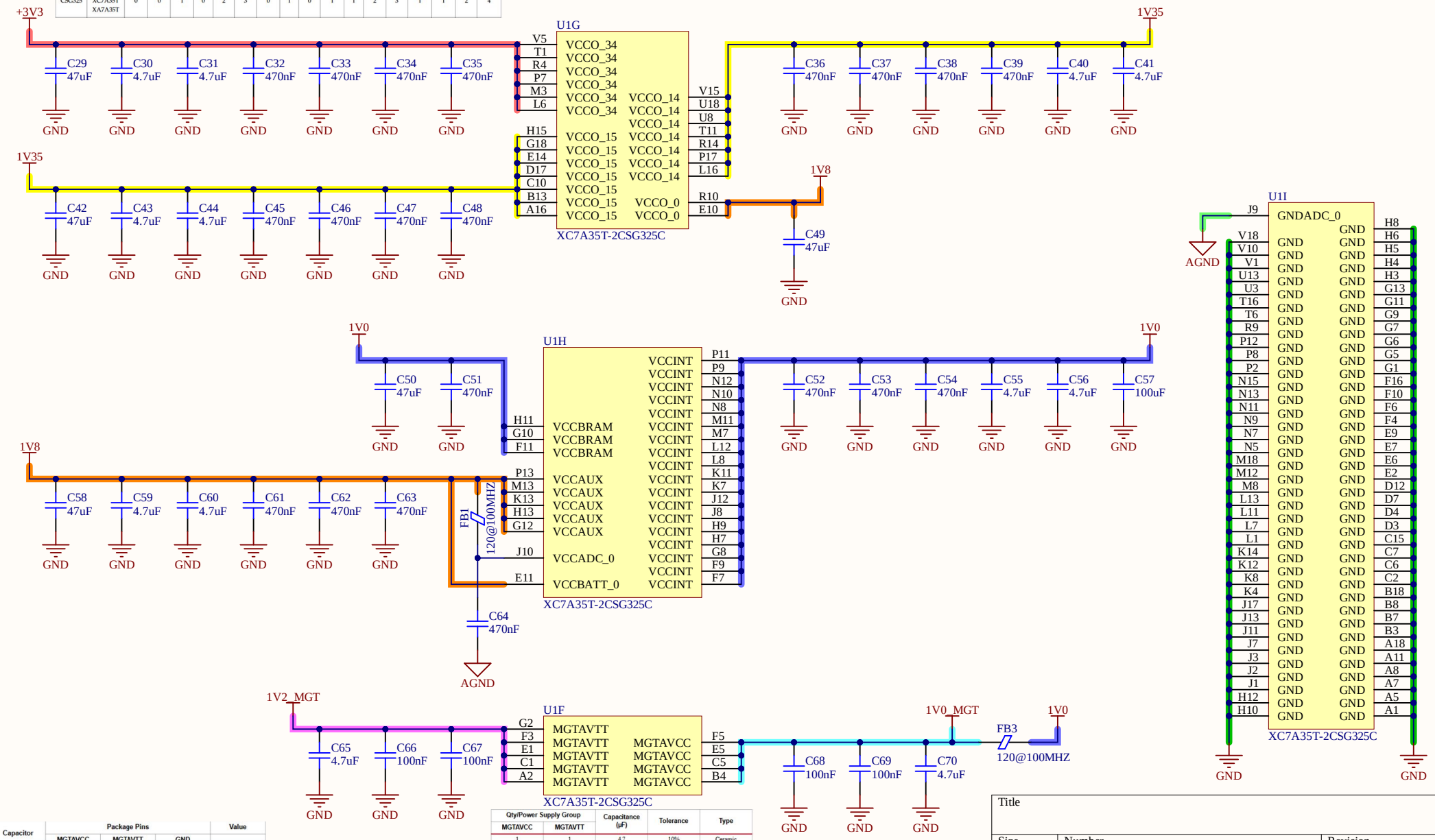


Figure 2: **FPGA and SPI Flash Configuration Schematic Diagram**

Title		
Size A4	Number	Revision
Date: 2-15-2022		Sheet of
File: C:\Users\..\FPGA_CFG.SchDoc		Drawn By:

Package	Device	V_{CCINT}						V_{CCBRAM}				V_{CCAUX}			V_{CCO} Bank 0	V_{CCO} all other Banks (per Bank)		
		680 µF	330 µF	100 µF	47 µF	4.7 µF	0.47 µF	100 µF	47 µF	4.7 µF	0.47 µF	47 µF	4.7 µF	0.47 µF	47 µF	47 µF or 100 µF[3]	4.7 µF	0.47 µF
CSG325	XC7A35T XA7A35T	0	0	1	0	2	3	0	1	0	1	1	2	3	1	1	2	4

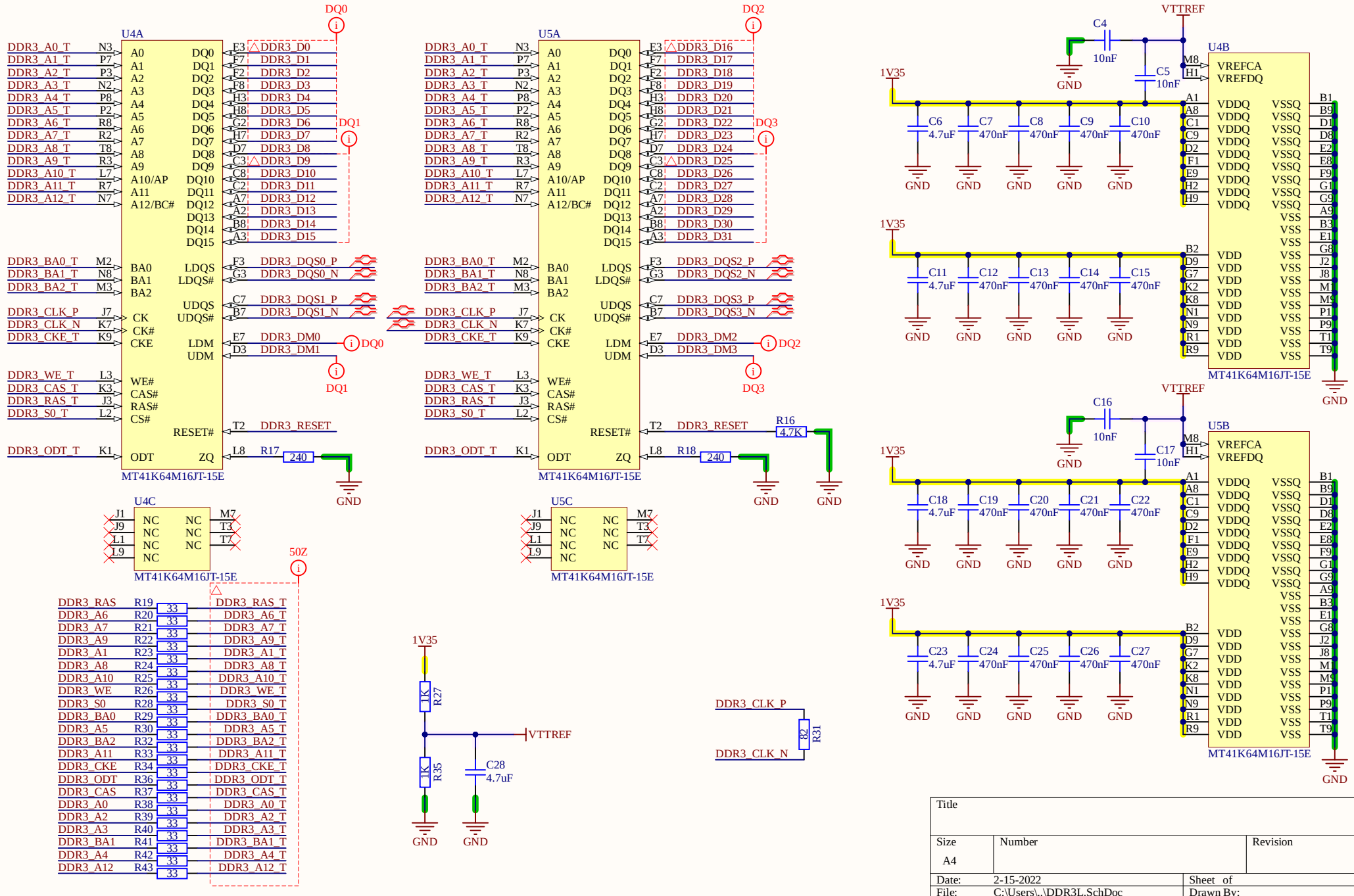
3. One 47 µF (or 100 µF) capacitor is required for up to four V_{CCO} banks when powered by the same voltage.

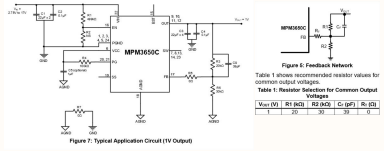


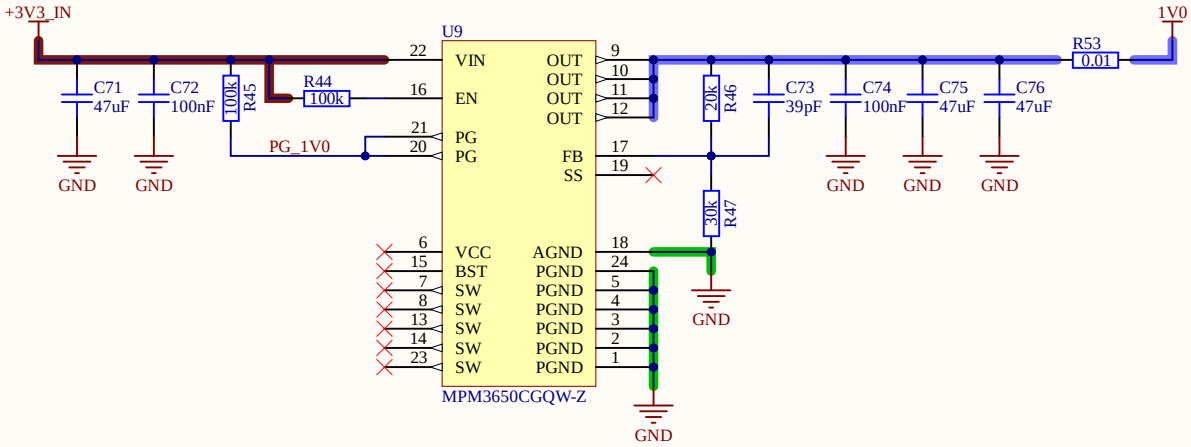
Capacitor	Package Pins			Value
	MGTAVCC	MGTAVTT	GND	
Cap1		F3	F4	0.1 µF
Cap2		A2	A1	
Cap3	B4		B3	
Cap4	F5		F6	

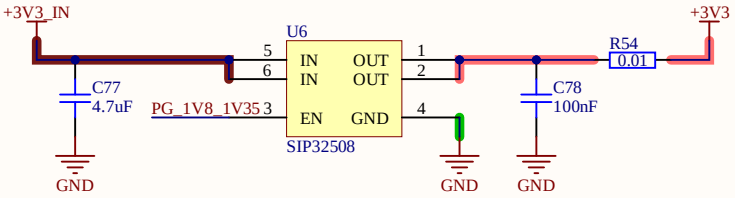
Qty/Power Supply Group		Capacitance (µF)	Tolerance	Type
MGTAVCC	MGTAVTT			
1	1	4.7	10%	Ceramic
2	2	0.1	10%	Ceramic

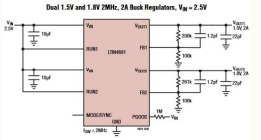
Title		
Size A4	Number	Revision
Date: 2-15-2022		Sheet of
File: C:\Users\..\FPGA_PWR.SchDoc		Drawn By:


U4A
U5A
U4B
U5B
U4C
U5C
MT41K64M16JT-15E
DDR3_A0_T
DDR3_A1_T
DDR3_A2_T
DDR3_A3_T
DDR3_A4_T
DDR3_A5_T
DDR3_A6_T
DDR3_A7_T
DDR3_A8_T
DDR3_A9_T
DDR3_A10_T
DDR3_A11_T
DDR3_A12_T
DDR3_BA0_T
DDR3_BA1_T
DDR3_BA2_T
DDR3_CLK_P
DDR3_CLK_N
DDR3_CKE_T
DDR3_WE_T
DDR3_CAS_T
DDR3_RAS_T
DDR3_S0_T
DDR3_ODT_T
DDR3_RESET
DDR3_DQS0_P
DDR3_DQS0_N
DDR3_DQS1_P
DDR3_DQS1_N
DDR3_DQS2_P
DDR3_DQS2_N
DDR3_DQS3_P
DDR3_DQS3_N
DDR3_DM0
DDR3_DM1
DDR3_DM2
DDR3_DM3
DQ0
DQ1
DQ2
DQ3
R16 4.7K
R17 240
R18 240
50Z
1V35
VTTREF
GND
C4 10nF
C5 10nF
C6 4.7uF
C7 470nF
C8 470nF
C9 470nF
C10 470nF
C11 4.7uF
C12 470nF
C13 470nF
C14 470nF
C15 470nF
C16 10nF
C17 10nF
C18 4.7uF
C19 470nF
C20 470nF
C21 470nF
C22 470nF
C23 4.7uF
C24 470nF
C25 470nF
C26 470nF
C27 470nF
C28 4.7uF
R19 33
R20 33
R21 33
R22 33
R23 33
R24 33
R25 33
R26 33
R27 33
R28 33
R29 33
R30 33
R32 33
R33 33
R34 33
R36 33
R37 33
R38 33
R39 33
R40 33
R41 33
R42 33
R43 33
R27 1K
R35 1K
R31 82
Title
Size A4
Number
Revision
Date: 2-15-2022
File: C:\Users\..\DDR3L.SchDoc
Sheet of
Drawn By:



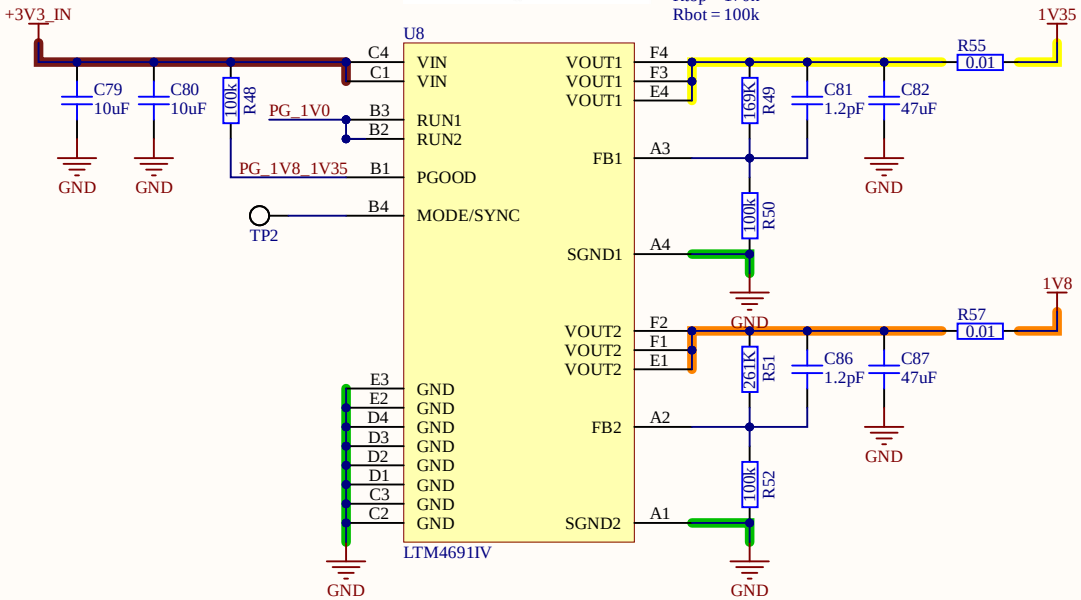


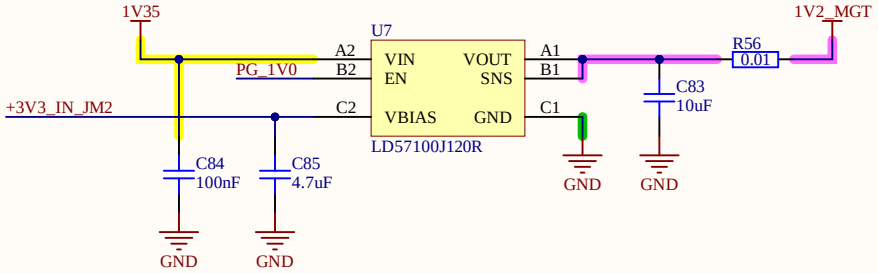




$$V_{OUT} = 0.5V \bullet \frac{R_{TOP} + R_{BOT}}{R_{BOT}}$$

1.35 = 0.5 * (170+100)/100
Rtop = 170k
Rbot = 100k





Title		
Size: A4	Number	Revision
Date: 2-15-2022		Sheet of
File: C:\Users\..\PWR.SchDoc		Drawn By: