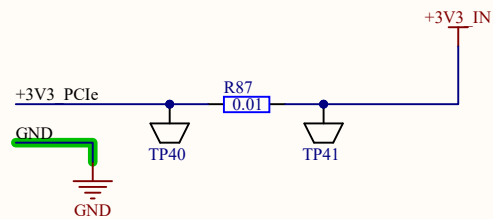
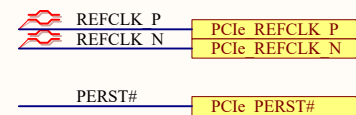
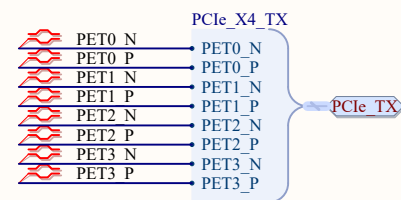
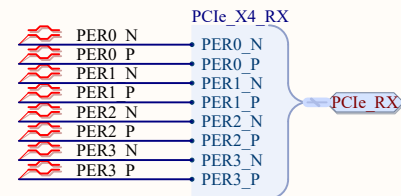
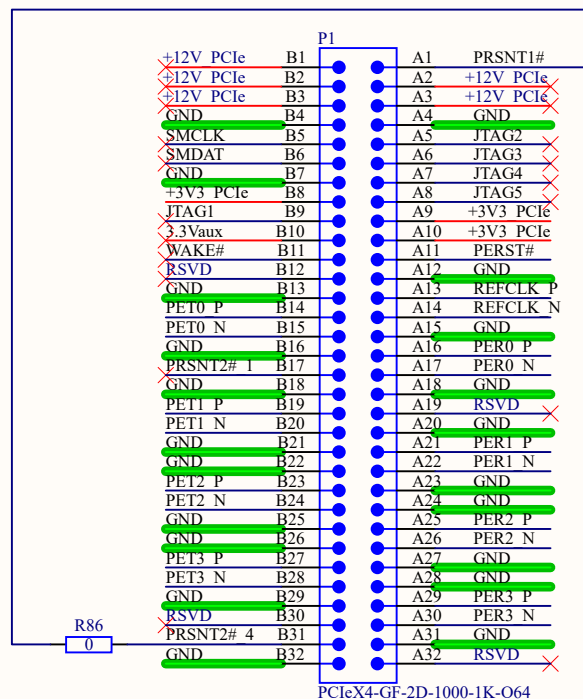
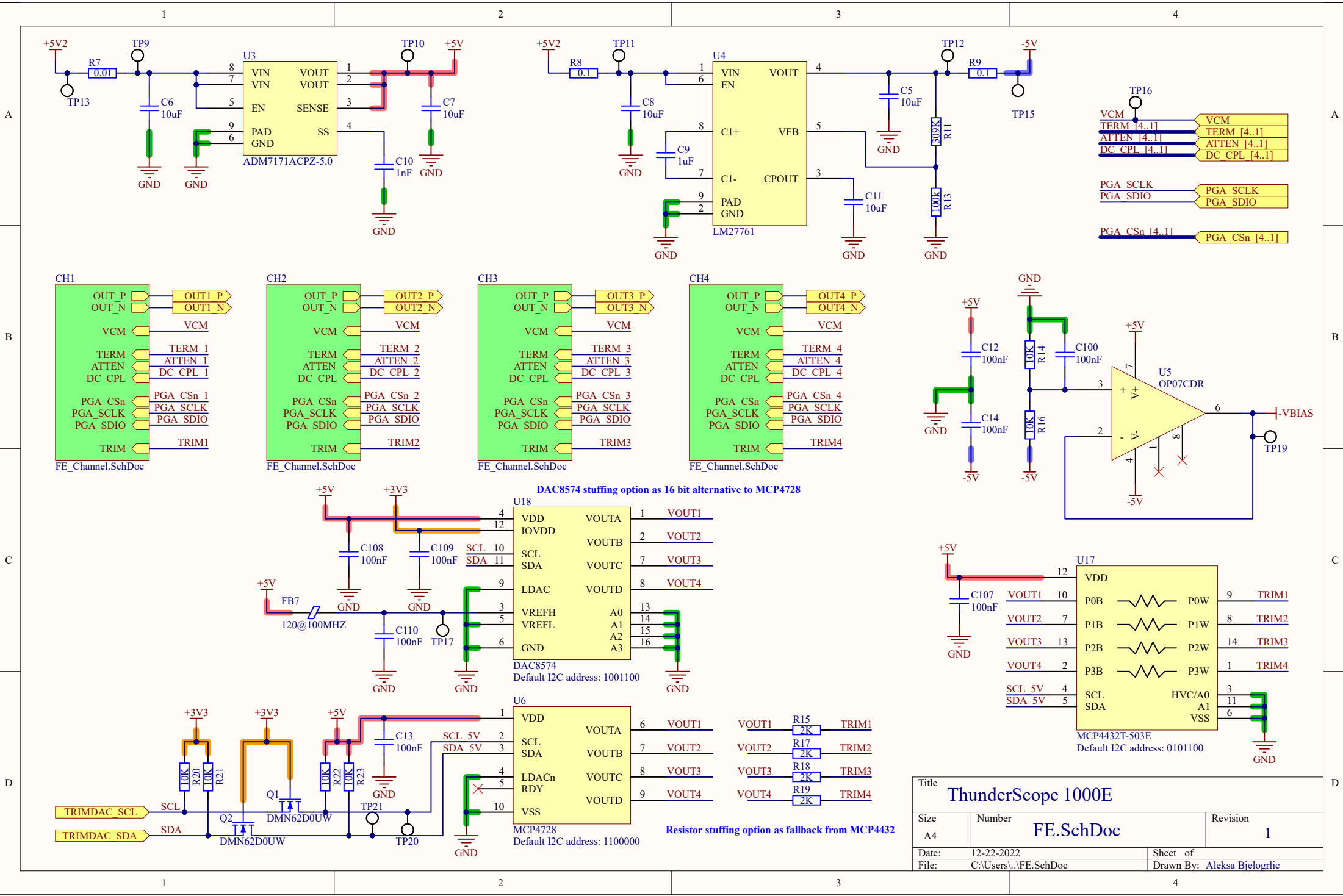


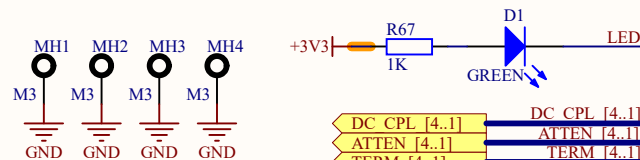
Title			
ThunderScope 1000E			
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File:	C:\Users\...\ADC.SchDoc	Drawn By:	Aleksa Bjelogrić

- Nominal values used, dimensions in mm  
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly  
- Component height rule and clearance rule derived from PCI\_Express\_CEM\_r2.0.pdf, Page 84.  
- Stackup is not specified in PCI\_Express\_CEM\_r2.0.pdf, nor implemented in this template.

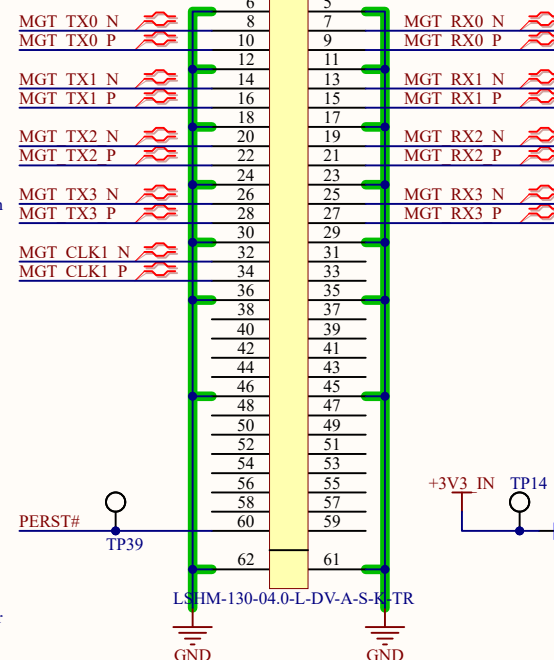
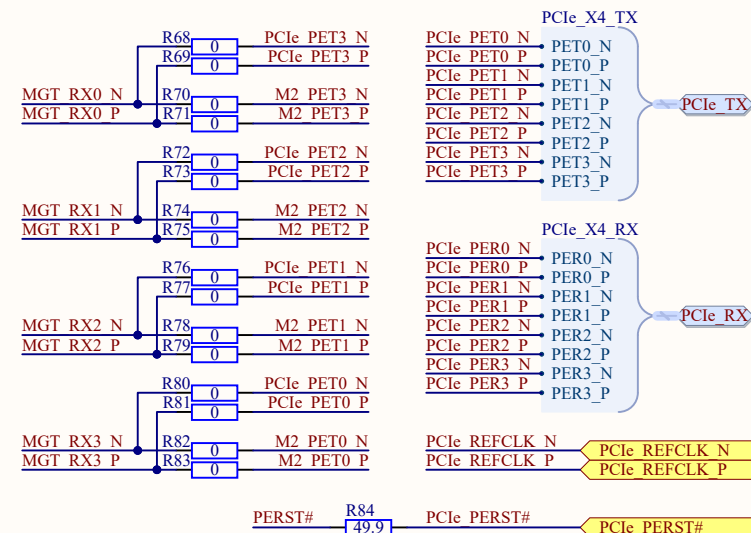
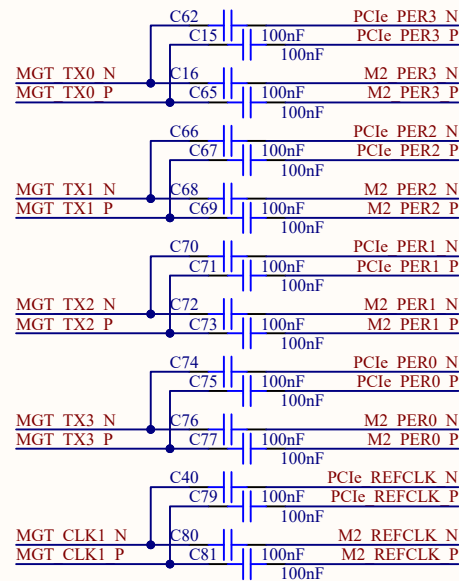
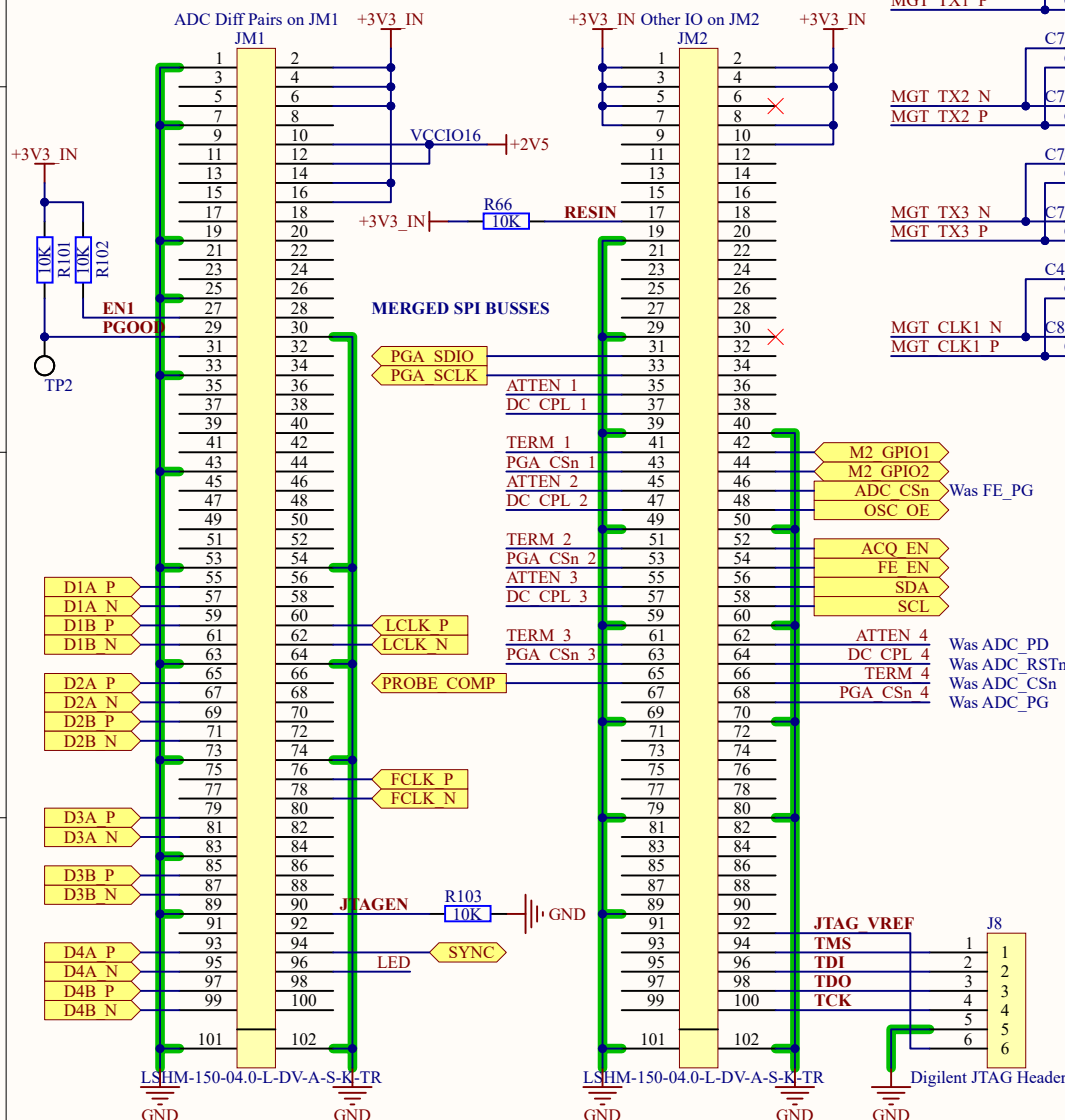




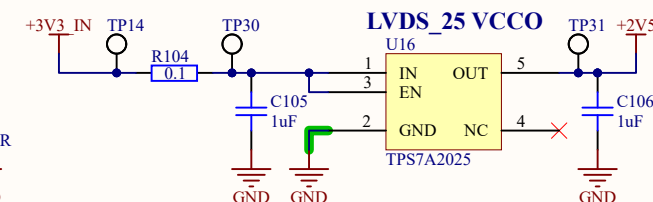




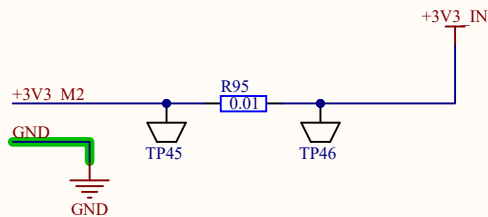
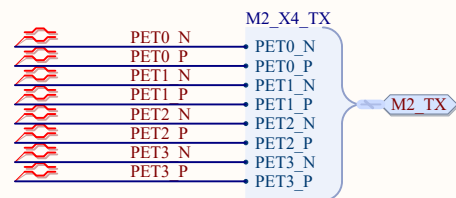
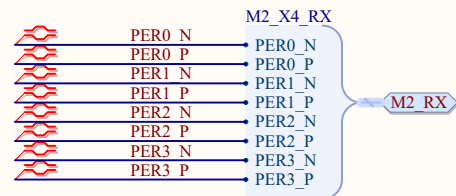
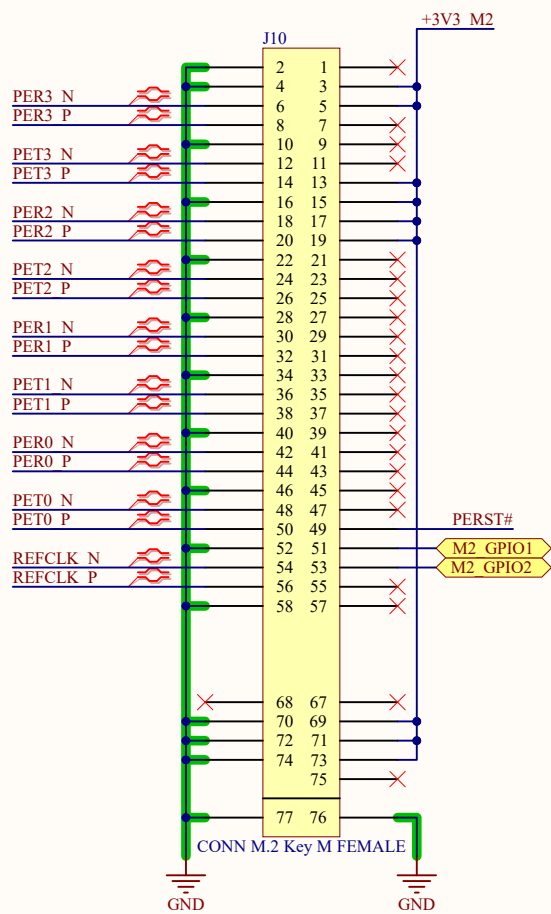
**DONE: Backwards compatibility with TE0712**



AC Couple PER Lines with 100nF  
 AC Couple REFCLK Lines with 100nF



These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

**Main Board  
Custom Pinout**

Title		
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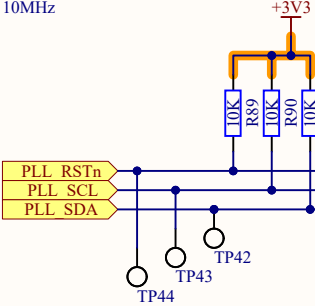
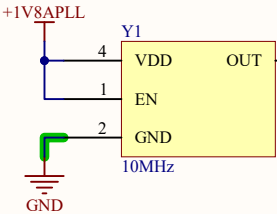
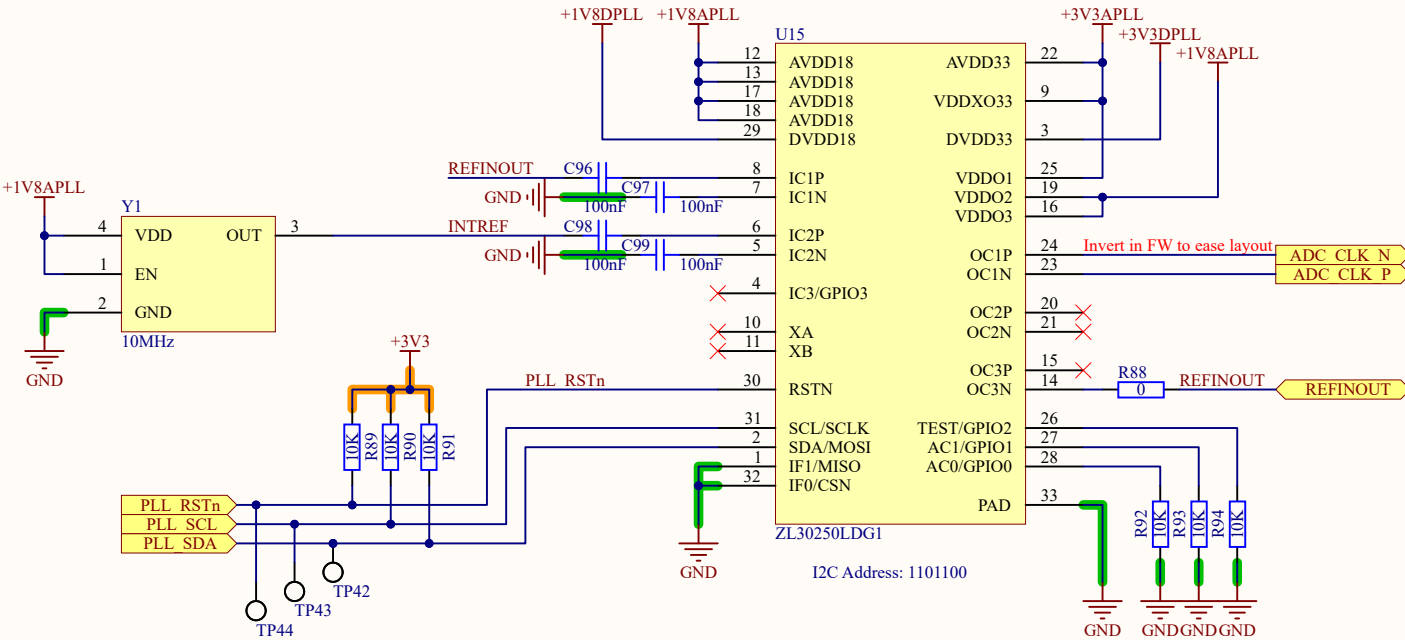
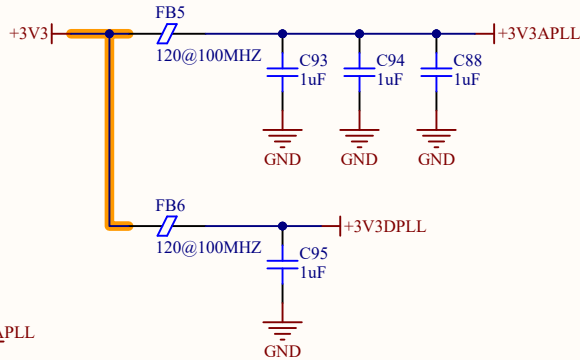
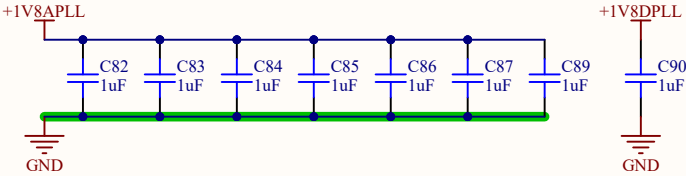


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A

A

B

B

C

C

D

D

Factory Test / General Purpose I/O 2							
					<i>Factory Test:</i> On the rising edge of RSTN the pin behaves as TEST. Factory test mode is enabled when TEST is high. For normal operation TEST must be low on the rising edge of RSTN.		
					<i>General-Purpose I/O:</i> After reset this pin is GPIO2. <a href="#">GPIOCR2</a> configures the pin. Its state is indicated in <a href="#">GPIOISR</a> .		
IF1	IF0	AC1	AC0		Processor Interface	External EEPROM	Auto Configuration
0	0	0	0		I <sup>2</sup> C, slave address 11011 00	No	n/a
0	1	0	0		I <sup>2</sup> C, slave address 11011 01	No	n/a
1	0	0	0		I <sup>2</sup> C, slave address 11011 10	No	n/a
1	1	0	0		SPI Slave	No	n/a
1	1	0	1		SPI Master to external EEPROM for auto-configuration then SPI Slave	Yes	Configuration 1
1	1	1	0			Yes	Configuration 2
1	1	1	1			Yes	Configuration 3

Title		
Size	Number	Revision
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