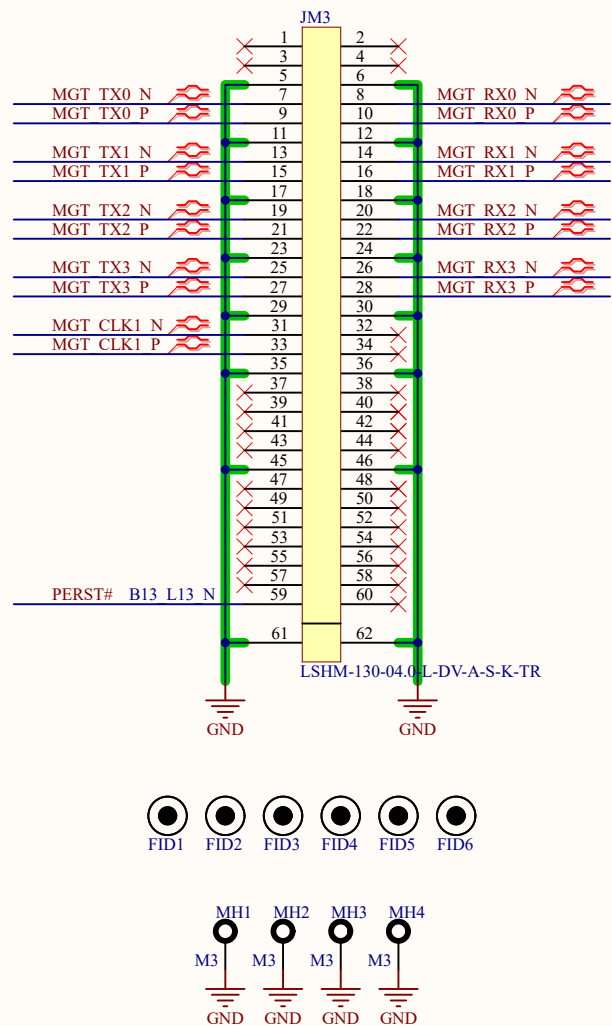
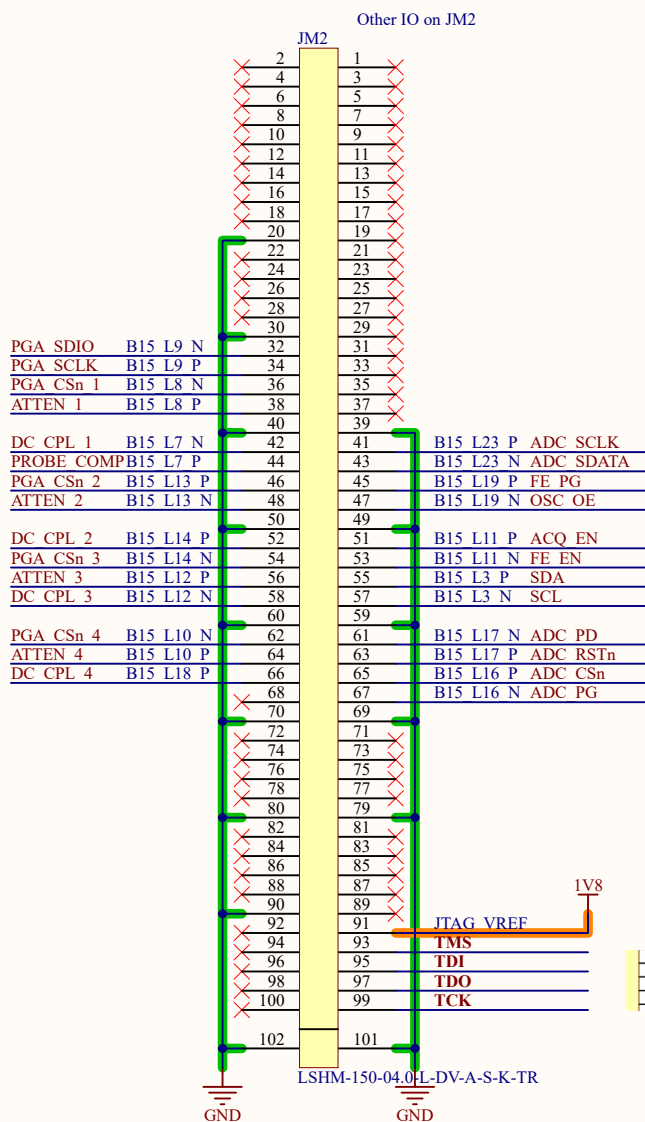
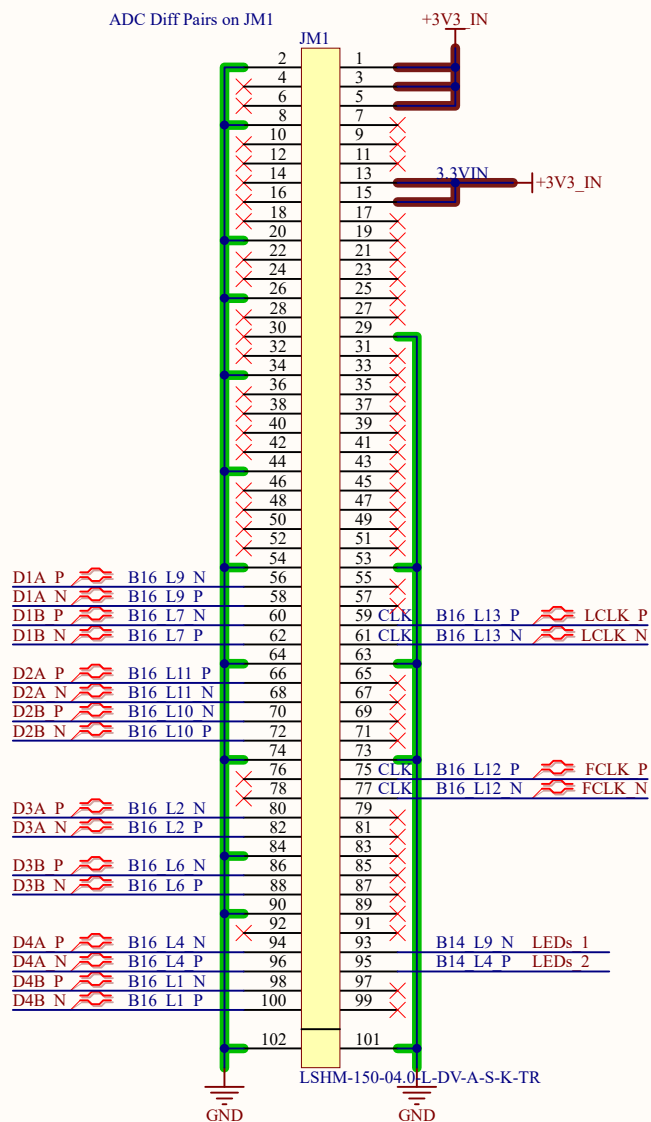


These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.



Title		
Size	Number	Revision
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Date:	10-19-2022	Sheet of
File:	C:\Users\...\Connectors.SchDoc	Drawn By:

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**BANK 34**

IO_0_34	J6	ADC_SCLK
IO_L1P_T0_34	K6	FE_EN
IO_L1N_T0_34	K5	SCL
IO_L2P_T0_34	J5	FE_PG
IO_L2N_T0_34	J4	ADC_CS <sub>n</sub>
IO_L3P_T0_DQS_34	K2	PGA_SCLK
IO_L3N_T0_DQS_34	K1	ATTEN_4
IO_L4P_T0_34	K3	DC_CPL_4
IO_L4N_T0_34	J2	PERST#
IO_L5P_T0_34	J4	ADC_PD
IO_L5N_T0_34	J3	PGA_SDIO
IO_L6P_T0_34	J5	ADC_SDATA
IO_L6N_T0_VREF_34	M5	PGA_CS <sub>n</sub> 2
IO_L7P_T1_34	M2	ATTEN_2
IO_L7N_T1_34	M1	PGA_CS <sub>n</sub> 1
IO_L8P_T1_34	M6	ADC_RST <sub>n</sub>
IO_L8N_T1_34	N6	LEDs_2
IO_L9P_T1_DQS_34	N1	PROBE_COMP
IO_L9N_T1_DQS_34	P1	ATTEN_3
IO_L10P_T1_34	M4	ACQ_EN
IO_L10N_T1_34	N4	SDA
IO_L11P_T1_SRCC_34	N3	OSC_OE
IO_L11N_T1_SRCC_34	N2	DC_CPL_2
IO_L12P_T1_MRCC_34	P4	ATTEN_1
IO_L12N_T1_MRCC_34	P3	DC_CPL_1
IO_L13P_T2_MRCC_34	K2	LCLK_P
IO_L13N_T2_MRCC_34	K1	LCLK_N
IO_L14P_T2_SRCC_34	K3	PGA_CS <sub>n</sub> 3
IO_L14N_T2_SRCC_34	J2	DC_CPL_3
IO_L15P_T2_DQS_34	U2	FCLK_P
IO_L15N_T2_DQS_34	U1	FCLK_N
IO_L16P_T2_34	V3	D1B_P
IO_L16N_T2_34	V2	D1B_N
IO_L17P_T2_34	T4	D3B_N
IO_L17N_T2_34	T3	D3B_P
IO_L17N_T2_34	U4	D1A_P
IO_L18P_T2_34	V4	D1A_N
IO_L18N_T2_34	P6	LEDs_1
IO_L19P_T3_34	P5	PGA_CS <sub>n</sub> 4
IO_L19N_T3_VREF_34	U6	D4A_N
IO_L20P_T3_34	U5	D4A_P
IO_L20N_T3_34	R5	D3A_P
IO_L21P_T3_DQS_34	T5	D3A_N
IO_L21N_T3_DQS_34	R7	D4B_N
IO_L22P_T3_34	T7	D4B_P
IO_L22N_T3_34	U7	D2A_N
IO_L23P_T3_34	V6	D2A_P
IO_L23N_T3_34	V8	D2B_N
IO_L24P_T3_34	V7	D2B_P
IO_L24N_T3_34	K6	ADC_PG
IO_25_34		

IC FPGA XC7A50T-2CSG325C

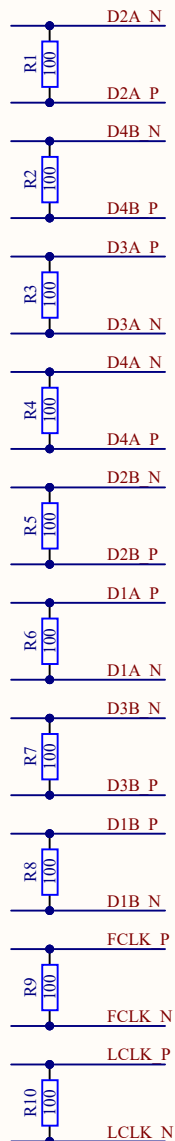
D3B Inversion!

D4A Inversion!

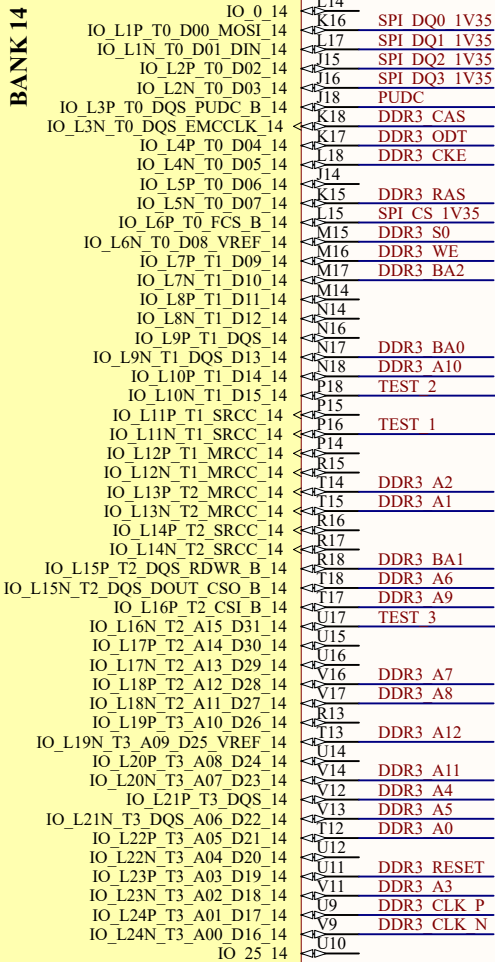
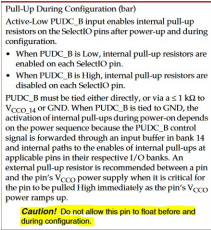
D4B Inversion!

D2A Inversion!

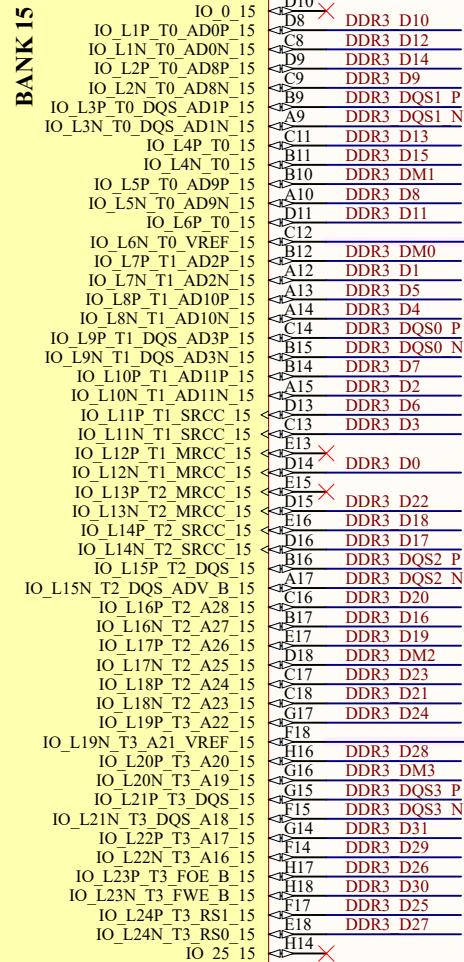
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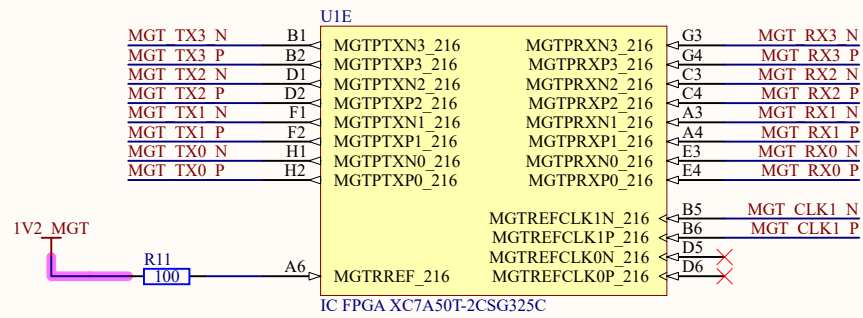


IC FPGA XC7A50T-2CSG325C



IC FPGA XC7A50T-2CSG325C

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Table 2-1: 7 Series FPGA Configuration Modes

Configuration Mode	M[2:0]	Bus Width	CCLK Direction
Master SPI	001	x1, x2, x4	Output

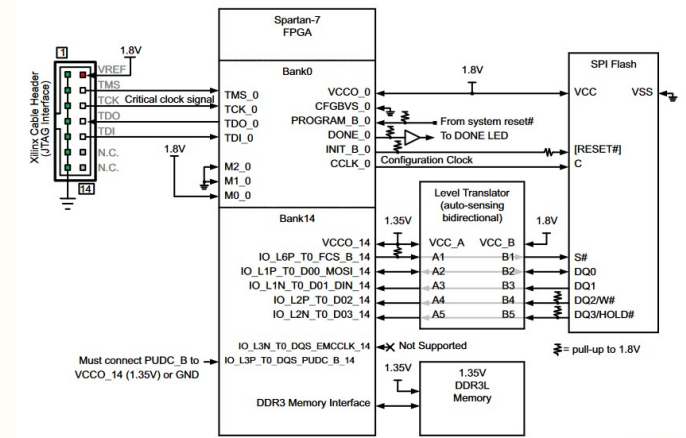
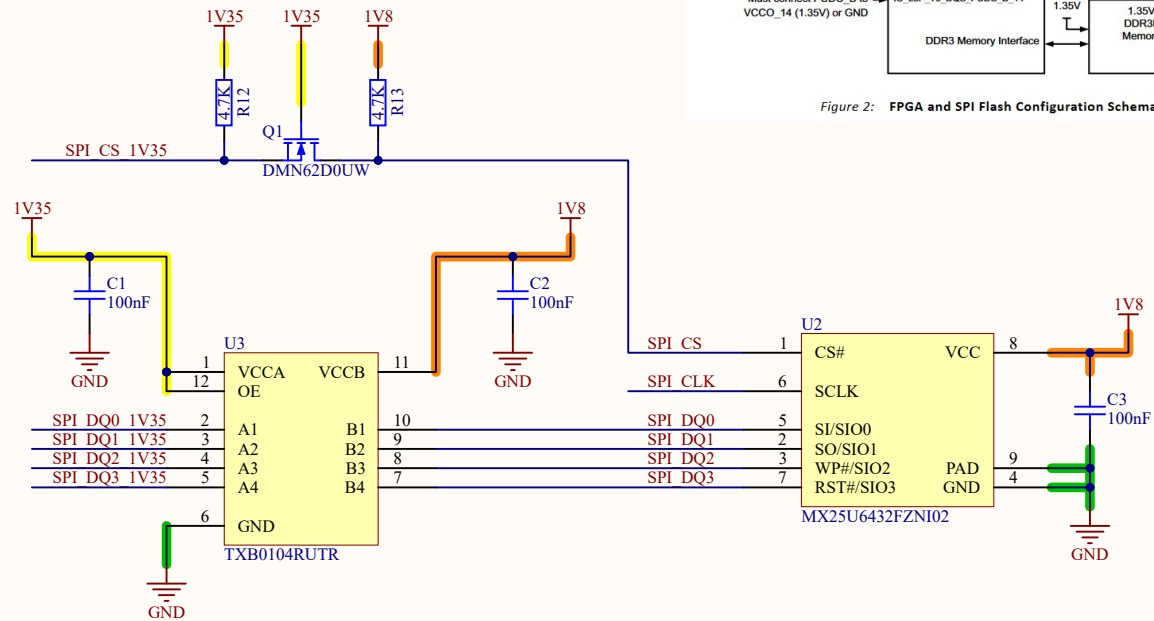
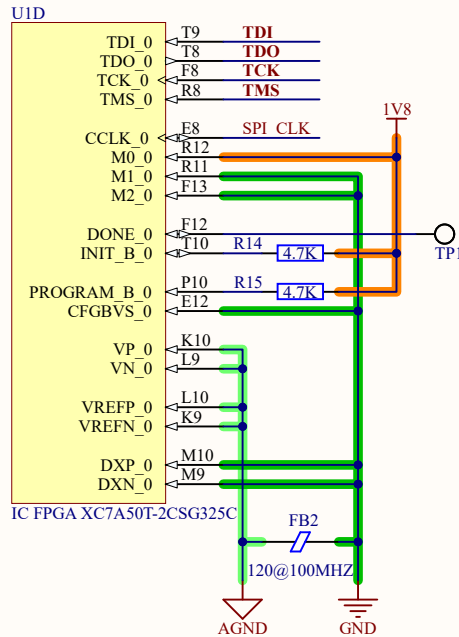
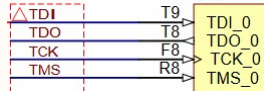


Figure 2: FPGA and SPI Flash Configuration Schematic Diagram

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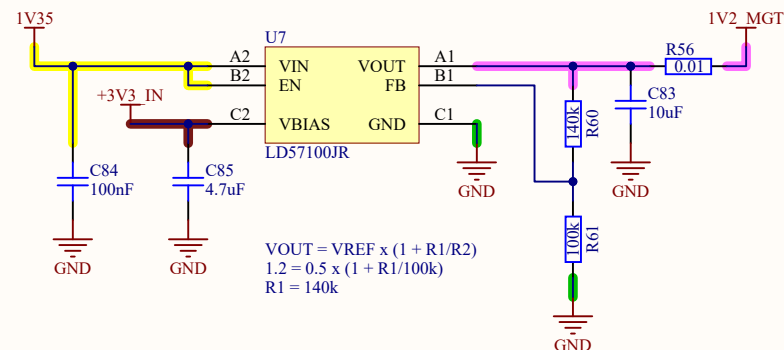
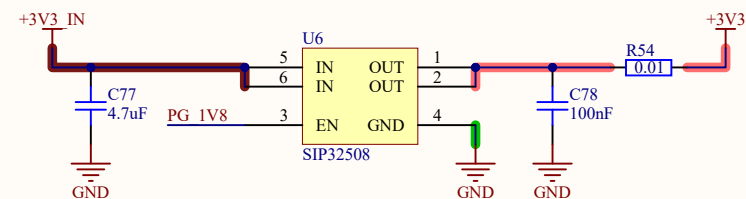
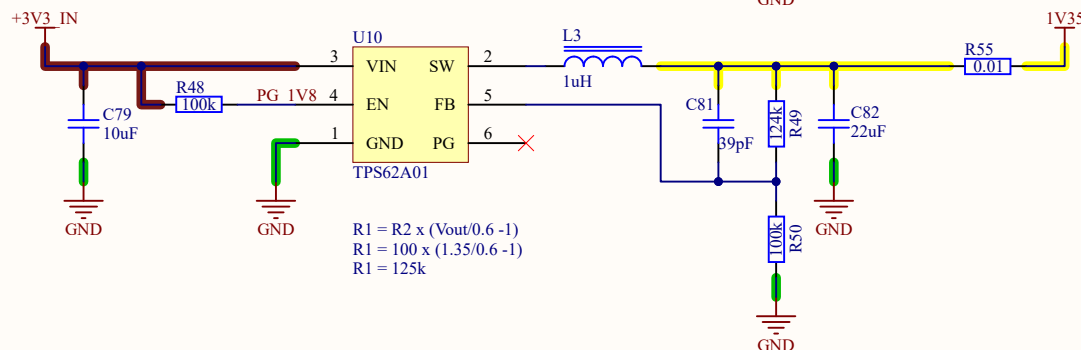
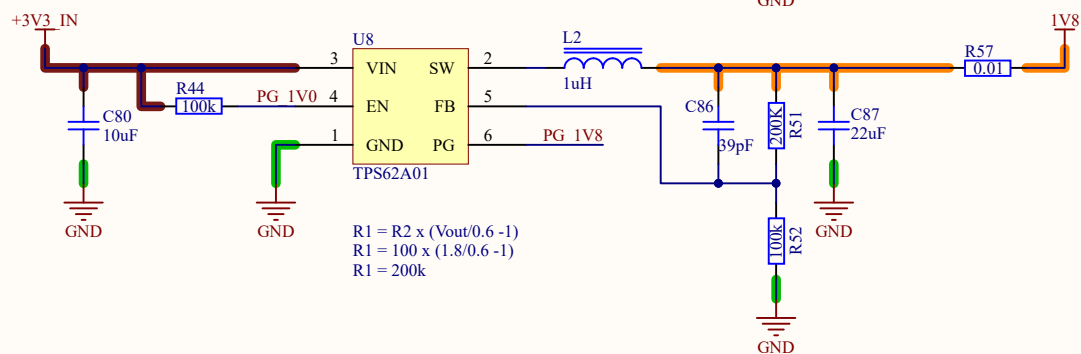
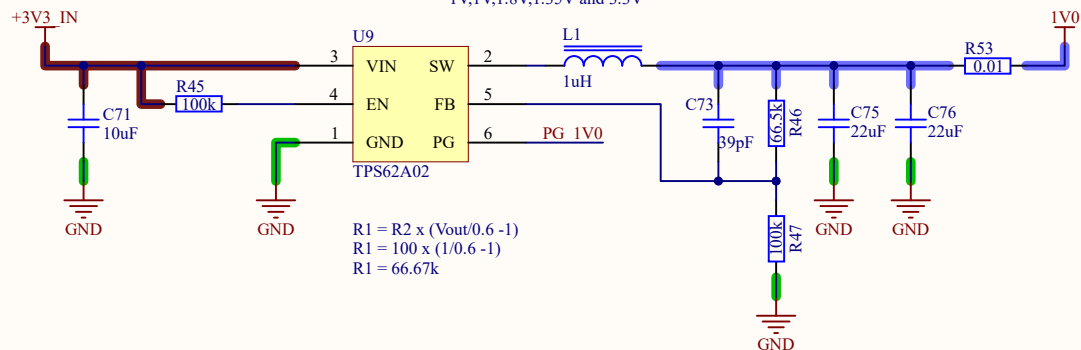
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4

The recommended power-on sequence is VCCINT, VCCBRAM, VCCAUX, and VCCO  
1V,1V,1.8V,1.35V and 3.3V



The recommended power-on sequence to achieve minimum current draw for the GTP transceivers is VCCINT, VMGTAVCC, VMGTAVTT  
1V,1V,1.2V

Title		
Size A4	Number	Revision
Date:	10-19-2022	Sheet of
File:	C:\Users\...\PWR.SchDoc	Drawn By:

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