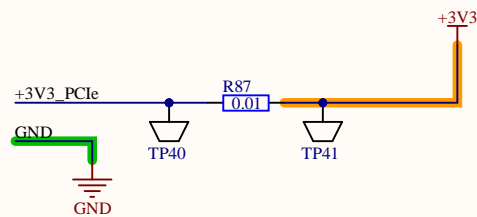
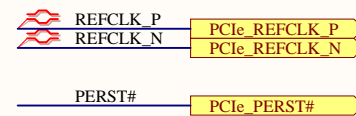
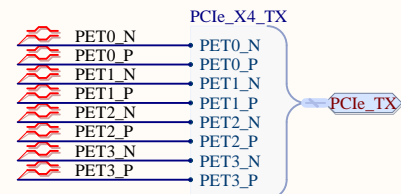
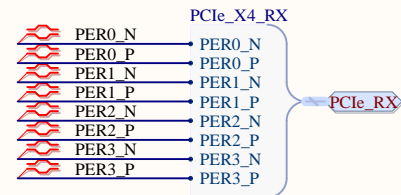
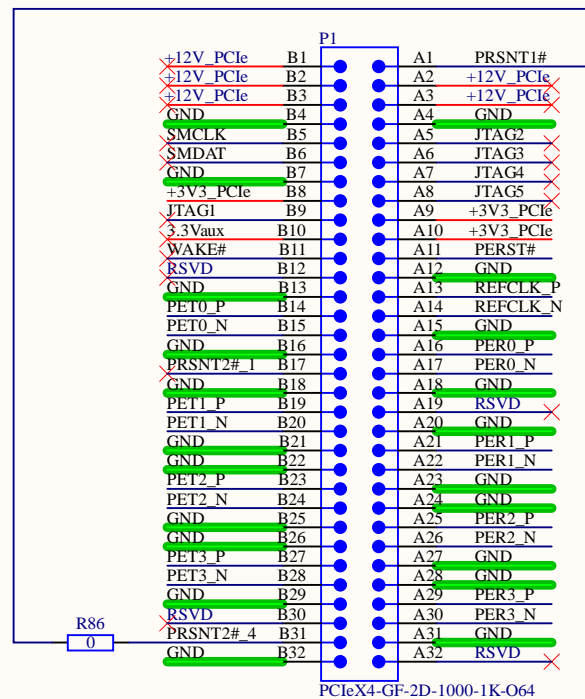
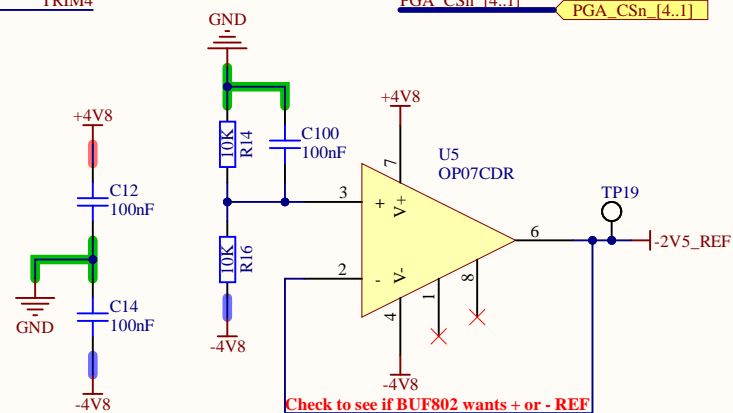
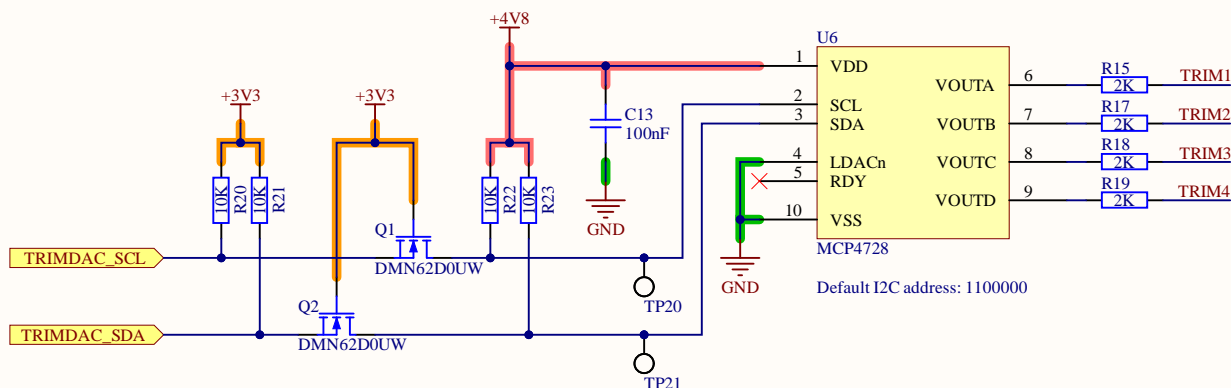
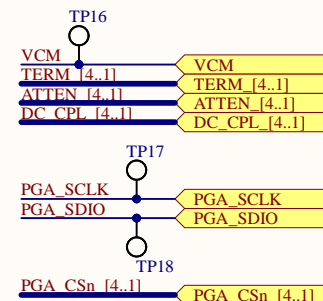
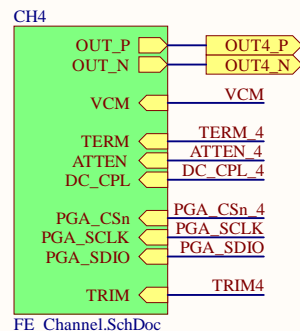
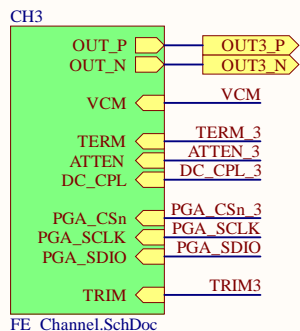
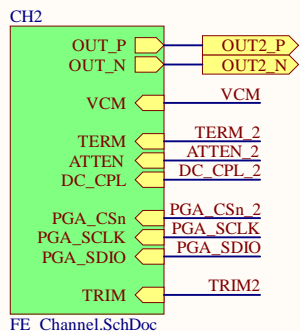
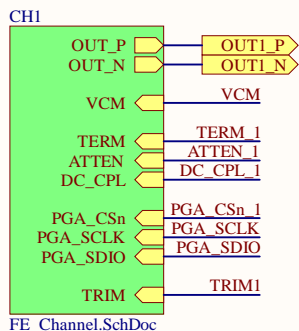
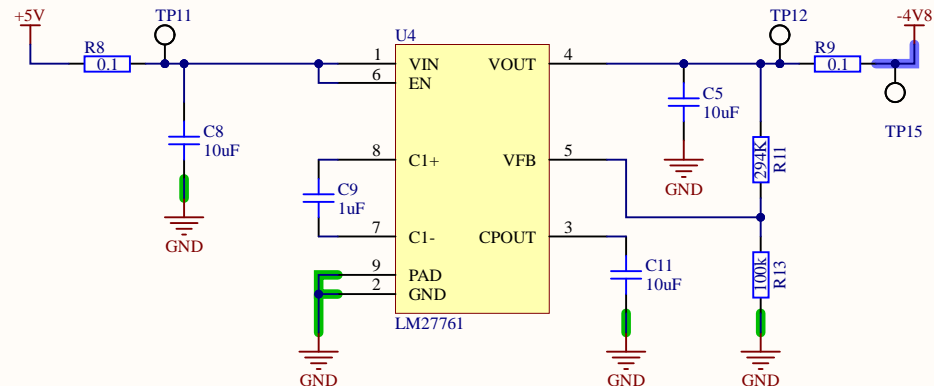
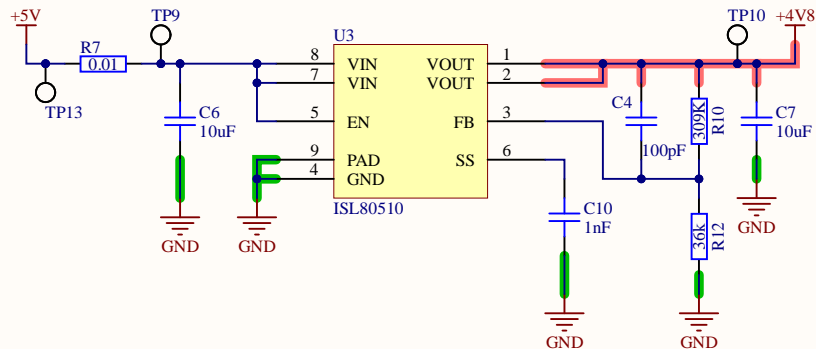


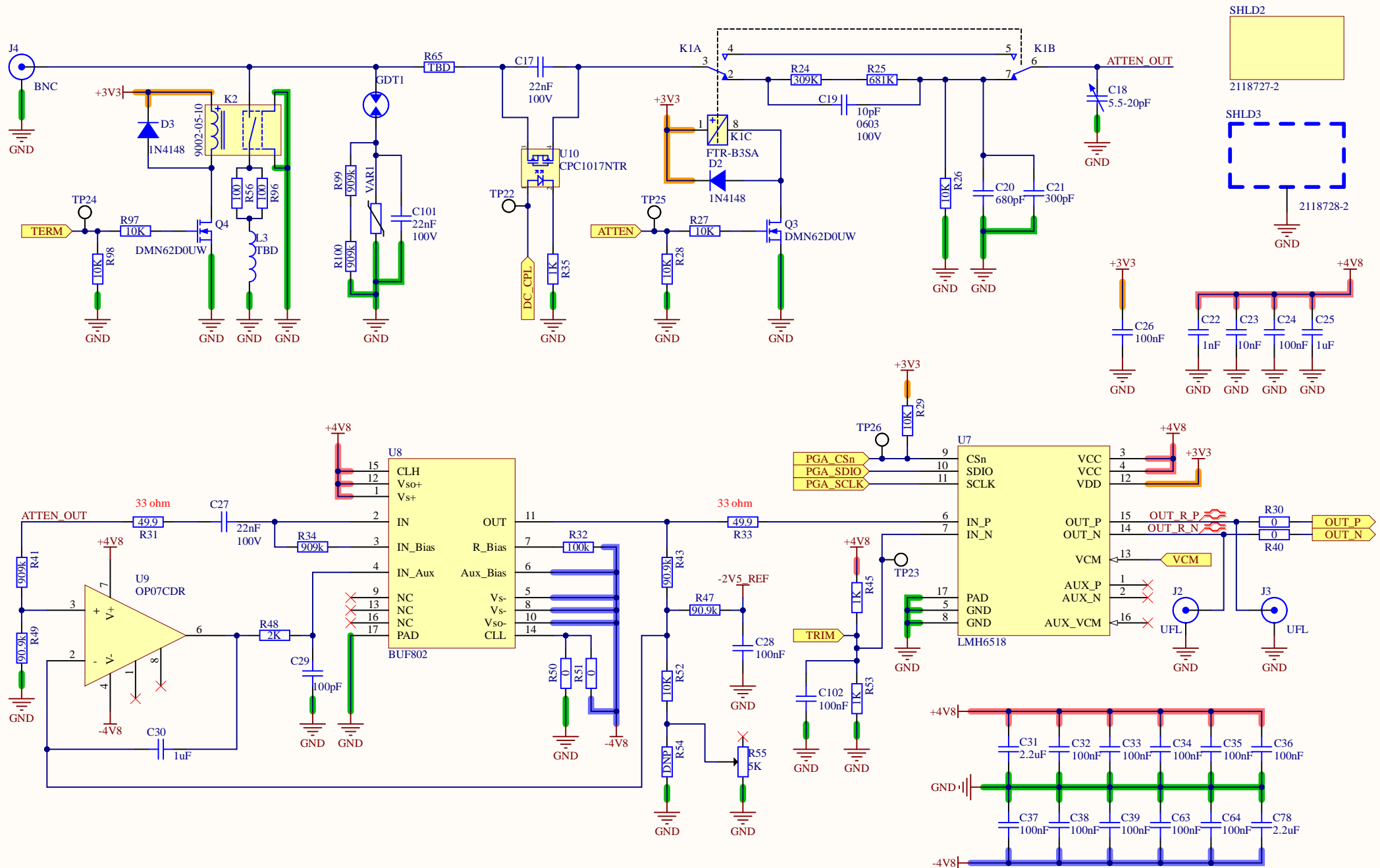
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Size	Number	Revision
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File:	C:\Users\...\ADC.SchDoc	Drawn By: Aleksa Bjelogrić

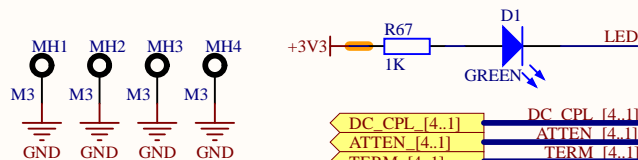
- Nominal values used, dimensions in mm
- The mounting holes and keep-out areas around them are only required when the I/O bracket is mounted on the card directly
- Component height rule and clearance rule derived from PCI_Express_CEM_r2.0.pdf, Page 84.
- Stackup is not specified in PCI_Express_CEM_r2.0.pdf, nor implemented in this template.



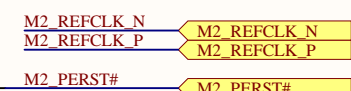
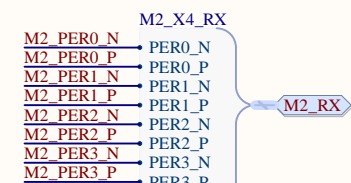
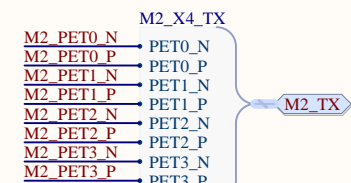
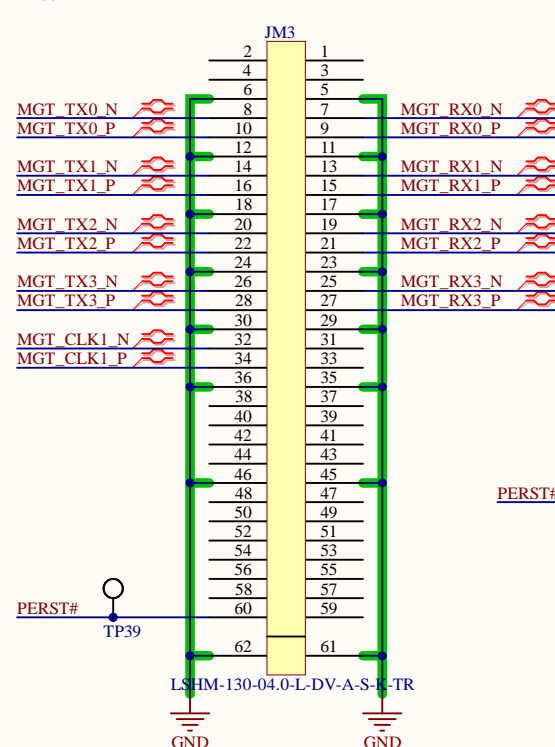
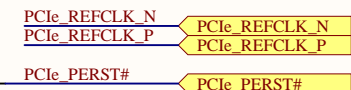
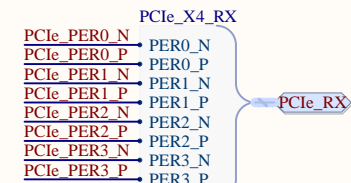
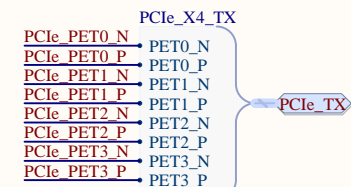
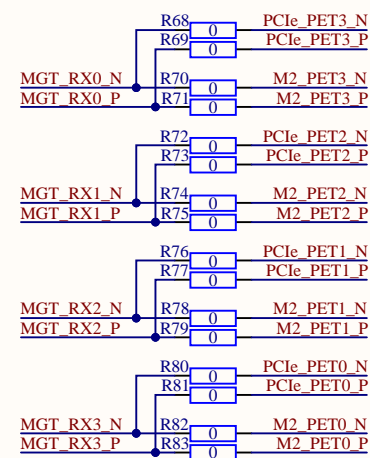
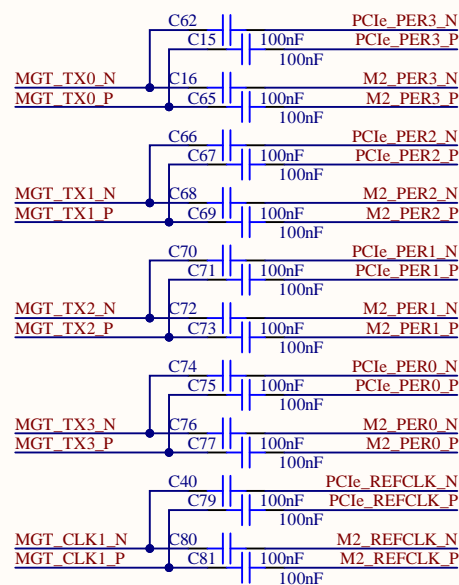
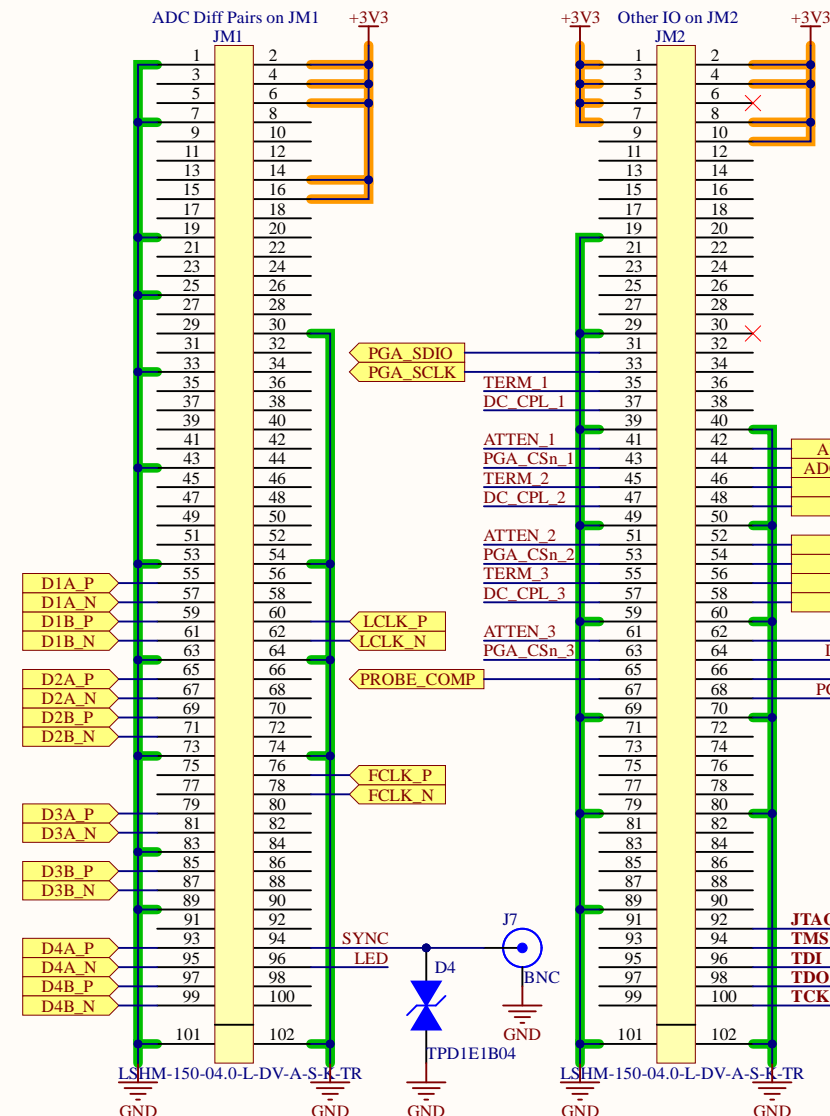


Title		
ThunderScope 1000E		
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Date:	4-13-2022	Sheet of
File:	C:\Users\...\FE.SchDoc	Drawn By: Aleksa Bjelogrić



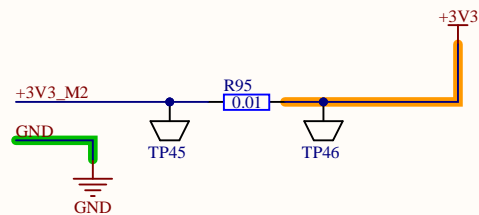
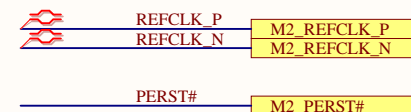
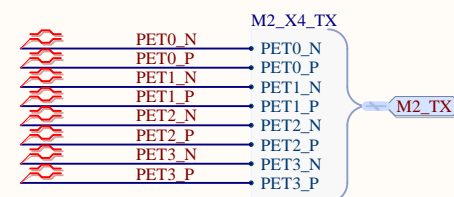
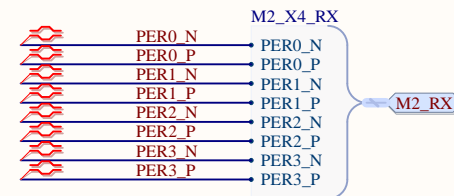
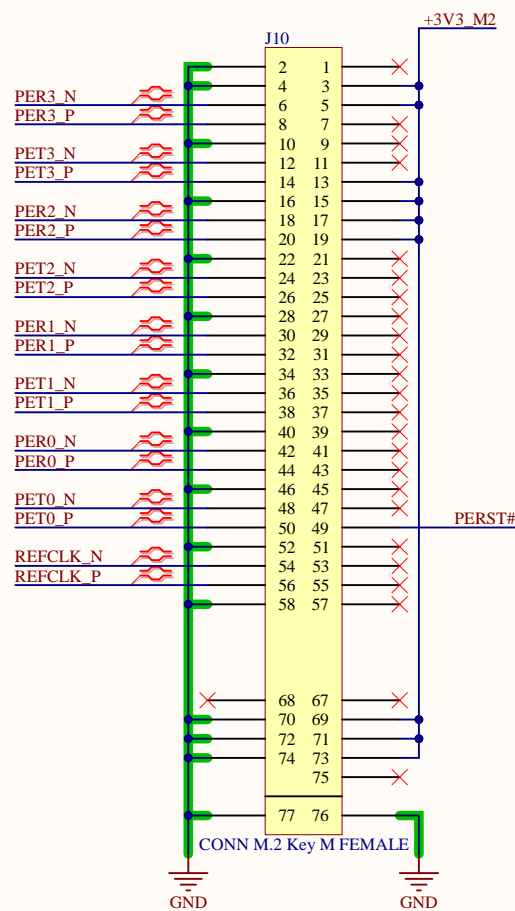


DC_CPL [4..1] DC_CPL [4..1]
 ATTN [4..1] ATTN [4..1]
 TERM [4..1] TERM [4..1]
 PGA_CS[n] [4..1] PGA_CS[n] [4..1]



AC Couple PER Lines with 100nF
 AC Couple REFCLK Lines with 100nF

These connectors are hermaphroditic. Odd pin numbers on the module are connected to even pin numbers on the baseboard and vice versa.

**Main Board
Custom Pinout**

Title		
Size	Number	Revision
A4		
Date:	4-13-2022	Sheet of
File:	C:\Users\...\M2_KEY_M.SchDoc	Drawn By:

Front End

ADC

FPGA Module

SHLD1

9204

PCIe_X4

CON_PCIe_X4.SchDoc

M.2_Key_M

M2_KEY_M.SchDoc

Title
ThunderScope 1000E

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Date: 4-13-2022	Sheet of	
File: C:\Users\...\Main.SchDoc	Drawn By: Aleksa Bjelogrić	

