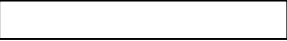



Title			
Block Diagram			
Size	Document Number		Rev
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PCB-2008\_1V1  
Davos REV1.1 6L L109mm W50mm T1.6mm





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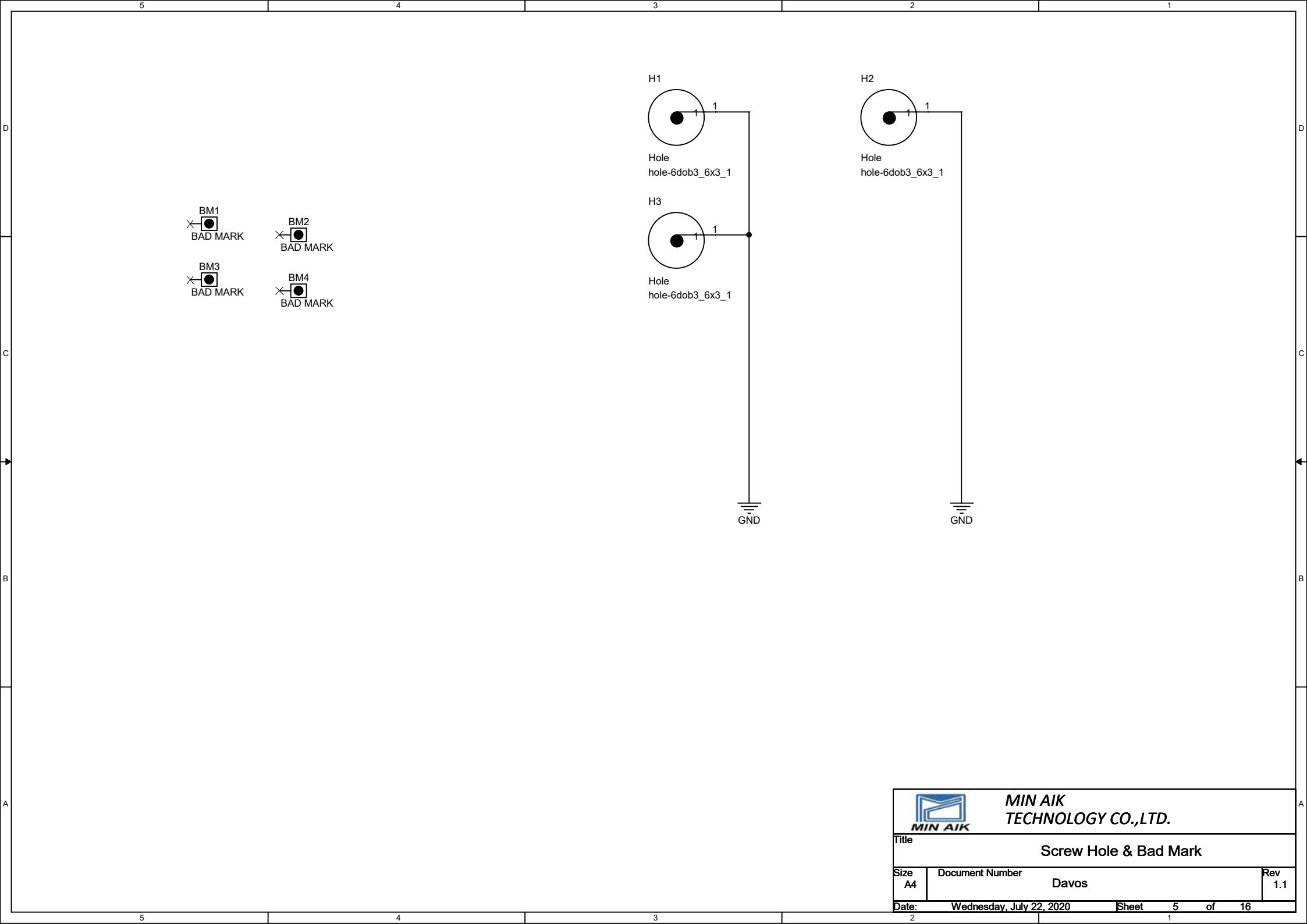
Title		
PCB Dimension		
Size	Document Number	Rev
A4	Davos	1.1
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Stack-Up - FR4 FL-170						Control Impedance																				Via Type	
Layer			Copper		Core/PP	Er (Dk)				Df				Single 50Ω @ 1GHz			Differential 85Ω @ 5GHz (CIO and USB3.1)				Differential 100Ω @ 2GHz (PCIe, DP, MDI, HDMI & USB2)				Reference Plane Layer	TH	
Name	Purpose	Type	Foil [Oz]	Final [mil]	[mil]	@ 1GHz	@ 2GHz	@ 5GHz	@ 10GHz	@ 1GHz	@ 2GHz	@ 5GHz	@ 10GHz	W1 [mil]	D [mil]	Z [Ohm]	W1 [mil]	S [mil]	D [mil]	Z [Ohm]	W1 [mil]	S [mil]	D [mil]	Z [Ohm]		v16c8	
CS	Sig	S	0.5	1.4										11	21	50.36	7.7	4	21	85.54	4.5	4	21	100.2	Ref (L2)		
	7628	CORE			7.00	4.30	4.10	3.90	4.00	0.014	0.015	0.015	0.015														
L2	GND	G	1	1.2																							
	2116	PP			4.6	4.10	4.00	3.90	3.70	0.015	0.016	0.017	0.018														
L3	SigPWR	V	0.5	0.6										6.5	15	49.27					3.5	4	15	99.89	Ref (L2)		
	6x 2116	CORE			30	4.30	4.10	3.90	3.80	0.015	0.015	0.015	0.015														
L4	SigPWR	V	0.5	0.6										6.5	15	49.27					3.5	4	15	99.89	Ref (L5)		
	2116	PP			4.6	4.10	4.00	3.90	3.70	0.015	0.016	0.017	0.018														
L5	GND	G	1	1.2																							
	7628	CORE			7.00	4.30	4.10	3.90	4.00	0.014	0.015	0.015	0.015														
PS	Sig	S	0.5	1.4										11	21	50.36	7.7	4	21	85.54	4.5	4	21	100.2	Ref (L5)		
		Total	4	6.4	53.2																						
		Total	59.6	mil																							
		Total	1.52	mm																							

Remarks

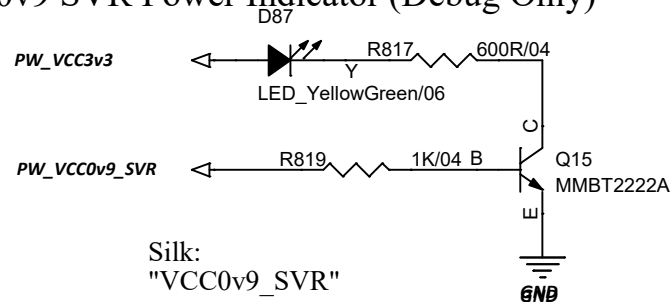
- 1 W means Width of line
- 2 S means Spacing between the differential lines
- 3 D means Distance from other signals
- 4 Assuming W1 = W + 0.5mil for inner layers and W1 = W + 0.75mil for external layers
- 5 Assuming H1 = 0.5mil

Title		
PCB Stack		
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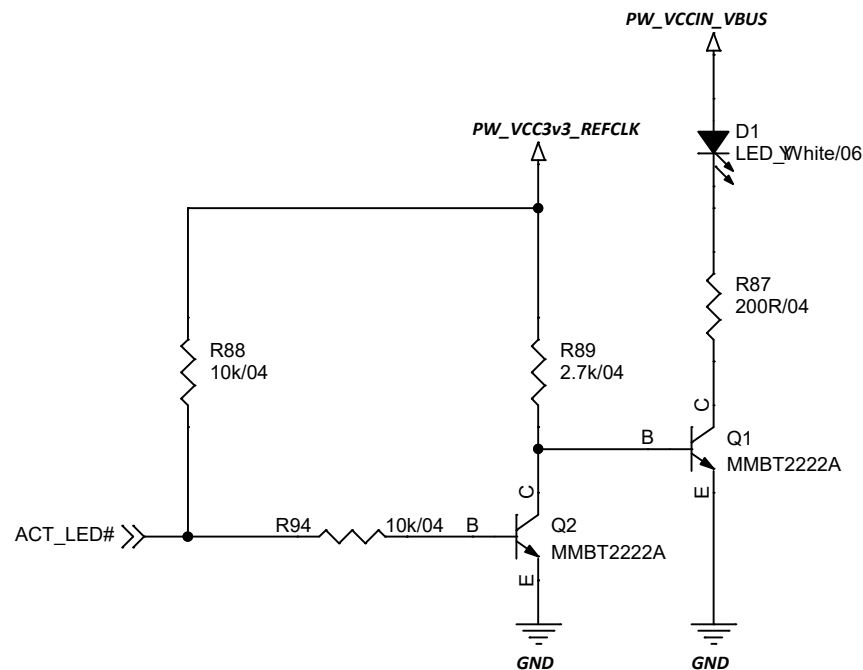
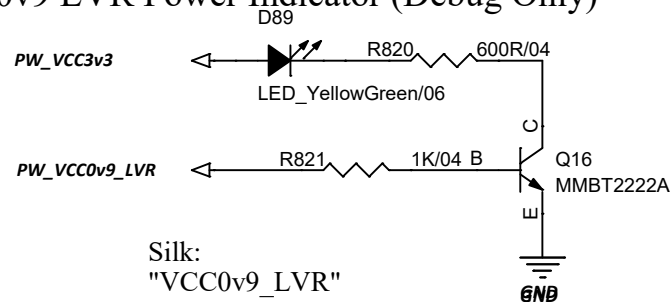


# Debug LEDs

## 0v9 SVR Power Indicator (Debug Only)



## 0v9 LVR Power Indicator (Debug Only)



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Title

Debug LEDs

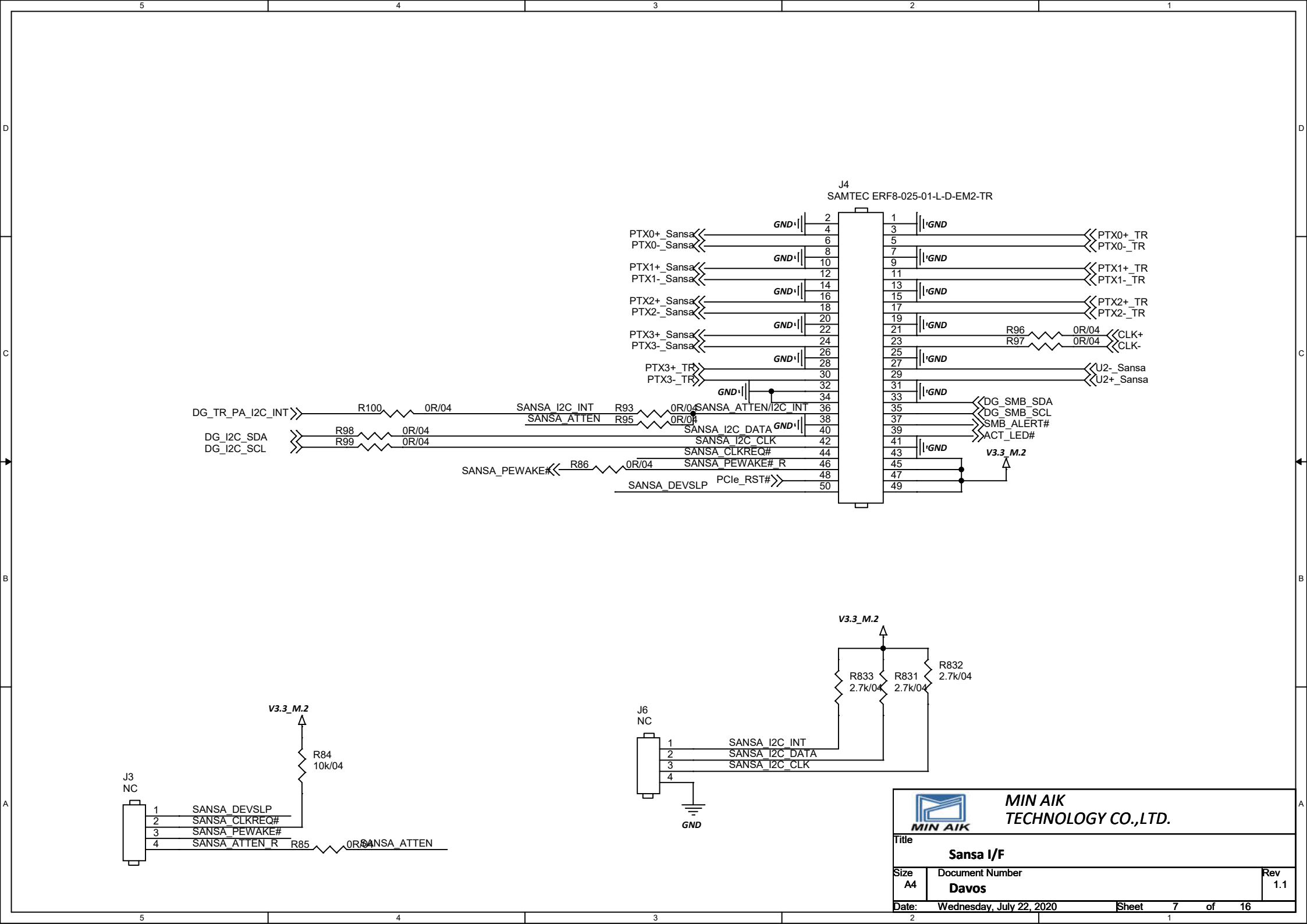
Size  
A

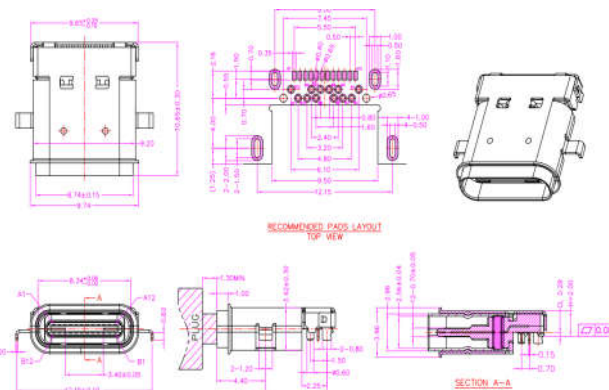
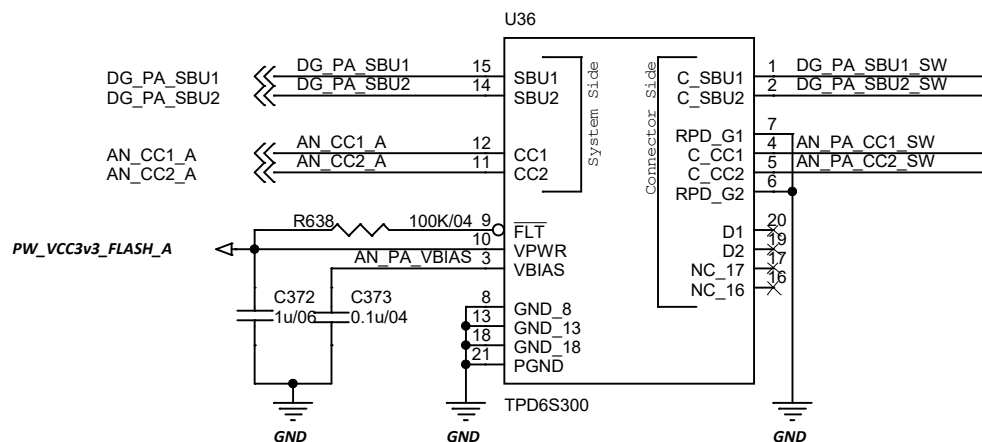
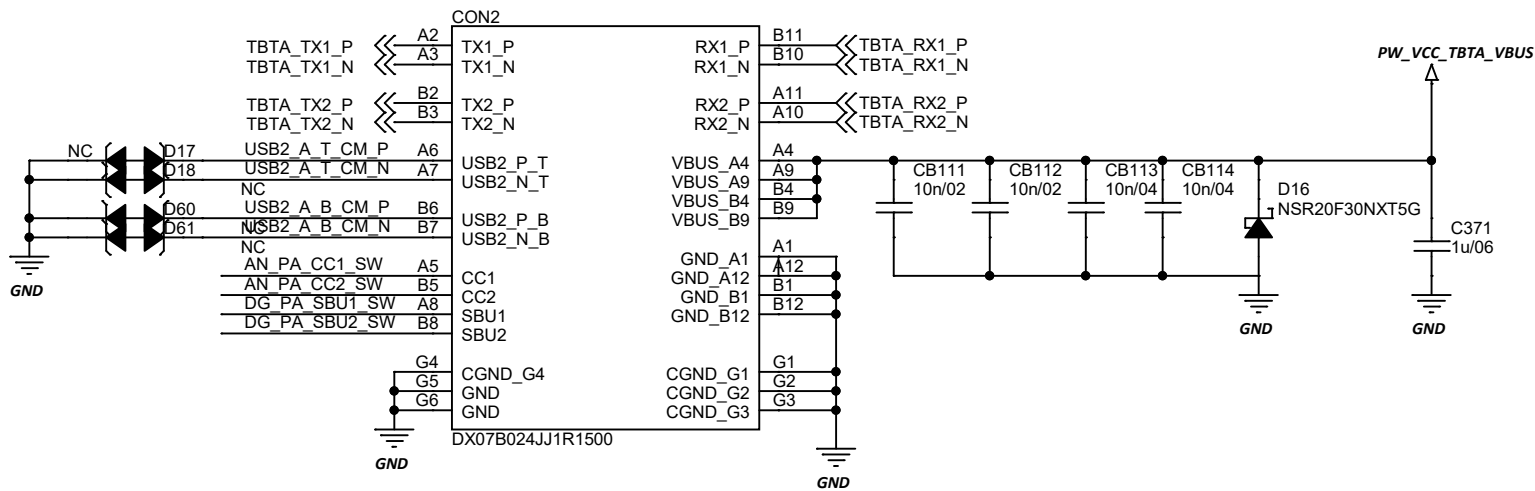
Document Number  
Davos

Rev  
1.1

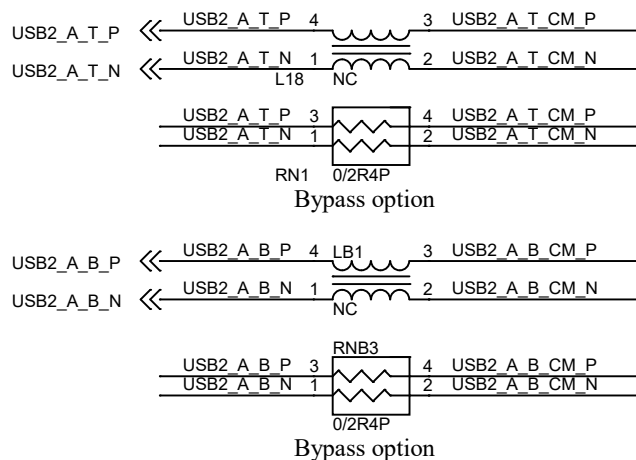
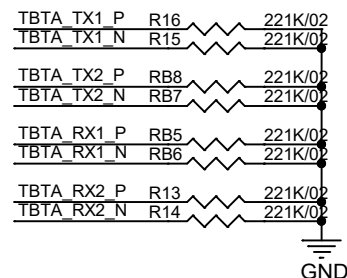
Date: Wednesday, July 22, 2020


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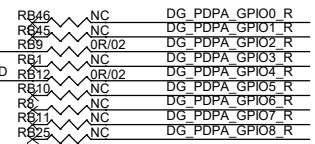
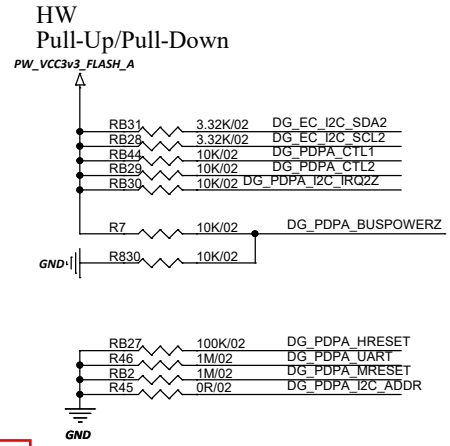
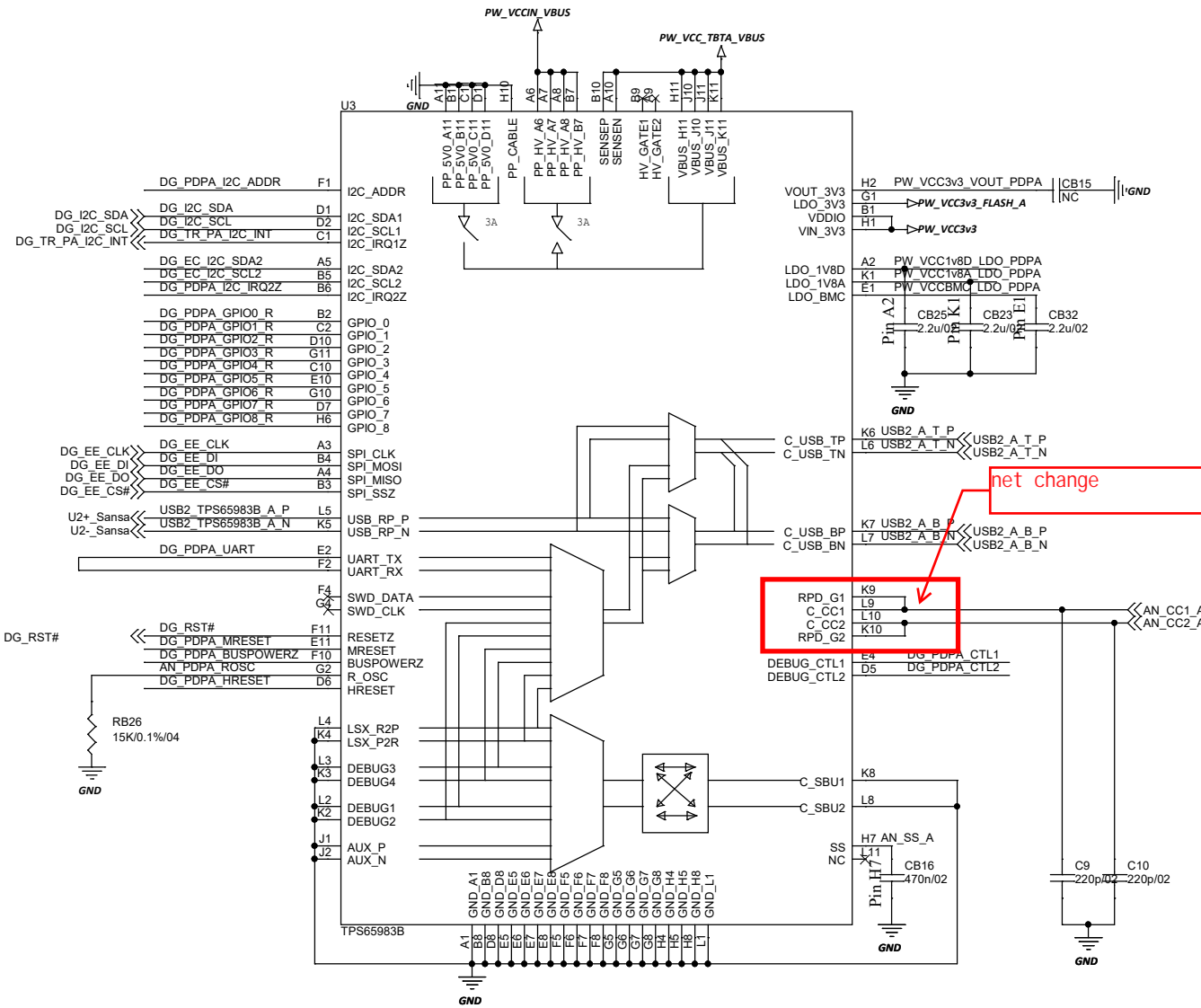


## Bleeding Resistors



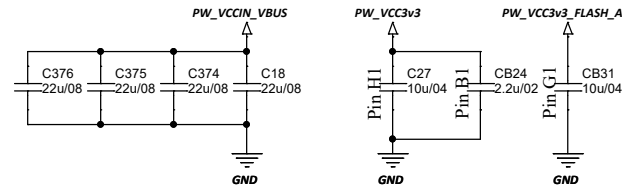
 <b>MIN AIK</b>		<b>MIN AIK TECHNOLOGY CO.,LTD.</b>	
Title			
<b>Thunderbolt Port</b>			
Size A4	Document Number <b>Davos</b>		Rev 1.1
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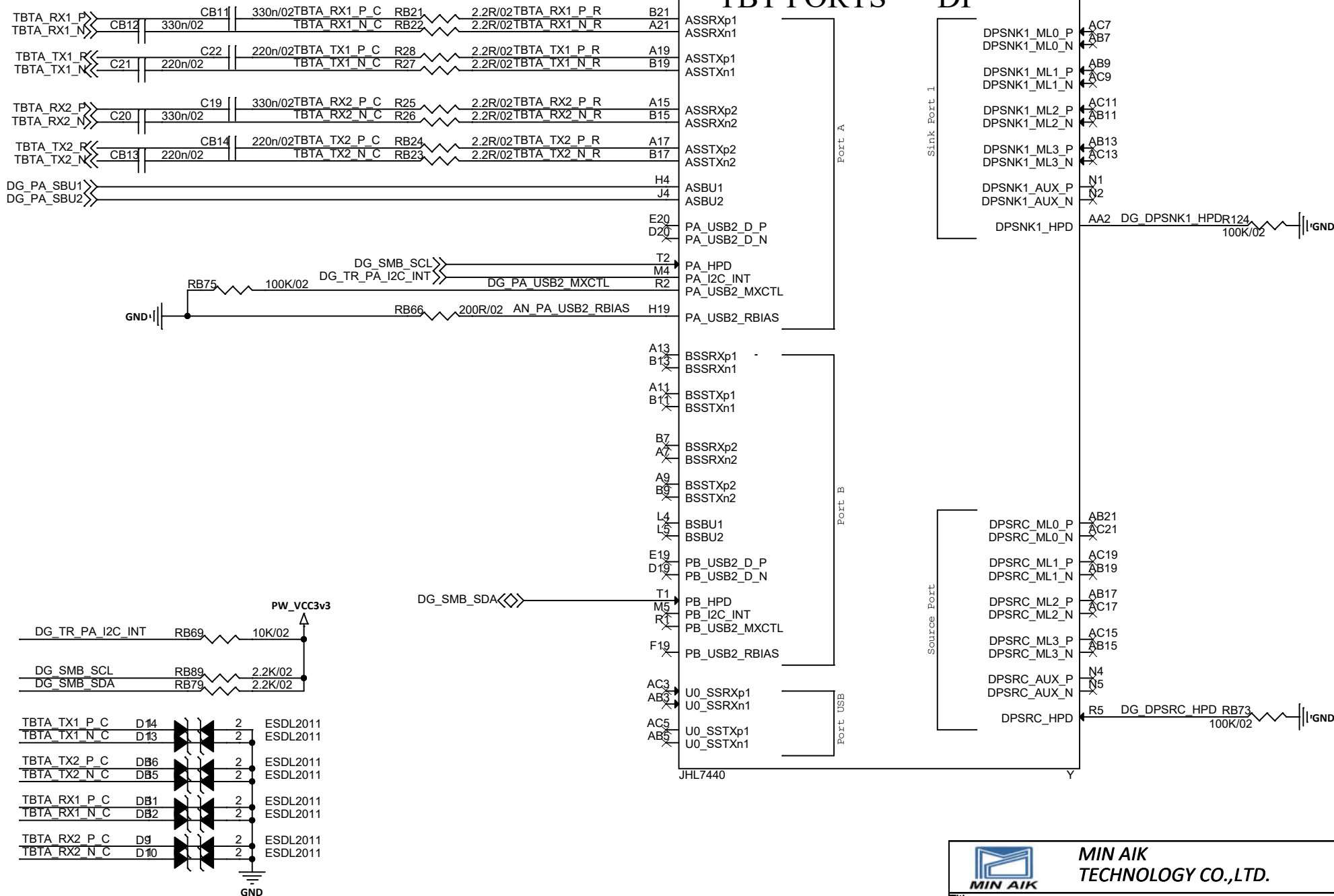



BPD:  
DG\_PDPA\_BUSPOWERZ = 1.65v bit2: DG\_PDPA\_I2C\_ADDR ('0')  
RPD\_G1 = CC1  
RPD\_G2 = CC2

Primary TPS65983 I2C Address:  
bit2: DG\_PDPA\_I2C\_ADDR ('0')  
bit1: DG\_PDPA\_CTL1 ('1')  
bit0: DG\_PDPA\_CTL2 ('1')

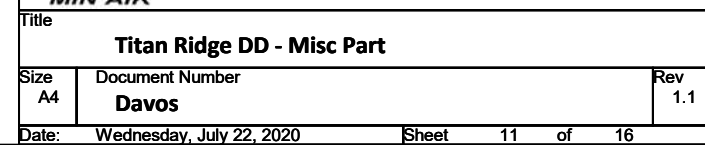


Z=85 ohm

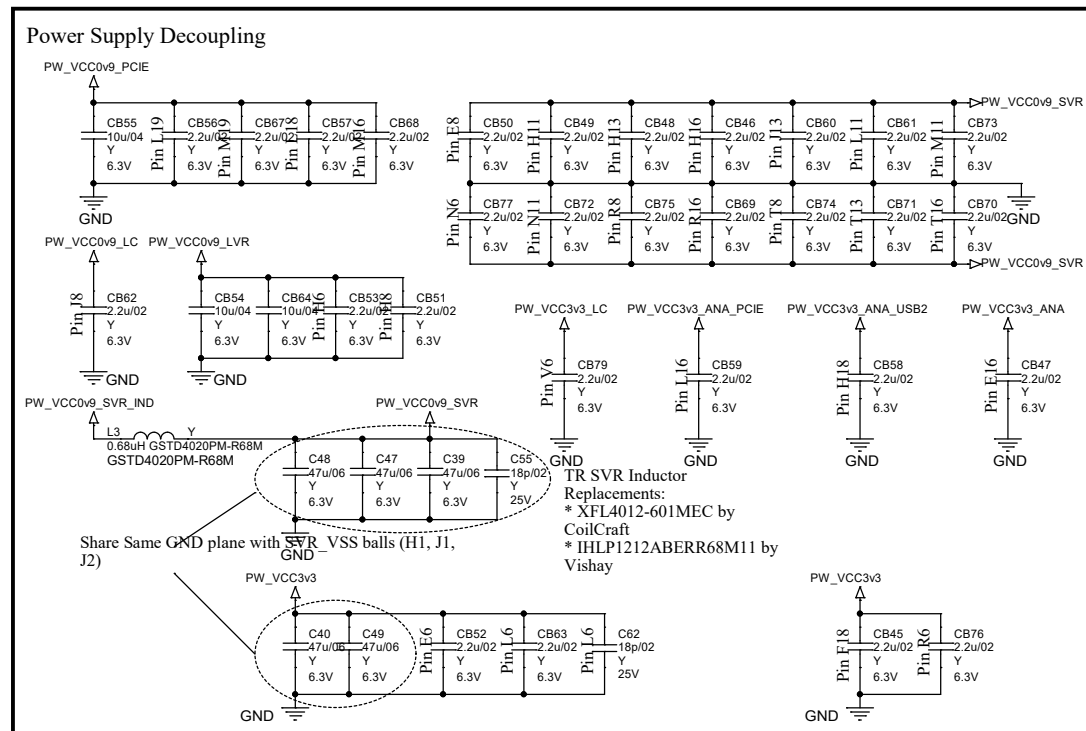
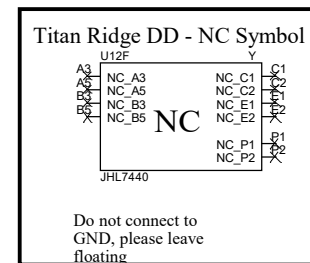
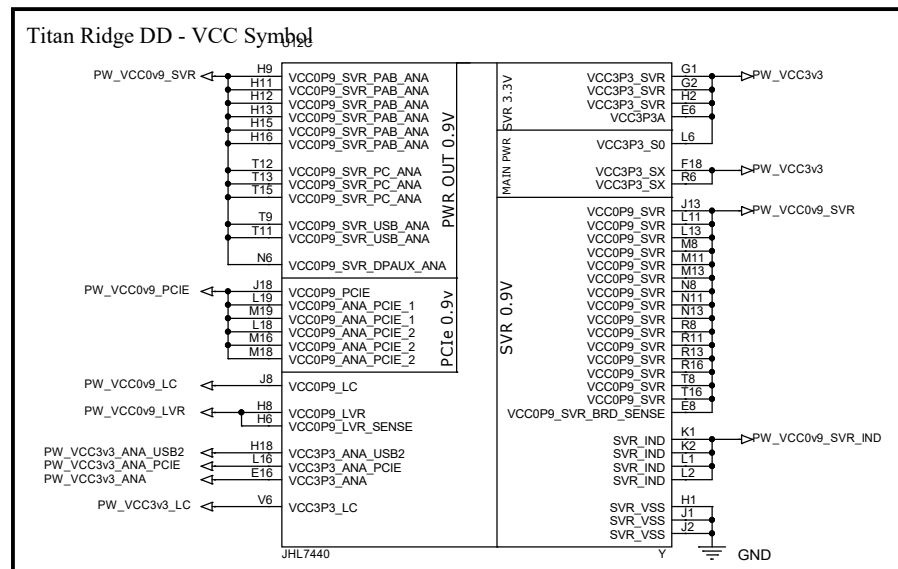
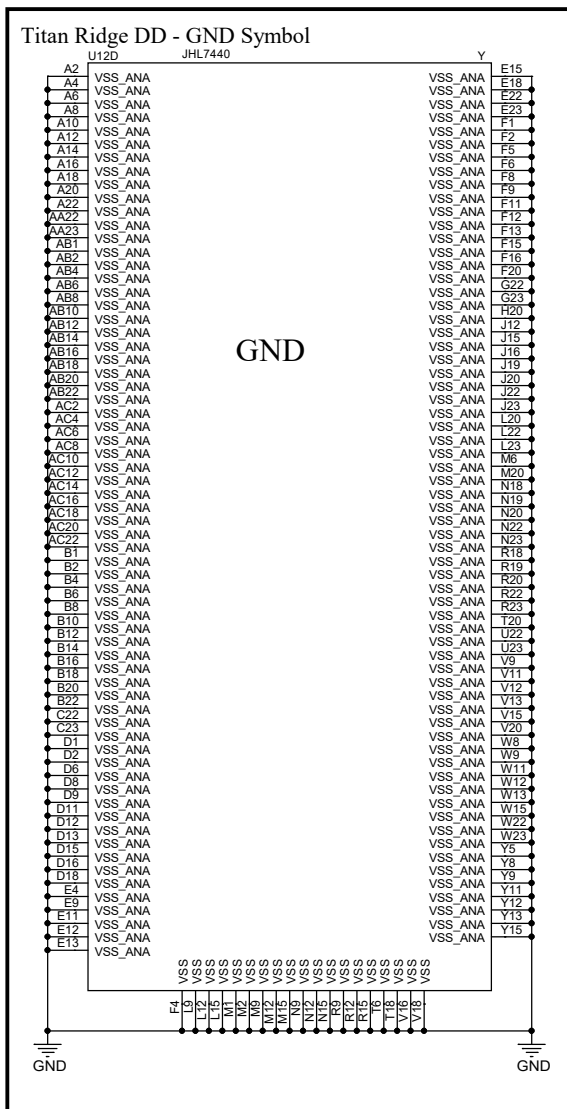


 <b>MIN AIK TECHNOLOGY CO.,LTD.</b>		
Title <b>Titan Ridge DD - High Speed</b>		
Size <b>A4</b>	Document Number <b>Davos</b>	Rev <b>1.1</b>
Date: <b>Wednesday, July 22, 2020</b> Sheet <b>10</b> of <b>16</b>		

## Titan Ridge DD - Misc Symbol



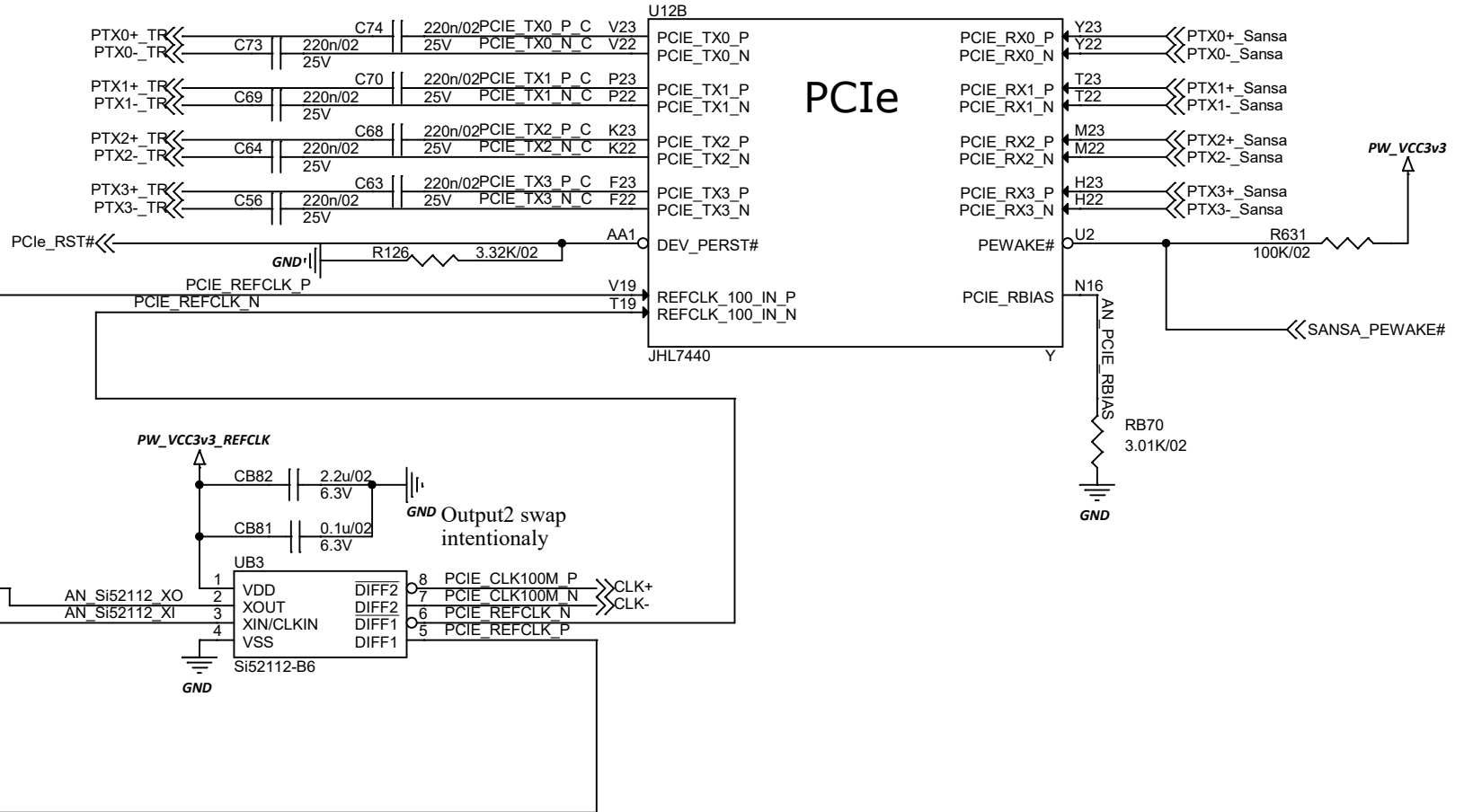
## Titan Ridge DD - Power Supply & GND Parts



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<b>Title</b> <b>Titan Ridge DD - Power Supply &amp; GND Parts</b>			
<b>Size</b> <b>A3</b>	<b>Document Number</b> <b>Davos</b>	<b>Rev</b> <b>1.1</b>	
<b>Date:</b> Wednesday, July 22, 2020		<b>Sheet</b> 12	<b>of</b> 16

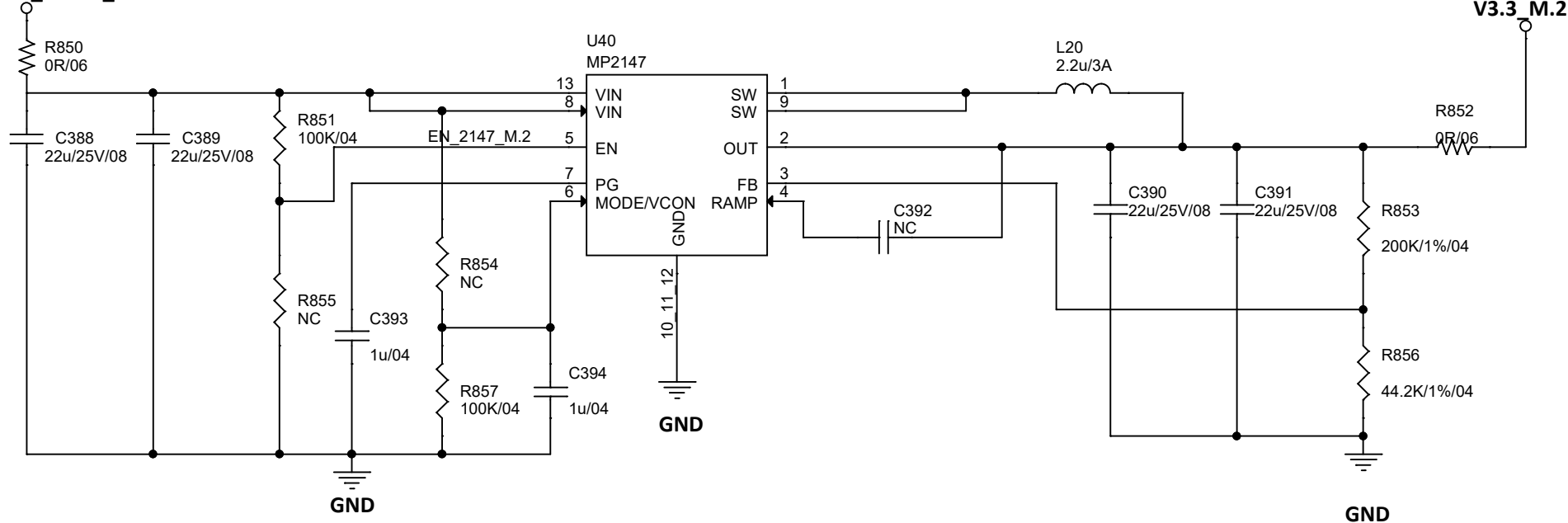
Z=100 ohm



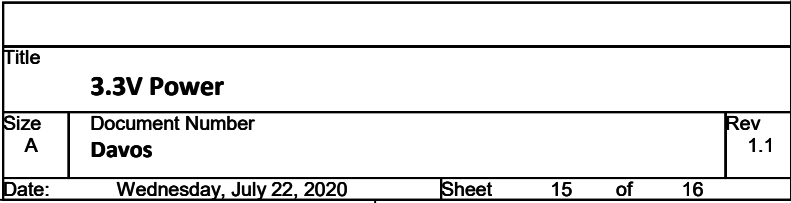
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Title		
Clk Generator, TR PCIe Part		
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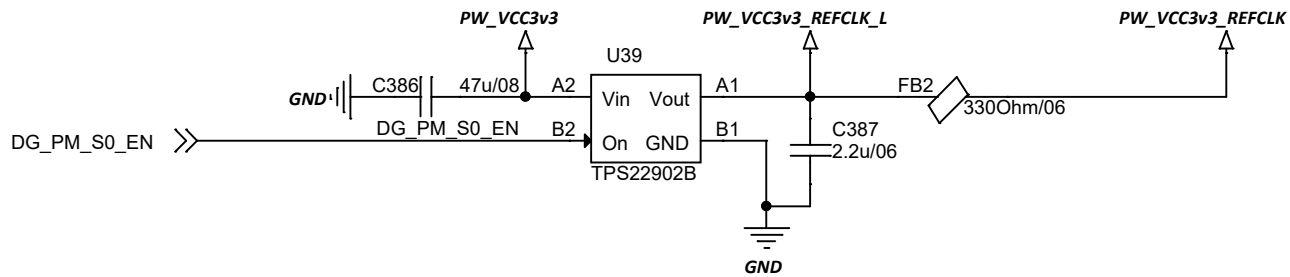
PW\_VCCIN\_VBUS



Title		
3.3V Power M.2		
Size A	Document Number Sansa	Rev 1.1
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### 3v3 Ref Clock Supply



Title			
3.3V Power			
Size A	Document Number Davos		Rev 1.1
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