

License: GNU General Public License, version 2

Copyright © 2013 Jared Boone

ShareBrained Technology, Inc.

Sheet: /

File: main_board.sch

Title: Daisio Project Main Board

Size: A3 Date: 10 Oct 2014

KiCad E.D.A. eeschema (2014-03-01 BZR 4730) -product

Rev: 0

Id: 1/15

ULPI_CLKD
 ULPI_DATA[7..0]
 ULPI_DIRD
 ULPI_STPD
 ULPI_NXTD
 PIPE_OUT_ENABLE
 PIPE_TX_MARGIN[2..0]
 PIPE_TX_DETRX_LPBK
 PIPE_TX_SWING
 PIPE_TX_ONESZEROS
 PIPE_TX_ELECIDLE
 PIPE_RATE
 PIPE_PHY_RESETN

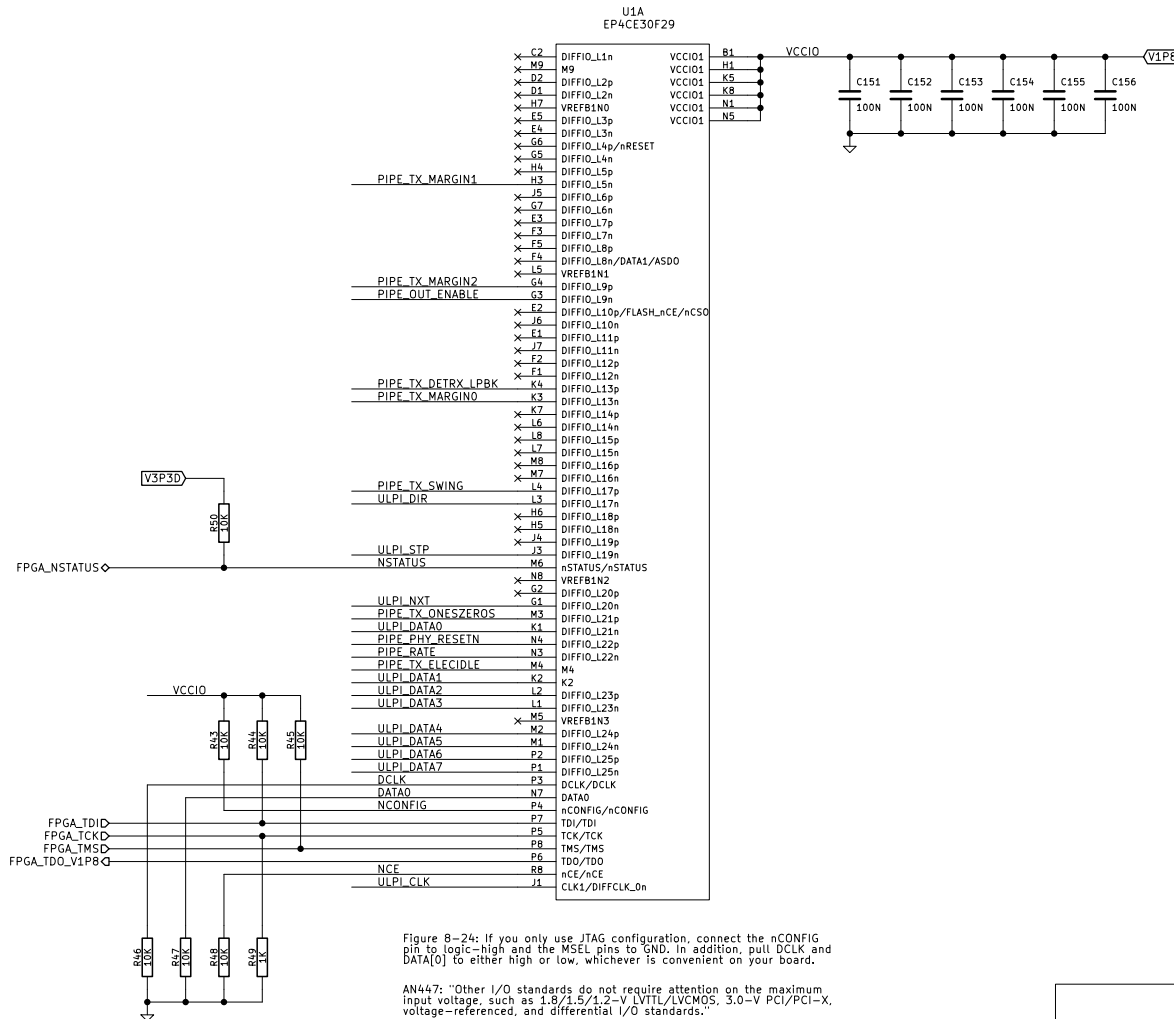


Figure 8-24: If you only use JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.

AN447: "Other I/O standards do not require attention on the maximum input voltage, such as 1.8/1.5/1.2-V LVTTTL/LVCMOS, 3.0-V PCI/PCI-X, voltage-referenced, and differential I/O standards."

License: GNU General Public License, version 2

Copyright © 2013 Jared Boone

ShareBrained Technology, Inc.

Sheet: /fpga_configuration/

File: fpga_configuration.sch

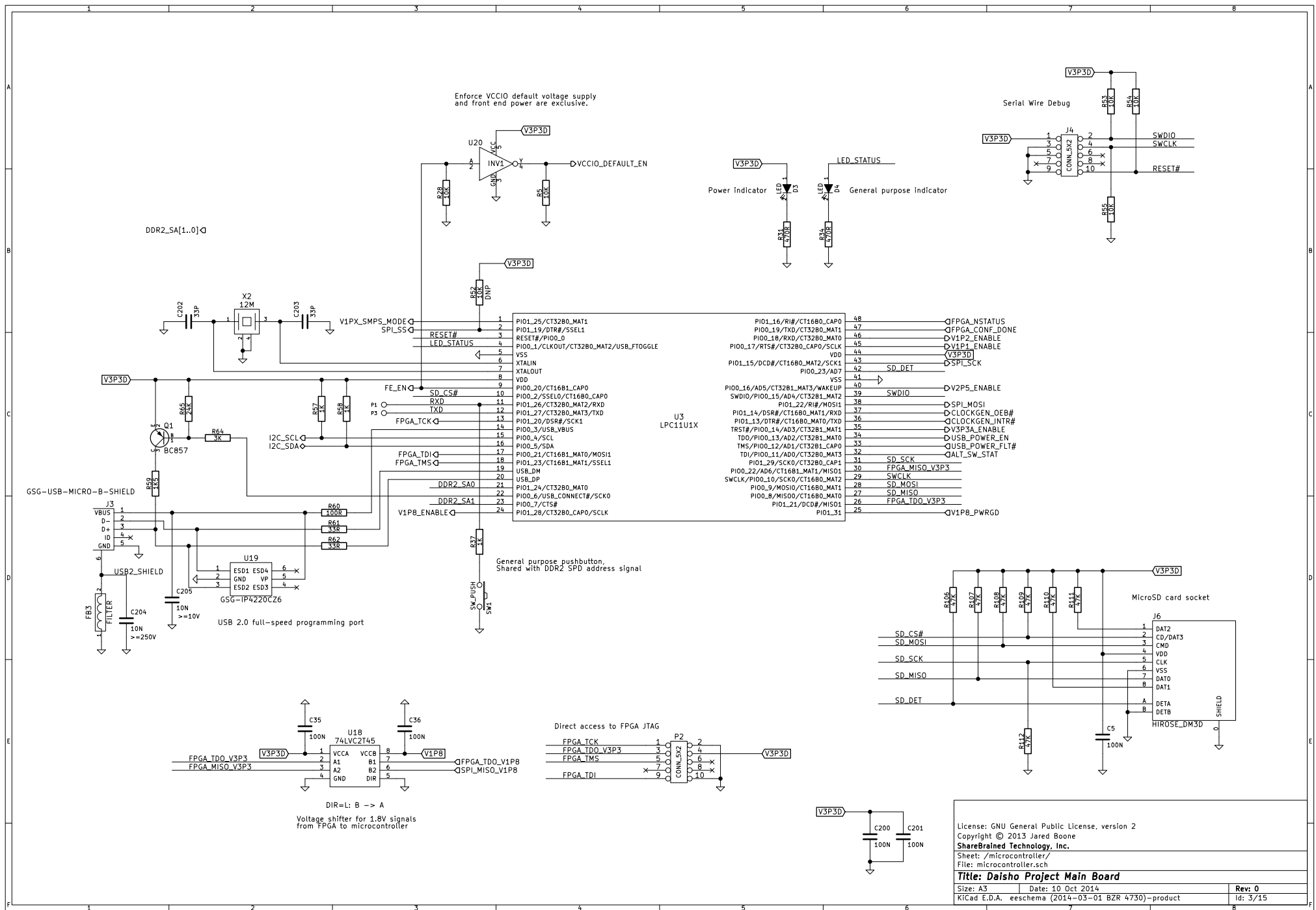
Title: **Dalsho Project Main Board**

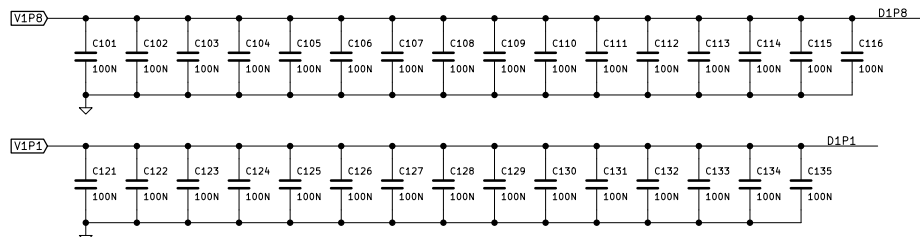
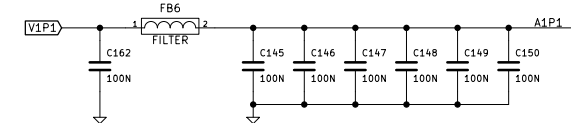
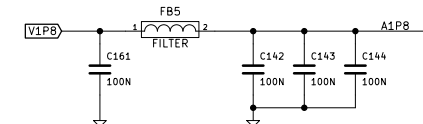
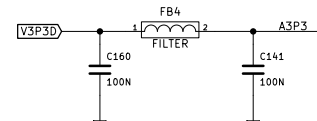
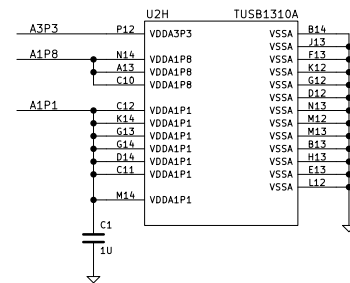
Size: A3 Date: 10 Oct 2014

KiCad E.D.A. eeschema (2014-03-01 BZR 4730) -product

Rev: 0

Id: 2/15



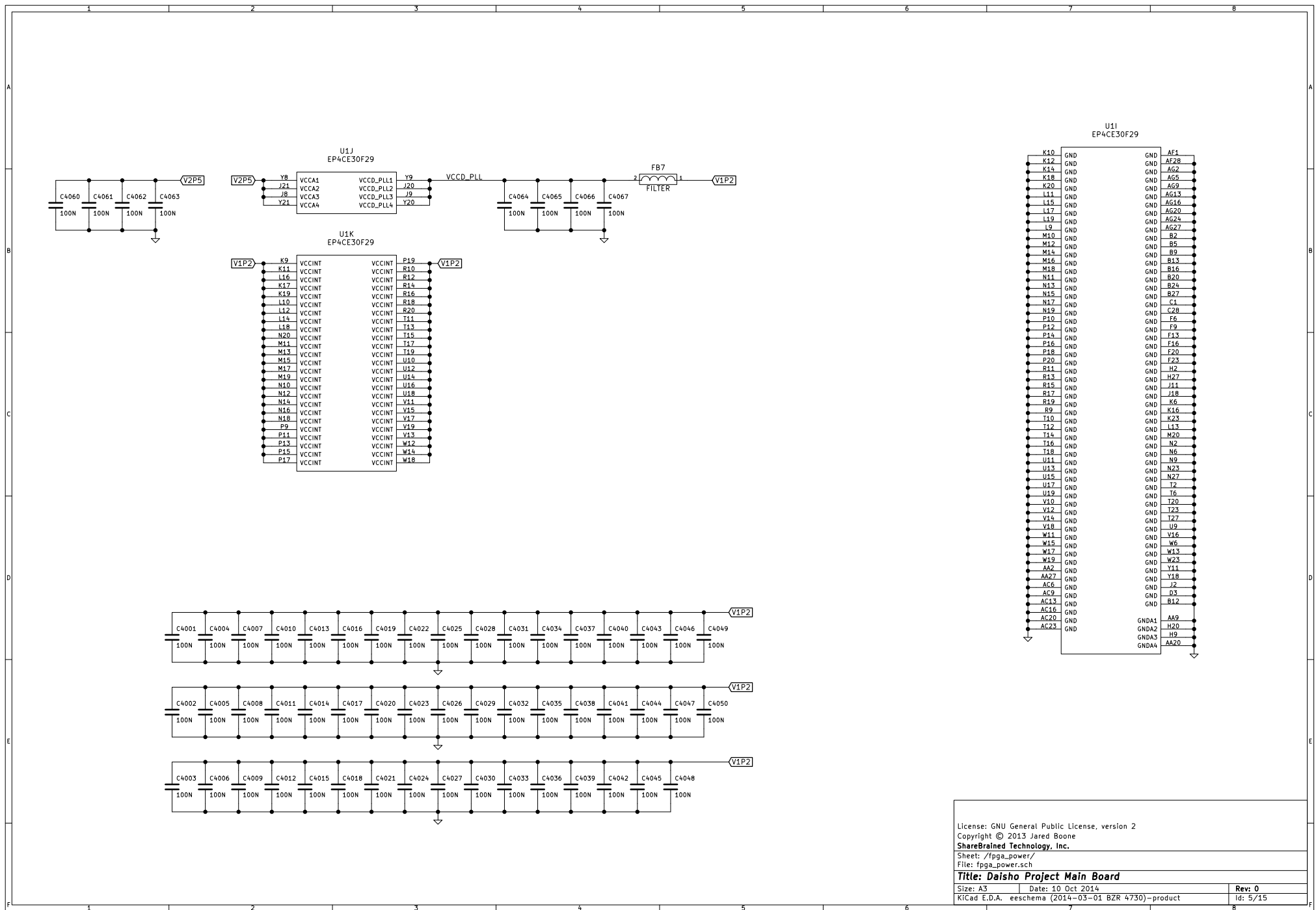


License: GNU General Public License, version 2
Copyright © 2013 Jared Boone
ShareBrained Technology, Inc.
Sheet: /usb0_power/
File: usb0_power.sch

Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product	

Rev: 0
Id: 4/15



License: GNU General Public License, version 2

Copyright © 2013 Jared Boone

ShareBrained Technology, Inc.

Sheet: /fpga_power/

File: fpga_power.sch

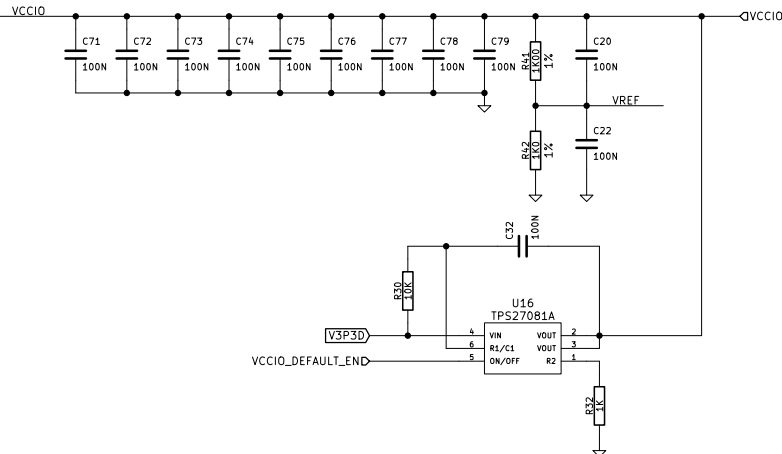
Title: Daisio Project Main Board

Size: A3 Date: 10 Oct 2014
KiCad E.D.A. eeschema (2014-03-01 BZR 4730) -product

Rev: 0
Id: 5/15

D[51..0]◊

U1H EP4CE30F29			
D23	A14	CLK10/DIFFCLK_4n	VCCIOB A2
D21	B14	CLK11/DIFFCLK_4p	VCCIOB A5
D12	C13	DIFFIO_T26n	VCCIOB A9
D10	D13	DIFFIO_T26p	VCCIOB A13
D9	C14	DIFFIO_T25n	VCCIOB E6
D7	D14	DIFFIO_T25p/PADD15	VCCIOB E9
D18	C12	DIFFIO_T24n/PADD16	VCCIOB E13
D16	D12	DIFFIO_T24p/PADD17	VCCIOB H11
D25	A12	DIFFIO_T23n	VCCIOB J13
VREF	G14	VREFB8N0	
	✕ K13	DIFFIO_T22n	
D4	✕ F14	DIFFIO_T22p	
	E14		
	✕ J12	DIFFIO_T21n	
	✕ J12	DIFFIO_T21p	
D29	A11	DIFFIO_T20n/DATA2	
D27	B11	DIFFIO_T20p/DATA3	
D33	A10	DIFFIO_T19n/PADD18	
D31	B10	DIFFIO_T19p/DATA4	
	✕ G13	DIFFIO_T18n/PADD19	
	✕ H13	DIFFIO_T18p/DATA15	
D37	B8	DIFFIO_T17n	
D24	C10	DIFFIO_T17p	
D22	D11	D11	
VREF	F11	VREFB8N1	
D3	E12	DIFFIO_T16n/DATA14	
D1	F12	DIFFIO_T16p/DATA13	
D13	D10	DIFFIO_T15n	
D11	F10	DIFFIO_T15p	
D2	E11	DIFFIO_T14n	
D0	E8	DIFFIO_T14p	
D8	E10	DIFFIO_T13n	
D6	E7	DIFFIO_T13p	
D39	A7	DIFFIO_T12p	
D14	G10	DIFFIO_T12p	
	✕ G11	DIFFIO_T11n	
D45	B7	DIFFIO_T11p/DATA5	
D51	B3	DIFFIO_T10n	
	✕ J10	DIFFIO_T10p	
D19	✕ F8	DIFFIO_T9n	
D17	F7	DIFFIO_T9p	
VREF	G12	VREFB8N2	
D43	A6	DIFFIO_T8n	
D41	B6	DIFFIO_T8p/DATA6	
D20	C11	DIFFIO_T7h/DATA7	
	✕ H10	DIFFIO_T7p	
D34	G8		
D28	C9	DIFFIO_T6n	
D26	D9	DIFFIO_T6p/DATA8	
D35	A8	DIFFIO_T5n/DATA9	
D5	C8	DIFFIO_T5p	
D15	D8		
D32	C7	DIFFIO_T4n/DATA10	
D30	D7	DIFFIO_T4p/DATA11	
VREF	G9	VREFB8N3	
D36	D6		
D49	A4	DIFFIO_T3n	
D47	B4	DIFFIO_T3p/DATA12	
D50	A3	DIFFIO_T2n	
D38	C6	DIFFIO_T2p	
	✕ H8	DIFFIO_T1n	
D44	C4	DIFFIO_T1p	
D46	D4		
D42	C5	PLL3_CLKOUTn	
D40	D5	PLL3_CLKOUTp	
D48	C3		



License: GNU General Public License, version 2

Copyright © 2013 Jared Boone

ShareBrained Technology, Inc.

Sheet: /fpga_front_end_bank_c/

File: fpga_front_end_bank_c.sch

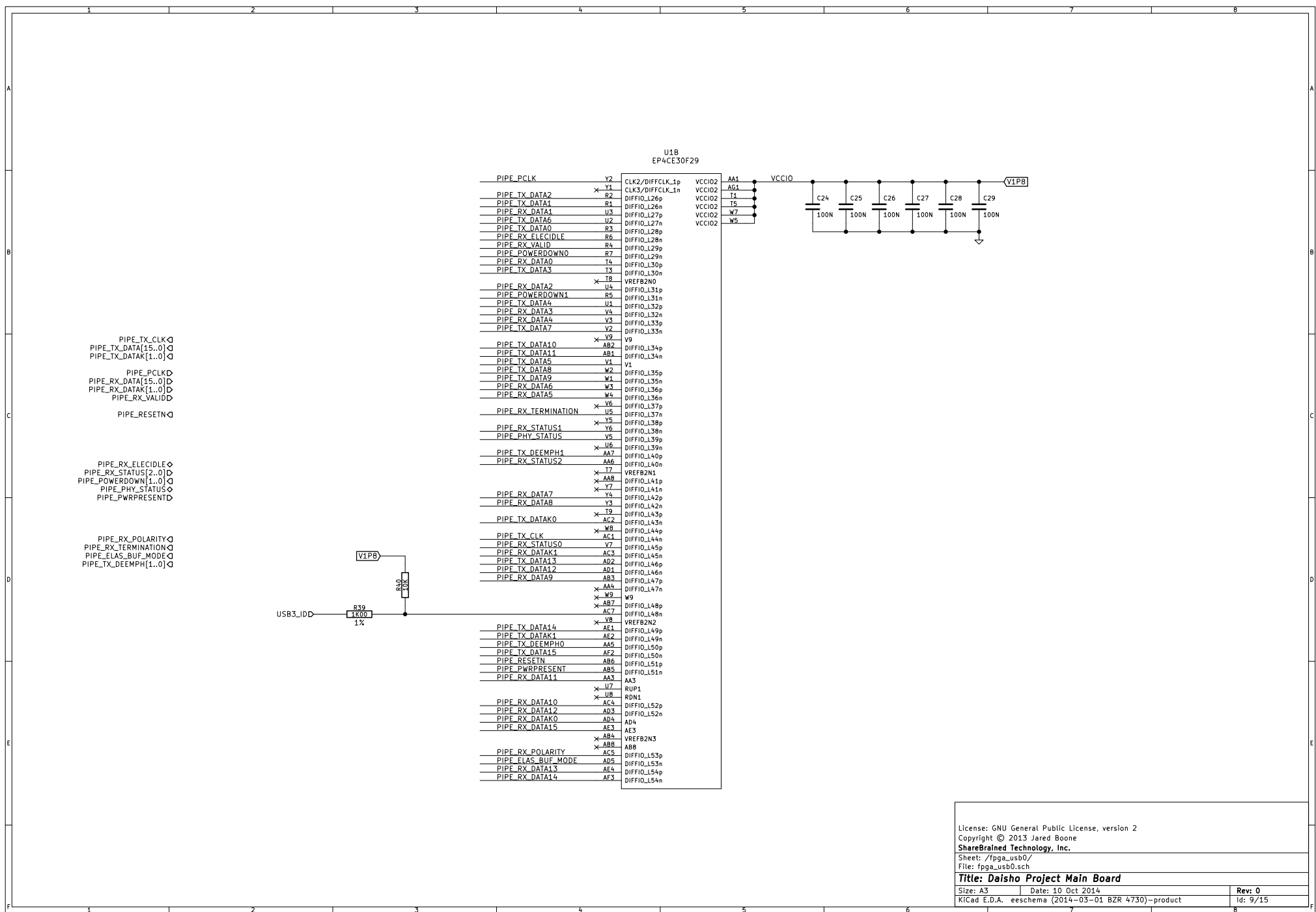
Title: Daisio Project Main Board

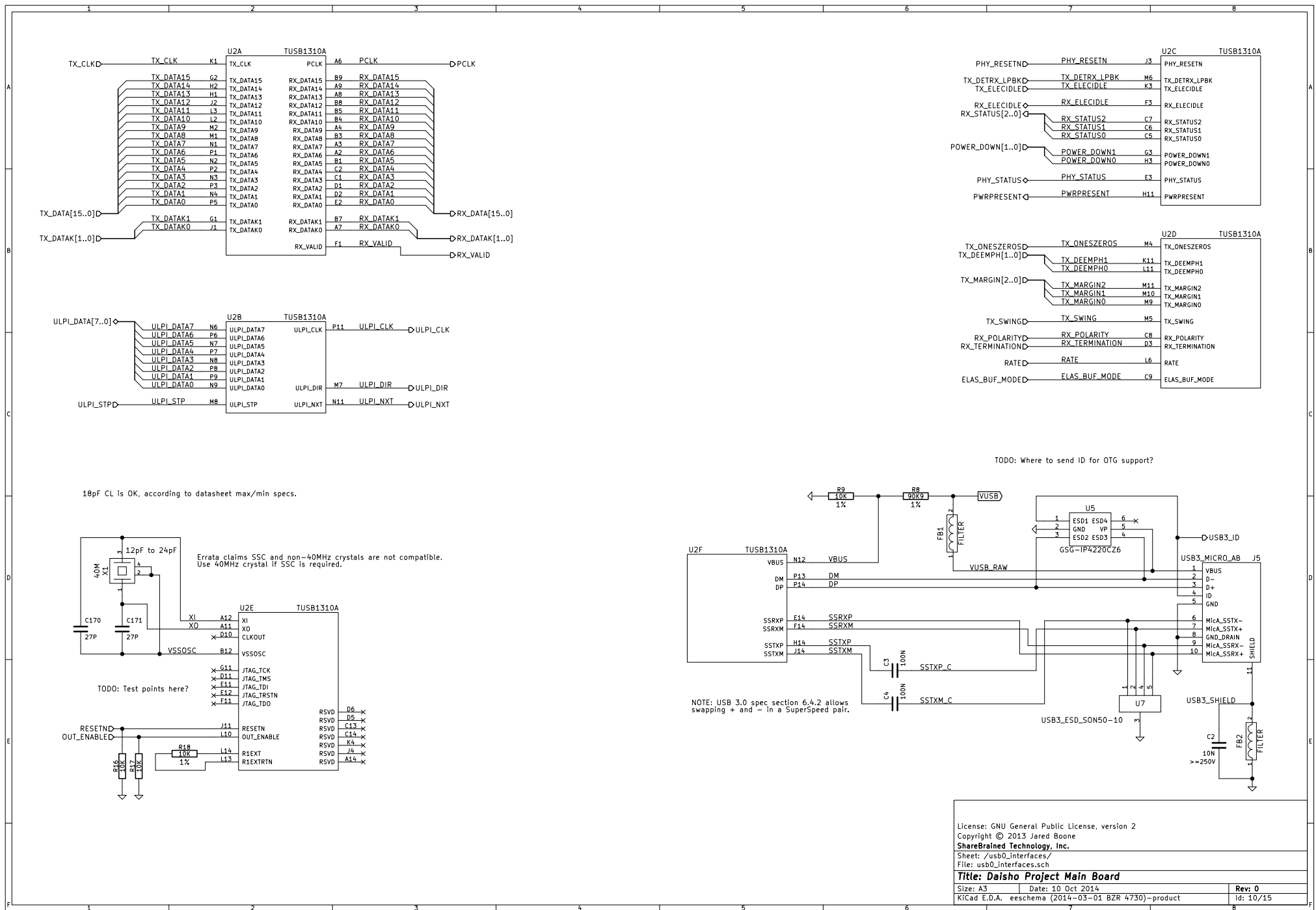
Size: A3 Date: 10 Oct 2014

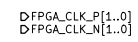
KiCad E.D.A. eeschema (2014-03-01 BZR 4730) -product

Rev: 0

Id: 8/15



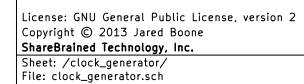




```

D>FE_CLK_P[1..0]
D>FE_CLK_N[1..0]

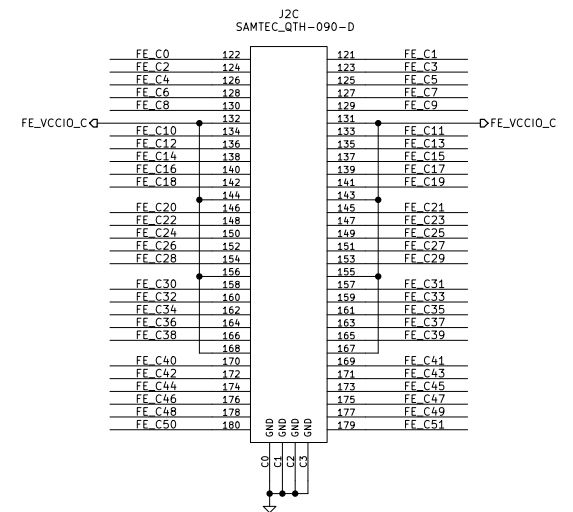
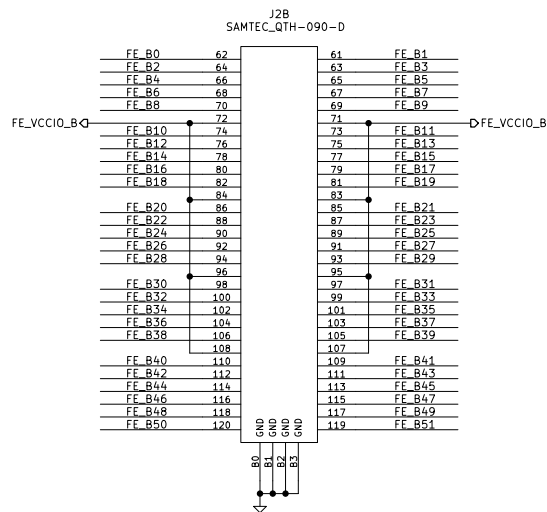
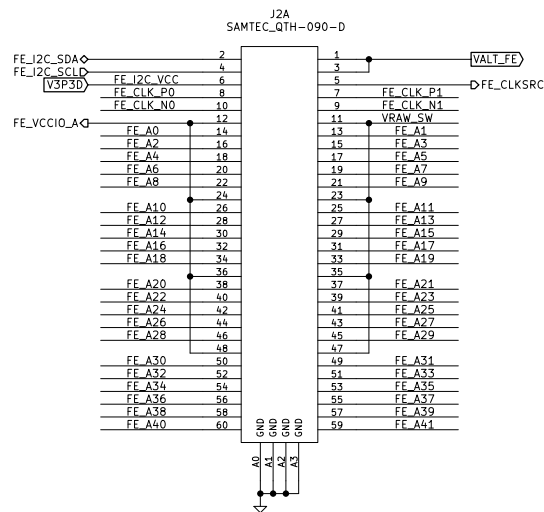
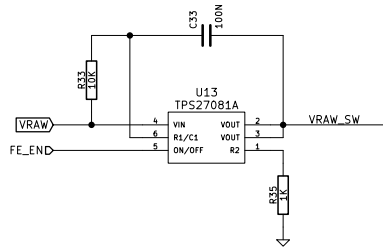
```



Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	Rev: 0
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 11/15

FE_A[41..0]◇
FE_B[51..0]◇
FE_C[51..0]◇
FE_CLK_P[1..0]D
FE_CLK_N[1..0]D



Ground unused pins at front-end side, assuming FPGA will be configured not to drive those pins?

Ground unused pins at FPGA to ensure low impedance to ground?

License: GNU General Public License, version 2

Copyright © 2013 Jared Boone

ShareBrained Technology, Inc.

Sheet: /front_end/

File: front_end.sch

Title: Daisho Project Main Board

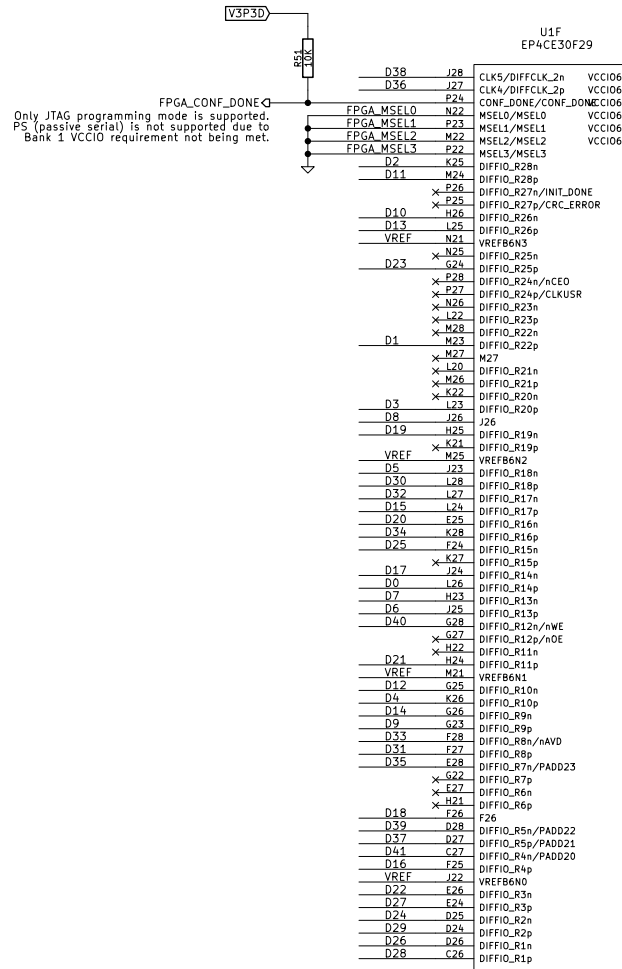
Size: A3 Date: 10 Oct 2014

KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product

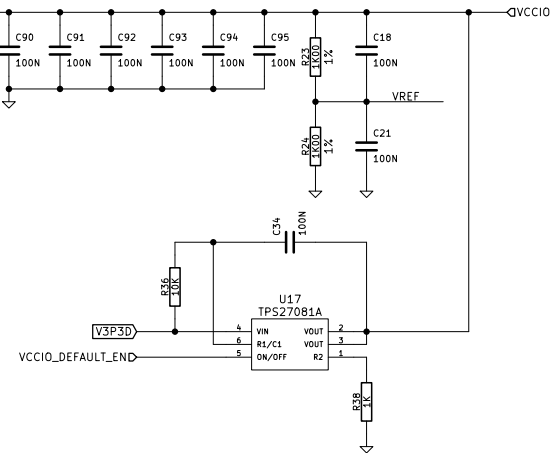
Rev: 0

Id: 12/15

D[41..0]◇



AN592: "The VREF pin is used mainly for voltage bias and does not source or sink much current. You can create the voltage with a regulator or resistor divider network."



nCEO, INIT_DONE, CRC_ERROR driven during configuration.

INIT_DONE is open-drain during configuration, only if INIT_DONE output is enabled in bitstream.
CRC_ERROR is open-drain during configuration, only if bitstream CRC error detection is enabled.

nCEO is open-drain during configuration.

Avoid use of VREF pins as I/O, as they have higher pin capacitance, and therefore are slow down both input and output signals.

License: GNU General Public License, version 2

Copyright © 2013 Jared Boone

ShareBrained Technology, Inc.

Sheet: /fpga_front_end_misc/

File: fpga_front_end_misc.sch

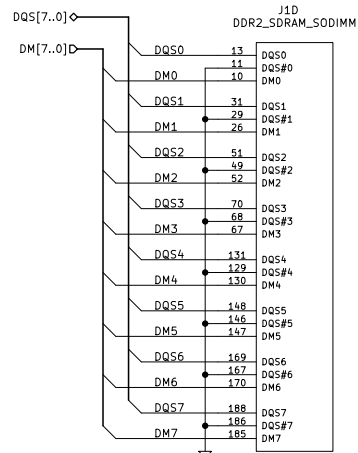
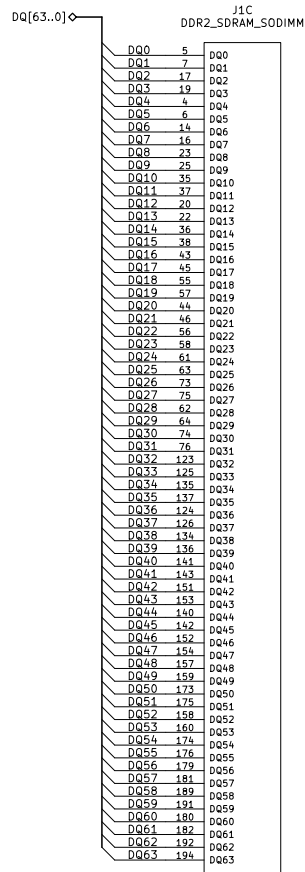
Title: Daisio Project Main Board

Size: A3 Date: 10 Oct 2014

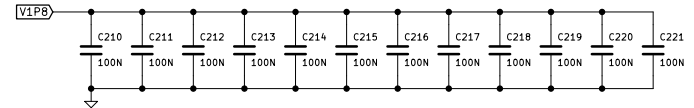
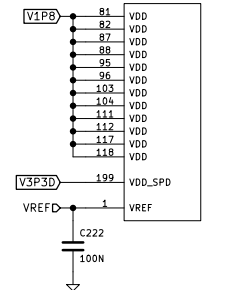
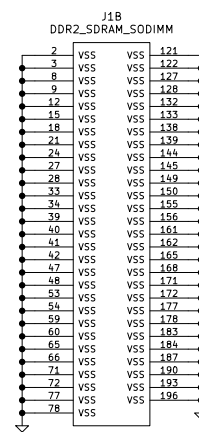
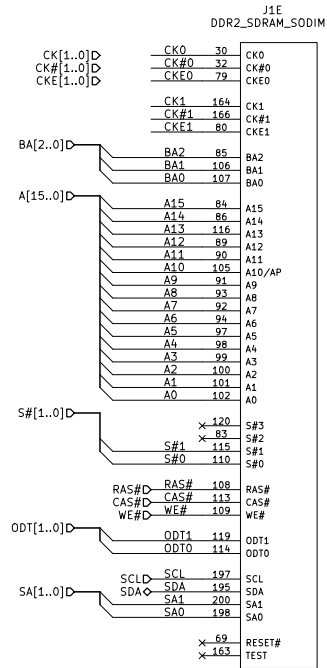
KiCad E.D.A. eeschema (2014-03-01 BZR 4730) -product

Rev: 0

Id: 13/15



DDR2 operates in DQS single-ended mode. All DQS# == VSS



License: GNU General Public License, version 2

Copyright © 2013 Jared Boone

ShareBrained Technology, Inc.

Sheet: /ddr2/

File: ddr2.sch

Title: Daisho Project Main Board

Size: A3 Date: 10 Oct 2014

KiCad E.D.A. eeschema (2014-03-01 BZR 4730) -product

Rev: 0

Id: 14/15

