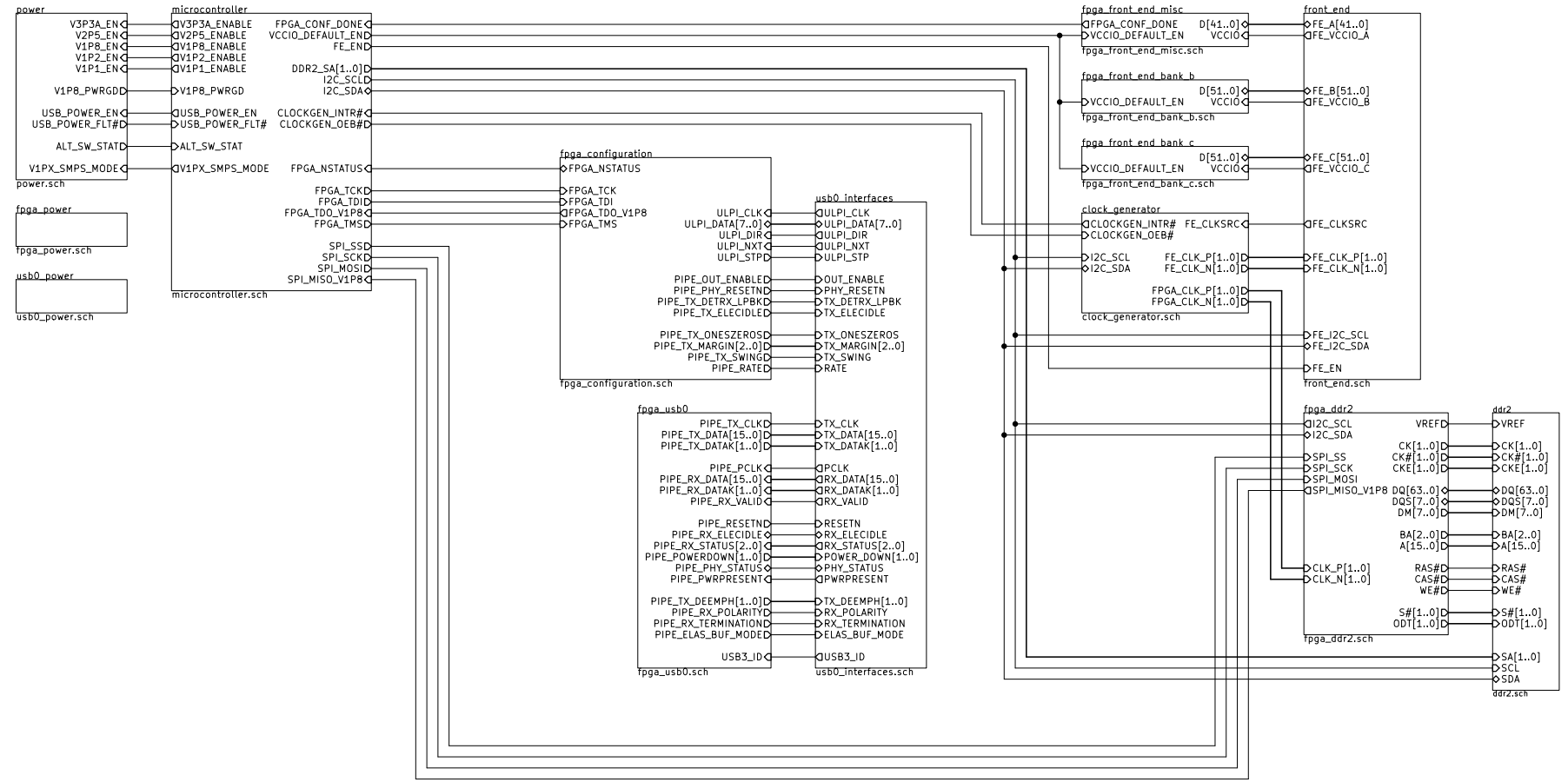


H1 H5 H7
HOLE HOLE HOLE

H2 H4 H6 H8
HOLE HOLE HOLE HOLE

Sheet: /	
File: main_board.sch	
Title: Daisho Project Main Board	
Size: A3	Date: 10 Oct 2014
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product	Id: 1/15

Rev: 0

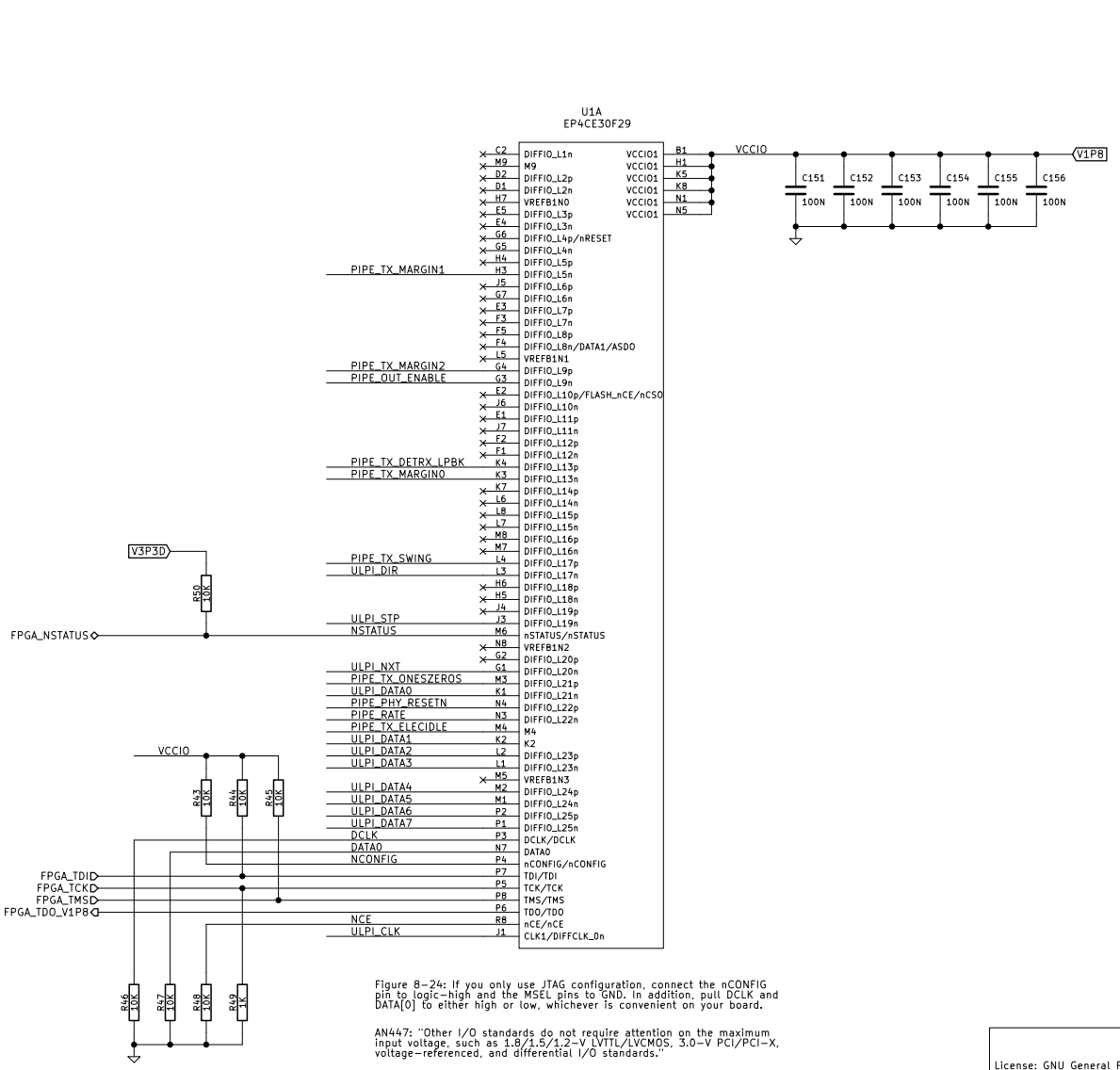


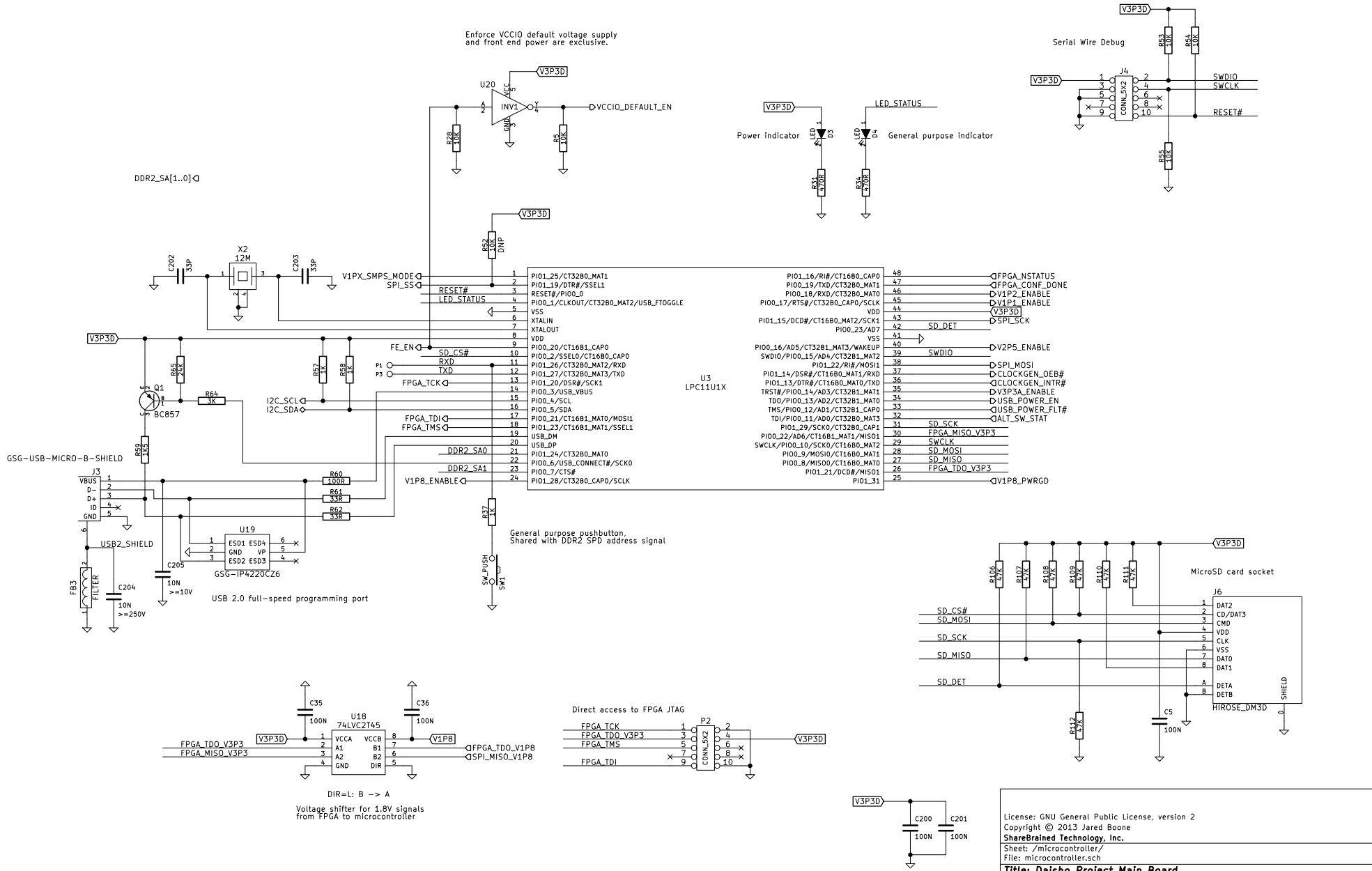
Figure 8-24: If you only use JTAG configuration, connect the nCONFIG pin to logic-high and the MSEL pins to GND. In addition, pull DCLK and DATA[0] to either high or low, whichever is convenient on your board.

AN447: "Other I/O standards do not require attention on the maximum input voltage, such as 1.8/1.5/1.2-V LVTTL/LVCMOS, 3.0-V PCI/PCI-X, voltage-referenced, and differential I/O standards."

Sheet: /fpga_configuration/
File: fpga_configuration.sch

Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 2/15



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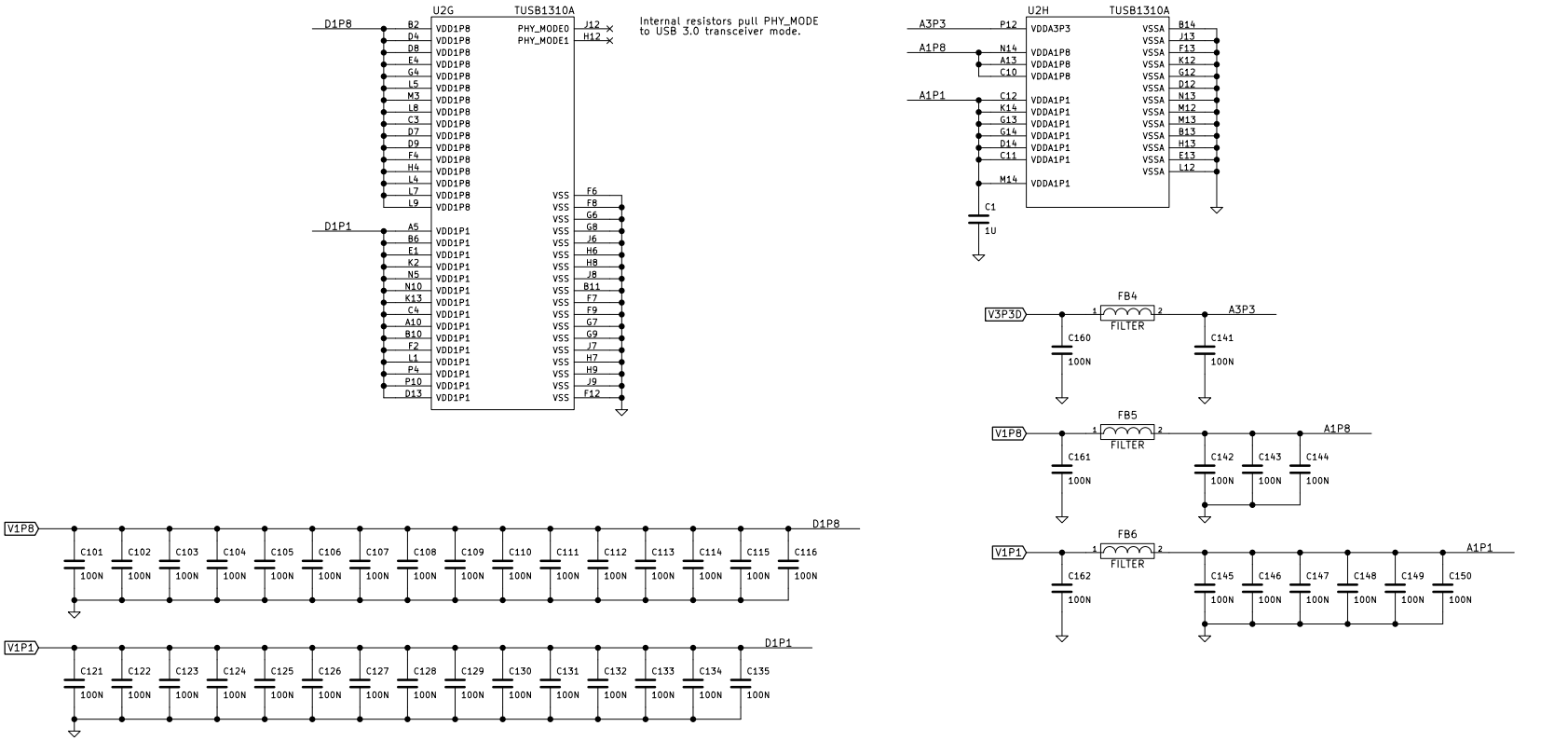
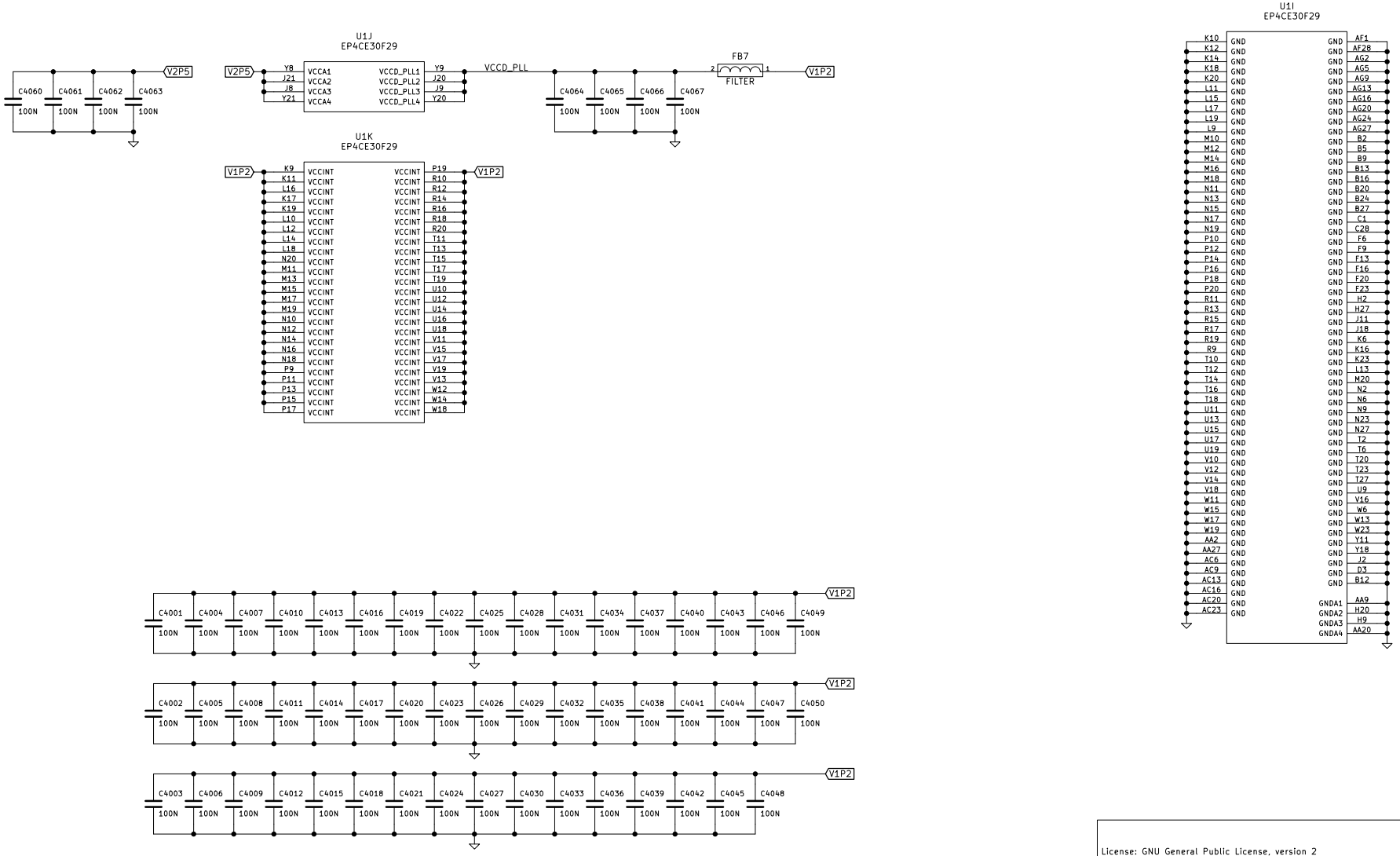
Sheet: /microcontroller/		
File: microcontroller.sch		
Title: Daisho Project Main Board		
Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 3/15



Sheet: /usb0_power/
File: usb0_power.sch

Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 4/15



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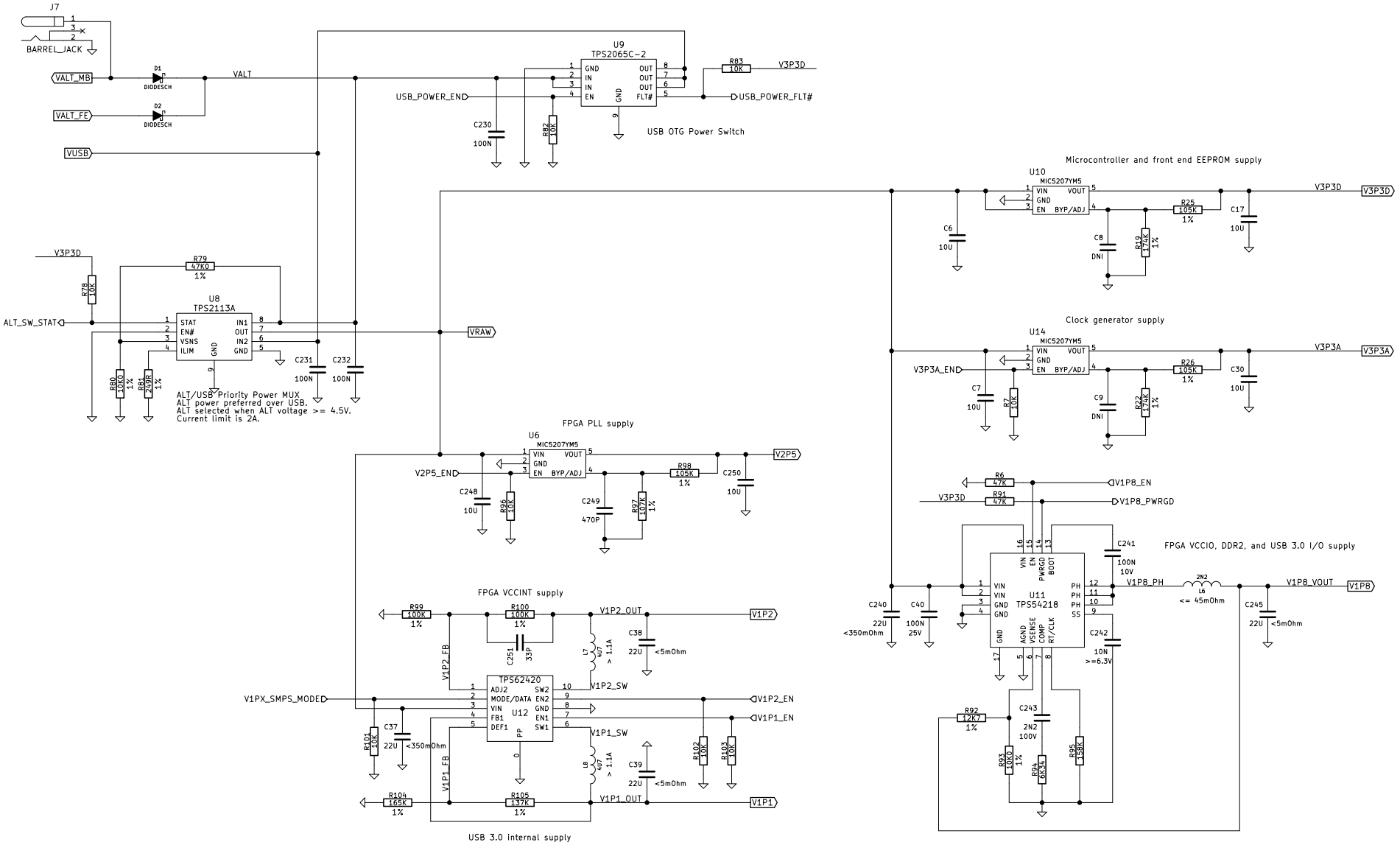
Sheet: /fpga_power/
File: fpga_power.sch

Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 5/15



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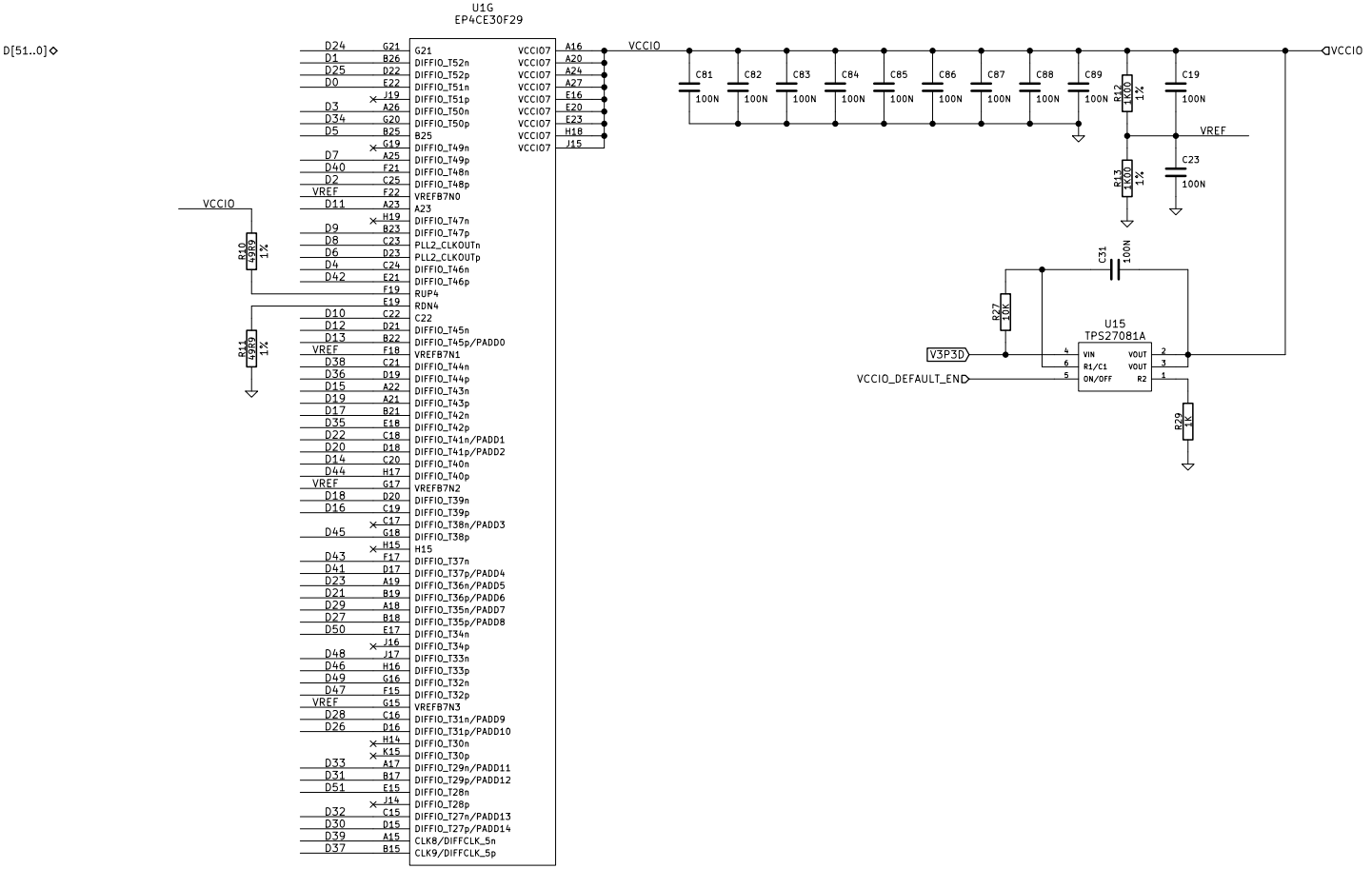
Sheet: /power/
File: power.sch

Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 6/15

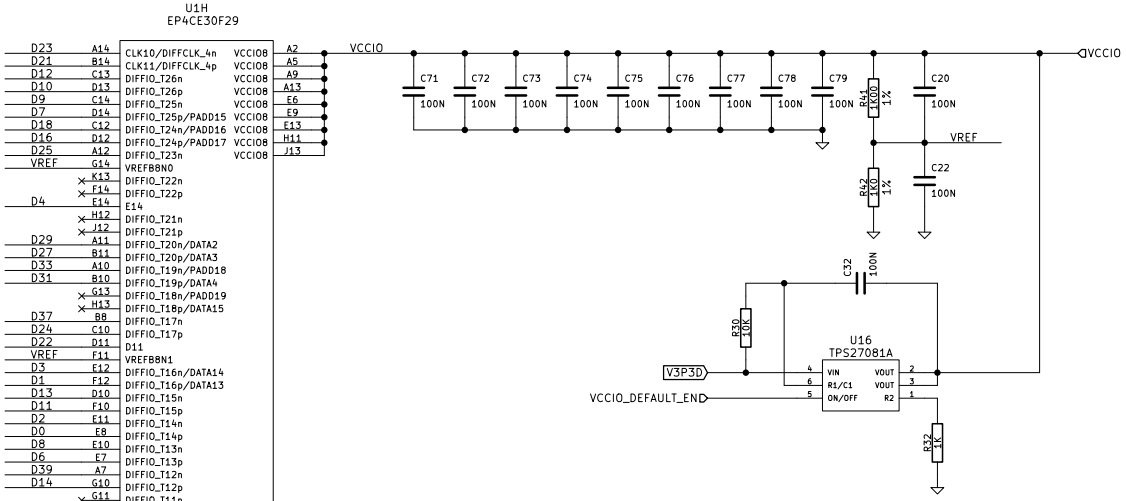


Sheet: /fpga_front_end_bank_b/
File: fpga_front_end_bank_b.sch

Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 7/15

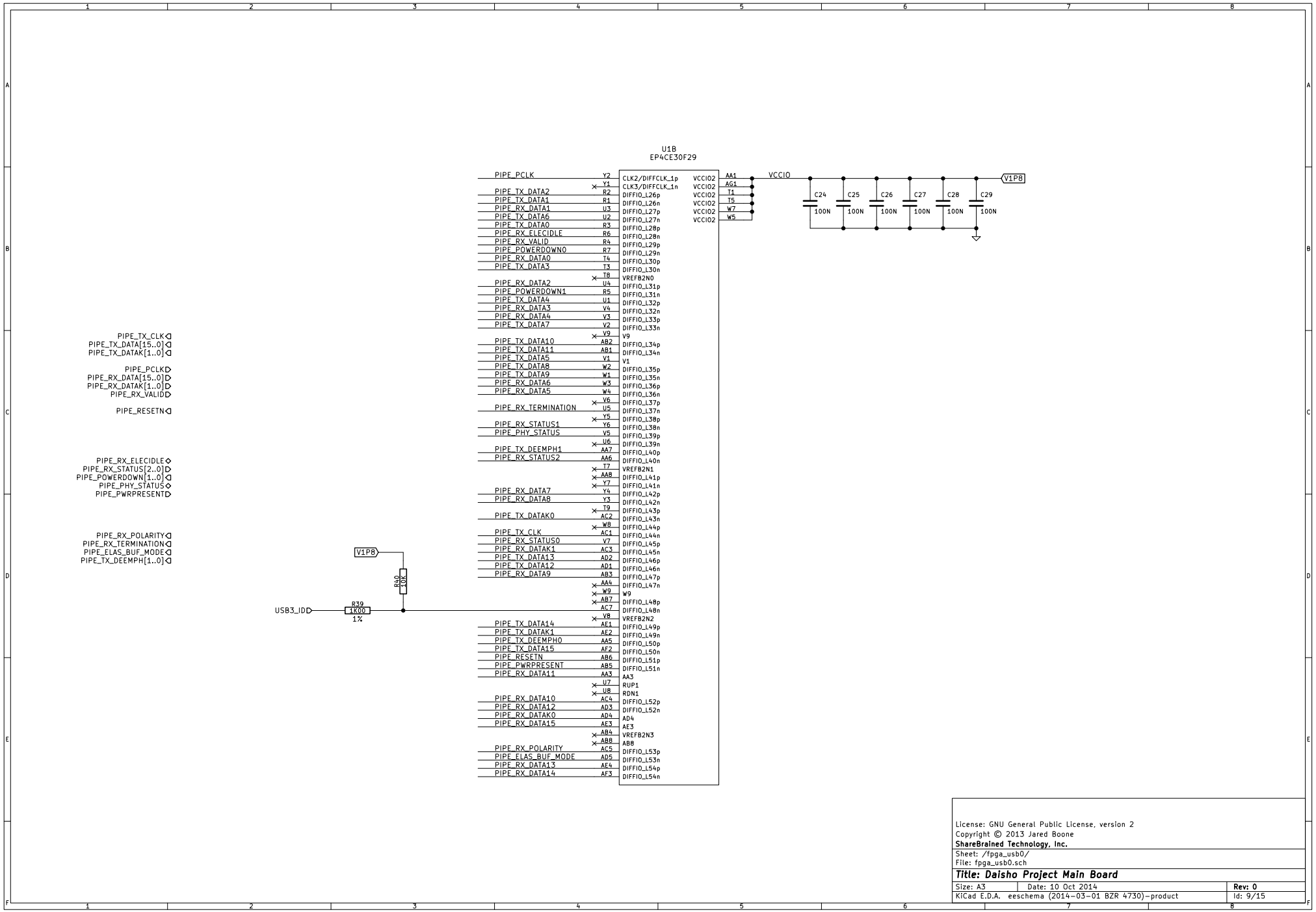
D[51..0]



Sheet: /fpga_front_end_bank_c/
File: fpga_front_end_bank_c.sch

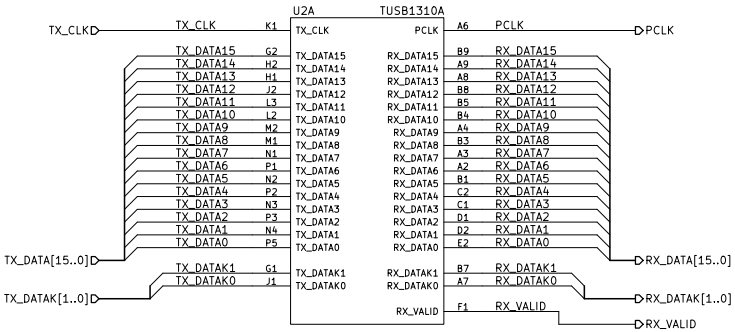
Title: Daisho Project Main Board

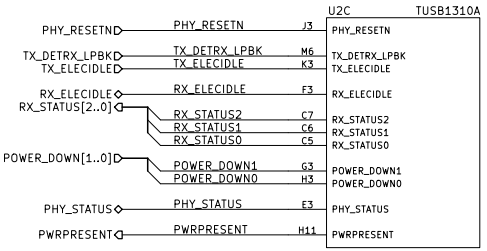
Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 8/15

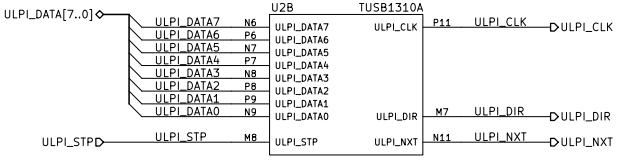


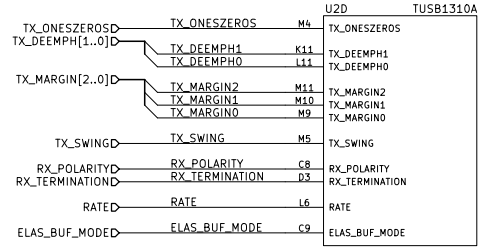
Sheet: /fpga_usb0/	
File: fpga_usb0.sch	
Title: Daisho Project Main Board	
Size: A3	Date: 10 Oct 2014
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product	Id: 9/15

Rev: 0

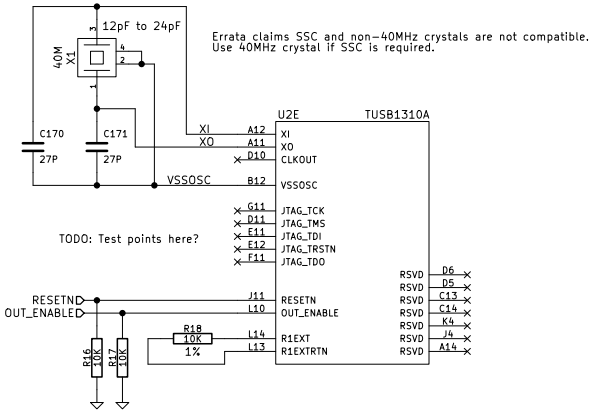




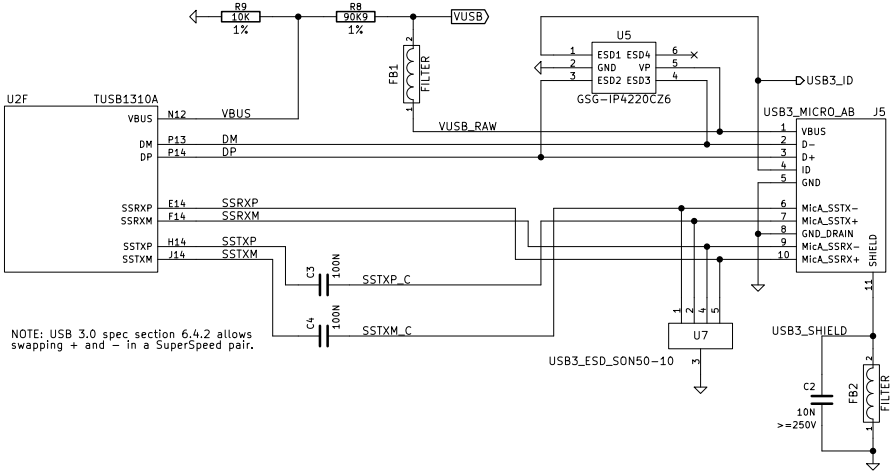




18pF CL is OK, according to datasheet max/min specs.



TODO: Where to send ID for OTG support?



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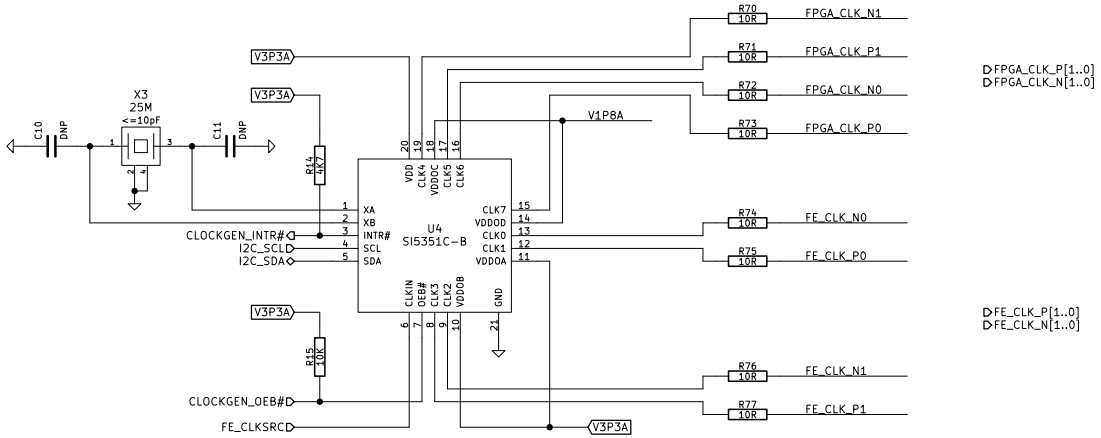
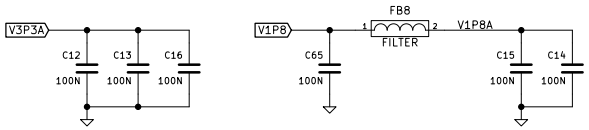
Sheet: /usb0_interfaces/
File: usb0_interfaces.sch

Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A.	eeschema (2014-03-01 BZR 4730)-product	Id: 10/15

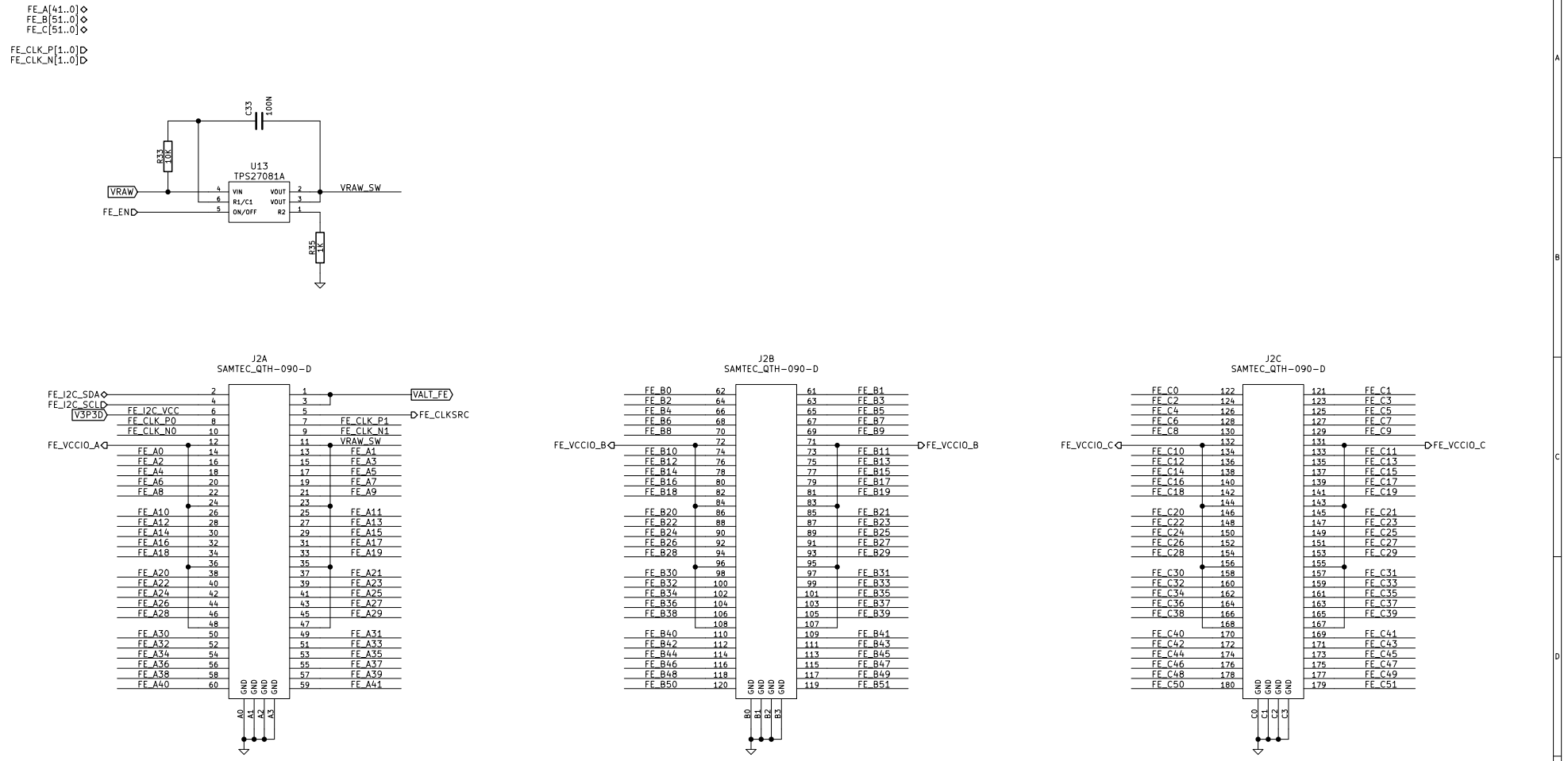




Sheet: /clock_generator/
File: clock_generator.sch

Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 11/15



Ground unused pins at front-end side, assuming FPGA will be configured not to drive those pins?

Ground unused pins at FPGA to ensure low impedance to ground?

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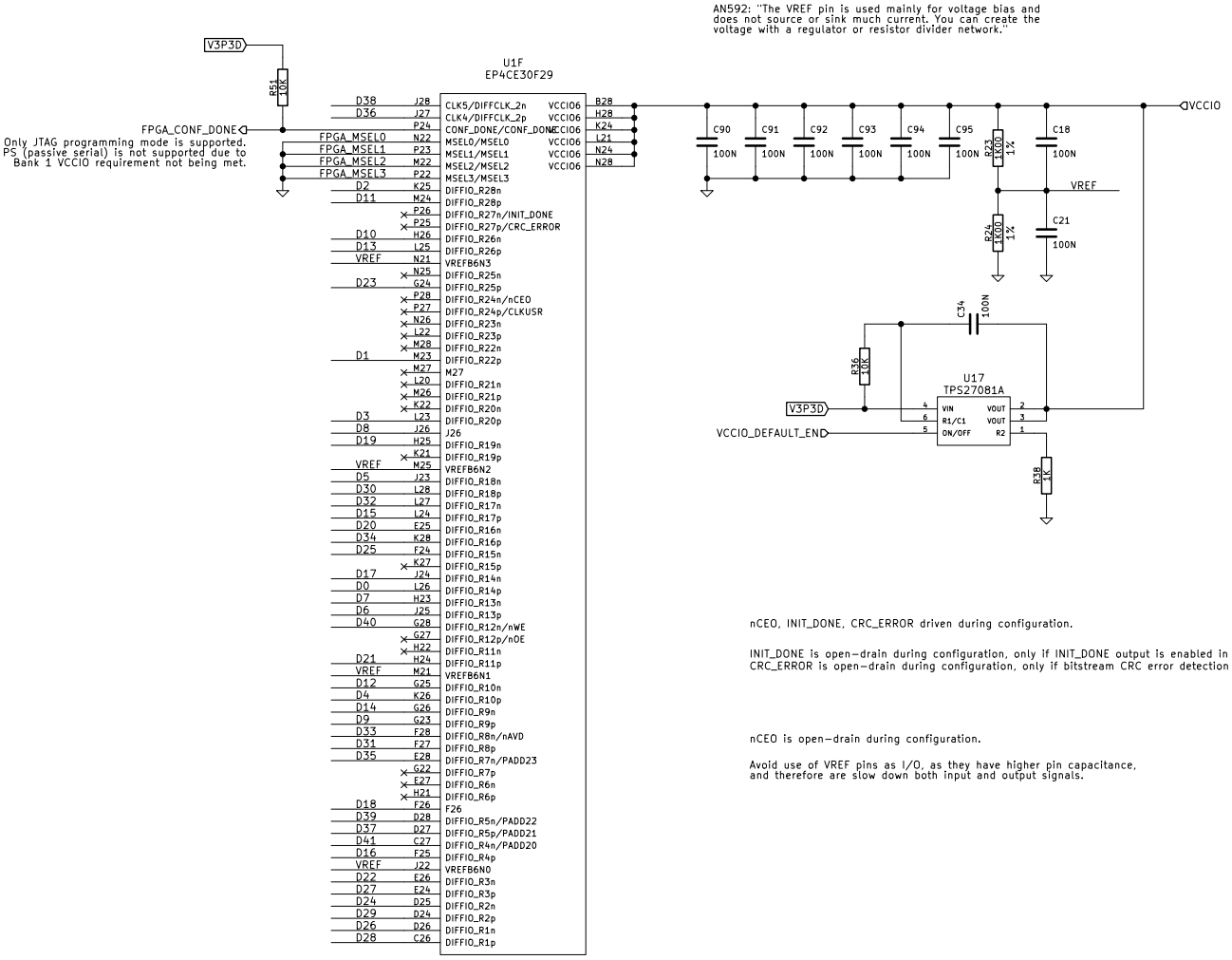
Sheet: /front_end/
File: front_end.sch

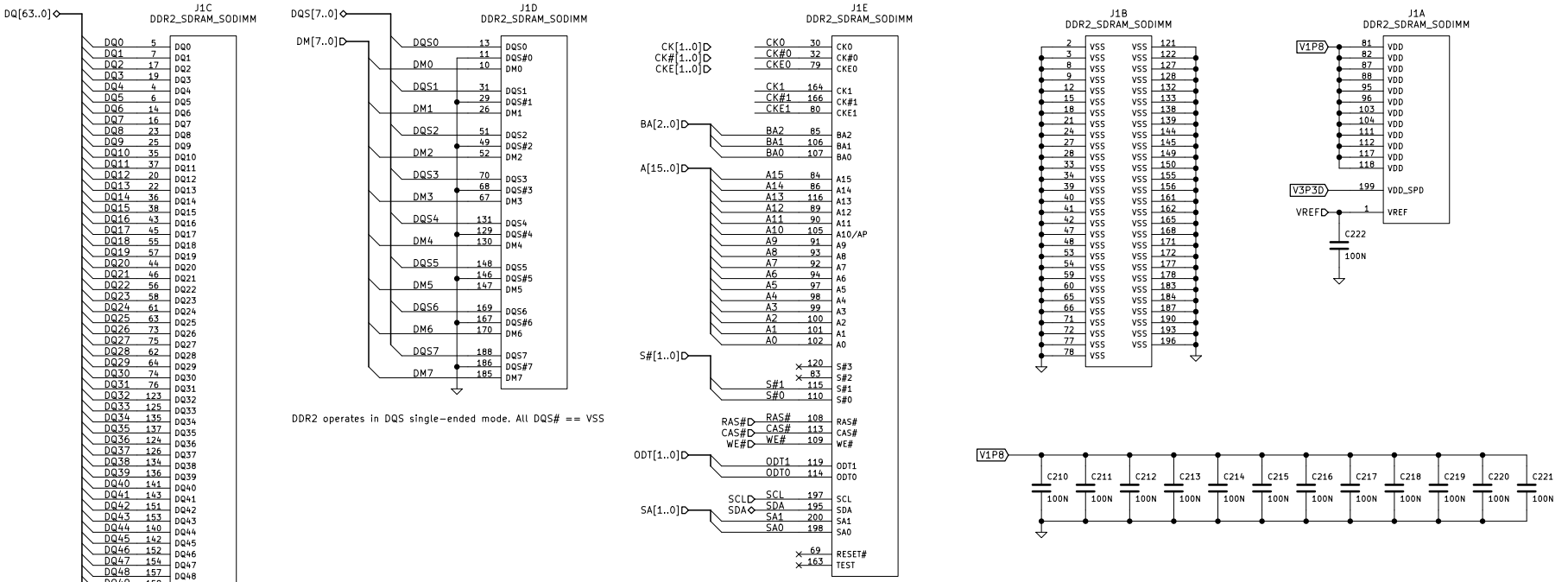
Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A.	eeschema (2014-03-01 BZR 4730)-product	Id: 12/15

D[41..0]



Sheet: /fpga_front_end_misc/	
File: fpga_front_end_misc.sch	
Title: Daisho Project Main Board	
Size: A3 | Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product	Id: 13/15



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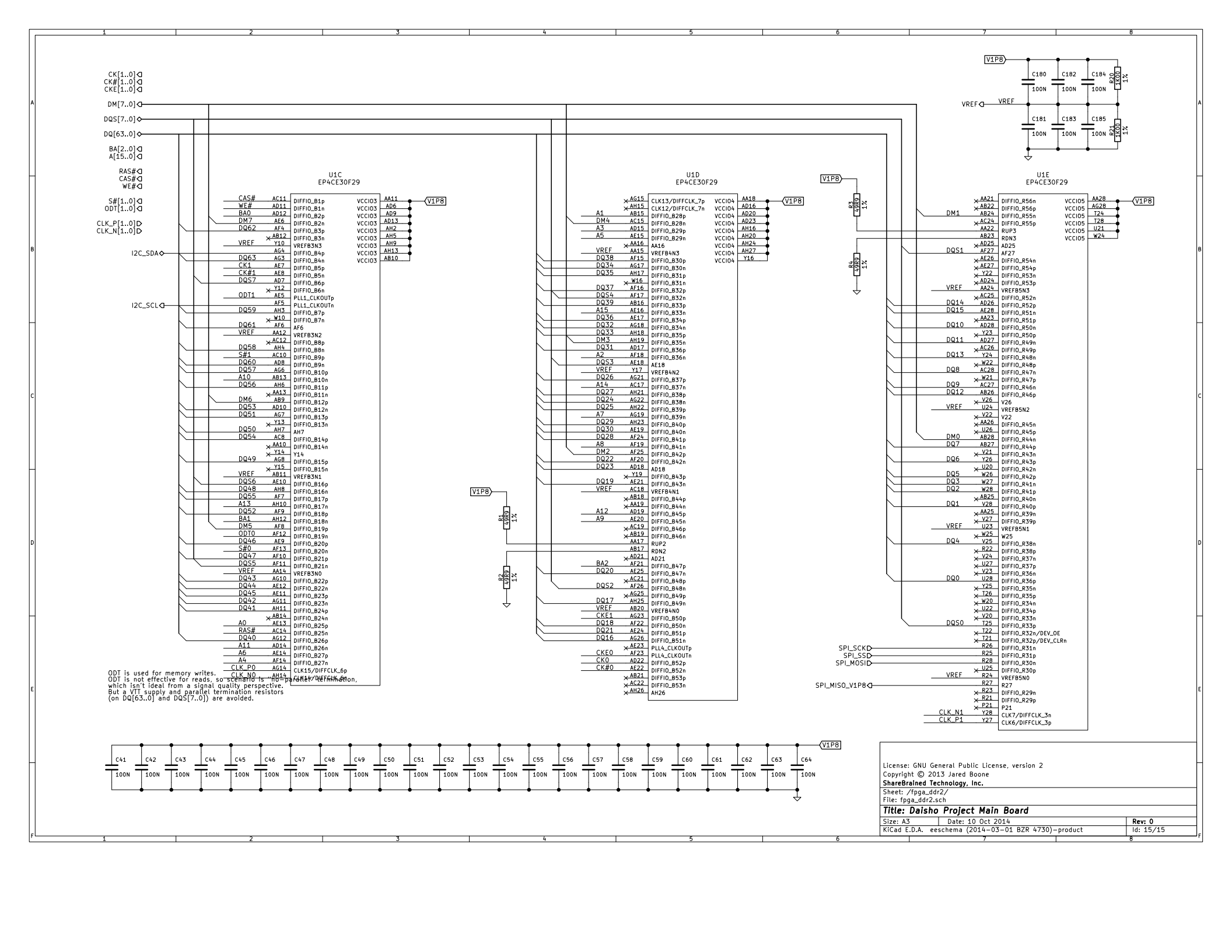
Sheet: /ddr2/
File: ddr2.sch

Title: Daisho Project Main Board

Size: A3	Date: 10 Oct 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 14/15


CK[1..0]
CK#[1..0]
CKE[1..0]
DM[7..0]
DQS[7..0]
DQ[63..0]
BA[2..0]
A[15..0]
RAS#
CAS#
WE#
S#[1..0]
ODT[1..0]
CLK_P[1..0]
CLK_N[1..0]
I2C_SDA
I2C_SCL
U1C
EP4CE30F29
U1D
EP4CE30F29
U1E
EP4CE30F29
V1P8
VREF
C180 100N
C182 100N
C184 100N
C181 100N
C183 100N
C185 100N
R80 1K00 1%
R81 1K00 1%
R83 499 1%
R84 499 1%
R82 499 1%
R84 499 1%
SPI_SCK
SPI_SS
SPI_MOSI
SPI_MISO_V1P8
ODT is used for memory writes.
ODT is not effective for reads, so scenario is "no-parallel termination",
which isn't ideal from a signal quality perspective.
But a VTT supply and parallel termination resistors
(on DQ[63..0] and DQS[7..0]) are avoided.
C41 100N
C42 100N
C43 100N
C44 100N
C45 100N
C46 100N
C47 100N
C48 100N
C49 100N
C50 100N
C51 100N
C52 100N
C53 100N
C54 100N
C55 100N
C56 100N
C57 100N
C58 100N
C59 100N
C60 100N
C61 100N
C62 100N
C63 100N
C64 100N
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Sheet: /fpga_ddr2/
File: fpga_ddr2.sch
Title: Daisho Project Main Board
Size: A3
Date: 10 Oct 2014
Rev: 0
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product
Id: 15/15