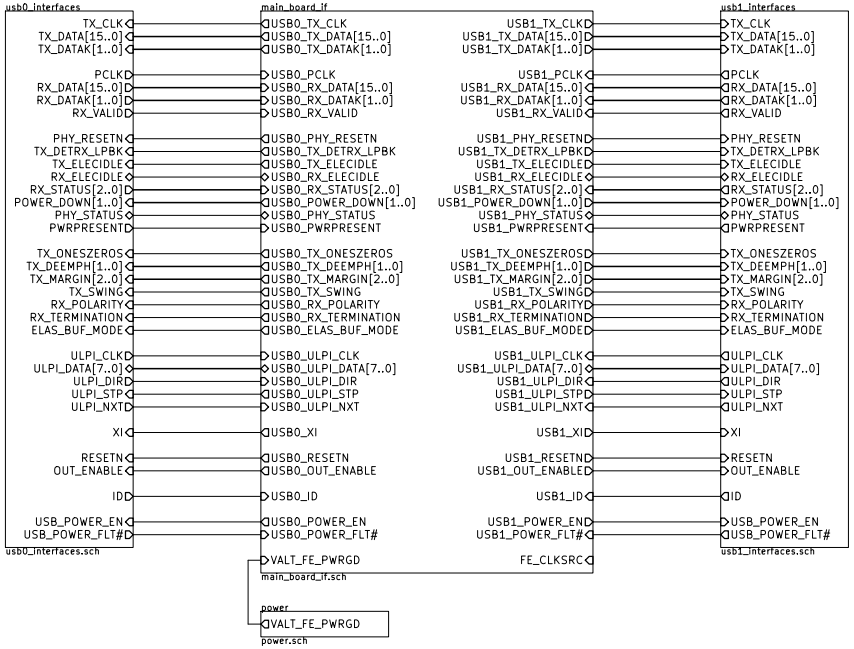


H1 HOLE
H5 HOLE
H7 HOLE
H2 HOLE
H4 HOLE
H6 HOLE
H8 HOLE

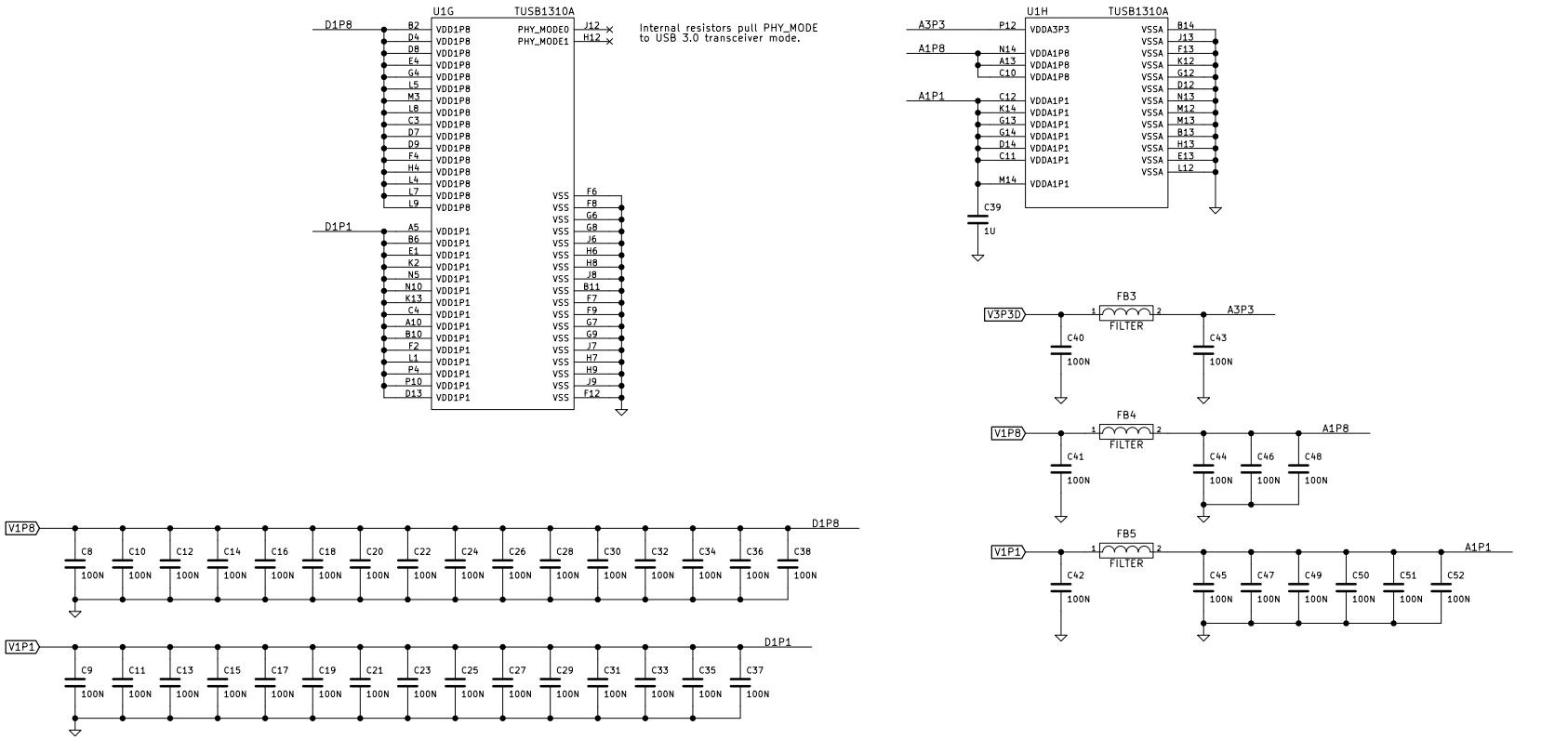
usb0_power
usb0_power.sch

usb1_power
usb1_power.sch

Sheet: /
File: usb.sch

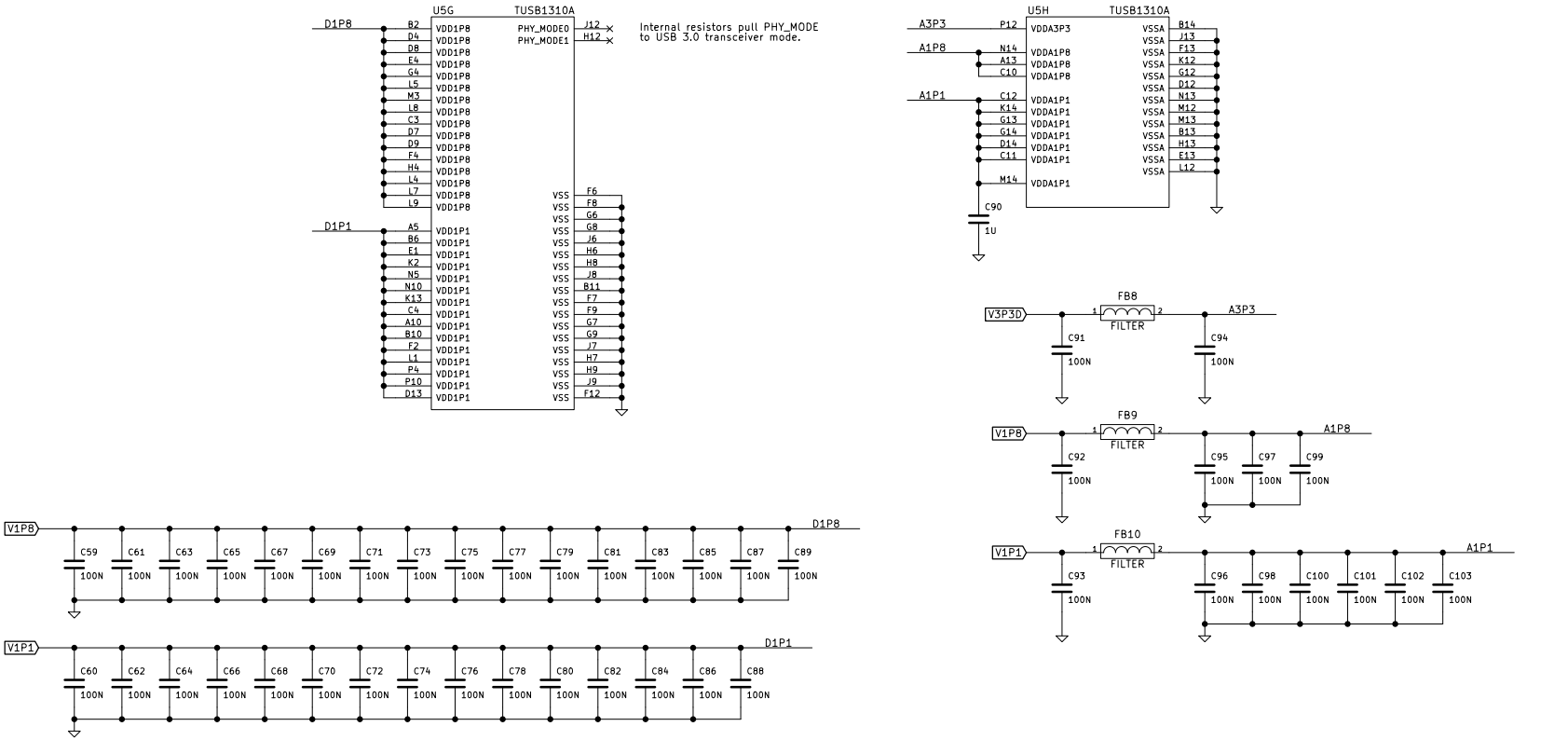
Title: Daisho Project USB Front-End

Size: A3	Date: 20 mar 2014	**Rev:**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 1/7



Sheet: /usb0_power/	
File: usb0_power.sch	
Title: Daisho Project USB Front-End	
Size: A3	Date: 20 mar 2014
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product	Id: 2/7

Rev: 0



Sheet: /usb1_power/
File: usb1_power.sch

Title: Daisho Project USB Front-End

Size: A3	Date: 20 mar 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 3/7

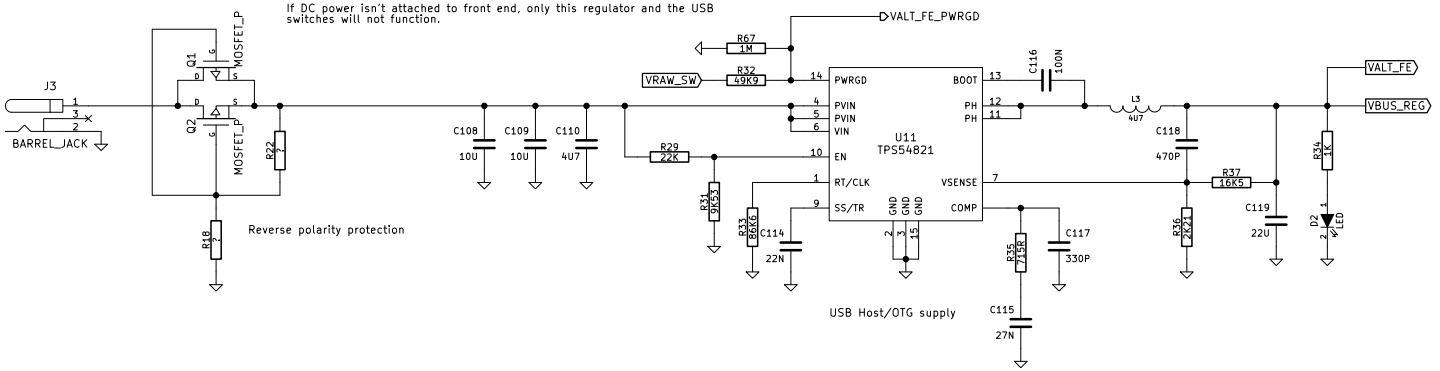
USB regulator accepts DC input from 5.5V to 12.5V.
Efficiency above 0.3A is >95.5% at 5.5V input, >91.5% across all inputs.
Power dissipation is 1.1W, worst case (12.5V in, 4.0A out).
IC dissipation is 0.8W worst case (12.5V in, 4.0A out).

USB regulator is on whenever DC power is attached.

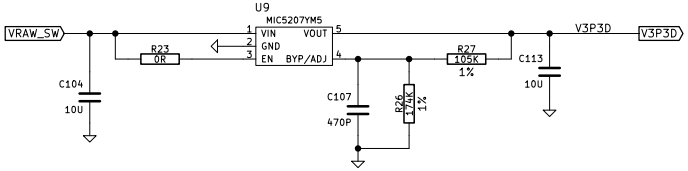
USB power switches must be held off when front end is powered down.

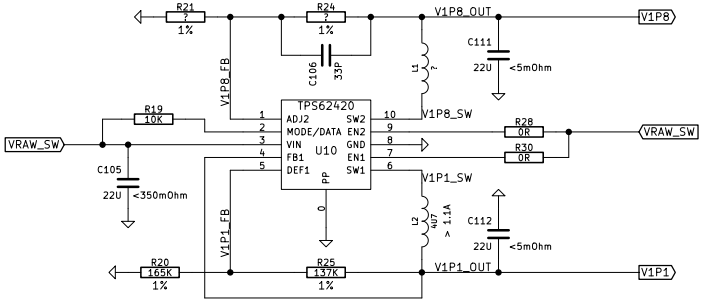
Regulator supplies power to main board (up to 5V@2A), if the main board doesn't have an overriding power source attached.

If DC power isn't attached to front end, only this regulator and the USB switches will not function.



USB 3.0 supply
Requirements:
3.3V output: 8mA (26mW) typical
Input: 8mA typical (36mW at 5V in)



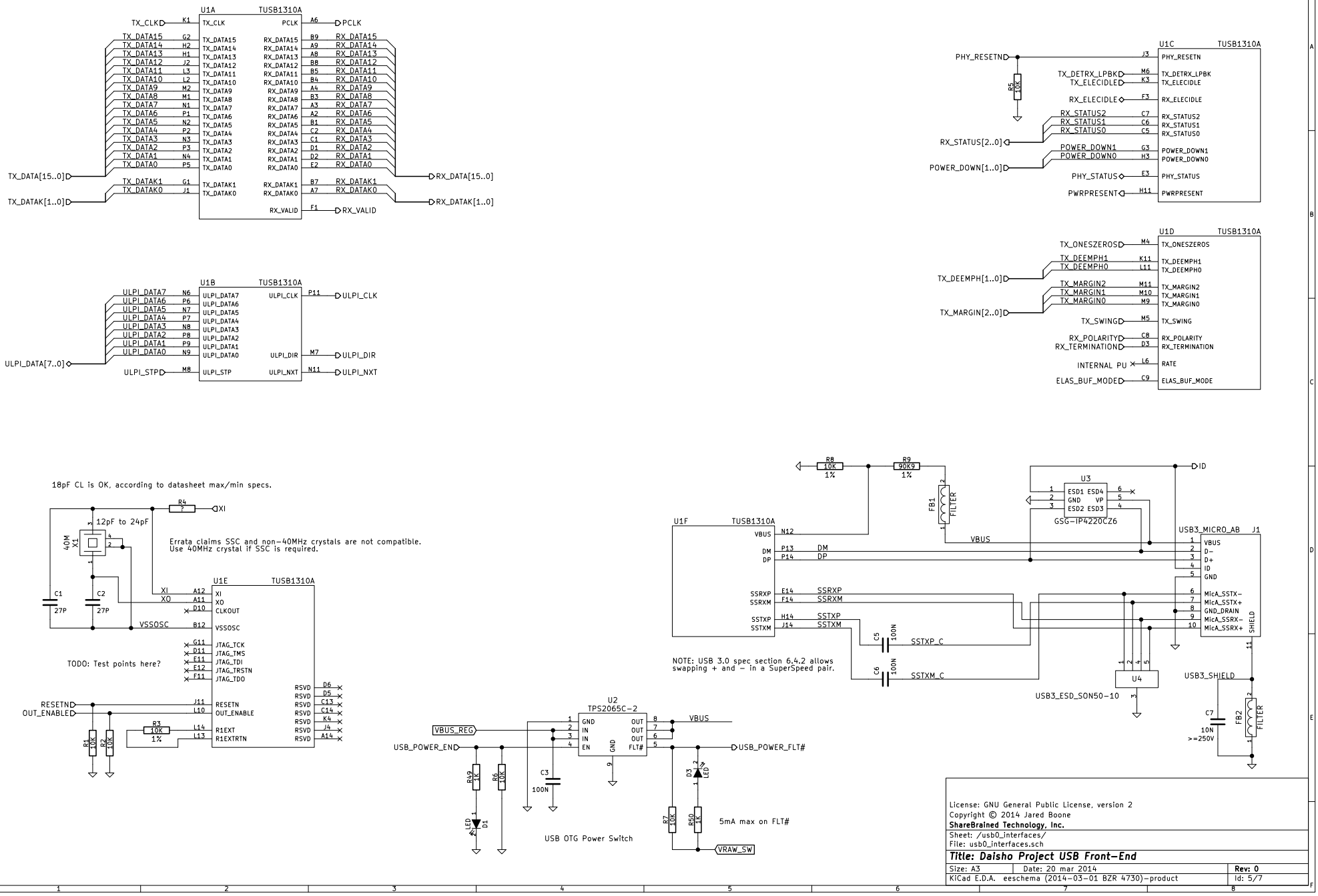


USB 3.0 internal supply
Requirements:
1.8V output: 228mA (410mW) typical
1.1V output: 393mA (432mW) typical
Input: 936mW typical (222mA at 4.2V in, 90% efficiency)

ShareBrained Technology, Inc.

Sheet: /power/	
File: power.sch	
Title: Daisho Project USB Front-End	
Size: A3	Date: 20 mar 2014
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product	Id: 4/7

Rev: 0


U1A TUSB1310A
TX_CLK K1
PCLK A6
TX_DATA15 G2
TX_DATA14 H2
TX_DATA13 H1
TX_DATA12 J2
TX_DATA11 L3
TX_DATA10 L2
TX_DATA9 M2
TX_DATA8 M1
TX_DATA7 N1
TX_DATA6 P1
TX_DATA5 N2
TX_DATA4 P2
TX_DATA3 N3
TX_DATA2 P3
TX_DATA1 N4
TX_DATA0 P5
RX_DATA15 B9
RX_DATA14 A9
RX_DATA13 A8
RX_DATA12 B8
RX_DATA11 B5
RX_DATA10 B4
RX_DATA9 A4
RX_DATA8 B3
RX_DATA7 A3
RX_DATA6 A2
RX_DATA5 B1
RX_DATA4 C2
RX_DATA3 C1
RX_DATA2 D1
RX_DATA1 D2
RX_DATA0 E2
TX_DATA[15..0]
RX_DATA[15..0]
TX_DATAK1 G1
TX_DATAK0 J1
RX_DATAK1 B7
RX_DATAK0 A7
TX_DATAK[1..0]
RX_DATAK[1..0]
RX_VALID F1
U1B TUSB1310A
ULPI_DATA7 N6
ULPI_DATA6 P6
ULPI_DATA5 N7
ULPI_DATA4 P7
ULPI_DATA3 N8
ULPI_DATA2 P8
ULPI_DATA1 P9
ULPI_DATA0 N9
ULPI_CLK P11
ULPI_DIR M7
ULPI_NXT N11
ULPI_STP M8
ULPI_DATA[7..0]
U1C TUSB1310A
PHY_RESETN J3
TX_DETRX_LPBK M6
TX_ELECIDLE K3
RX_ELECIDLE F3
RX_STATUS2 C7
RX_STATUS1 C6
RX_STATUS0 C5
POWER_DOWN1 G3
POWER_DOWN0 H3
PHY_STATUS E3
PWRPRESENT H11
R5 10K
RX_STATUS[2..0]
POWER_DOWN[1..0]
U1D TUSB1310A
TX_ONESZEROS M4
TX_DEEMPH1 K11
TX_DEEMPH0 L11
TX_MARGIN2 M11
TX_MARGIN1 M10
TX_MARGIN0 M9
TX_SWING M5
RX_POLARITY C8
RX_TERMINATION D3
INTERNAL PU L6
ELAS_BUF_MODE C9
TX_DEEMPH[1..0]
TX_MARGIN[2..0]
18pF CL is OK, according to datasheet max/min specs.
12pF to 24pF
R4 ?
XI
40M
X1
C1 27P
C2 27P
Errata claims SSC and non-40MHz crystals are not compatible.
Use 40MHz crystal if SSC is required.
U1E TUSB1310A
XI A12
XO A11
CLKOUT D10
VSSOSC B12
JTAG_TCK G11
JTAG_TMS D11
JTAG_TDI E11
JTAG_TRSTN E12
JTAG_TDO F11
TODO: Test points here?
RESETN J11
OUT_ENABLE L10
R1EXT L14
R1EXTRTN L13
RSVD D6
RSVD D5
RSVD C13
RSVD C14
RSVD K4
RSVD J4
RSVD A14
R1 10K
R2 10K
R3 10K 1%
U1F TUSB1310A
VBUS N12
DM P13
DP P14
SSRXP E14
SSRXM F14
SSTXP H14
SSTXM J14
R8 10K 1%
R9 90K9 1%
FB1 FILTER
VBUS
DM
DP
SSRXP
SSRXM
SSTXP
SSTXM
C5 100N
C6 100N
SSTXP_C
SSTXM_C
NOTE: USB 3.0 spec section 6.4.2 allows
swapping + and - in a SuperSpeed pair.
U3
ESD1 ESD4
GND VP
ESD2 ESD3
GSG-IP4220CZ6
ID
USB3_MICRO_AB J1
VBUS
D-
D+
ID
GND
MicA_SSTX-
MicA_SSTX+
GND_DRAIN
MicA_SSRX-
MicA_SSRX+
SHIELD
U4
USB3_ESD_SON50-10
USB3_SHIELD
C7 10N >=250V
FB2 FILTER
U2 TPS2065C-2
GND
IN
IN
EN
OUT
OUT
OUT
FLT#
VBUS_REG
USB_POWER_EN
USB_POWER_FLT#
VBUS
R49 1K
R6 10K
C3 100N
D1 LED
D5 LED
R7 10K
R50 1K
5mA max on FLT#
VRAW_SW
USB OTG Power Switch
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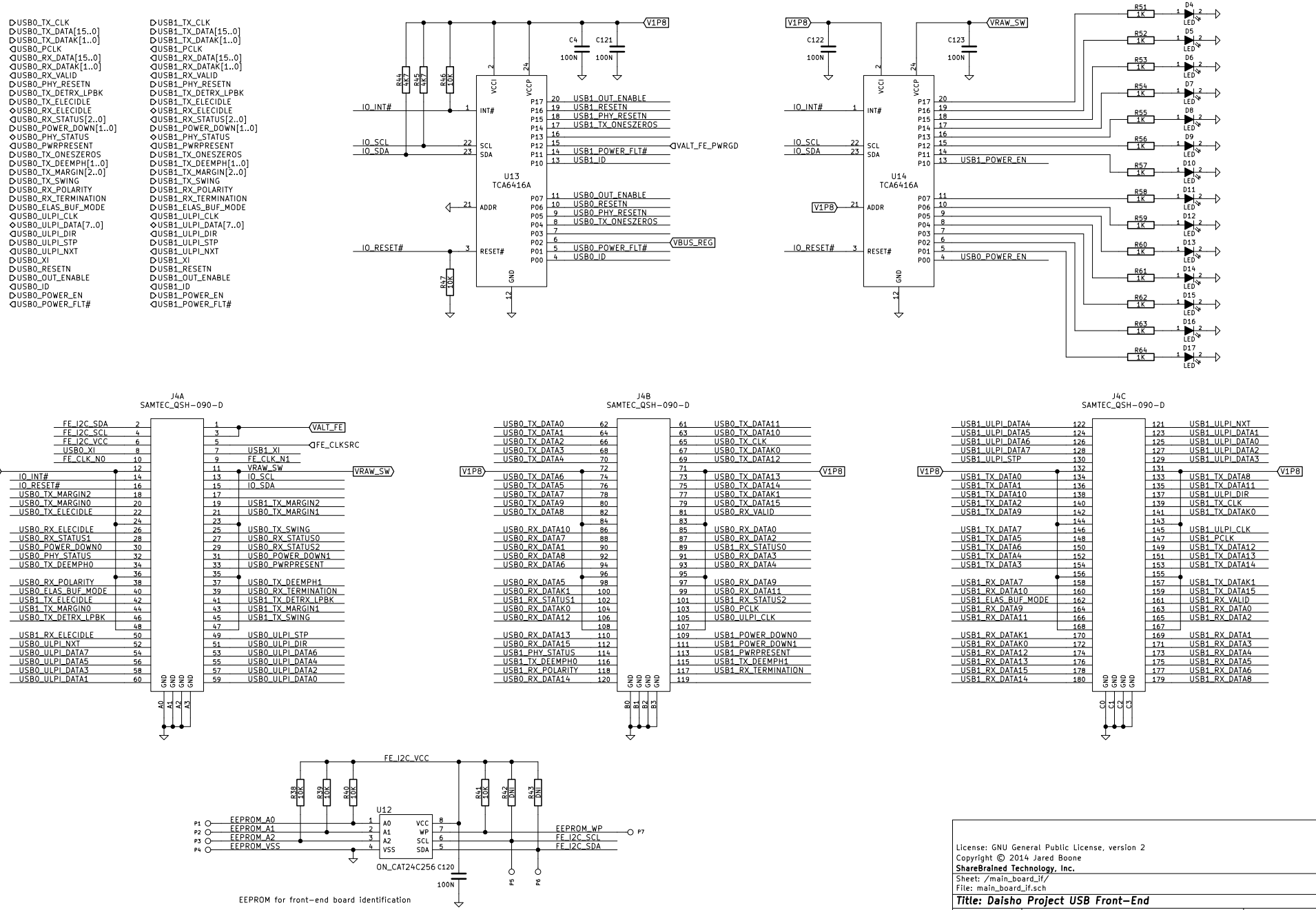
ShareBrained Technology, Inc.
Sheet: /usb0_interfaces/
File: usb0_interfaces.sch
Title: Daisho Project USB Front-End
Size: A3
Date: 20 mar 2014
Rev: 0
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product
Id: 5/7


USB0_TX_CLK
USB0_TX_DATA[15..0]
USB0_TX_DATAK[1..0]
USB0_PCLK
USB0_RX_DATA[15..0]
USB0_RX_DATAK[1..0]
USB0_RX_VALID
USB0_PHY_RESETN
USB0_TX_DETRX_LPBK
USB0_TX_ELECIDLE
USB0_RX_ELECIDLE
USB0_RX_STATUS[2..0]
USB0_POWER_DOWN[1..0]
USB0_PHY_STATUS
USB0_PWRPRESENT
USB0_TX_ONESZEROS
USB0_TX_DEEMPH[1..0]
USB0_TX_MARGIN[2..0]
USB0_TX_SWING
USB0_RX_POLARITY
USB0_RX_TERMINATION
USB0_ELAS_BUF_MODE
USB0_ULPI_CLK
USB0_ULPI_DATA[7..0]
USB0_ULPI_DIR
USB0_ULPI_STP
USB0_ULPI_NXT
USB0_XI
USB0_RESETN
USB0_OUT_ENABLE
USB0_ID
USB0_POWER_EN
USB0_POWER_FLT#
USB1_TX_CLK
USB1_TX_DATA[15..0]
USB1_TX_DATAK[1..0]
USB1_PCLK
USB1_RX_DATA[15..0]
USB1_RX_DATAK[1..0]
USB1_RX_VALID
USB1_PHY_RESETN
USB1_TX_DETRX_LPBK
USB1_TX_ELECIDLE
USB1_RX_ELECIDLE
USB1_RX_STATUS[2..0]
USB1_POWER_DOWN[1..0]
USB1_PHY_STATUS
USB1_PWRPRESENT
USB1_TX_ONESZEROS
USB1_TX_DEEMPH[1..0]
USB1_TX_MARGIN[2..0]
USB1_TX_SWING
USB1_RX_POLARITY
USB1_RX_TERMINATION
USB1_ELAS_BUF_MODE
USB1_ULPI_CLK
USB1_ULPI_DATA[7..0]
USB1_ULPI_DIR
USB1_ULPI_STP
USB1_ULPI_NXT
USB1_XI
USB1_RESETN
USB1_OUT_ENABLE
USB1_ID
USB1_POWER_EN
USB1_POWER_FLT#
V1P8
C4 100N
C121 100N
R44 4K7
R45 4K7
R46 10K
R47 10K
IO_INT#
IO_SCL
IO_SDA
IO_RESET#
U13
TCA6416A
VCCI
VCCP
INT#
SCL
SDA
ADDR
RESET#
GND
USB1_OUT_ENABLE
USB1_RESETN
USB1_PHY_RESETN
USB1_TX_ONESZEROS
USB1_POWER_FLT#
USB1_ID
USB0_OUT_ENABLE
USB0_RESETN
USB0_PHY_RESETN
USB0_TX_ONESZEROS
USB0_POWER_FLT#
USB0_ID
VALT_FE_PWRGD
VBUS_REG
C122 100N
C123 100N
VRAW_SW
U14
TCA6416A
USB1_POWER_EN
USB0_POWER_EN
R51 1K
R52 1K
R53 1K
R54 1K
R55 1K
R56 1K
R57 1K
R58 1K
R59 1K
R60 1K
R61 1K
R62 1K
R63 1K
R64 1K
D4 LED
D5 LED
D6 LED
D7 LED
D8 LED
D9 LED
D10 LED
D11 LED
D12 LED
D13 LED
D14 LED
D15 LED
D16 LED
D17 LED
J4A
SAMTEC_QSH-090-D
FE_I2C_SDA
FE_I2C_SCL
FE_I2C_VCC
USB0_XI
FE_CLK_N0
IO_INT#
IO_RESET#
USB0_TX_MARGIN2
USB0_TX_MARGIN0
USB0_TX_ELECIDLE
USB0_RX_ELECIDLE
USB0_RX_STATUS1
USB0_POWER_DOWN0
USB0_PHY_STATUS
USB0_TX_DEEMPH0
USB0_RX_POLARITY
USB0_ELAS_BUF_MODE
USB1_TX_ELECIDLE
USB1_TX_MARGIN0
USB1_TX_DETRX_LPBK
USB1_RX_ELECIDLE
USB0_ULPI_NXT
USB0_ULPI_DATA7
USB0_ULPI_DATA5
USB0_ULPI_DATA3
USB0_ULPI_DATA1
USB0_TX_SWING
USB0_RX_STATUS0
USB0_RX_STATUS2
USB0_POWER_DOWN1
USB0_PWRPRESENT
USB0_TX_DEEMPH1
USB0_RX_TERMINATION
USB1_TX_DETRX_LPBK
USB1_TX_MARGIN1
USB1_TX_SWING
USB0_ULPI_STP
USB0_ULPI_DIR
USB0_ULPI_DATA6
USB0_ULPI_DATA4
USB0_ULPI_DATA2
USB0_ULPI_DATA0
VALT_FE
FE_CLKSRC
USB1_XI
FE_CLK_N1
VRAW_SW
IO_SCL
IO_SDA
USB1_TX_MARGIN2
USB0_TX_MARGIN1
J4B
SAMTEC_QSH-090-D
USB0_TX_DATA0
USB0_TX_DATA1
USB0_TX_DATA2
USB0_TX_DATA3
USB0_TX_DATA4
USB0_TX_DATA6
USB0_TX_DATA5
USB0_TX_DATA7
USB0_TX_DATA9
USB0_TX_DATA8
USB0_RX_DATA10
USB0_RX_DATA7
USB0_RX_DATA1
USB0_RX_DATA8
USB0_RX_DATA6
USB0_RX_DATA5
USB0_RX_DATAK1
USB1_RX_STATUS1
USB0_RX_DATAK0
USB0_RX_DATA12
USB0_RX_DATA13
USB0_RX_DATA15
USB1_PHY_STATUS
USB1_TX_DEEMPH0
USB1_RX_POLARITY
USB0_RX_DATA14
USB0_TX_DATA11
USB0_TX_DATA10
USB0_TX_CLK
USB0_TX_DATAK0
USB0_TX_DATA12
USB0_TX_DATA13
USB0_TX_DATA14
USB0_TX_DATAK1
USB0_TX_DATA15
USB0_RX_VALID
USB0_RX_DATA0
USB0_RX_DATA2
USB1_RX_STATUS0
USB0_RX_DATA3
USB0_RX_DATA4
USB0_RX_DATA9
USB0_RX_DATA11
USB1_RX_STATUS2
USB0_PCLK
USB0_ULPI_CLK
USB1_POWER_DOWN0
USB1_POWER_DOWN1
USB1_PWRPRESENT
USB1_TX_DEEMPH1
USB1_RX_TERMINATION
J4C
SAMTEC_QSH-090-D
USB1_ULPI_DATA4
USB1_ULPI_DATA5
USB1_ULPI_DATA6
USB1_ULPI_DATA7
USB1_ULPI_STP
USB1_TX_DATA0
USB1_TX_DATA1
USB1_TX_DATA10
USB1_TX_DATA2
USB1_TX_DATA9
USB1_TX_DATA7
USB1_TX_DATA5
USB1_TX_DATA6
USB1_TX_DATA4
USB1_TX_DATA3
USB1_RX_DATA7
USB1_RX_DATA10
USB1_ELAS_BUF_MODE
USB1_RX_DATA9
USB1_RX_DATA11
USB1_RX_DATAK1
USB1_RX_DATAK0
USB1_RX_DATA12
USB1_RX_DATA13
USB1_RX_DATA15
USB1_RX_DATA14
USB1_ULPI_NXT
USB1_ULPI_DATA1
USB1_ULPI_DATA0
USB1_ULPI_DATA2
USB1_ULPI_DATA3
USB1_TX_DATA8
USB1_TX_DATA11
USB1_ULPI_DIR
USB1_TX_CLK
USB1_TX_DATAK0
USB1_ULPI_CLK
USB1_PCLK
USB1_TX_DATA12
USB1_TX_DATA13
USB1_TX_DATA14
USB1_TX_DATAK1
USB1_TX_DATA15
USB1_RX_VALID
USB1_RX_DATA0
USB1_RX_DATA2
USB1_RX_DATA1
USB1_RX_DATA3
USB1_RX_DATA4
USB1_RX_DATA5
USB1_RX_DATA6
USB1_RX_DATA8
FE_I2C_VCC
R38 10K
R39 10K
R40 10K
R41 10K
R42 DNI
R43 DNI
U12
ON_CAT24C256
C120 100N
EEPROM_A0
EEPROM_A1
EEPROM_A2
EEPROM_VSS
EEPROM_WP
FE_I2C_SCL
FE_I2C_SDA
EEPROM for front-end board identification
License: GNU General Public License, version 2
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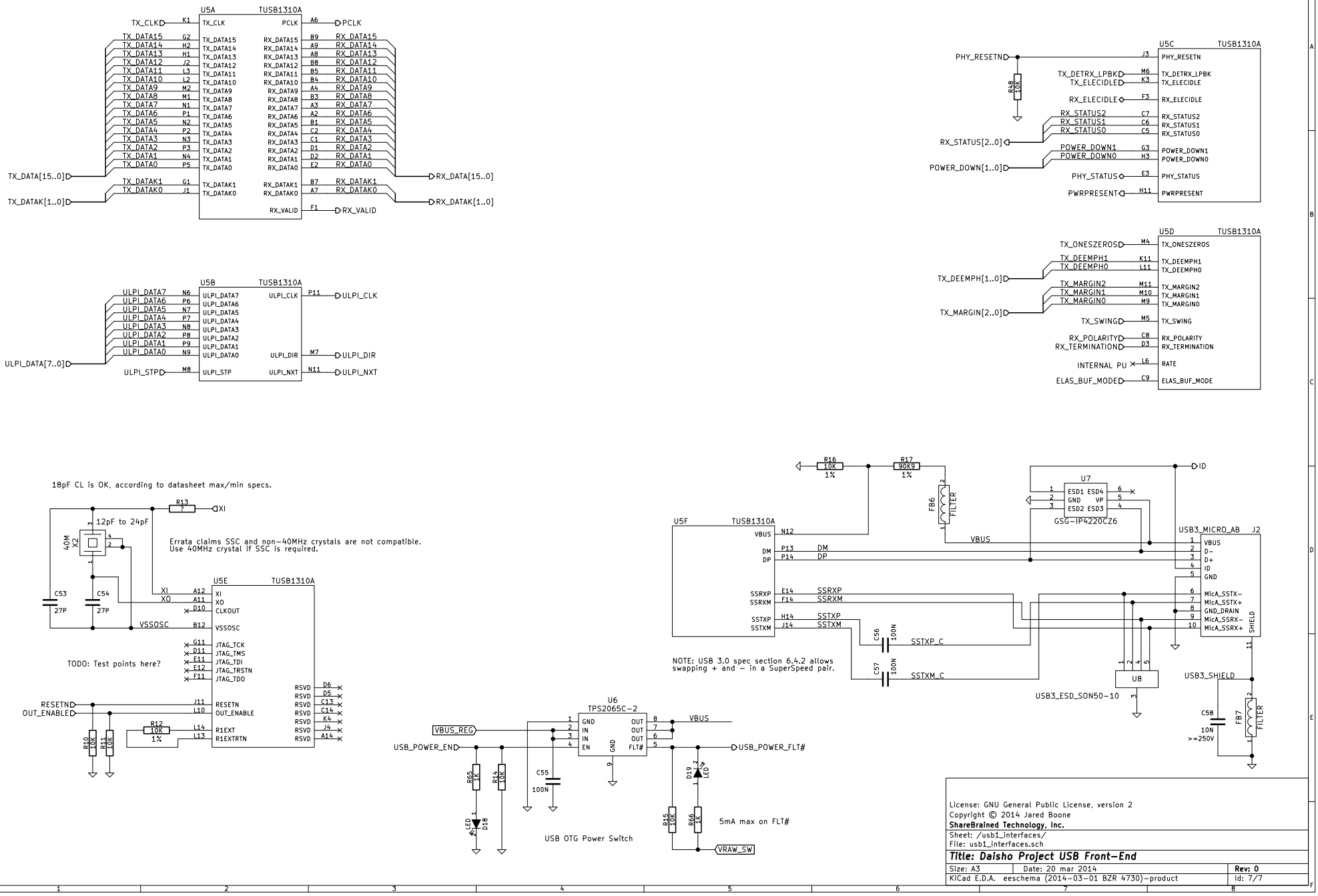
ShareBrained Technology, Inc.
Sheet: /main_board_lf/
File: main_board_lf.sch
Title: Daisho Project USB Front-End
Size: A3
Date: 20 mar 2014
Rev: 0
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product
Id: 6/7


U5A TUSB1310A
TX_CLK K1
TX_DATA15 G2
TX_DATA14 H2
TX_DATA13 H1
TX_DATA12 J2
TX_DATA11 L3
TX_DATA10 L2
TX_DATA9 M2
TX_DATA8 M1
TX_DATA7 N1
TX_DATA6 P1
TX_DATA5 N2
TX_DATA4 P2
TX_DATA3 N3
TX_DATA2 P3
TX_DATA1 N4
TX_DATA0 P5
TX_DATAK1 G1
TX_DATAK0 J1
TX_DATA[15..0]
TX_DATAK[1..0]
PCLK A6
RX_DATA15 B9
RX_DATA14 A9
RX_DATA13 A8
RX_DATA12 B8
RX_DATA11 B5
RX_DATA10 B4
RX_DATA9 A4
RX_DATA8 B3
RX_DATA7 A3
RX_DATA6 A2
RX_DATA5 B1
RX_DATA4 C2
RX_DATA3 C1
RX_DATA2 D1
RX_DATA1 D2
RX_DATA0 E2
RX_DATAK1 B7
RX_DATAK0 A7
RX_VALID F1
RX_DATA[15..0]
RX_DATAK[1..0]
U5B TUSB1310A
ULPI_DATA7 N6
ULPI_DATA6 P6
ULPI_DATA5 N7
ULPI_DATA4 P7
ULPI_DATA3 N8
ULPI_DATA2 P8
ULPI_DATA1 P9
ULPI_DATA0 N9
ULPI_STP M8
ULPI_DATA[7..0]
ULPI_CLK P11
ULPI_DIR M7
ULPI_NXT N11
U5C TUSB1310A
PHY_RESETN J3
TX_DETRX_LPBK M6
TX_ELECIDLE K3
RX_ELECIDLE F3
RX_STATUS2 C7
RX_STATUS1 C6
RX_STATUS0 C5
POWER_DOWN1 G3
POWER_DOWN0 H3
PHY_STATUS E3
PWRPRESENT H11
R48 10K
RX_STATUS[2..0]
POWER_DOWN[1..0]
U5D TUSB1310A
TX_ONESZEROS M4
TX_DEEMPH1 K11
TX_DEEMPH0 L11
TX_MARGIN2 M11
TX_MARGIN1 M10
TX_MARGIN0 M9
TX_SWING M5
RX_POLARITY C8
RX_TERMINATION D3
INTERNAL PU L6
ELAS_BUF_MODE C9
TX_DEEMPH[1..0]
TX_MARGIN[2..0]
18pF CL is OK, according to datasheet max/min specs.
12pF to 24pF
40M X2
C53 27P
C54 27P
R13 ?
XI
XO
VSSOSC
Errata claims SSC and non-40MHz crystals are not compatible.
Use 40MHz crystal if SSC is required.
U5E TUSB1310A
XI A12
XO A11
CLKOUT D10
VSSOSC B12
JTAG_TCK G11
JTAG_TMS D11
JTAG_TDI E11
JTAG_TRSTN E12
JTAG_TDO F11
RESETN J11
OUT_ENABLE L10
R1EXT L14
R1EXTRTN L13
RSVD D6
RSVD D5
RSVD C13
RSVD C14
RSVD K4
RSVD J4
RSVD A14
TODO: Test points here?
R10 10K
R11 10K
R12 10K 1%
R16 10K 1%
R17 90K9 1%
FB6 FILTER
U5F TUSB1310A
VBUS N12
DM P13
DP P14
SSRXP E14
SSRXM F14
SSTXP H14
SSTXM J14
C56 100N
C57 100N
SSTXP_C
SSTXM_C
NOTE: USB 3.0 spec section 6.4.2 allows swapping + and - in a SuperSpeed pair.
U7
ESD1 ESD4
GND VP
ESD2 ESD3
GSG-IP4220CZ6
ID
VBUS
USB3_MICRO_AB J2
D-
D+
ID
GND
MicA_SSTX-
MicA_SSTX+
GND_DRAIN
MicA_SSRX-
MicA_SSRX+
SHIELD
U8
USB3_ESD_SON50-10
USB3_SHIELD
C58 10N >=250V
FB7 FILTER
U6 TPS2065C-2
GND
IN
IN
EN
OUT
OUT
OUT
FLT#
VBUS_REG
USB_POWER_EN
USB_POWER_FLT#
C55 100N
R65 1K
R14 10K
R15 10K
R66 1K
D19 LED
D18 LED
5mA max on FLT#
USB OTG Power Switch
VRAW_SW
License: GNU General Public License, version 2
Copyright © 2014 Jared Boone
ShareBrained Technology, Inc.
Sheet: /usb1_interfaces/
File: usb1_interfaces.sch
Title: Daisho Project USB Front-End
Size: A3
Date: 20 mar 2014
Rev: 0
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product
Id: 7/7