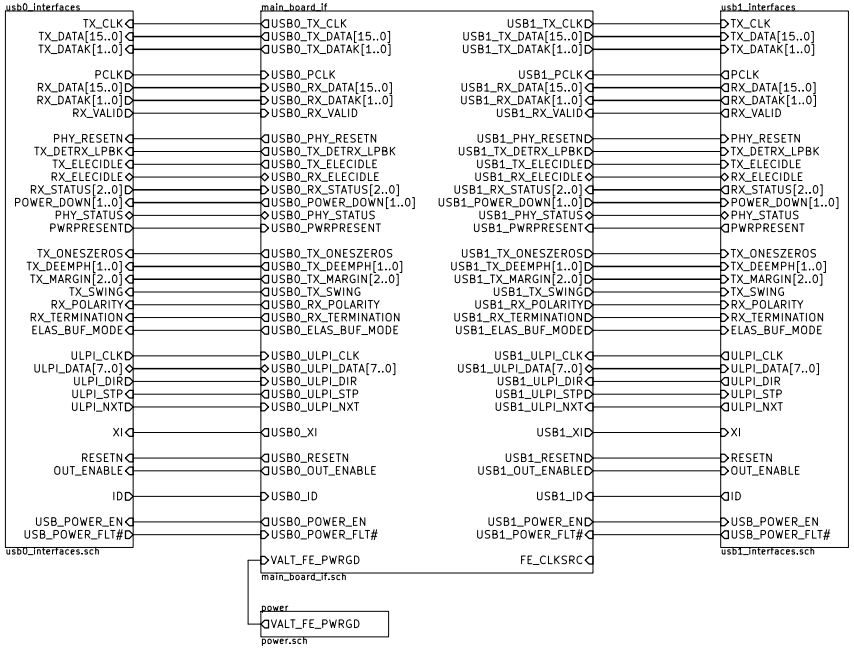

H1 HOLE

H5 HOLE

H7 HOLE

H2 HOLE

H4 HOLE

H6 HOLE

H8 HOLE

usb0_power

usb0_power.sch

usb1_power

usb1_power.sch

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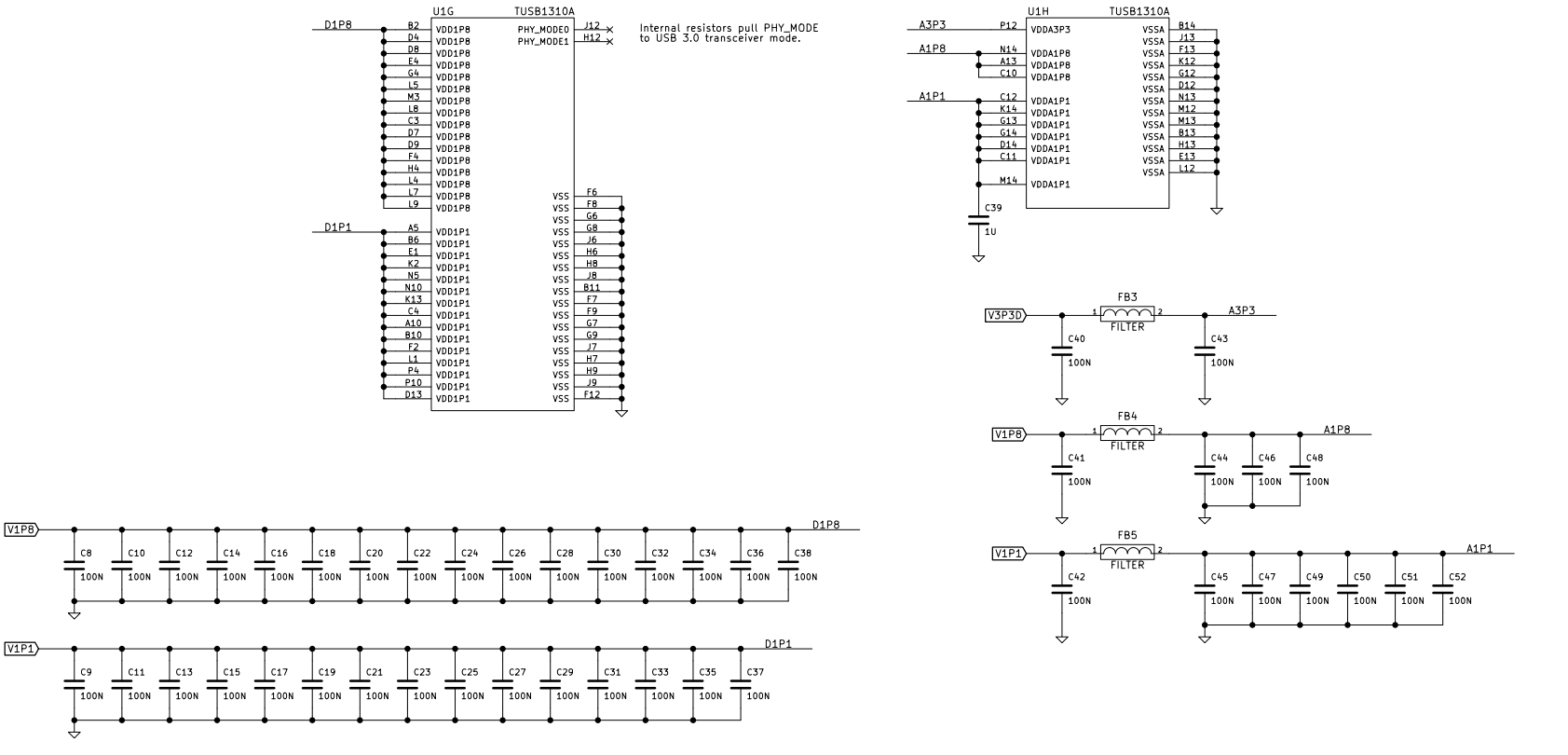
Sheet: /
File: usb.sch

Title: Daisho Project USB Front-End

Size: A3	Date: 4 apr 2014	**Rev:**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 1/7



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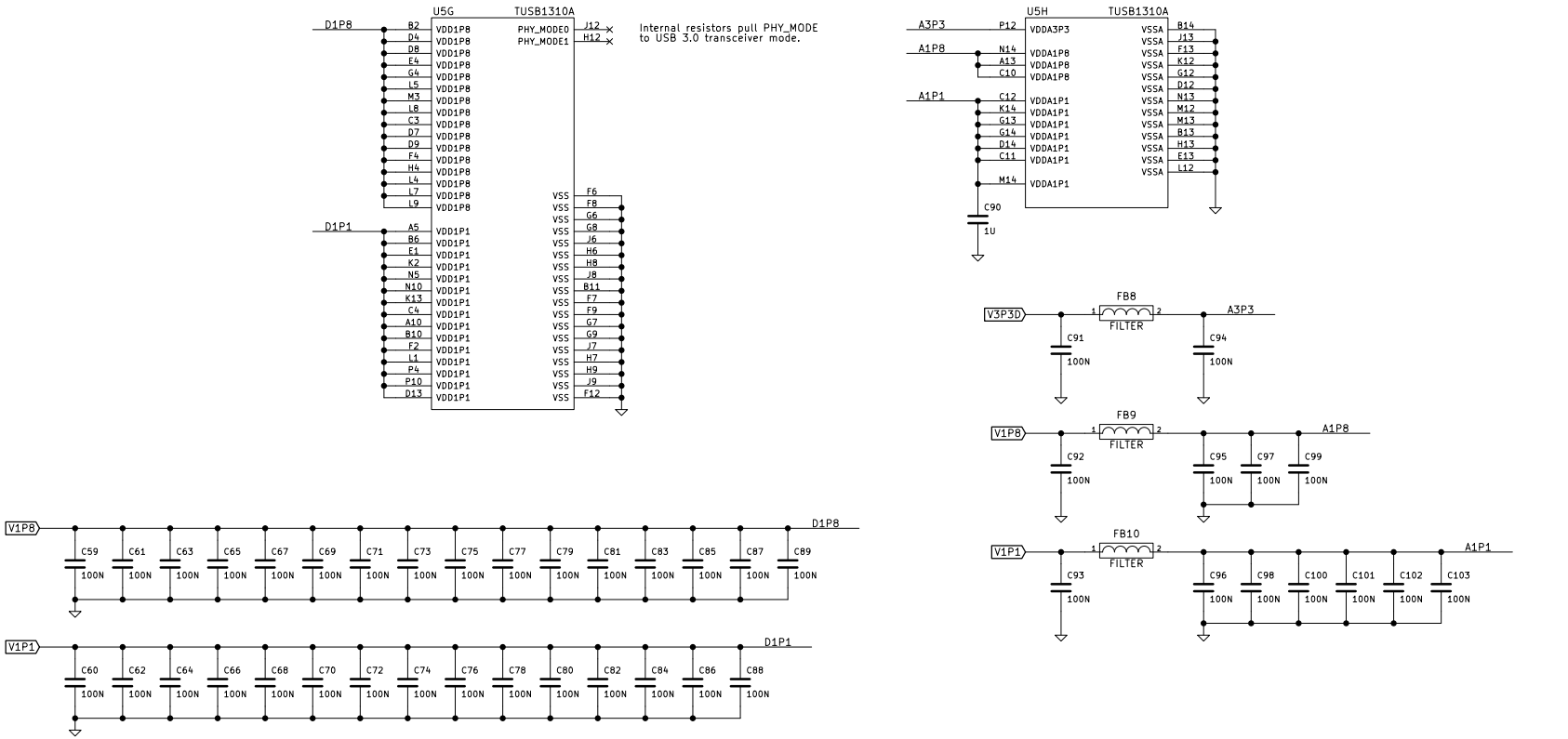
Sheet: /usb0_power/
File: usb0_power.sch

Title: Daisho Project USB Front-End

Size: A3	Date: 4 apr 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 2/7



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Sheet: /usb1_power/
File: usb1_power.sch

Title: Daisho Project USB Front-End

Size: A3	Date: 4 apr 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 3/7

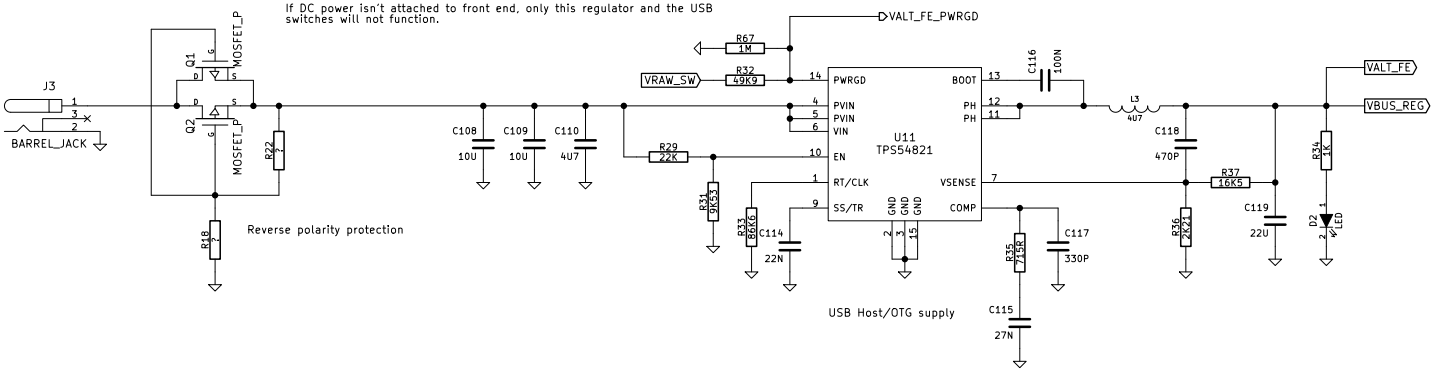
USB regulator accepts DC input from 5.5V to 12.5V.
Efficiency above 0.3A is >95.5% at 5.5V input, >91.5% across all inputs.
Power dissipation is 1.1W, worst case (12.5V in, 4.0A out).
IC dissipation is 0.8W worst case (12.5V in, 4.0A out).

USB regulator is on whenever DC power is attached.

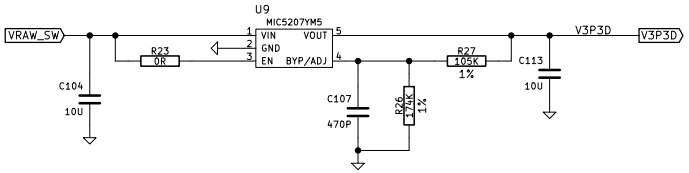
USB power switches must be held off when front end is powered down.

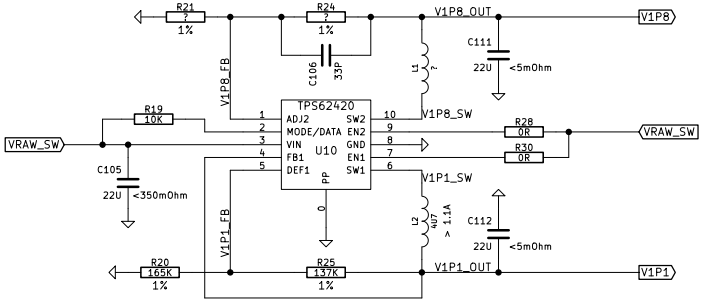
Regulator supplies power to main board (up to 5V@2A), if the main board doesn't have an overriding power source attached.

If DC power isn't attached to front end, only this regulator and the USB switches will not function.



USB 3.0 supply
Requirements:
3.3V output: 8mA (26mW) typical
Input: 8mA typical (36mW at 5V in)





USB 3.0 internal supply
Requirements:
1.8V output: 228mA (410mW) typical
1.1V output: 393mA (432mW) typical
Input: 936mW typical (222mA at 4.2V in, 90% efficiency)

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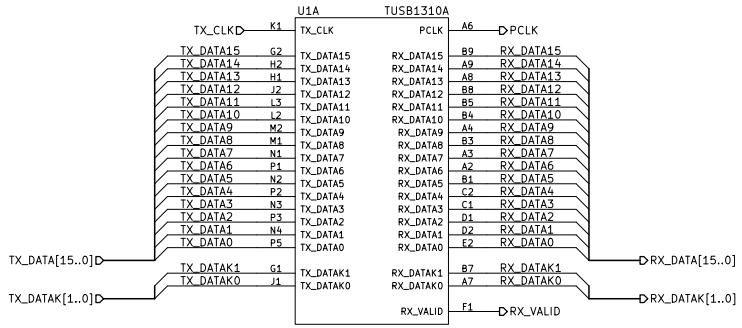
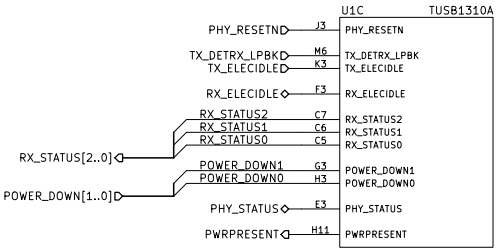
Sheet: /power/	
File: power.sch	
Title: Daisho Project USB Front-End	
Size: A3	Date: 4 apr 2014
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product	Id: 4/7

Rev: 0

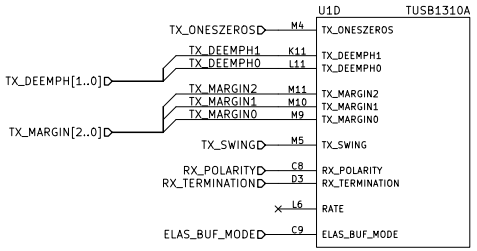


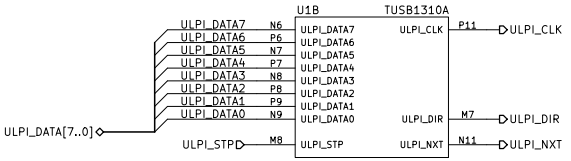
PIPE interfaces:

* Match lengths to <250mil.
* Length <2" if no termination.
* 50 Ohms +/- 10%.
* PHY_STATUS, RX_STATUS[2..0] timed to PCLK.



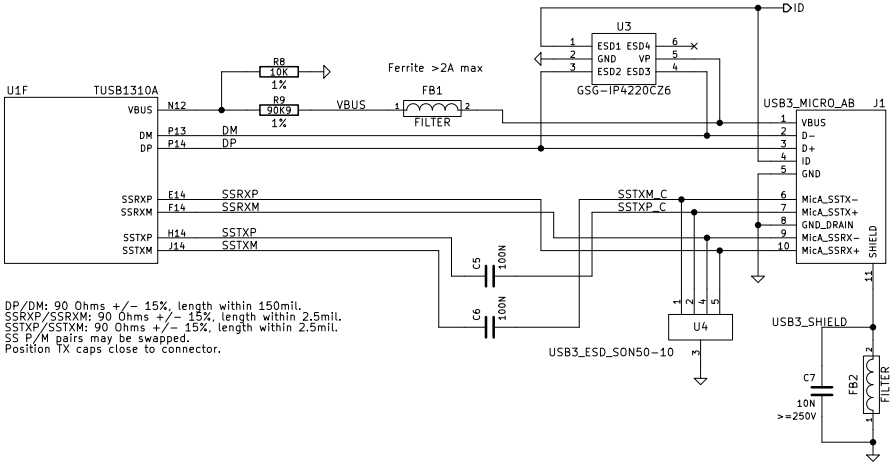
PHY_RESETN: Internal pull-up
RATE: Internal pull-up





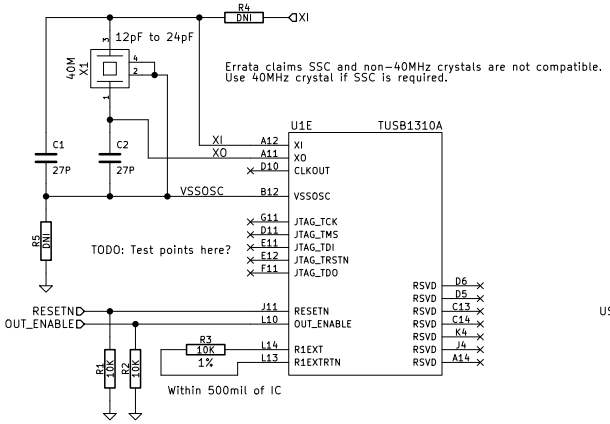
ULPI interface:

* 50 Ohms +/- 10%.

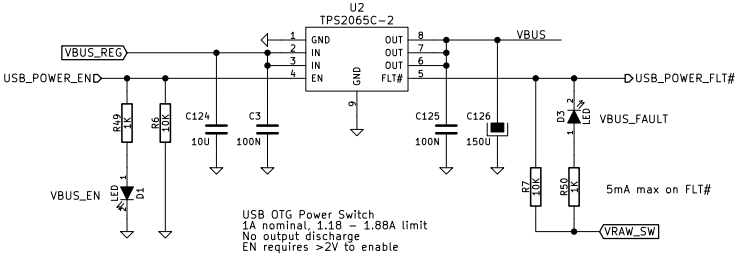


DP/DM: 90 Ohms +/- 15%, length within 150mil.
SSRXP/SSRXM: 90 Ohms +/- 15%, length within 2.5mil.
SSTXP/SSTXM: 90 Ohms +/- 15%, length within 2.5mil.
SS P/M pairs may be swapped.
Position TX caps close to connector.

18pF CL is OK, according to datasheet max/min specs.



RESETN, OUT_ENABLE pull-downs:
Hold PHY in reset, outputs hi-Z until supplies and clocks are stable, and FPGA configures strapping.



USB OTG Power Switch
1A nominal, 1.18 - 1.88A limit
No output discharge
EN requires >2V to enable

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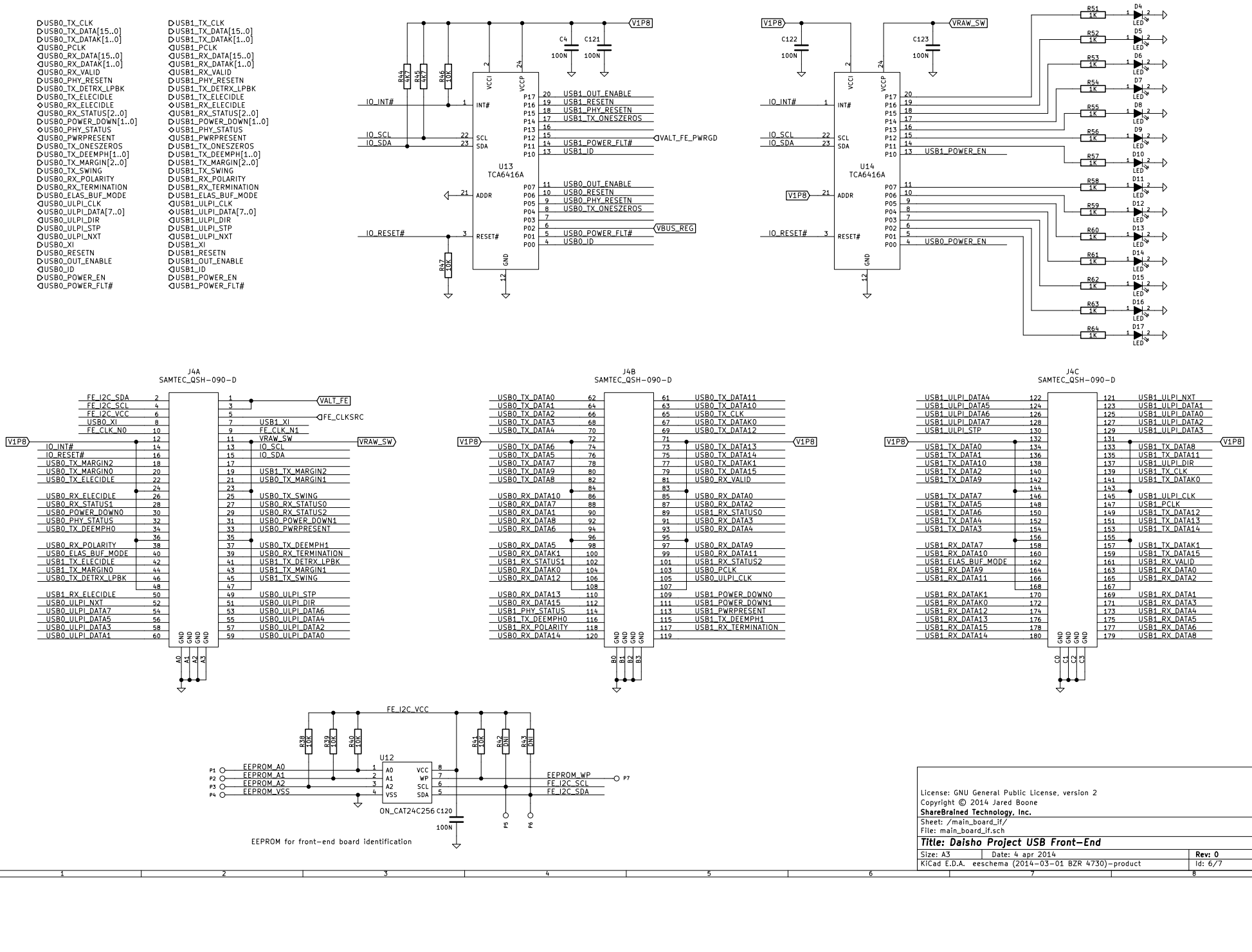
Sheet: /usb0_interfaces/		
File: usb0_interfaces.sch		
Title: Daisho Project USB Front-End		
Size: A3	Date: 4 apr 2014	**Rev: 0**
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product		Id: 5/7


USB0_TX_CLK
USB0_TX_DATA[15..0]
USB0_TX_DATAK[1..0]
USB0_PCLK
USB0_RX_DATA[15..0]
USB0_RX_DATAK[1..0]
USB0_RX_VALID
USB0_PHY_RESETN
USB0_TX_DETRX_LPBK
USB0_TX_ELECIDLE
USB0_RX_ELECIDLE
USB0_RX_STATUS[2..0]
USB0_POWER_DOWN[1..0]
USB0_PHY_STATUS
USB0_PWRPRESENT
USB0_TX_ONESZEROS
USB0_TX_DEEMPH[1..0]
USB0_TX_MARGIN[2..0]
USB0_TX_SWING
USB0_RX_POLARITY
USB0_RX_TERMINATION
USB0_ELAS_BUF_MODE
USB0_ULPI_CLK
USB0_ULPI_DATA[7..0]
USB0_ULPI_DIR
USB0_ULPI_STP
USB0_ULPI_NXT
USB0_XI
USB0_RESETN
USB0_OUT_ENABLE
USB0_ID
USB0_POWER_EN
USB0_POWER_FLT#
USB1_TX_CLK
USB1_TX_DATA[15..0]
USB1_TX_DATAK[1..0]
USB1_PCLK
USB1_RX_DATA[15..0]
USB1_RX_DATAK[1..0]
USB1_RX_VALID
USB1_PHY_RESETN
USB1_TX_DETRX_LPBK
USB1_TX_ELECIDLE
USB1_RX_ELECIDLE
USB1_RX_STATUS[2..0]
USB1_POWER_DOWN[1..0]
USB1_PHY_STATUS
USB1_PWRPRESENT
USB1_TX_ONESZEROS
USB1_TX_DEEMPH[1..0]
USB1_TX_MARGIN[2..0]
USB1_TX_SWING
USB1_RX_POLARITY
USB1_RX_TERMINATION
USB1_ELAS_BUF_MODE
USB1_ULPI_CLK
USB1_ULPI_DATA[7..0]
USB1_ULPI_DIR
USB1_ULPI_STP
USB1_ULPI_NXT
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USB1_RESETN
USB1_OUT_ENABLE
USB1_ID
USB1_POWER_EN
USB1_POWER_FLT#
V1P8
C4
100N
C121
100N
R44
4K7
R45
4K7
R46
10K
R47
10K
IO_INT#
IO_SCL
IO_SDA
IO_RESET#
U13
TCA6416A
VCCI
VCCP
INT#
SCL
SDA
ADDR
RESET#
GND
USB1_OUT_ENABLE
USB1_RESETN
USB1_PHY_RESETN
USB1_TX_ONESZEROS
USB1_POWER_FLT#
USB1_ID
USB0_OUT_ENABLE
USB0_RESETN
USB0_PHY_RESETN
USB0_TX_ONESZEROS
USB0_POWER_FLT#
USB0_ID
VALT_FE_PWRGD
VBUS_REG
C122
100N
C123
100N
VRAW_SW
U14
TCA6416A
USB1_POWER_EN
USB0_POWER_EN
R51
1K
R52
1K
R53
1K
R54
1K
R55
1K
R56
1K
R57
1K
R58
1K
R59
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R60
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R61
1K
R62
1K
R63
1K
R64
1K
D4
D5
D6
D7
D8
D9
D10
D11
D12
D13
D14
D15
D16
D17
LED
J4A
SAMTEC_QSH-090-D
FE_I2C_SDA
FE_I2C_SCL
FE_I2C_VCC
USB0_XI
FE_CLK_N0
IO_INT#
IO_RESET#
USB0_TX_MARGIN2
USB0_TX_MARGIN0
USB0_TX_ELECIDLE
USB0_RX_ELECIDLE
USB0_RX_STATUS1
USB0_POWER_DOWN0
USB0_PHY_STATUS
USB0_TX_DEEMPH0
USB0_RX_POLARITY
USB0_ELAS_BUF_MODE
USB1_TX_ELECIDLE
USB1_TX_MARGIN0
USB1_TX_DETRX_LPBK
USB1_RX_ELECIDLE
USB0_ULPI_NXT
USB0_ULPI_DATA7
USB0_ULPI_DATA5
USB0_ULPI_DATA3
USB0_ULPI_DATA1
USB0_TX_SWING
USB0_RX_STATUS0
USB0_RX_STATUS2
USB0_POWER_DOWN1
USB0_PWRPRESENT
USB0_TX_DEEMPH1
USB0_RX_TERMINATION
USB1_TX_DETRX_LPBK
USB1_TX_MARGIN1
USB1_TX_SWING
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USB0_ULPI_DIR
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USB0_ULPI_DATA4
USB0_ULPI_DATA2
USB0_ULPI_DATA0
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USB0_TX_MARGIN1
VALT_FE
FE_CLKSRC
FE_CLK_N1
VRAW_SW
IO_SCL
IO_SDA
J4B
SAMTEC_QSH-090-D
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USB0_TX_DATA1
USB0_TX_DATA2
USB0_TX_DATA3
USB0_TX_DATA4
USB0_TX_DATA6
USB0_TX_DATA5
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USB0_TX_DATA9
USB0_TX_DATA8
USB0_RX_DATA10
USB0_RX_DATA7
USB0_RX_DATA1
USB0_RX_DATA8
USB0_RX_DATA6
USB0_RX_DATA5
USB0_RX_DATAK1
USB1_RX_STATUS1
USB0_RX_DATAK0
USB0_RX_DATA12
USB0_RX_DATA13
USB0_RX_DATA15
USB1_PHY_STATUS
USB1_TX_DEEMPH0
USB1_RX_POLARITY
USB0_RX_DATA14
USB0_TX_DATA11
USB0_TX_DATA10
USB0_TX_CLK
USB0_TX_DATAK0
USB0_TX_DATA12
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USB0_TX_DATA14
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USB1_RX_TERMINATION
J4C
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USB1_ULPI_DATA5
USB1_ULPI_DATA6
USB1_ULPI_DATA7
USB1_ULPI_STP
USB1_TX_DATA0
USB1_TX_DATA1
USB1_TX_DATA10
USB1_TX_DATA2
USB1_TX_DATA9
USB1_TX_DATA7
USB1_TX_DATA5
USB1_TX_DATA6
USB1_TX_DATA4
USB1_TX_DATA3
USB1_RX_DATA7
USB1_RX_DATA10
USB1_ELAS_BUF_MODE
USB1_RX_DATA9
USB1_RX_DATA11
USB1_RX_DATAK1
USB1_RX_DATAK0
USB1_RX_DATA12
USB1_RX_DATA13
USB1_RX_DATA15
USB1_RX_DATA14
USB1_ULPI_NXT
USB1_ULPI_DATA1
USB1_ULPI_DATA0
USB1_ULPI_DATA2
USB1_ULPI_DATA3
USB1_TX_DATA8
USB1_TX_DATA11
USB1_ULPI_DIR
USB1_TX_CLK
USB1_TX_DATAK0
USB1_ULPI_CLK
USB1_PCLK
USB1_TX_DATA12
USB1_TX_DATA13
USB1_TX_DATA14
USB1_TX_DATAK1
USB1_TX_DATA15
USB1_RX_VALID
USB1_RX_DATA0
USB1_RX_DATA2
USB1_RX_DATA1
USB1_RX_DATA3
USB1_RX_DATA4
USB1_RX_DATA5
USB1_RX_DATA6
USB1_RX_DATA8
FE_I2C_VCC
R38
10K
R39
10K
R40
10K
R41
10K
R42
DNI
R43
DNI
U12
ON_CAT24C256
C120
100N
EEPROM_A0
EEPROM_A1
EEPROM_A2
EEPROM_VSS
EEPROM_WP
FE_I2C_SCL
FE_I2C_SDA
EEPROM for front-end board identification
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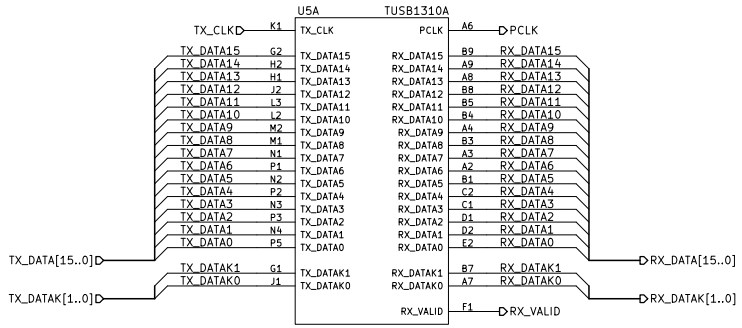
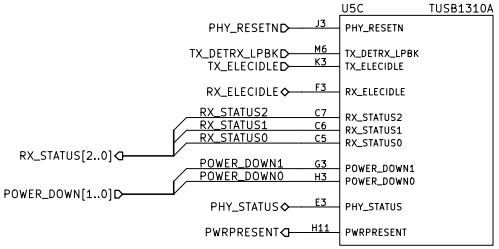
Sheet: /main_board_lf/
File: main_board_lf.sch
Title: Daisho Project USB Front-End
Size: A3
Date: 4 apr 2014
Rev: 0
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product
Id: 6/7

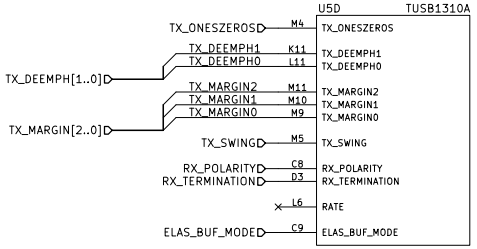


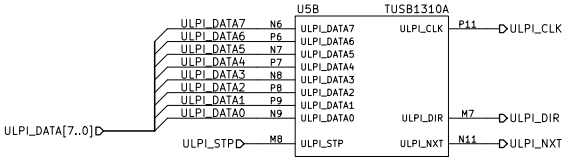
PIPE interfaces:

* Match lengths to <250mil.
* Length <2" if no termination.
* 50 Ohms +/- 10%.
* PHY_STATUS, RX_STATUS[2..0] timed to PCLK.



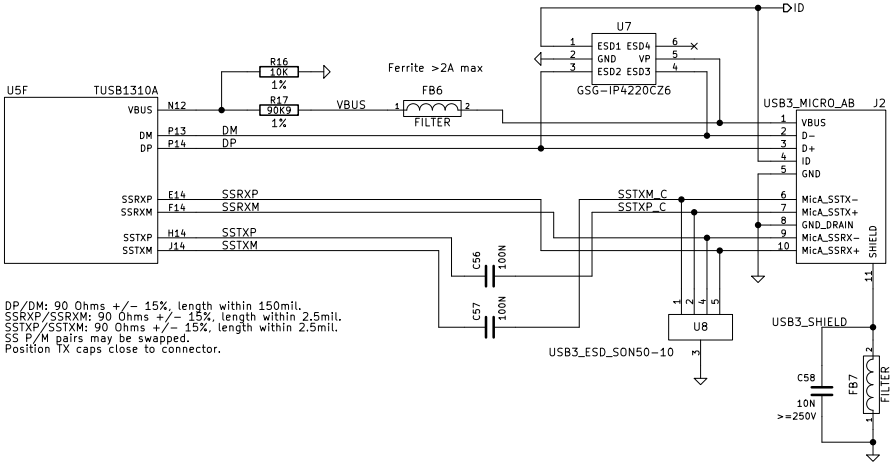
PHY_RESETN: Internal pull-up
RATE: Internal pull-up





ULPI interface:

* 50 Ohms +/- 10%.



DP/DM: 90 Ohms +/- 15%, length within 150mil.
SSRXP/SSRXM: 90 Ohms +/- 15%, length within 2.5mil.
SSTXP/SSTXM: 90 Ohms +/- 15%, length within 2.5mil.
SS P/M pairs may be swapped.
Position TX caps close to connector.

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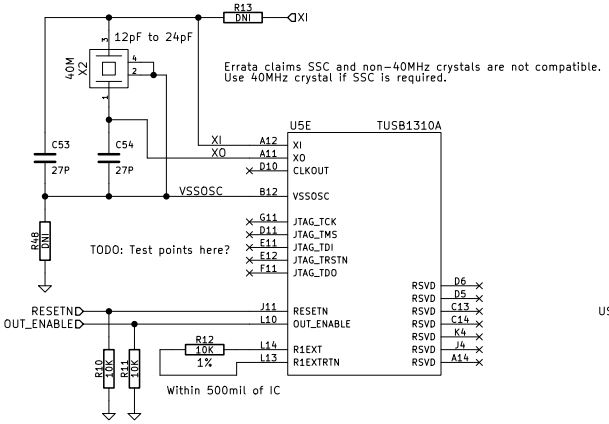
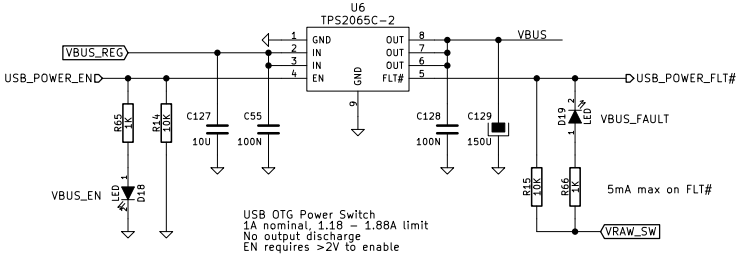


Errata claims SSC and non-40MHz crystals are not compatible.
Use 40MHz crystal if SSC is required.

RESETN, OUT_ENABLE pull-downs:
Hold PHY in reset, outputs hi-Z until supplies and clocks are stable, and FPGA configures strapping.



USB OTG Power Switch
1A nominal, 1.18 - 1.88A limit
No output discharge
EN requires >2V to enable

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Sheet: /usb1_interfaces/	
File: usb1_interfaces.sch	
Title: Daisho Project USB Front-End	
Size: A3	Date: 4 apr 2014
KiCad E.D.A. eeschema (2014-03-01 BZR 4730)-product	**Rev: 0**
	Id: 7/7