ESP32-S3

Datasheet

2.4 GHz Wi-Fi + Bluetooth LE SoC

Supporting IEEE 802.11 b/g/n and Bluetooth 5

Prerelease version 0.3
Espressif System

Product Overview

ESP32-S3 is a low-power MCU-based SoC that supports 2.4 GHz Wi-Fi and Bluetooth® Low Energy (Bluetooth LE). It has:

- A complete Wi-Fi subsystem that complies with IEEE 802.11b/g/n protocol and supports Station, SoftAP, and SoftAP + Station modes
- A Bluetooth LE subsystem that supports features of Bluetooth 5 and Bluetooth mesh
- State-of-the-art power and RF performance
- Xtensa® 32-bit LX7 dual-core processor with a five-stage pipeline that operates at up to 240 MHz
  - A 128-bit data bus and dedicated SIMD commands to provide high computing performance
  - Efficient L1 cache to improve execution of external memory
- Powerful storage capacities ensured by 512 KB of SRAM and 384 KB of ROM on the chip, and SPI, Dual SPI, Quad SPI, Octal SPI, QPI, and OPI interfaces that allow connection to flash and external RAM
- Reliable security features ensured by
  - Cryptographic hardware accelerators that support AES-128/256, Hash, RSA, HMAC, digital signature and secure boot
  - Random number generator
  - Permission control on accessing internal and external memory
  - External memory encryption and decryption
- Rich set of peripheral interfaces and GPIOs, ideal for various scenarios and complex applications

Block Diagram

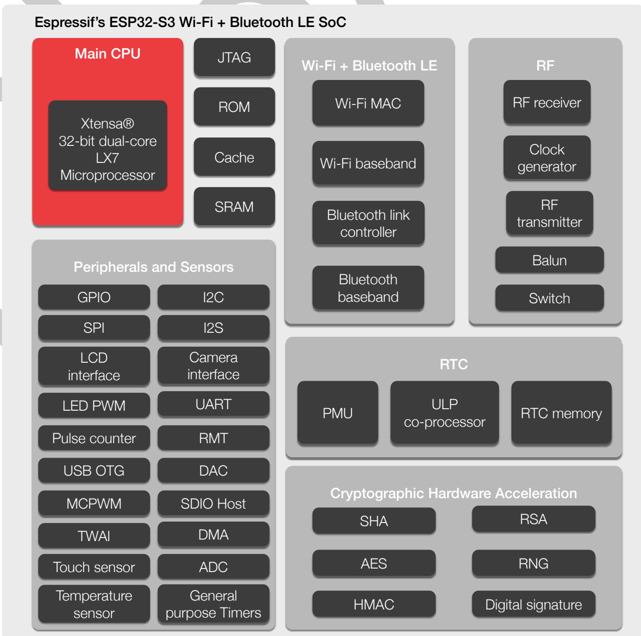

Figure 1: Block Diagram of ESP32-S3

Features

Wi-Fi

- IEEE 802.11 b/g/n-compliant
- Supports 20 MHz, 40 MHz bandwidth in 2.4 GHz band
- 1T1R mode with data rate up to 150 Mbps
- Wi-Fi Multimedia (WMM)
- TX/RX A-MPDU, RX A-MSDU
- Immediate Block ACK
- Fragmentation and defragmentation
- Automatic Beacon monitoring (hardware TSF)
- 4 × virtual Wi-Fi interfaces
- Simultaneous support for Infrastructure BSS in Station, SoftAP, or Station + SoftAP modes
  Note that when ESP32-S3 scans in Station mode, the SoftAP channel will change along with the Station channel
- Antenna diversity
- 802.11mc FTM

Bluetooth

- Bluetooth LE: Bluetooth 5, Bluetooth mesh
- 2 Mbps PHY
- Long range mode
- Advertising extensions
- Multiple advertisement sets
- Channel selection algorithm #2

CPU and Memory

- Xtensa® dual-core 32-bit LX7 microprocessor, up to 240 MHz
- 128-bit data bus and SIMD commands
- 384 KB ROM
- 512 KB SRAM
- 16 KB SRAM in RTC
- SPI, Dual SPI, Quad SPI, Octal SPI, QPI and OPI interfaces that allow connection to multiple flash and external RAM

Advanced Peripheral Interfaces

- 44 × programmable GPIOs
- 2 × 12-bit SAR ADCs, up to 20 channels
- 2 × 8-bit DAC
- 1 × temperature sensor
- 14 × touch sensing IOs
- 4 × SPI
- 1 × LCD interface (8-bit ~16-bit parallel RGB, I8080 and MOTO6800), supporting conversion between RGB565, YUV422, YUV420 and YUV411
- 1 × DVP 8-bit ~16-bit camera interface
- 3 × UART
- 2 × I2C
- 2 × I2S
- 4 × RMT (TX/RX)
- 1 × pulse counter
- LED PWM controller, up to eight channels
- 1 × full-speed USB OTG
- 2 × SDIO host interfaces
- 2 × MCPWM
- DMA controller, with five transmit channels and 5 receive channels
- 1 × TWAI™ controller (compatible with ISO 11898-1)

Low Power Management

- Power Management Unit with five power modes
- Ultra-Low-Power (ULP) co-processors:
  - ULP-RISC-V co-processor
  - ULP-FSM co-processor

Security

- Secure boot
- Flash encryption
- 4096-bit OTP, up to 1760 bits for users
- Cryptographic hardware acceleration:
  - AES-128/256 (FIPS PUB 197)
  - Hash (FIPS PUB 180-4)
  - RSA
  - Random Number Generator (RNG)
  - HMAC
  - Digital signature

Applications (A Non-exhaustive List)

With ultra-low power consumption, ESP32-S3 is an ideal choice for IoT devices in the following areas:

- Smart Home
  - Light control
  - Smart button
  - Smart plug
- Industrial Automation
  - Industrial robot
  - Mesh network
  - Human machine interface (HMI)
- Health Care
  - Health monitor
  - Baby monitor
- Consumer Electronics
  - Smart watch and bracelet
  - Over-the-top (OTT) devices
  - Wi-Fi and bluetooth speaker
  - Logger toys and proximity sensing toys
- Smart Agriculture
  - Smart greenhouse
  - Smart irrigation
  - Agriculture robot
- Retail and Catering
  - POS machines
  - Service robot
- Audio Device
  - Internet music players
  - Live streaming devices
  - Internet radio players
- Generic Low-power IoT Sensor Hubs
- Generic Low-power IoT Data Loggers
- Cameras for Video Streaming
- USB Devices
- Speech Recognition
- Image Recognition
- SDIO Dual-Mode Network
- Touch Sensing
  - Waterproof design
  - Distance sensing applications
  - Linear slider, wheel slider designs

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1.1 Pin Layout

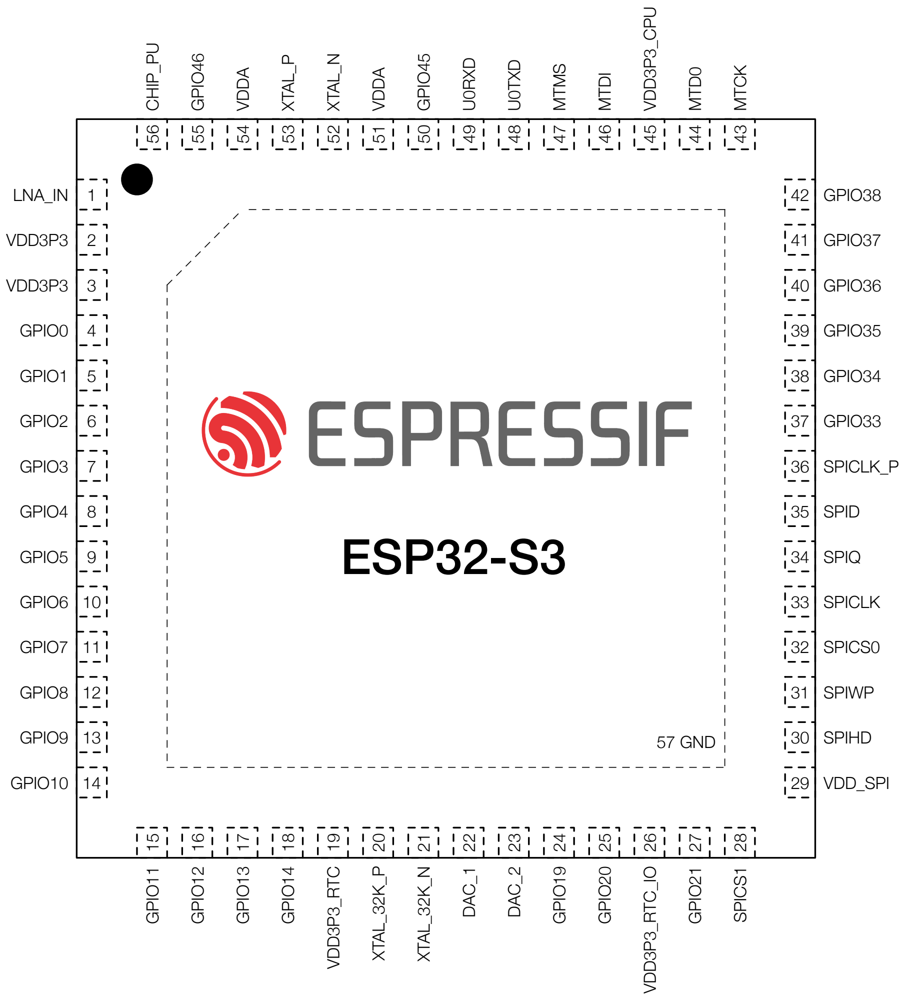

Figure 2: ESP32-S3 Pin Layout (Top View)

1.2 Pin Description

Table 1: Pin Description

Name	No.	Type	Power domain	Function
LNA_IN	1	I/O	—	RF input and output
VDD3P3	2	P_A	—	Analog power supply
VDD3P3	3	P_A	—	Analog power supply
GPIO0	4	I/O/T	VDD3P3_RTC_IO	RTC_GPIO0, GPIO0
GPIO1	5	I/O/T	VDD3P3_RTC_IO	RTC_GPIO1, GPIO1, TOUCH1, ADC1_CH0
GPIO2	6	I/O/T	VDD3P3_RTC_IO	RTC_GPIO2, GPIO2, TOUCH2, ADC1_CH1
GPIO3	7	I/O/T	VDD3P3_RTC_IO	RTC_GPIO3, GPIO3, TOUCH3, ADC1_CH2
GPIO4	8	I/O/T	VDD3P3_RTC_IO	RTC_GPIO4, GPIO4, TOUCH4, ADC1_CH3
GPIO5	9	I/O/T	VDD3P3_RTC_IO	RTC_GPIO5, GPIO5, TOUCH5, ADC1_CH4
GPIO6	10	I/O/T	VDD3P3_RTC_IO	RTC_GPIO6, GPIO6, TOUCH6, ADC1_CH5
GPIO7	11	I/O/T	VDD3P3_RTC_IO	RTC_GPIO7, GPIO7, TOUCH7, ADC1_CH6
GPIO8	12	I/O/T	VDD3P3_RTC_IO	RTC_GPIO8, GPIO8, TOUCH8, ADC1_CH7, SUBSPICS1
GPIO9	13	I/O/T	VDD3P3_RTC_IO	RTC_GPIO9, GPIO9, TOUCH9, ADC1_CH8, SUBSPIHD, FSPIHD
GPIO10	14	I/O/T	VDD3P3_RTC_IO	RTC_GPIO10, GPIO10, TOUCH10, ADC1_CH9, FSPIIO4, SUBSPICS0, FSPICS0
GPIO11	15	I/O/T	VDD3P3_RTC_IO	RTC_GPIO11, GPIO11, TOUCH11, ADC2_CH0, FSPIIO5, SUBSPID, FSPID
GPIO12	16	I/O/T	VDD3P3_RTC_IO	RTC_GPIO12, GPIO12, TOUCH12, ADC2_CH1, FSPIIO6, SUBSPICLK, FSPICLK
GPIO13	17	I/O/T	VDD3P3_RTC_IO	RTC_GPIO13, GPIO13, TOUCH13, ADC2_CH2, FSPIIO7, SUBSPIQ, FSPIQ
GPIO14	18	I/O/T	VDD3P3_RTC_IO	RTC_GPIO14, GPIO14, TOUCH14, ADC2_CH3, FSPIDQS, SUBSPIWP, FSPIWP
VDD3P3_RTC	19	P_A	—	Analog power supply
XTAL_32K_P	20	I/O/T	VDD3P3_RTC_IO	RTC_GPIO15, GPIO15, U0RTS, ADC2_CH4, XTAL_32K_P
XTAL_32K_N	21	I/O/T	VDD3P3_RTC_IO	RTC_GPIO16, GPIO16, U0CTS, ADC2_CH5, XTAL_32K_N
DAC_1	22	I/O/T	VDD3P3_RTC_IO	RTC_GPIO17, GPIO17, U1TXD, ADC2_CH6, DAC_1
DAC_2	23	I/O/T	VDD3P3_RTC_IO	RTC_GPIO18, GPIO18, U1RXD, ADC2_CH7, DAC_2, CLK_OUT3
GPIO19	24	I/O/T	VDD3P3_RTC_IO	RTC_GPIO19, GPIO19, U1RTS, ADC2_CH8, CLK_OUT2, USB_D-
GPIO20	25	I/O/T	VDD3P3_RTC_IO	RTC_GPIO20, GPIO20, U1CTS, ADC2_CH9, CLK_OUT1, USB_D+
VDD3P3_RTC_IO	26	P_D	VDD3P3_RTC_IO	Input power supply for RTC IO

Name	No.	Type	Power domain	Function
GPIO21	27	I/O/T	VDD3P3_RTC_IO	RTC_GPIO21, GPIO21
SPICS1	28	I/O/T	VDD_SPI	SPICS1, GPIO26
VDD_SPI	29	P_D	—	Output power supply: 1.8 V or VDD3P3_RTC_IO
SPIHD	30	I/O/T	VDD_SPI	SPIHD GPIO27
SPIWP	31	I/O/T	VDD_SPI	SPIWP GPIO28
SPICS0	32	I/O/T	VDD_SPI	SPICS0 GPIO29
SPICLK	33	I/O/T	VDD_SPI	SPICLK GPIO30
SPIQ	34	I/O/T	VDD_SPI	SPIQ GPIO31
SPID	35	I/O/T	VDD_SPI	SPID GPIO32
SPICLK_P	36	I/O/T	VDD_SPI	SPICLK_P GPIO47 SUBSPICLK_DIFF
GPIO33	37	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO4, GPIO33, FSPIHD, SUBSPIHD
GPIO34	38	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO5, GPIO34, FSPICS0, SUBSPICS0
GPIO35	39	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO6, GPIO35, FSPID, SUBSPID
GPIO36	40	I/O/T	VDD3P3_CPU / VDD_SPI	SPIIO7, GPIO36, FSPICLK, SUBSPICLK
GPIO37	41	I/O/T	VDD3P3_CPU / VDD_SPI	SPIDQS, GPIO37, FSPIQ, SUBSPIQ
GPIO38	42	I/O/T	VDD3P3_CPU	GPIO38, FSPIWP, SUBSPIWP
MTCK	43	I/O/T	VDD3P3_CPU	MTCK, GPIO39, CLK_OUT3, SUBSPICS1
MTDO	44	I/O/T	VDD3P3_CPU	MTDO, GPIO40, CLK_OUT2
VDD3P3_CPU	45	P_D	—	Input power supply for CPU IO
MTDI	46	I/O/T	VDD3P3_CPU	MTDI, GPIO41, CLK_OUT1
MTMS	47	I/O/T	VDD3P3_CPU	MTMS, GPIO42
U0TXD	48	I/O/T	VDD3P3_CPU	U0TXD, GPIO43, CLK_OUT1
U0RXD	49	I/O/T	VDD3P3_CPU	U0RXD, GPIO44, CLK_OUT2
GPIO45	50	I/O/T	VDD3P3_CPU	GPIO45
VDDA	51	P_A	—	Analog power supply
XTAL_N	52	—	—	External crystal output
XTAL_P	53	—	—	External crystal input
VDDA	54	P_A	—	Analog power supply
GPIO46	55	I	VDD3P3_CPU	GPIO46

Name	No.	Type	Power domain	Function
CHIP_PU	56	I	VDD3P3_RTC_IO	High: on, enables the chip. Low: off, the chip powers off. Note: Do not leave the CHIP_PU pin floating.
GND	57	G	—	Ground

Note:

1. P: power pin; I: input; O: output; T: high impedance.
2. ESP32-S3's pins SPIHD, SPIWP, SPICS0, SPICLK, SPIQ and SPID are used for connecting the embedded flash and external RAM, and are not recommended for other uses.
3. For the data port connection between ESP32-S3 and external flash please refer to Section 2.4.2.
4. Power supply for GPIO33, GPIO34, GPIO35, GPIO36 and GPIO37 is configurable to be either VDD3P3_CPU (default) or VDD_SPI.
5. The pin function in this table refers only to some fixed settings and do not cover all cases for signals that can be input and output through the GPIO matrix. For more information on the GPIO matrix, please refer to ESP32-S3 Technical Reference Manual.

1.3 Power Scheme

ESP32-S3's digital pins are divided into four different power domains:

- VDD3P3_RTC_IO
- VDD3P3_CPU
- VDD_SPI
- VDD3P3_RTC

VDD3P3_RTC_IO is the input power supply for RTC and CPU.

VDD3P3_CPU is the input power supply for CPU.

VDD_SPI can be an input power supply or an output power supply. VDD_SPI connects to the output of an internal LDO whose input is VDD3P3_RTC_IO. When VDD_SPI is connected to the same PCB net together with VDD3P3_RTC_IO, the internal LDO should be disabled.

VDD3P3_RTC is the input power supply for RTC analog domain.

The power scheme diagram is shown in Figure 3.

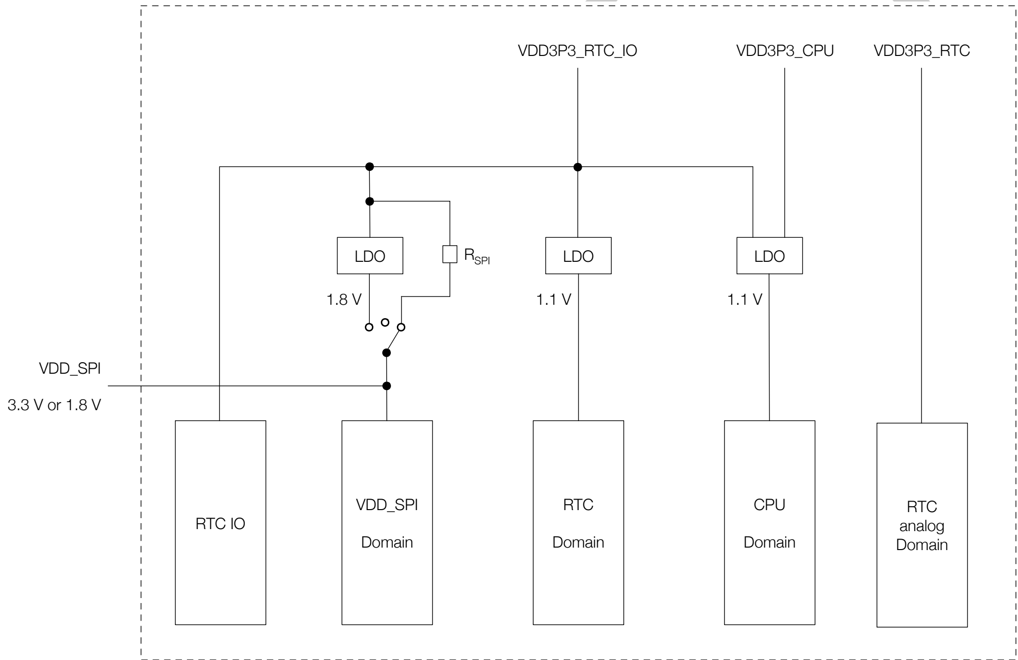

Figure 3: ESP32-S3 Power Scheme

The VDD_SPI voltage can be configured at 1.8 V using an internal LDO, or powered by VDD3P3_RTC_IO via R$_{SPI}$ (nominal 3.3 V). The VDD_SPI can be powered off via software to minimize the current leakage of flash in Deep-sleep mode.

1.4 Strapping Pins

ESP32-S3 has three strapping pins:

- GPIO0
- GPIO45
- GPIO46

Software can read the values of corresponding bits from register "GPIO_STRAPPING".

During the chip's system reset (power-on-reset, RTC watchdog reset, brownout reset, analog super watchdog reset, and crystal clock glitch detection reset), the latches of the strapping pins sample the voltage level as strapping bits of "0" or "1", and hold these bits until the chip is powered down or shut down.

GPIO0, GPIO45 and GPIO46 are connected to the chip's internal pull-up/pull-down during the chip reset. Consequently, if they are unconnected or the connected external circuit is high-impedance, the internal weak pull-up/pull-down will determine the default input level of these strapping pins.

To change the strapping bit values, users can apply the external pull-down/pull-up resistances, or use the host MCU's GPIOs to control the voltage level of these pins when powering on ESP32-S3.

After reset, the strapping pins work as normal-function pins.

Refer to Table 2 for a detailed boot-mode configuration of the strapping pins.

Table 2: Strapping Pins

VDD_SPI Voltage [1]			
Pin	Default	3.3 V	1.8 V
GPIO45	Pull-down	0	1
Booting Mode [2]			
Pin	Default	SPI Boot	Download Boot
GPIO0	Pull-up	1	0
GPIO46	Pull-down	Don't care	0
Enabling/Disabling ROM Code Print During Booting [3] [4]			
Pin	Default	Enabled	Disabled
GPIO46	Pull-down	See the fourth note	See the fourth note

Note:

1. The functionality of strapping pin GPIO45 to select VDD_SPI voltage may be disabled by setting VDD_SPI_FORCE eFuse to 1. In such a case the voltage is selected with eFuse bit VDD_SPI_TIEH.
2. The strapping combination of GPIO46 = 1 and GPIO0 = 0 is invalid and will trigger unexpected behavior.
3. ROM code can be printed over U0TXD (by default) or DAC_1, depending on the eFuse bit.
4. When eFuse UART_PRINT_CONTROL value is:
   0, print is normal during boot and not controlled by GPIO46.
   1 and GPIO46 is 0, print is normal during boot; but if GPIO46 is 1, print is disabled.
   2 and GPIO46 is 0, print is disabled; but if GPIO46 is 1, print is normal.
   3, print is disabled and not controlled by GPIO46.

2. Functional Description

2.1 CPU and Memory

2.1.1 CPU

ESP32-S3 has a low-power Xtensa® dual-core 32-bit LX7 microprocessor with the following features:

- five-stage pipeline that supports the clock frequency of up to 240 MHz
- 16-bit/24-bit instruction set providing high code-density
- 32-bit customized instruction set and 128-bit data bus that provide high computing performance
- 32-bit multiplier and 32-bit divider
- unbuffered GPIO instructions
- 32 interrupts at six levels
- windowed ABI with 64 physical general registers
- trace function with TRAX compressor, up to 16 KB trace memory
- JTAG for debugging

2.1.2 Internal Memory

ESP32-S3's internal memory includes:

- **384 KB of ROM**: for booting and core functions
- **512 KB of on-chip SRAM**: for data and instructions
- **RTC FAST memory**: 8 KB of SRAM that can be accessed by the main CPU. It can retain data in Deep-sleep mode.
- **RTC SLOW Memory**: 8 KB of SRAM that can be accessed by the main CPU or co-processors. It can retain data in Deep-sleep mode.
- **4 kbit of eFuse**: 1760 bits are reserved for user data, such as encryption key and device ID.

2.1.3 External Flash and RAM

ESP32-S3 supports SPI, Dual SPI, Quad SPI, Octal SPI, QPI and OPI interfaces that allow connection to multiple external flash and RAM.

The external flash and RAM can be mapped into the CPU instruction memory space and read-only data memory space. The RAM can also be mapped into the CPU data memory space. ESP32-S3 supports up to 1 GB of external flash and RAM, and hardware encryption/decryption based on XTS-AES to protect developers' programs and data in flash and RAM.

Through high-speed caches, ESP32-S3 can support at a time up to:

- 32 MB of instruction memory space which can be mapped into flash and external RAM as individual blocks of 64 KB.
- 32 MB of data memory space which can be mapped into external RAM as individual blocks of 64 KB. 8-bit, 16-bit and 32-bit reads and writes are supported. Such data memory space can also be read-only and mapped into flash, supporting 8-bit, 16-bit, 32-bit and 128-bit reads.

Note:
After ESP32-S3 is initialized, firmware can customize the mapping of external RAM or flash into the CPU address space.

2.1.4 Address Mapping Structure

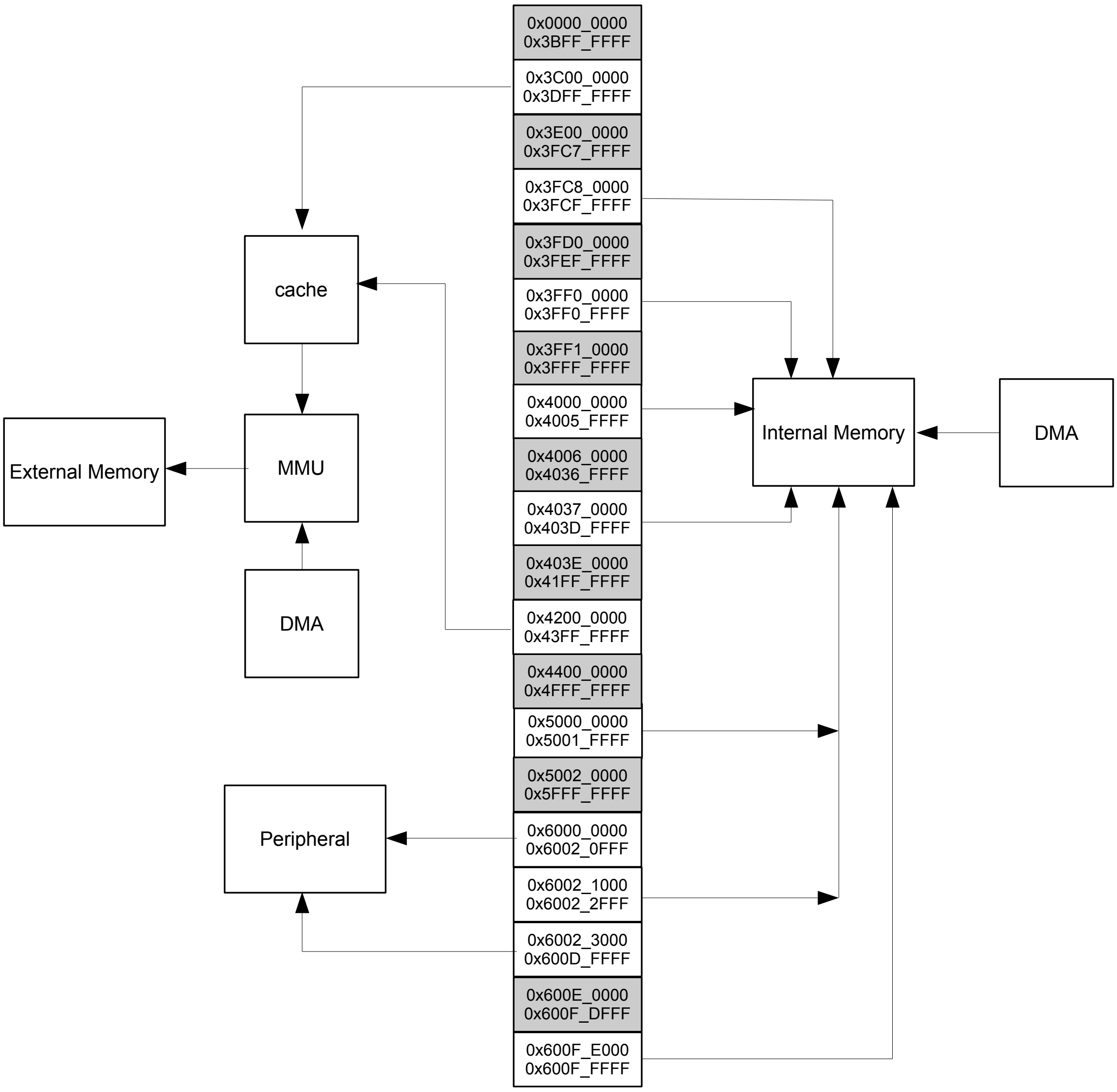

Figure 4: Address Mapping Structure

> **Note:**
> The memory space with gray background is not available to users.

2.1.5 Cache

ESP32-S3 has an instruction cache and a data cache shared by the two CPU cores. Each cache can be partitioned into multiple banks and have the following features:

- instruction cache: 16 KB (one bank) or 32 KB (two banks)
  data cache: 32 KB (one bank) or 64 KB (two banks)
- instruction cache: four-channel or eight-channel group association

data cache: four-channel group association

- block size of 16 bytes or 32 bytes for both instruction cache and data cache
- pre-load function
- lock function
- critical word first and early restart

2.2 System Clocks

2.2.1 CPU Clock

The CPU clock has three possible sources:

- external main crystal clock
- internal 8 MHz oscillator
- PLL clock

The application can select the clock source from the three clocks above. The selected clock source drives the CPU clock directly, or after division, depending on the application.

2.2.2 RTC Clock

The RTC slow clock is used for RTC counter, RTC watchdog and low-power controller. It has three possible sources:

- external low-speed (32 kHz) crystal clock
- internal RC oscillator (typically about 90 kHz, and adjustable)
- internal 31.25 kHz clock (derived from the internal 8 MHz oscillator divided by 256)

The RTC fast clock is used for RTC peripherals and sensing controllers. It has two possible sources:

- external crystal clock divided by 4
- internal 8 MHz oscillator

2.3 Analog Peripherals

2.3.1 Analog-to-Digital Converter (ADC)

ESP32-S3 integrates two 12-bit SAR ADCs and supports measurements on 20 channels (analog-enabled pins). ULP coprocessors in ESP32-S3 can also measure voltage in sleep modes. By using threshold settings or other methods, we can awaken the CPU from sleep modes.

2.3.2 Digital-to-Analog Converter (DAC)

ESP32-S3 has two 8-bit DAC channels that convert two digital signals into two analog voltage signal outputs. The two DAC channels can convert signals independently. The DAC circuit consists of built-in resistor strings and a buffer. This dual DAC supports VDD3P3_RTC_IO power supply as input voltage reference.

2.3.3 Temperature Sensor

The temperature sensor generates a voltage that varies with temperature. The voltage is internally converted via an ADC into a digital value.

The temperature sensor has a range of –20 °C to 110 °C. It is designed primarily to sense the temperature changes inside the chip. The temperature value depends on factors like microcontroller clock frequency or I/O load. Generally, the chip's internal temperature is higher than the ambient temperature.

2.3.4 Touch Sensor

ESP32-S3 has 14 capacitive-sensing GPIOs, which detect variations induced by touching or approaching the GPIOs with a finger or other objects. The low-noise nature of the design and the high sensitivity of the circuit allow relatively small pads to be used. Arrays of pads can also be used, so that a larger area or more points can be detected. The touch sensing performance can be further enhanced by the waterproof design and digital filtering feature.

2.4 Digital Peripherals

2.4.1 General Purpose Input / Output Interface (GPIO)

ESP32-S3 has 44 GPIO pins which can be assigned various functions by configuring corresponding registers. Besides digital signals, some GPIOs can be also used for analog functions, such as ADC, DAC and touch sensing.

All GPIOs have selectable internal pull-up or pull-down, or can be set to high impedance, except for GPIO46, which is fixed to pull-down. When these GPIOs are configured as an input, the input value can be read by software through the register. Input GPIOs can also be set to generate edge-triggered or level-triggered CPU interrupts. Except for GPIO46 (input only), all digital IO pins are bi-directional, non-inverting and tristate, including input and output buffers with tristate control. These pins can be multiplexed with other functions, such as the UART, SPI, etc. For low-power operations, the GPIOs can be set to holding state.

The IO MUX and the GPIO matrix are used to route signals from peripherals to GPIO pads. Together they provide highly configurable I/O. Using GPIO Matrix, peripheral input signals can be configured from any IO pads while peripheral output signals can be configured to any IO pad except GPIO46. For more information about IO MUX and GPIO matrix, please refer to Figure *5 IO MUX* and ESP32-S3 Technical Reference Manual.

2.4.2 Serial Peripheral Interface (SPI)

ESP32-S3 features four SPI interfaces (SPI0, SPI1, SPI2 and SPI3). SPI0 and SPI1 can only be configured to operate in SPI memory mode; SPI2 can be configured to operate in SPI memory and general-purpose SPI modes; SPI3 can only be configured to operate in general-purpose SPI mode.

- **SPI Memory mode**

  In SPI memory mode, SPI0, SPI1 and SPI2 interface with external SPI memory. Data transmission is in multiples of bytes. Up to 8-line STR/DDR reads and writes are supported. The clock frequency is configurable to a maximum of 120 MHz in STR mode and a maximum of 80 MHz in DDR mode.

- **SPI2 General-purpose SPI (GP-SPI) mode**

  When SPI2 acts as a general-purpose SPI, it can operate in master and slave modes. The master mode supports two-line full-duplex communication and single-/two-/four-/eight-line half-duplex communication. The slave mode supports two-line full-duplex communication and single-/two-/four-line half-duplex communication. The host's clock frequency is configurable. Data transmission is in multiples of bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI2 interface supports DMA.

  - In two-line full-duplex communication mode, the host's clock frequency is configurable to 80 MHz at most, and the slave's clock frequency to 80 MHz at most. Four modes of SPI transfer format are supported.
  - In single-/two-/four-/eight-line half-duplex communication mode, the host's clock frequency is configurable to 80 MHz at most and the four modes of SPI transfer format are supported.
  - In single-/two-/four-line half-duplex communication mode, the slave's clock frequency is configurable to 40 MHz at most, and the four modes of SPI transfer format are also supported.

- **SPI3 General-purpose SPI (GP-SPI) mode**

  As a general-purpose SPI interface, SPI3 can operate in master and slave modes, in two-line full-duplex and single-line, two-line and four-line half-duplex communication modes. The host's clock frequency is configurable. Data transmission is in multiples of bytes. The clock polarity (CPOL) and phase (CPHA) are also configurable. The SPI3 interface supports DMA.

  - In two-line full-duplex communication mode, both the host's and the slave's clock frequency are configurable to a maximum of 80 MHz. Four modes of SPI transfer format are supported.
  - In single-line, two-line and four-line half-duplex communication mode, the host's clock frequency is configurable to a maximum of 80 MHz, and the slave's clock frequency to 40 MHz at most. The four modes of SPI transfer format are supported.

In most cases, the data port connection between ESP32-S3 and external flash is as follows:

SPI eight-line mode:

- SPID (SPID) = IO0
- SPIQ (SPIQ) = IO1
- SPIWP (SPIWP) = IO2
- SPIHD (SPIHD) = IO3
- GPIO33 = IO4
- GPIO34 = IO5
- GPIO35 = IO6
- GPIO36 = IO7
- GPIO37 = DQS

SPI four-line mode:

- SPID (SPID) = IO0
- SPIQ (SPIQ) = IO1
- SPIWP (SPIWP) = IO2
- SPIHD (SPIHD) = IO3

SPI two-line mode:

- SPID (SPID) = IO0

- SPIQ (SPIQ) = IO1

SPI single-line mode:

- SPIQ (SPIQ) = DO
- SPID (SPID) = DI
- SPIHD (SPIHD) = HOLD#
- SPIWP (SPIWP) = WP#

2.4.3 LCD Interface

ESP32-S3 supports 8-bit ~16-bit parallel RGB, I8080 and MOTO6800 interfaces. These interfaces operate at 40 MHz or lower, and support conversion among RGB565, YUV422, YUV420 and YUV411.

2.4.4 Camera Interface

ESP32-S3 supports an 8-bit ~16-bit DVP image sensor, with clock frequency of up to 40 MHz. The camera interface supports conversion among RGB565, YUV422, YUV420 and YUV411.

2.4.5 Universal Asynchronous Receiver Transmitter (UART)

ESP32-S3 has three UART interfaces, i.e., UART0, UART1, and UART2, which support IrDA and asynchronous communication (RS232 and RS485) at a speed of up to 5 Mbps. The UART controller provides hardware management of the CTS and RTS signals and software flow control (XON and XOFF). All of the interfaces can be accessed by the DMA controller or directly by the CPU.

2.4.6 I2C Interface

ESP32-S3 has two I2C bus interfaces which are used for I2C master mode or slave mode, depending on the user's configuration. The I2C interfaces support:

- standard mode (100 kbit/s)
- fast mode (400 kbit/s)
- up to 800 kbit/s (constrained by SDA pull-up strength)
- 7-bit and 10-bit addressing mode
- double addressing mode

Users can configure instruction registers to control I2C interfaces for more flexibility.

2.4.7 I2S Interface

ESP32-S3 includes two standard I2S interfaces. They can operate in master mode or slave mode, in full-duplex mode or half-duplex communication mode, and can be configured to operate with an 8-bit, 16-bit, 24-bit, or 32-bit resolution as an input or output channel. BCK clock frequency, from 10 kHz up to 40 MHz, is supported.

The I2S interface has a dedicated DMA controller. PCM interface is supported.

2.4.8 Remote Control Peripheral

The Remote Control Peripheral (RMT) supports four channels of infrared remote transmission and four channels of infrared remote reception. By controlling pulse waveform through software, it supports various infrared and other single wire protocols. All eight channels share a 384 × 32-bit memory block to store transmit or receive waveform.

2.4.9 Pulse Counter

The pulse counter captures pulse and counts pulse edges through multiple modes. It has four channels, each of which captures four signals at a time. The four input signals include two pulse signals and two control signals.

2.4.10 LED PWM Controller

The LED PWM controller can generate independent digital waveform on eight channels. The LED PWM controller:

- can generate digital waveform with configurable periods and duty cycle. The accuracy of duty cycle can be up to 18 bits within a 1 ms period.
- has multiple clock sources, including APB clock and external crystal clock.
- can operate when the CPU is in Light-sleep mode.
- supports gradual increase or decrease of duty cycle, which is useful for the LED RGB color-gradient generator.

2.4.11 USB 1.1 OTG

ESP32-S3 features a full-speed USB OTG interface which is compliant with the USB 1.1 specification. It has the following features:

- software-configurable endpoint settings and suspend/resume
- dynamic FIFO size
- session request protocol (SRP) and host negotiation protocol (HNP)
- a full-speed USB PHY integrated in the chip

2.4.12 Motor Control PWM (MCPWM)

ESP32-S3 integrates two MCPWM that can be used to drive digital motors and smart light. This controller includes PWM timers, PWM operators, and a dedicated capture submodule.

PWM timers can be synchronized or work independently.

Each PWM operator generate waveform for one PWM channel.

The dedicated capture submodule can accurately capture external timing events.

2.4.13 SD/MMC Host Controller

ESP32-S3 has an SD/MMC Host Controller with the following features:

- Secure Digital (SD) memory version 3.0 and version 3.01
- Secure Digital I/O (SDIO) version 3.0
- Consumer Electronics Advanced Transport Architecture (CE-ATA) version 1.1
- Multimedia Cards (MMC version 4.41, eMMC version 4.5 and version 4.51)

The controller allows up to 80 MHz clock output in 1-bit, 4-bit or 8-bit data bus mode. In 4-bit mode, ESP32-S3 supports two SD/SDIO/MMC 4.41 cards, and one SD card operating at 1.8 V.

2.4.14 DMA Controller

ESP32-S3 has a general-purpose DMA controller with five independent channels, all used for both transmit and receive directions. These five channels are shared by peripehrals with DMA feature, and support dynamic priority.

The DMA controller controls data transfer using linked lists. It allows peripheral-to-memory and memory-to-memory data transfer at a high speed. All channels can access internal and external RAM.

Peripherals on ESP32-S3 with DMA feature are SPI2, SPI3, UHCI0, I2S0, I2S1, LCD/CAM, AES, SHA, and ADC/DAC.

2.4.15 TWAI™ Controller

ESP32-S3 has a TWAI™ controller with the following features:

- compatible with ISO 11898-1 protocol
- standard frame format (11-bit ID) and extended frame format (29-bit ID)
- bit rates from 1 Kbit/s to 1 Mbit/s
- multiple modes of operation: Normal, Listen Only, and Self-Test (no acknowledgment required)
- 64-byte receive FIFO
- acceptance filter (single and dual filter modes)
- error detection and handling: error counters, configurable error interrupt threshold, error code capture, arbitration lost capture

2.5 Radio and Wi-Fi

The ESP32-S3 radio consists of the following blocks:

- 2.4 GHz receiver
- 2.4 GHz transmitter
- Bias and regulators
- Balun and transmit-receive switch
- Clock generator

2.5.1 2.4 GHz Receiver

The 2.4 GHz receiver demodulates the 2.4 GHz RF signal to quadrature baseband signals and converts them to the digital domain with two high-resolution, high-speed ADCs. To adapt to varying signal channel conditions, ESP32-S3 integrates RF filters, Automatic Gain Control (AGC), DC offset cancelation circuits, and baseband filters.

2.5.2 2.4 GHz Transmitter

The 2.4 GHz transmitter modulates the quadrature baseband signals to the 2.4 GHz RF signal, and drives the antenna with a high-powered CMOS power amplifier. The use of digital calibration further improves the linearity of the power amplifier.

Additional calibrations are integrated to cancel any radio imperfections, such as:

- carrier leakage

- I/Q amplitude/phase matching
- baseband nonlinearities
- RF nonlinearities
- antenna matching

These built-in calibration routines reduce the cost, time, and specialized equipment required for product testing.

2.5.3 Clock Generator

The clock generator produces quadrature clock signals of 2.4 GHz for both the receiver and the transmitter. All components of the clock generator are integrated into the chip, including inductors, varactors, filters, regulators and dividers.

The clock generator has built-in calibration and self-test circuits. Quadrature clock phases and phase noise are optimized on chip with patented calibration algorithms which ensure the best performance of the receiver and the transmitter.

2.5.4 Wi-Fi Radio and Baseband

The ESP32-S3 Wi-Fi radio and baseband support the following features:

- 802.11b/g/n
- 802.11n MCS0-7 that supports 20 MHz and 40 MHz bandwidth
- 802.11n MCS32
- 802.11n 0.4 μs guard-interval
- data rate up to 150 Mbps
- RX STBC (single spatial stream)
- adjustable transmitting power
- antenna diversity;
  ESP32-S3 supports antenna diversity with an external RF switch. This switch is controlled by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections.

2.5.5 Wi-Fi MAC

ESP32-S3 implements the full 802.11 b/g/n Wi-Fi MAC protocol. It supports the Basic Service Set (BSS) STA and SoftAP operations under the Distributed Control Function (DCF). Power management is handled automatically with minimal host interaction to minimize the active duty period.

The ESP32-S3 Wi-Fi MAC applies the following low-level protocol functions automatically:

- 4 × virtual Wi-Fi interfaces
- simultaneous Infrastructure BSS Station mode, SoftAP mode, and Station + SoftAP mode
- RTS protection, CTS protection, Immediate Block ACK
- fragmentation and defragmentation
- TX/RX A-MPDU, RX A-MSDU
- TXOP

- WMM
- GCMP, CCMP, TKIP, WAPI, WEP, and BIP
- automatic beacon monitoring (hardware TSF)
- 802.11mc FTM

2.5.6 Networking Features

Users are provided with libraries for TCP/IP networking, ESP-WIFI-MESH networking, and other networking protocols over Wi-Fi. TLS 1.0, 1.1 and 1.2 support is also provided.

2.6 Bluetooth LE

ESP32-S3 includes a Bluetooth Low Energy subsystem that integrates a hardware link layer controller, an RF/modem block and a feature-rich software protocol stack. It supports the core features of Bluetooth 5 and Bluetooth mesh.

2.6.1 Bluetooth LE Radio and PHY

Bluetooth Low Energy radio and PHY in ESP32-S3 support:

- 1 Mbps PHY
- 2 Mbps PHY for high transmission speed and high data throughput
- coded PHY for high RX sensitivity and long range (125 Kbps and 500 Kbps)
- high transmit power up to +20 dBm without external PA
- high receiver sensitivity in NZIF: -97 dBm at 1Mbps and -102 dBm at 125 Kbps
- listen before talk (LBT), implemented in hardware
- antenna diversity with an external RF switch. This switch is controller by one or more GPIOs, and used to select the best antenna to minimize the effects of channel imperfections

2.6.2 Bluetooth LE Link Layer Controller

Bluetooth Low Energy Link Layer Controller in ESP32-S3 support:

- LE advertising extensions, to enhance broadcasting capacity and broadcast more intelligent data
- multiple advertisement sets
- simultaneous advertising and scanning
- multiple connections in simultaneous central and peripheral roles
- adaptive frequency hopping and channel assessment
- LE channel selection algorithm #2
- connection parameter update
- high duty cycle non-connectable advertising
- LE privacy 1.2
- LE data packet length extension
- link layer extended scanner filter policies

- low duty cycle directed advertising
- link layer encryption
- LE Ping

2.7 RTC and Low-Power Management

2.7.1 Power Management Unit (PMU)

With the use of advanced power-management technologies, ESP32-S3 can switch between different power modes.

- Active mode: CPU and chip radio are powered on. The chip can receive, transmit, or listen.
- Modem-sleep mode: The CPU is operational and the clock speed can be reduced. The Wi-Fi baseband and radio are disabled, but Wi-Fi connection can remain active.
- Light-sleep mode: The CPU is paused. The RTC peripherals, as well as the ULP co-processor are running. Any wake-up events (MAC, host, RTC timer, or external interrupts) will wake up the chip. Wi-Fi connection can remain active.
- Deep-sleep mode: CPU and most peripherals are powered down. Only the RTC memory and RTC peripherals are powered on. Wi-Fi connection data are stored in the RTC memory. The ULP co-processor is functional.
- Hibernation mode: The internal 8-MHz oscillator and ULP co-processor are disabled. Only one RTC timer on the slow clock and certain RTC GPIOs are active. The RTC timer or the RTC GPIOs can wake up the chip from the Hibernation mode.

2.7.2 Ultra-Low-Power Co-processor

The ULP co-processor is designed as a simplified, low-power replacement of CPU in sleep modes. It can be also used to supplement the functions of the CPU in normal working mode. The ULP co-processor and RTC memory remain powered on during the Deep-sleep mode. Hence, the developer can store a program for the ULP co-processor in the RTC slow memory to access RTC GPIO, RTC peripheral devices, RTC timers and internal sensors in Deep-sleep mode.

ESP32-S3 has two ULP co-processors, one based on RISC-V instruction set architecture (ULP-RISC-V) and the other on finite state machine (ULP-FSM).

ULP-RISC-V has the following features:

- support for RV32IMC instruction set
- 32 32-bit general-purpose registers
- 32-bit multiplier and divider
- support for interrupts
- booted by the CPU, its dedicated timer, or RTC GPIO

ULP-FSM has the following features:

- support for common instructions including arithmetic, jump, and program control instructions
- support for on-board sensor measurement instructions
- booted by the CPU, its dedicated timer, or RTC GPIO

Note that these two co-processors cannot work simultaneously.

2.8 Timers and Watchdogs

2.8.1 General Purpose Timers

ESP32-S3 is embedded with four 54-bit general-purpose timers, which are based on 16-bit prescalers and 54-bit auto-reload-capable up/down-timers.

The timers' features are summarized as follows:

- a 16-bit clock prescaler, from 1 to 65536
- a 54-bit time-base counter programmable to be incrementing or decrementing
- able to read real-time value of the time-base counter
- halting and resuming the time-base counter
- programmable alarm generation
- timer value reload (Auto-reload at alarm or software-controlled instant reload)
- level interrupt generation

2.8.2 System Timer

ESP32-S3 integrates a 52-bit system timer, which has two counters and three comparators. The system timer has the following features:

- counters with a clock frequency of 16 MHz
- three types of independent interrupts generated according to alarm value
- two alarm modes: target mode and period mode
- 52-bit target alarm value and 26-bit periodic alarm value
- read sleep time from RTC timer when the chip is awaken from deep-sleep or light-sleep mode
- counters can be stalled if the CPU is stalled or in OCD mode

2.8.3 Watchdog Timers

The ESP32-S3 contains three watchdog timers: one in each of the two timer groups (called Main System Watchdog Timers, or MWDT) and one in the RTC Module (called the RTC Watchdog Timer, or RWDT).

During the flash boot process, RWDT and the first MWDT are enabled automatically in order to detect and recover from booting errors.

Watchdog timers have the following features:

- four stages, each with a programmable timeout value. Each stage can be configured, enabled and disabled separately
- interrupt, CPU reset, or core reset for MWDT upon expiry of each stage; interrupt, CPU reset, core reset, or system reset for RWDT upon expiry of each stage
- 32-bit expiry counter
- write protection, to prevent RWDT and MWDT configuration from being altered inadvertently

- flash boot protection
  If the boot process from an SPI flash does not complete within a predetermined period of time, the watchdog will reboot the entire main system.

2.9 Cryptographic Hardware Accelerators

ESP32-S3 is equipped with hardware accelerators of general algorithms, such as AES (FIPS PUB 197), ECB/CBC/OFB/CFB/CTR (NIST SP 800-38A), SHA (FIPS PUB 180-4), RSA, and ECC. The chip also supports independent arithmetic, such as Big Integer Multiplication and Big Integer Modular Multiplication. The maximum operation length for RSA, Big Integer Multiplication and Big Integer Modular Multiplication is 4096 bits. The maximum factor length for Big Integer Multiplication is 2048 bits.

2.10 Physical Security Features

- transparent external flash and RAM encryption (AES-XTS) with software inaccessible key prevents unauthorized readout of user application code or data.
- secure Boot feature uses a hardware root of trust to ensure only signed firmware (with RSA-PSS signature) can be booted.
- HMAC module can use a software inaccessible MAC key to generate MAC signatures for identity verification, as well as other uses.
- Digital Signature module can use a software inaccessible secure key to generate RSA signatures for identity verification.
- World controller provides two running environment for software. All hardware and software resources are sorted to two groups, and placed in either secure or general world. The secure world cannot be accessed by hardware in the general world, thus establishing a security boundary.

2.11 Peripheral Pin Configurations

Table 3: Peripheral Pin Configurations

Interface	Signal	Pin	Function
ADC	ADC1_CH0	GPIO1	Two 12-bit SAR ADCs
	ADC1_CH1	GPIO2	
	ADC1_CH2	GPIO3	
	ADC1_CH3	GPIO4	
	ADC1_CH4	GPIO5	
	ADC1_CH5	GPIO6	
	ADC1_CH6	GPIO7	
	ADC1_CH7	GPIO8	
	ADC1_CH8	GPIO9	
	ADC1_CH9	GPIO10	
	ADC2_CH0	GPIO11	
	ADC2_CH1	GPIO12	
	ADC2_CH2	GPIO13	
	ADC2_CH3	GPIO14	

Interface	Signal	Pin	Function
	ADC2_CH4	XTAL_32K_P	
	ADC2_CH5	XTAL_32K_N	
	ADC2_CH6	DAC_1	
	ADC2_CH7	DAC_2	
	ADC2_CH8	GPIO19	
	ADC2_CH9	GPIO20	
DAC	DAC_1	DAC_1	Two 8-bit DACs
	DAC_2	DAC_2	
Touch sensor	TOUCH1	GPIO1	Capacitive touch sensors
	TOUCH2	GPIO2	
	TOUCH3	GPIO3	
	TOUCH4	GPIO4	
	TOUCH5	GPIO5	
	TOUCH6	GPIO6	
	TOUCH7	GPIO7	
	TOUCH8	GPIO8	
	TOUCH9	GPIO9	
	TOUCH10	GPIO10	
	TOUCH11	GPIO11	
	TOUCH12	GPIO12	
	TOUCH13	GPIO13	
	TOUCH14	GPIO14	
JTAG	MTDI	MTDI	JTAG for software debugging
	MTCK	MTCK	
	MTMS	MTMS	
	MTDO	MTDO	
UART	U0RXD_in	Any GPIO pins	Three UART devices with hardware flow-control and DMA
	U0CTS_in		
	U0DSR_in		
	U0TXD_out		
	U0RTS_out		
	U0DTR_out		
	U1RXD_in		
	U1CTS_in		
	U1DSR_in		
	U1TXD_out		
	U1RTS_out		
	U1DTR_out		
	U2CTS_in		
	U2DSR_in		
	U2TXD_out		
	U2RTS_out		
	U2DTR_out		
I2C	I2CEXT0_SCL_in	Any GPIO pins	Two I2C devices in slave or master mode
	I2CEXT0_SDA_in		

Interface	Signal	Pin	Function
	I2CEXT1_SCL_in		
	I2CEXT1_SDA_in		
	I2CEXT0_SCL_out		
	I2CEXT0_SDA_out		
	I2CEXT1_SCL_out		
	I2CEXT1_SDA_out		
LED_PWM	ledc_ls_sig_out0~7	Any GPIO pins	Eight independent channels. 80 MHz clock, RTC clock or XTAL clock. Duty cycle accuracy: 14 bits
I2S	I2S0O_BCK_in	Any GPIO pins	Stereo input and output from/to the audiocodec
	I2S0_MCLK_in		
	I2S0O_WS_in		
	I2S0I_SD_in		
	I2S0I_SD1_in		
	I2S0I_SD2_in		
	I2S0I_SD3_in		
	I2S0I_BCK_in		
	I2S0I_WS_in		
	I2S1O_BCK_in		
	I2S1_MCLK_in		
	I2S1O_WS_in		
	I2S1I_SD_in		
	I2S1I_BCK_in		
	I2S1I_WS_in		
	I2S0O_BCK_out		
	I2S0_MCLK_out		
	I2S0O_WS_out		
	I2S0O_SD_out		
	I2S0I_BCK_out		
	I2S0I_WS_out		
	I2S1O_BCK_out		
	I2S1_MCLK_out		
	I2S1O_WS_out		
	I2S1O_SD_out		
	I2S1I_BCK_out		
	I2S1I_WS_out		
LCD_CAMERA	LCD_PCLK	Any GPIO pins	8-bit ~16-bit data transmission to LCD interface and 8-bit ~16-bit data reception by camera interface
	LCD_DC		
	LCD_V_SYNC		
	LCD_H_SYNC		
	LCD_H_ENABLE		
	LCD_DATA_out0~15		
	LCD_CS		
	CAM_CLK		
	CAM_V_SYNC		

Interface	Signal	Pin	Function
	CAM_H_SYNC		
	CAM_H_ENABLE		
	CAM_PCLK		
	CAM_DATA_in0~15		
Remote Control Peripheral	RMT_SIG_IN0~3	Any GPIO pins	Four channels for an IR transceiver of various waveforms
	RMT_SIG_OUT0~3		
SPI0/1	SPICLK_out_mux	SPICLK	Support Standard SPI, Dual SPI, QSPI, QPI, OSPI, and OPI that allow connection to external flash and RAM.
	SPICS0_out	SPICS0	
	SPICS1_out	SPICS1	
	SPID_in/out	SPID	
	SPIQ_in/out	SPIQ	
	SPIWP_in/out	SPIWP	
	SPIHD_in/out	SPIHD	
	SPID4_in/out	GPIO33	
	SPID5_in/out	GPIO34	
	SPID6_in/out	GPIO35	
	SPID7_in/out	GPIO36	
	SPIDQS_in/out	GPIO37	
SPI2	FSPICLK_in/_out_mux	Any GPIO pins	Support: • master mode of SPI, Dual SPI, Quad SPI, Octal SPI, QPI, and OPI, and slave mode of SPI, Dual SPI, Quad SPI, and QPI; • connection to external flash, RAM, and other SPI devices; • four modes of SPI transfer format; • configurable SPI frequency; • 64-byte FIFO or DMA buffer.
	FSPICS0_in/_out		
	FSPICS1~5_out		
	FSPID_in/_out		
	FSPIQ_in/_out		
	FSPIWP_in/_out		
	FSPIHD_in/_out		
	FSPIIO4~7_in/_out		
	FSPIDQS_out		
SPI3	SPI3_CLK_in/_out_mux	Any GPIO pins	Support: • master and slave modes of SPI, Dual SPI, Quad SPI, and QPI; • four modes of SPI transfer format; • configurable SPI frequency; • 64-byte FIFO or DMA buffer.
	SPI3_CS0_in/_out		
	SPI3_CS1_in/_out		
	SPI3D_in/_out		
	SPI3Q_in/_out		
	SPI3_WP_in/_out		
	SPI3_HD_in/_out		
Pulse counter	pcnt_sig_ch0_in0	Any GPIO pins	Capture pulse and count pulse edges in seven modes
	pcnt_sig_ch1_in0		
	pcnt_ctrl_ch0_in0		
	pcnt_ctrl_ch1_in0		
	pcnt_sig_ch0_in1		
	pcnt_sig_ch1_in1		
	pcnt_ctrl_ch0_in1		
	pcnt_ctrl_ch1_in1		
	pcnt_sig_ch0_in2		
	pcnt_sig_ch1_in2		

Interface	Signal	Pin	Function
	pcnt_ctrl_ch0_in2		
	pcnt_ctrl_ch1_in2		
	pcnt_sig_ch0_in3		
	pcnt_sig_ch1_in3		
	pcnt_ctrl_ch0_in3		
	pcnt_ctrl_ch1_in3		
USB OTG	D-	GPIO19	Full-speed USB OTG
	D+	GPIO20	

Note:

- GPIO46 is input-only and can not be used for output function.

Appendix A – ESP32-S3 IO MUX

IO MUX

Pin No.	Power Supply Pin	Analog Pin	Digital Pin	Power Domain	Analog Function0	Analog Function1	RTC_GPIO	Digital Function0	Type	Digital Function1	Type	Digital Function2	Type	Digital Function3	Type	Digital Function4	Type	Drive Strength (Default)	At Reset	After Reset
1	LNA_IN																			
2	VDD3P3																			
3	VDD3P3																			
4			GPIO0	VDD3P3_RTC_IO			RTC_GPIO0	GPIO0	I/O/T	GPIO0	I/O/T							2'd2	oe=0, ie=1, wpu	oe=0, ie=1, wpu,
5			GPIO1	VDD3P3_RTC_IO	TOUCH1	ADC1_CH0	RTC_GPIO1	GPIO1	I/O/T	GPIO1	I/O/T							2'd2	oe=0, ie=1	oe=0, ie=1
6			GPIO2	VDD3P3_RTC_IO	TOUCH2	ADC1_CH1	RTC_GPIO2	GPIO2	I/O/T	GPIO2	I/O/T							2'd2	oe=0, ie=1	oe=0, ie=1
7			GPIO3	VDD3P3_RTC_IO	TOUCH3	ADC1_CH2	RTC_GPIO3	GPIO3	I/O/T	GPIO3	I/O/T							2'd2	oe=0, ie=1	oe=0, ie=0
8			GPIO4	VDD3P3_RTC_IO	TOUCH4	ADC1_CH3	RTC_GPIO4	GPIO4	I/O/T	GPIO4	I/O/T							2'd2	oe=0, ie=1	oe=0, ie=0
9			GPIO5	VDD3P3_RTC_IO	TOUCH5	ADC1_CH4	RTC_GPIO5	GPIO5	I/O/T	GPIO5	I/O/T							2'd2	oe=0, ie=0	oe=0, ie=0
10			GPIO6	VDD3P3_RTC_IO	TOUCH6	ADC1_CH5	RTC_GPIO6	GPIO6	I/O/T	GPIO6	I/O/T							2'd2	oe=0, ie=0	oe=0, ie=0
11			GPIO7	VDD3P3_RTC_IO	TOUCH7	ADC1_CH6	RTC_GPIO7	GPIO7	I/O/T	GPIO7	I/O/T							2'd2	oe=0, ie=0	oe=0, ie=0
12			GPIO8	VDD3P3_RTC_IO	TOUCH8	ADC1_CH7	RTC_GPIO8	GPIO8	I/O/T	GPIO8	I/O/T			SUBSPICS1	O/T			2'd2	oe=0, ie=0	oe=0, ie=0
13			GPIO9	VDD3P3_RTC_IO	TOUCH9	ADC1_CH8	RTC_GPIO9	GPIO9	I/O/T	GPIO9	I/O/T			SUBSPIHD	I1/O/T	FSPIHD	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
14			GPIO10	VDD3P3_RTC_IO	TOUCH10	ADC1_CH9	RTC_GPIO10	GPIO10	I/O/T	GPIO10	I/O/T	FSPIIO4	I1/O/T	SUBSPICS0	O/T	FSPICS0	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
15			GPIO11	VDD3P3_RTC_IO	TOUCH11	ADC2_CH0	RTC_GPIO11	GPIO11	I/O/T	GPIO11	I/O/T	FSPIIO5	I1/O/T	SUBSPID	I1/O/T	FSPID	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
16			GPIO12	VDD3P3_RTC_IO	TOUCH12	ADC2_CH1	RTC_GPIO12	GPIO12	I/O/T	GPIO12	I/O/T	FSPIIO6	I1/O/T	SUBSPICLK	O/T	FSPICLK	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
17			GPIO13	VDD3P3_RTC_IO	TOUCH13	ADC2_CH2	RTC_GPIO13	GPIO13	I/O/T	GPIO13	I/O/T	FSPIIO7	I1/O/T	SUBSPIQ	I1/O/T	FSPIQ	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
18			GPIO14	VDD3P3_RTC_IO	TOUCH14	ADC2_CH3	RTC_GPIO14	GPIO14	I/O/T	GPIO14	I/O/T	FSPIDQS	O/T	SUBSPIWP	I1/O/T	FSPIWP	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
19	VDD3P3_RTC																			
20			XTAL_32K_P	VDD3P3_RTC_IO	XTAL_32K_P	ADC2_CH4	RTC_GPIO15	GPIO15	I/O/T	GPIO15	I/O/T	U0RTS	O					2'd2	oe=0, ie=0	oe=0, ie=0
21			XTAL_32K_N	VDD3P3_RTC_IO	XTAL_32K_N	ADC2_CH5	RTC_GPIO16	GPIO16	I/O/T	GPIO16	I/O/T	U0CTS	I1					2'd2	oe=0, ie=0	oe=0, ie=0
22			DAC_1	VDD3P3_RTC_IO	DAC_1	ADC2_CH6	RTC_GPIO17	GPIO17	I/O/T	GPIO17	I/O/T	U1TXD	O					2'd2	oe=0, ie=0	oe=0, ie=1
23			DAC_2	VDD3P3_RTC_IO	DAC_2	ADC2_CH7	RTC_GPIO18	GPIO18	I/O/T	GPIO18	I/O/T	U1RXD	I1	CLK_OUT3	O			2'd2	oe=0, ie=0	oe=0, ie=1
24			GPIO19	VDD3P3_RTC_IO	USB_D-	ADC2_CH8	RTC_GPIO19	GPIO19	I/O/T	GPIO19	I/O/T	U1RTS	O	CLK_OUT2	O			2'd2	oe=0, ie=0	oe=0, ie=0
25			GPIO20	VDD3P3_RTC_IO	USB_D+	ADC2_CH9	RTC_GPIO20	GPIO20	I/O/T	GPIO20	I/O/T	U1CTS	I1	CLK_OUT1	O			2'd2	oe=0, ie=0	oe=0, ie=0
26	VDD3P3_RTC_IO																			
27			GPIO21	VDD3P3_RTC_IO			RTC_GPIO21	GPIO21	I/O/T	GPIO21	I/O/T							2'd2	oe=0, ie=0	oe=0, ie=0
28			SPICS1	VDD_SPI				SPICS1	O/T	GPIO26	I/O/T							2'd2	oe=0, ie=1, wpu	oe=0, ie=1
29	VDD_SPI																			
30			SPIHD	VDD_SPI				SPIHD	I1/O/T	GPIO27	I/O/T							2'd2	oe=0, ie=1, wpu	oe=0, ie=1
31			SPIWP	VDD_SPI				SPIWP	I1/O/T	GPIO28	I/O/T							2'd2	oe=0, ie=1, wpu	oe=0, ie=1
32			SPICS0	VDD_SPI				SPICS0	O/T	GPIO29	I/O/T							2'd2	oe=0, ie=1, wpu	oe=0, ie=1
33			SPICLK	VDD_SPI				SPICLK	O/T	GPIO30	I/O/T							2'd2	oe=0, ie=1, wpu	oe=0, ie=1
34			SPIQ	VDD_SPI				SPIQ	I1/O/T	GPIO31	I/O/T							2'd2	oe=0, ie=1, wpu	oe=0, ie=1
35			SPID	VDD_SPI				SPID	I1/O/T	GPIO32	I/O/T							2'd2	oe=0, ie=1, wpu	oe=0, ie=1
36			SPICLK_P	VDD_SPI				SPICLK_DIFF	O/T	GPIO47	I/O/T	SUBSPICLK_DIFF	O/T					2'd2	oe=0, ie=1	oe=0, ie=1
37			GPIO33	VDD3P3_CPU / VDD_SPI				GPIO33	I/O/T	GPIO33	I/O/T	FSPIHD	I1/O/T	SUBSPIHD	I1/O/T	SPIIO4	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
38			GPIO34	VDD3P3_CPU / VDD_SPI				GPIO34	I/O/T	GPIO34	I/O/T	FSPICS0	I1/O/T	SUBSPICS0	O/T	SPIIO5	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
39			GPIO35	VDD3P3_CPU / VDD_SPI				GPIO35	I/O/T	GPIO35	I/O/T	FSPID	I1/O/T	SUBSPID	I1/O/T	SPIIO6	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
40			GPIO36	VDD3P3_CPU / VDD_SPI				GPIO36	I/O/T	GPIO36	I/O/T	FSPICLK	I1/O/T	SUBSPICLK	O/T	SPIIO7	I1/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
41			GPIO37	VDD3P3_CPU / VDD_SPI				GPIO37	I/O/T	GPIO37	I/O/T	FSPIQ	I1/O/T	SUBSPIQ	I1/O/T	SPIDQS	I0/O/T	2'd2	oe=0, ie=0	oe=0, ie=1
42			GPIO38	VDD3P3_CPU				GPIO38	I/O/T	GPIO38	I/O/T	FSPIWP	I1/O/T	SUBSPIWP	I1/O/T			2'd2	oe=0, ie=0	oe=0, ie=1
43			MTCK	VDD3P3_CPU				MTCK	I1	GPIO39	I/O/T	CLK_OUT3	O	SUBSPICS1	O/T			2'd2	oe=0, ie=0	oe=0, ie=1, wpu (see Notes)
44			MTDO	VDD3P3_CPU				MTDO	O/T	GPIO40	I/O/T	CLK_OUT2	O					2'd2	oe=0, ie=0	oe=0, ie=1
45	VDD3P3_CPU																			
46			MTDI	VDD3P3_CPU				MTDI	I1	GPIO41	I/O/T	CLK_OUT1	O					2'd2	oe=0, ie=0	oe=0, ie=1
47			MTMS	VDD3P3_CPU				MTMS	I1	GPIO42	I/O/T							2'd2	oe=0, ie=0	oe=0, ie=1
48			U0TXD	VDD3P3_CPU				U0TXD	O	GPIO43	I/O/T	CLK_OUT1	O					2'd2	oe=0, ie=1, wpu	oe=1, ie=1, wpu
49			U0RXD	VDD3P3_CPU				U0RXD	I1	GPIO44	I/O/T	CLK_OUT2	O					2'd2	oe=0, ie=1, wpu	oe=0, ie=1, wpu
50			GPIO45	VDD3P3_CPU				GPIO45	I/O/T	GPIO45	I/O/T							2'd2	oe=0, ie=1, wpd	oe=0, ie=1, wpd
51	VDDA																			
52		XTAL_N																		
53		XTAL_P																		
54	VDDA																			
55			GPIO46	VDD3P3_CPU				GPIO46	I	GPIO46	I								oe=0, wpd, ie=1	oe=0, wpd, ie=1
56		CHIP_PU		VDD3P3_RTC_IO																
Total	9	3	44																	

Notes:
- Power supply for GPIO33, GPIO34, GPIO35, GPIO36 and GPIO37 is configurable to be either VDD3P3_CPU (default) or VDD_SPI.
- When eFuse bit EFUSE_HARD_DIS_JTAG is set to 1, MTCK floats after reset; when eFuse bit EFUSE_HARD_DIS_JTAG is 0, MTCK connects to internal pull-up after reset.
- wpu: weak pull-up
- wpd: weak pull-down
- ie: input enable
- oe: output enable
- Each column about digital "Function" is accompanied by a column about "Type". Please see the following explanations for the meanings of "type" with respect to each "function" they are associated with. For each "Function-*N*", "type" signifies:
  - I: input only. If a function other than "Function-*N*" is assigned, the input signal of "Function-*N*" is still from this pin.
  - I1: input only. If a function other than "Function-*N*" is assigned, the input signal of "Function-*N*" is always "1".
  - I0: input only. If a function other than "Function-*N*" is assigned, the input signal of "Function-*N*" is always "0".
  - O: output only.
  - T: high-impedance.
  - I/O/T: combinations of input, output, and high-impedance according to the function signal.
  - I1/O/T: combinations of input, output, and high-impedance, according to the function signal. If a function is not selected, the input signal of the function is "1".

Figure 5: IO MUX

Revision History

Date	Version	Release notes
2020-08-14	V0.3	Preliminary version.

Solutions, Documentation and Legal Information

Must-Read Documents

- *ESP-IDF Programming Guide*
- *Espressif Product Ordering Information*
- Certificates
- Notification Subscription

Sales and Technical Support

- Sales Questions
- Technical Inquiries
- Get Samples

Developer Zone

- ESP32 Forum
- GitHub
- Courses
- Videos

Products

- SoCs
- Modules
- DevKits

Must-Have Resources

- SDKs and Demos
- APPs
- Tools
- AT

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