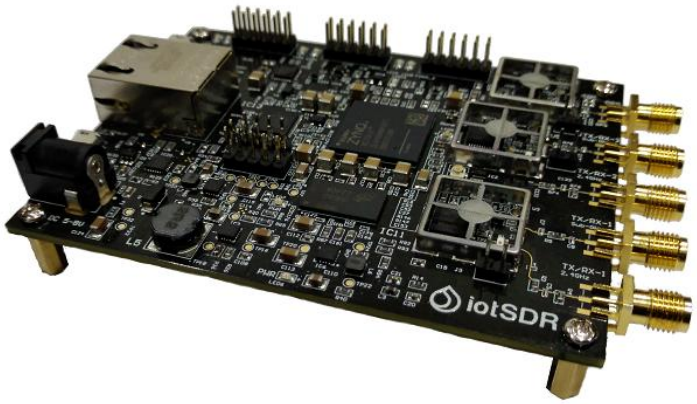
iotSDR Programmers Reference

Ver 0.2

Contents



1 Introduction

iotSDR provides a platform that allows SDR developers and enthusiasts to develop cutting-edge solutions in the IoT radio and network domains. It has two Microchip AT86RF215 frontends, capable of providing I/Q streams and modem functionality for the Xilinx ZYNQ SoC, as well as a MAX2769 GNSS chip for custom GPS, Galileo, BieDou, and Glonass development. It is also compatible with the popular GNURadio SDR software.

If you want to design and develop a physical layer protocol for IOT – a protocol like LoRa, SigFox, WightLess, Bluetooth, BLE, 802.15.4, ZigBee, or something of your own – this board is for you. It is also a great place to start if you want to build a custom IoT gateway along the lines of The Things Network, LPWAN, or Google Thread.

2 Peripherals

- **RF Transceiver**: 2x Atmel AT86RF215
  - European band: 863-870 MHz / 870-876 MHz / 915-921 MHz
  - Chinese band: 470-510 MHz / 779-787 MHz
  - North American band: 902-928 MHz
  - Korean band: 917-923.5 MHz
  - Japanese band: 920-928 MHz
  - World-wide ISM band: 2400-2483.5 MHz
- **GNSS Receiver**: MAX2769B
- **SoC**: Xilinx ZYNQ XC7Z010-1CLG400C
  - Dual-Core ARM Cortex-A9 MPCore
  - 256 kb on-chip memory
  - DDR3 support
  - 28,000 logic cells
  - 17,600 LUTs
  - 2.1 Mb block RAM

    - 80 DSP slices
    - 2x UART, 2x CAN 2.0 B, 2x I²C, 2x SPI, 4x 32-bit GPIO
    - FPGA configuration via JTAG
- **EEPROM Memory**: 1x AT24MAC602 for RF transciever MCU firmware and data
- **Flash Memory**: 1x QSPI 128 Mb flash memory for firmware
- **RAM**: 256 MB DDR3
- **SD Card**: Micro SD card slot
- **General User Inputs/Outputs**:
    - 2x 8-bit PL interfaces
    - 1x 8-bit PS interface
- **Connectivity**:
    - 1x Gigabit Ethernet
    - USB 2.0 high-speed (USB3310)
    - USB 2.0 full-speed (CP2104)
    - 2x SMA RF connector for Low Frequency IoT Bands transceiver
    - 2x SMA RF connector for 2.4 GHz Band transceiver
    - 1x GNSS receiver RF connector
    - FPGA JTAG connector for external JTAG programmer/debugger
- **Clock System**:
    - Single clock source for both RF frontends
    - Separate clock for GNSS receiver
- **Board Dimensions**: 76.2 mm x 101.6 mm

3 Overview

iotSDR provides a platform that allows SDR developers and enthusiasts to develop cutting-edge solutions in the IoT radio and network domains. It has two Microchip AT86RF215 frontends, capable of providing I/Q streams and modem functionality for the Xilinx ZYNQ SoC, as well as a MAX2769 GNSS chip for custom GPS, Galileo, BieDou, and Glonass development. It is also compatible with the popular GNURadio SDR software.

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3.1 Key Features

- Xilinx XC7Z SoC (XC7Z010 or XC7Z020)
    - Processing system (PS):
        - XC7Z020: Dual-core ARM Cortex-A9 MPCore™ with CoreSight™
        - XC7Z014S: Single-core ARM Cortex-A9 MPCore™ with CoreSight™
        - L1 cache: 32 KByte instruction, 32 KByte data per processor
        - L2 cache: Unified 512 KByte
    - Programmable logic (PL): Artix-7 FPGA
        - Programmable logic cells: 85K (XC7Z020), 65K (XC7Z014S)
        - Block RAM: 4.9 MByte (XC7Z020), 3.8 MByte (XC7Z014S)

    - DSP slices: 220 (XC7Z020), 170 (XC7Z014S)
    - Peak DSP performance: 276 GMACs (XC7Z020), 187 GMACs (XC7Z014S)
    - 2x 12 bit, MSPS ADCs with up to 17 differential inputs
- 8 I/O (MIO) and 16 I/O (2x8 PL) pins
- 512 MByte DDR3/L SDRAM memory (2 x 256 Mbit x 16, 32-bit wide data bus).
- 32 MByte Quad SPI Flash memory
- Gigabit Ethernet transceiver PHY (Marvell 88E1512)
- serial EEPROM
- Highly integrated full-featured hi-speed USB 2.0 ULPI transceiver (Microchip USB3320C-EZK)
- User LED 1 (Green), user LED 2 (Red), user LED 3 - FPGA DONE (Green)
- On-board high-efficiency DC-DC converters for all voltages used
- Rugged for shock and high vibration

3.2 Block Diagram

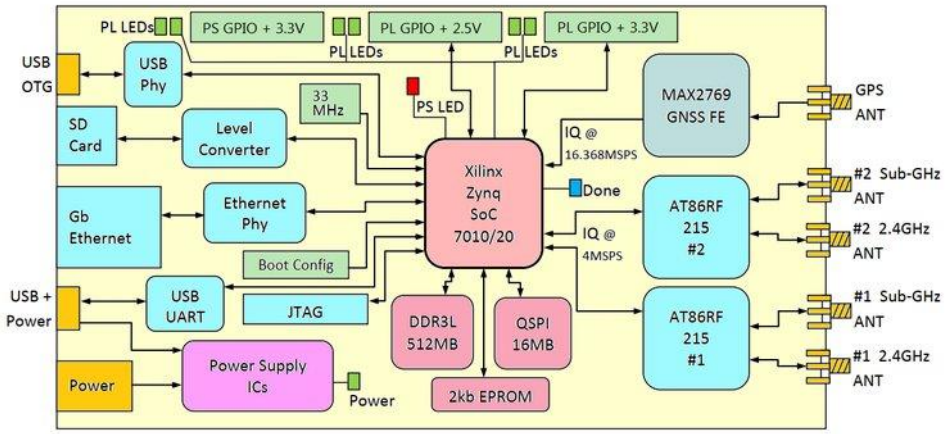


Figure 1: iotSDR Block Diagram

Components and connections marked with dashed lines are optional or may be missing on some module variants, please contact us for additional information.

3.3 Main Components

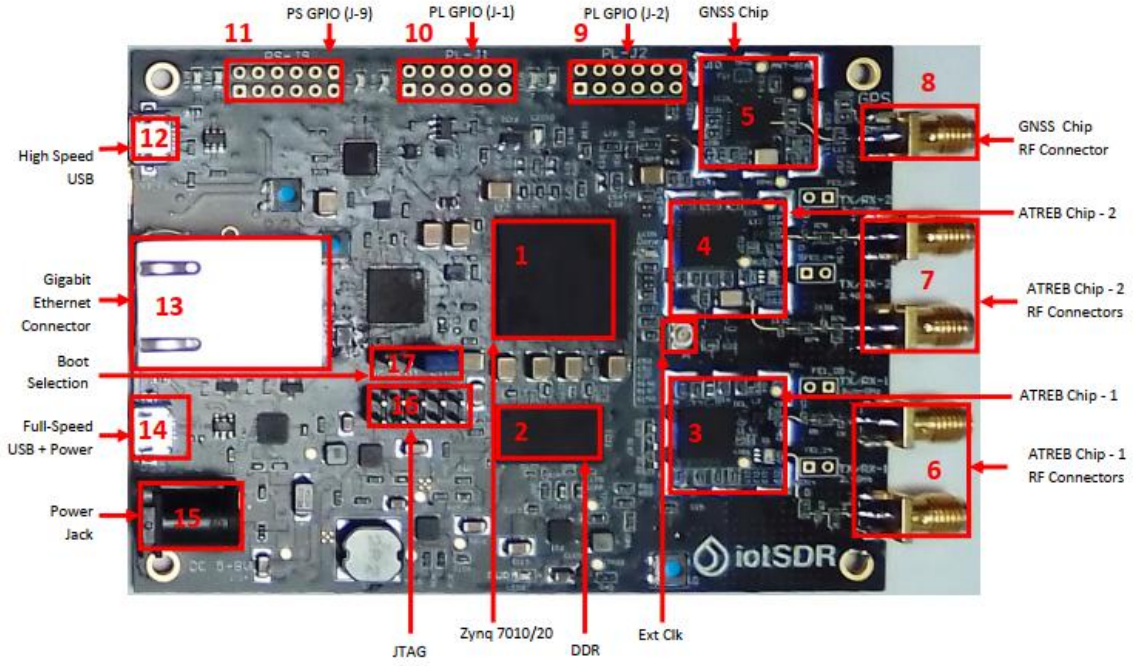


Figure 2: Main Components

1. Xilinx Zynq XC7Z010/7020 SoC, U2
2. 4 Gbit DDR3/L SDRAM, IC-11
3. ATREB Chip -1, IC-1
4. ATREB Chip-2, IC-9
5. GNSS CHIP , IC-21
6. Analog Front-ends Atreb-1, SMA-1 & SMA-2
7. Analog Front-ends Atreb-2, SMA-3 & SMA-4
8. GNSS Front-end, SMA-5
9. PL Header-1, J1
10. PL Header-2, J2
11. PS Header, J9
12. High Speed USB Connector, J11
13. Gigabit Ethernet (GbE) transceiver, J10
14. Full Speed USB, with USB board power , J12
15. 5V DC power jack for board power, J7
16. JTAG Header, J5
17. Boot Mode Selection Header, U6

3.4 Initial Delivery State

Table 1 Initial State of EEPROM and QSPI Flash

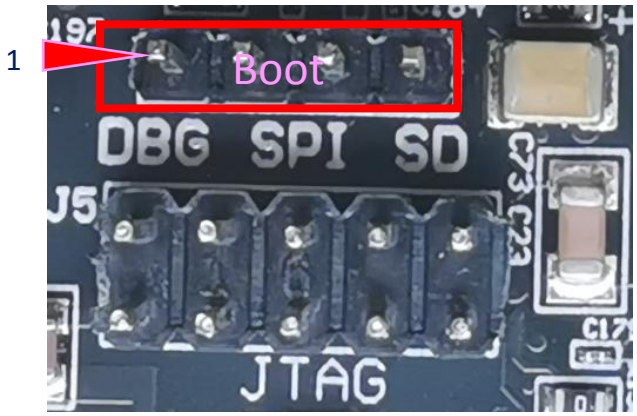
Quad SPI Flash	IC-14	Empty
EEPROM	U-4	Empty

4 Boot Process

By default, the iotSDR supports JTAG, QSPI and SD Card boot modes which is controlled by the MODE Jumpers at P4 connector.

Table 2 Boot Mode Jumper Settings

Pins to Short	Boot option
1-2	JTAG
2-3	QSPI Flash
3-4	SD Card



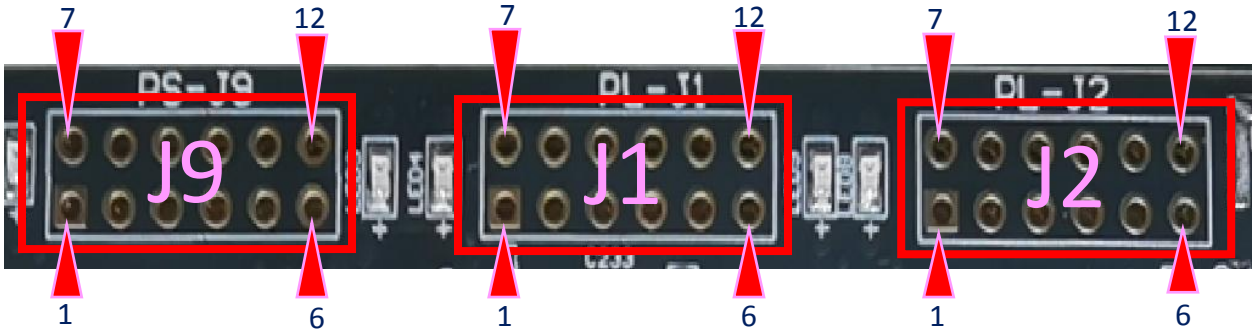
5 Signals, Interfaces and Pins

5.1 Pin Header I/Os

PL I/O signal connections between Zynq SoC's I/O banks and external connectors are 24 in total, where 8 are connected to PS and 16 are connected to PL.

Table 3 Pin Header SoC Interface

Part Number	Type	Supply Reference	Zynq Pins	Zynq PS/PL
J9	HR GPIO	VCCIO13(3.3V)	E6, B5, E9, C6, D9, E8, C5, C8	PS BANK 500
J1	HR GPIO	VCCIO34(3.3V)	V17, V18, W18, N20, P20, V15, T10, T12	PL BANK 34
J2	HR GPIO	VCCIO35(2.5V)	E17, D18, C20, B20, F19, F20, L19, L20	PL BANK 35



PS MIO bank 500 signal connections to J9 connector.

Table 4 PS MIO signals to J9 connector

Pin Number	Net Name	Bank Number	Voltage	ZYNQ Pin Name
1	PS_MIO0	500	3.3V	E6
2	PS_MIO15	500	3.3V	C8
3	PS_MIO9	500	3.3V	B5
4	PS_MIO10	500	3.3V	E9
5	GND		0V	

6	VCCIO13		3.3V	
7	PS_MIO11	500	3.3V	C6
8	PS_MIO12	500	3.3V	D9
9	PS_MIO13	500	3.3V	E8
10	PS_MIO14	500	3.3V	C5
11	GND		0V	
12	VCCIO13		3.3V	

PL Bank 35 signal connections to J1 connector.

Table 5 BANK-35 to J1 CONNECTOR

Pin Number	**Net Name**	**General Name**	**Voltage**	**ZYNQ Pin**
1	PMOD35_1	IO_L3P_T0_DQS_AD1P_35	2.5	E17
2	PMOD35_2	IO_L3N_T0_DQS_AD1N_35	2.5	D18
3	PMOD35_3	IO_L1P_T0_AD0P_35	2.5	C20
4	PMOD35_4	IO_L1N_T0_AD0N_35	2.5	B20
5	GND		0V	
6	VCCO_35		2.5V	
7	PMOD35_5	IO_L15P_T2_DQS_AD12P_35	2.5	F19
8	PMOD35_6	IO_L15N_T2_DQS_AD12N_35	2.5	F20
9	PMOD35_7	IO_L9P_T1_DQS_AD3P_35	2.5	L19
10	PMOD35_8	IO_L9N_T1_DQS_AD3N_35	2.5	L20
11	GND		0V	
12	VCCO_35		2.5V	

PL Bank 34 signal connections to J2 connector.

Table 6 BANK-34 to J2 CONNECTOR

Pin Number	Net Name	General Name	Voltage	ZYNQ Pin
1	PMOD34_1	IO_L21P_T3_DQS_34	3.3	V17
2	PMOD34_2	IO_L21N_T3_DQS_34	3.3	V18
3	PMOD34_3	IO_L22P_T3_34	3.3	W18
4	PMOD34_4	IO_L14P_T2_SRCC_34	3.3	N20
5	GND		0V	
6	VCCO_34		2.5V	
7	PMOD34_5	IO_L14N_T2_SRCC_34	3.3	P20
8	PMOD34_6	IO_L10P_T1_34	3.3	V15
9	PMOD34_7	IO_L1N_T1_34	3.3	T10
10	PMOD34_8	IO_L2P_T1_34	3.3	T12
11	GND		0V	
12	VCCO_34		2.5V	

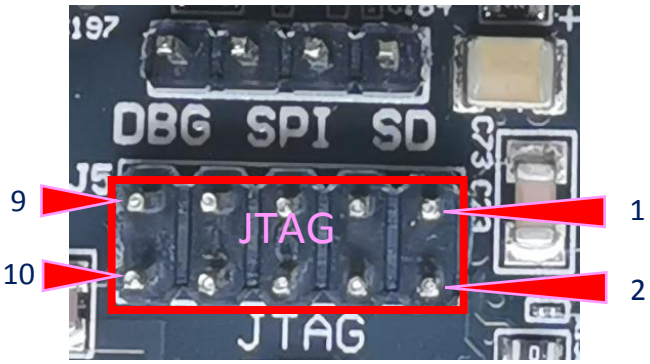
5.2 JTAG Interface

JTAG access to the Zynq SoC is provided through Connector J5.

Table 7 BANK-0 to JTAG PINS

Signals	Pins	Connector Pin Number
JTAG_TDI	G6, TDI_0	1
JTAG_TDO	F6, TDO_0	3
JTAG_TCK	F9, TCK_0	5
JTAG_TMS	J6, TMS_0	7
JTAG_RST	wire to PS_SRST, B10	2
JTAG_VREF	3.3V	9
GND	GND	4, 6, 8, 10

Table 4: JTAG pins connection.



5.3 Quad SPI Interface

Quad SPI Flash (U7) is connected to the Zynq PS QSPI0 interface via PS MIO bank 500, pins MIO1..6.

Table 8 QUAD SPI interface MIOs and pins

ZYNQ PINS	SPI PINS	DESCRIPTION
PS_MIO1_500, A7	CS, C2	SPI CHIP SELECT PIN
PS_MIO2_500, B6	SI/IO0, D3	SPI DATA-0 PIN
PS_MIO3_500, D6	SO/IO1, D2	SPI DATA-1 PIN
PS_MIO4_500, B7	WP#/IO2, C4	SPI DATA-2 PIN
PS_MIO5_500, A6	HOLD#/IO3, D4	SPI DATA-3 PIN
PS_MIO6_500, A5	SCK, B2	SPI CLK PIN

5.4 Ethernet Interface

The Marvell Alaska 88E1512 (IC13) is a physical layer device containing a single Gigabit Ethernet transceiver and three separate major electrical interfaces: MDI interface to copper cable, SERDES/SGMII interface and RGMII interface. RGMII interface is connected to the Zynq SoC PS bank 501 MIO pins, see tables below.

MDI interface to copper cable are routed to the ethernet connector J10 and MDI pins are routed to the ethernet connector J10 (see table below).

Table 9 Ethernet PHY to Ethernet connector connections

PHY PINS	CONNECTOR PINS	DESCRIPTION
MDIP [0], PIN 28	TRD1+, PIN 11	Tx1 Differential Signal, positive
MDIN [0], PIN 27	TRD1-, PIN 10	Tx1 Differential Signal, negative
MDIP [1], PIN 24	TRD2+, PIN 4	Tx2 Differential Signal, positive
MDIN [1], PIN 23	TRD2-, PIN 5	Tx2 Differential Signal, negative
MDIP [2], PIN 22	TRD3+, PIN 3	Tx3 Differential Signal, positive
MDIN [2], PIN 21	TRD3-, PIN 2	Tx3 Differential Signal, negative
MDIP [3], PIN 18	TRD4+, PIN 8	Tx4 Differential Signal, positive
MDIN [3], PIN 17	TRD4-, PIN 9	Tx4 Differential Signal, negative

Table 10 Ethernet PHY to Zynq SoC connections.

ZYNQ PINS	PHY PINS	DESCRIPTION
PS_MIO22_500, B17	RX_CLK, PIN 46	Receiver Clock
PS_MIO27_500, D13	RX_CTRL, PIN 43	Receiver Control Signal
PS_MIO23_500, D11	RXD [0], PIN44	Data-0 bit of Receiver
PS_MIO24_500, A16	RXD [1], PIN45	Data-1 bit of Receiver
PS_MIO25_500, F15	RXD [2], PIN47	Data-2 bit of Receiver
PS_MIO26_500, A15	RXD [3], PIN48	Data3 bit of Receiver
PS_MIO16_500, A19	TX_CLK, PIN 53	Transmitter Clock
PS_MIO21_500, F14	TX_CTRL, PIN 56	Transmitter Control Signal
PS_MIO17_500, E14	TXD [0], PIN50	Data-0 bit of Transmitter
PS_MIO18_500, B18	TXD [1], PIN51	Data-1 bit of Transmitter
PS_MIO19_500, D10	TXD [2], PIN54	Data-2 bit of Transmitter
PS_MIO20_500, A17	TXD [3], PIN55	Data3 bit of Transmitter
PS_MIO52_500, C10	MDC, PIN7	Control signal
PS_MIO53_500, C11	MDIO, PIN8	Control signal

5.5 High Speed USB Interface

Hi-speed USB ULPI PHY is provided by CP2104 from SI LABS (IC20). The ULPI interface is connected to the Zynq SoC PS UART via MIO48.49, bank 501. It is used as USB to UART bridge. The signals except power signals not mentioned here are left un-connected.

Table 11 High-Speed USB PHY to ZYNQ SoC Connections

ZYNQ PINS	**USB PHY-CP2104**	**Description**
PS_MIO48_500, B12	RXD, PIN 20	Receiver, Rx, UART
PS_MIO49_500, C12	TXD, PIN 21	Transmitter, Tx, UART

Table 12 High-Speed USB PHY to USB CONNECTOR Connections

USB PHY-CP2104	**USB CONNECTOR**	**Description**
D+, PIN 3	D+, PIN3	D+, differential, USB
D-, PIN 4	D-, PIN2	D-, differential, USB
GND	ID, PIN4	Identity Pin

5.6 Full Speed USB Interface

Full-speed USB ULPI PHY is provided by USB3320 from Microchip (IC-19). The I interface is connected to the Zynq SoC PS USB via MIO27…. MIO39, bank 501. It is used Full Speed USB with speed up to 480Mbits/s. The signals except power signals not mentioned here are left un-connected.

Table 13 ZYNQ to USB Full Speed Connections

ZYNQ PINS	**USB PHY-USB3320**	**Description**
PS_MIO28_501, C16	USB_D4	Data pin 4, USB
PS_MIO29_501, C13	USB_DIR	Control signal for direction
PS_MIO30_501, C15	USB_STP	Control Signal for STP,
PS_MIO31_501, E16	USB_NXT	Control Signal for NXT

PS_MIO32_501, A14	USB_D0	Data pin 0, USB
PS_MIO33_501, D15	USB_D1	Data pin 1, USB
PS_MIO34_501, A12	USB_D2	Data pin 2, USB
PS_MIO35_501, F12	USB_D3	Data pin 3, USB
PS_MIO36_501, A11	USB_CLK	Clock Signal, USB
PS_MIO37_501, A10	USB_D5	Data pin 5, USB
PS_MIO38_501, E13	USB_D6	Data pin 6, USB
PS_MIO39_501, C18	USB_D7	Data pin 7, USB

Table 14 Full Speed USB PHY to USB Connector Connections

USB PHY-USB3320	**USB CONNECTOR**	**Description**
DP, PIN 18	D+, PIN3	D+, differential, USB
DM, PIN 19	D-, PIN2	D-, differential, USB
GND	ID, PIN4	Identity Pin

5.7 SD CARD

The board supports SD Card of size 8,16, 32…, GBs. The SD card can be used for large data files storage or storing image file for running OS. There is a level converter IC between SD-Card pins and ZYNQ and SD-CARD connector IC-10 which level shifts from 1.8V to 3.3V.

Table 15 SD Card to ZYNQ SoC Connections

ZYNQ PINS	**ZYNQ→Level Shifter**	**Level Shifter→ Connector**	**Connector**	**Description**
PS_MIO40_501, D14	CLKA, PIN9	CLKB0, PIN19	CLK, PIN5	Clock for SD Card
PS_MIO41_501, C17	CMDA, PIN4	CMDB0, PIN20	CMD, PIN3	Command Signals
PS_MIO42_501, E12	DAT0, PIN6	DA0B0, PIN18	DAT0, PIN7	Data 0 Pin
PS_MIO43_501, A9	DAT1, PIN7	DAT1B0, PIN16	DAT1, PIN8	Data 1 Pin
PS_MIO44_501, F13	DAT2, PIN1	DAT2B0, PIN23	DAT2, PIN1	Data 2 Pin
PS_MIO45_501, B15	DAT3, PIN3	DAT3B0, PIN22	DAT3, PIN2	Data 3 Pin
PS_MIO46_501, D16	NC,	NC,	DET_SW, PIN 10	Switch detect pin

5.8 GNSS Front-End INTERFACE

There is on-board GNSS IC MAX2769 (IC-21) with front end connector. The GNSS front-end chip is connected on the FPGA bank-34. There is analog and digital section of GNSS, and given below is the digital section connected with ZYNQ.

Table 16 GNSS chip to ZYNQ pin Connections

GNSS MAX 2769 Digital IOs	**ZYNQ, FPGA BANK 34**	**DESCRIPTION**
IDLE, PIN 24	IO_L16N_T2_34, W20	Control Signal GNSS
SHDN, PIN 7	IO_L17P_T2_34, Y18	Control Signal GNSS
SDATA, PIN 8	IO_L17N_T2_34, Y19	Config Data GNSS
SCLK, PIN 9	IO_L13P_T2_MRCC_34, N18	Config Clock GNSS
CS, PIN 10	IO_L18N_T2_34, W16	Control Signal GNSS
PGM, PIN 26	IO_L18P_T2_34, V16	Control Signal GNSS
I1, PIN 21	IO_L19N_T3_VREF_34, R17	MSB I
I0, PIN 20	IO_L19P_T3_34, R16	LSB I
Q0, PIN 18	IO_L20P_T3_34, T17	LSB Q
Q1, PIN 17	IO_L24P_T3_34, P15	MSB Q
CLKOUT, PIN16	IO_L13N_T2_MRCC_34, P19	IQ Clock
ANTFLAG, PIN1	IO_L24N_T3_34, P16	Antenna Connect
LD, PIN6	IO_25_34, T19	PLL Lock Detect

5.9 ATREB INTERFACE

There are two on-board ATREB (IC-1, IC-9) with two front end connectors each. The ATREB front-end chip is connected on the FPGA bank-34 and bank 35. The differential signals are connected to bank 35(LVDS25) where control signals are connected to bank 34(LVCMOS33) There is analog and digital section of ATREB ICs, and given below is the digital section connected with ZYNQ.

5.9.1 ATREB-1 Interface

Table 16 ATREB-1 to ZYNQ pin Connections

ATREB-1 Digital IOs	**ZYNQ, FPGA BANK 34, 35**	**DESCRIPTION**
TXCLKN, PIN 25	IO_L11N_T1_SRCC_35, K18	Transmit Clock -
TXCLKP, PIN 26	IO_L11P_T1_SRCC_35, K17	Transmit Clock +
TXDN, PIN 27	IO_L17N_T2_AD5N_35, H20	Transmit Data -
TXDP, PIN 28	IO_L17P_T2_AD5P_35, J20	Transmit Data -
RXDN09, PIN 30	IO_L18N_T2_AD13N_35, G20	Receive Data Sub GHz -
RXDP09, PIN 31	IO_L18P_T2_AD13P_35, G19	Receive Data Sub GHz +
RXCLKN, PIN 33	IO_L14N_T2_AD4N_SRCC_35, H18	Receive Clock -
RXCLKP, PIN 34	IO_L14P_T2_AD4P_SRCC_35, J18	Receive Clock +
RXDN24, PIN 35	IO_L16N_T2 _35, G18	Receive Data 2.4 GHz -
RXDP24, PIN 36	IO_L16P_T2 _35, G17	Receive Data 2.4 GHz +
SCLK, PIN 41	IO_L11N_T1_SRCC_34, U15	SPI Clock
SELN, PIN 42	IO_L8N_T1_34, Y14	SPI Select
MOSI, PIN 43	IO_L2N_T0_34, U12	SPI MOSI
MISO, PIN 44	IO_L3P_T0_DQS_PUDC_B_34, U13	SPI MISO
IRQ, PIN 40	IO_L7N_T1_34, Y17	ATREB SIGNALS IRQ
RSTN, PIN 13	IO_L8P_T1_34, W14	ATREB SIGNALS Reset
CLKO, PIN 22	IO_L12P_T1_MRCC_34, U18	ATREB SIGNALS Clock Out

5.9.2 ATREB-2 Interface

Table 17 ATREB-2 to ZYNQ pin Connections

ATREB-2 Digital IOs	**ZYNQ, FPGA BANK 34, 35**	**DESCRIPTION**
TXCLKN, PIN 25	IO_L13N_T2_MRCC_35, H17	Transmit Clock -
TXCLKP, PIN 26	IO_L13P_T2_MRCC_35, H16	Transmit Clock +
TXDN, PIN 27	IO_L4N_T0_35, D20	Transmit Data -
TXDP, PIN 28	IO_L4P_T0_35, D19	Transmit Data -
RXDN09, PIN 30	IO_L5N_T0_AD9N_35, E19	Receive Data Sub GHz -

RXDP09, PIN 31	IO_L5P_T0_AD9P_35, E18	Receive Data Sub GHz +
RXCLKN, PIN 33	IO_L11N_T1_SRCC_35, L17	Receive Clock -
RXCLKP, PIN 34	IO_L11P_T1_SRCC_35, L16	Receive Clock +
RXDN24, PIN 35	IO_L2N_T0_AD8P_35, A20	Receive Data 2.4 GHz -
RXDP24, PIN 36	IO_L2P_T0_AD8P_35, B19	Receive Data 2.4 GHz +
SCLK, PIN 41	IO_L11P_T1_SRCC_34, U14	SPI Clock
SELN, PIN 42	IO_L5N_T0_34, T15	SPI Select
MOSI, PIN 43	IO_L4P_T0_34, V12	SPI MOSI
MISO, PIN 44	IO_L3N_T0_DQS_34, V13	SPI MISO
IRQ, PIN 40	IO_L6N_T0_VREF_34, R14	ATREB SIGNALS IRQ
RSTN, PIN 13	IO_L6P_T0_34, P14	ATREB SIGNALS Reset
CLKO, PIN 22	IO_L12N_T1_MRCC_34, U19	ATREB SIGNALS Clock Out

6 On-board Peripherals

6.1 DDR Memory

The board has MT41K256M16TW-107_IT_P DDR3/L SDRAM chip with 16-bit wide memory bus providing total on-board memory size up to 4 Gbit. Size of memory depends on the module variant, refer to the variants table.

6.2 Quad SPI Flash Memory

On-board 128-Mbit QSPI flash memory S25FL128S (IC-14) is used to store initial FPGA configuration. Besides FPGA configuration, remaining free flash memory can be used for user application and data storage. All four SPI data lines are connected to the FPGA allowing x1, x2 or x4 data bus widths. Maximum data rate depends on the selected bus width and clock frequency used.

SPI Flash QE (Quad Enable) bit must be set to high or FPGA is unable to load its configuration from flash during power-on. By default this bit is set to high at the manufacturing plant.

6.3 Gigabit Ethernet PHY

On-board Gigabit Ethernet PHY is provided with Marvell Alaska 88E1512 IC (IC-13). The Ethernet PHY RGMII interface is connected to the Zynq Ethernet0 PS GEM0. I/O voltage is fixed at 1.8V for HSTL signaling. The reference clock input of the PHY is supplied from an on-board 25.000000 MHz oscillator (Y2).

6.4 High-speed USB ULPI PHY

Hi-speed USB ULPI PHY is provided with USB3320 from Microchip. The ULPI interface is connected to the Zynq PS USB0 via MIO28..39, bank 501 (see also section. The I/O voltage is fixed at 1.8V and PHY reference clock input is supplied from the on-board 24.000000 MHz oscillator (Y3).

6.5 MAC-Address EEPROM

A Microchip 2Kbit AT24MAC602 serial EEPROM (U4) is connected to the ZYNQ PL bank pin M14 via 2 IO signals. The EEPROM is I2C based. Chip is programmed at the factory with a globally unique node address stored in the upper 1/4 of the memory array and write-protected through the STATUS register. The remaining 1,536 bits are available for application use.

6.6 Oscillators

Table 18: Board Oscillators

Designator	Purpose	Frequency
Y1	PS clock	33.333333 MHz
XC1	ATREB clock	26MHz
Y4	GPS clock	16.368MHz
Y2	Ethernet clock	25MHz
Y3	USB Full Speed clock	24Mhz

6.7 On-board LEDs

Table 19: LEDs

Designator	Zynq Connection	Purpose	Color
LED1	L15	USER LED PL	Green
LED2	L14	USER LED PL	Green
LED3	N16	USER LED PL	Green
LED4	N15	USER LED PL	Green
LED5	R11	FPGA done pin	Blue
LED6	-	Power LED	Green
LED8	Y16	ATREB LED PL	Green
LED9	T16	ATREB LED PL	Green
LED10	B14	USER LED PS	Red

6.8 On-board Switches

Table 20: Switches

Designator	Zynq Connection	Purpose
S1	L6	PL Reset through PROGRAM_B_0
S2	B9	User defined
S3	B10	PS Reset through PS_SRST

7 Power and Power-On Sequence

7.1 Power Supply

Power supply with minimum current capability of 1A for system startup is recommended.

Power Consumption

Parameter	Conditions	Value
Input current	Vin = 5V; (No Bit File Loaded, Processor Stopped)	140 mA
	Vin = 5V; (Bit File Loaded, Processor and Most of peripherals are running)	450 mA

Table 18: Power Consumption.

7.2 Power-On Sequence

For highest efficiency of the on-board DC-DC regulators, it is recommended to use single 3.3V power source for both VIN and 3.3VIN power rails. Although VIN and 3.3VIN can be powered up in any order, it is recommended to power them up simultaneously.

7.3 Power Rails

Voltage	TP	Connector	Comments
VIN	TP16, TP33		Supply voltage from USB or external Source
VCCIO35			bank voltage
VCCIO33			bank voltage
VCCIO13			bank voltage
VCCIO34			bank voltage
3.3V	TP22		Internal 3.3V voltage
1.8V	TP23		Internal 1.8V voltage
2.5V	TP30		Internal 2.5V voltage

8 Variants Currently in Production

Model	SoC Part Number	DRAM	SPI Flash	Temp Grade	Comments
iotSDR-C710	XC7Z010-2CLG484I	512 MByte	32 Mb	Commercial	-
iotSDR-C720	XC7Z020-2CLG484I	512 MByte	32 Mb	Commercial	-

Table 21: Module variants currently in production.

9 Disclaimer

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