		MC Dir	CU module (2 x 20-	pin)	В	Dir	Status: Mandatory	
	A GND	ווע		_	GND	ווע		
1				2			Network	
3	N.C.		connected	4	N.C.		Not connected	
5	+VAUX		kup DC power	6	NRESET	0	Master reset (active low)	
7	+3V3		power	8	NFAULT	I	Fault (active low)	
9	CH3_IRQ	∣ #3 I	•	10	SYNC	0	Sync output	
11	CH3_CSA		Chip select A	12	SSCL	0	Shared I ² C SCL	
13	CH3_CSB	0 #3 0	Chip select B	14	SSDA	I/O	Shared I ² C SDA	
15	GND			16	GND			
17	CH3 SCLK	0 #3 9	SPI CLK	18	CH3 MISO	- 1	#3 MISO	
19	CH2 IRQ	#2 I	RQ	20	CH3 MOSI	0	#3 MOSI	
21	CH2_CSB	0 #2 0	Chip select B	22	CH2_CSA	0	#2 Chip select A	
23	CH2_SCLK		SPI CLK	24	CH2 MISO	- 1	#2 MISO	
25	CH1_IRQ	#1		26	CH2_MOSI	0	#2 MOSI	
27	CH1 CSB		Chip select B	28	CH1 CSA	0	#1 Chip select A	
29	GND		Jp 00.001 2	30	GND		"_ Cp co.co	
31	CH1_MISO	∣ #1 N	MISO	32	CH1_SCLK	0	#1 SPI CLK	
33	CH1_MOSI		MOSI	34	GND	Ü	WI SI I SER	
35	+5V		power	36	+5V		DC power	
37	+12V		power	38	+12V		DC power	
37 39	GND	DC	howei	36 40	GND		DC howel	
აყ	GND			40	GND	l		
	Peripheral modules (2 x 13-pin) Status: Mandatory							
	Α	Dir	nerai modules (2 x	13-р	B	Div	Status. Manuatory	
		DIL				Dir		
1	GND +5V	D.C.		2	GND +5V		DC mayyar	
3			power	4			DC power	
5	+12V	DC	power	6	+12V		DC power	
7	GND		L L. ODLOUK	8	GND		Manager and Confirm In N	
9	SCLK		lule SPI CLK	10	NRESET		Master reset (active low)	
11	MISO	O Mod	lule MISO	12	NFAULT		Fault (active low)	
13	GND			14	SSCL	I	Shared I ² C SCL	
15	MOSI		lule MOSI	16	SSDA	I/O		
17	CSA		lule Chip select A	18	+3V3		DC power	
19	CSB		lule Chip select B	20	+VAUX		Backup DC power	
21	IRQ	O Mod	lule IRQ	22	SYNC	- 1	Sync input	
23	A1	I ² C /	A1	24	A0	- 1	I ² C A0	
25	A2	I2C /	A2	26	GND			
AUX PS module (2 x 8-pin) Status: Recommended								
	Α	Dir			В	Dir		
1	PE			2	PE			
3	+12V	DC	power	4	+12V		DC power	
5	+5V	DC	power	6	+5V		DC power	
7	GND			8	GND			
9	GND			10	+VAUX		Backup DC power	
11	PWR_SSTART	AC	soft-start	12	PWR_DIRECT	ı	AC power on	
13	SSCL	∣ Sha	red I ² C SCL	14	SSDA	I/O	Shared I ² C SDA	
15	NFAULT	I/O Fau	It (active low)	16	+3V3		DC power	
			,				•	
Power source module (2 x 10-pin) Status: Optional								
	Α	Dir	,		В	Dir	•	
1	IN+		er positive input	2	IN+	-	Power positive input	
3	IN+		er positive input	4	IN+	ı	Power positive input	
			er positive input	6	OUT+	0	Power positive output	
5	IN+	l Pow						
	IN+			8	OUT+	0		
7	IN+ OUT+	O Pow	er positive output	8 10	OUT+	0	Power positive output	
7 9	IN+ OUT+ OUT+	O Pow	ver positive output ver positive output	10	OUT+		Power positive output Power positive output	
7 9 11	IN+ OUT+ OUT+ OUT-	O Pow O Pow	ver positive output ver positive output ver negative output	10 12	OUT+ OUT-	0	Power positive output Power positive output Power negative output	
7 9 11 13	IN+ OUT+ OUT+ OUT- OUT-	O Pow O Pow O Pow	ver positive output ver positive output ver negative output ver negative output	10 12 14	OUT+ OUT- OUT-	0	Power positive output Power positive output Power negative output Power negative output	
7 9 11 13 15	IN+ OUT+ OUT+ OUT- OUT- OUT-	O Pow O Pow O Pow O Pow O Pow	ver positive output ver positive output ver negative output ver negative output ver negative output	10 12 14 16	OUT+ OUT- OUT- IN-	0 0	Power positive output Power positive output Power negative output Power negative output Power negative input	
7 9 11 13	IN+ OUT+ OUT+ OUT- OUT-	O Pow O Pow O Pow O Pow O Pow I Pow	ver positive output ver positive output ver negative output ver negative output	10 12 14	OUT+ OUT- OUT-	0 0	Power positive output Power positive output Power negative output Power negative output	

Notes:

If two or more modules have to be galvanically isolated (e.g. like in case of power modules with floating outputs) use appropriate isolators for control and data lines (e.g. Silabs Si86xx, Maxim MAX14850).