1. Description

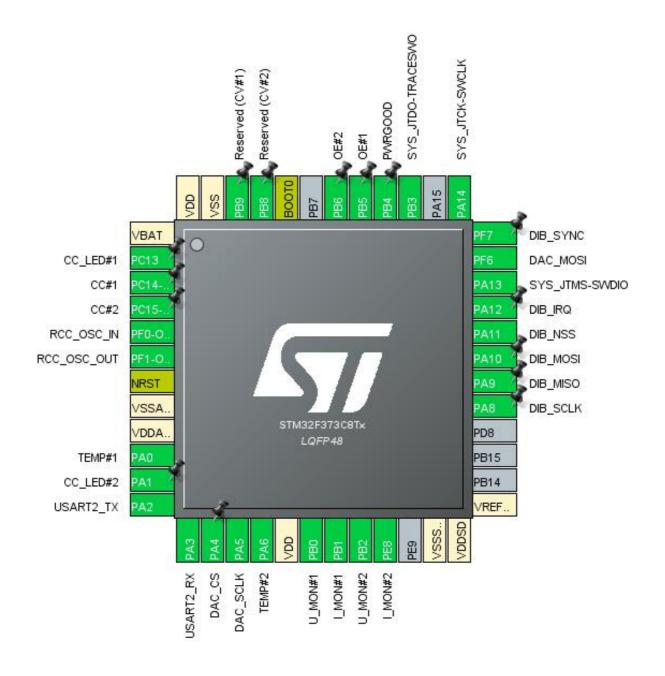
1.1. Project

Project Name	EEZ DIB DCM220 r2B2
Board Name	custom
Generated with:	STM32CubeMX 5.3.0
Date	09/04/2019

1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F373
MCU name	STM32F373C8Tx
MCU Package	LQFP48
MCU Pin number	48

2. Pinout Configuration



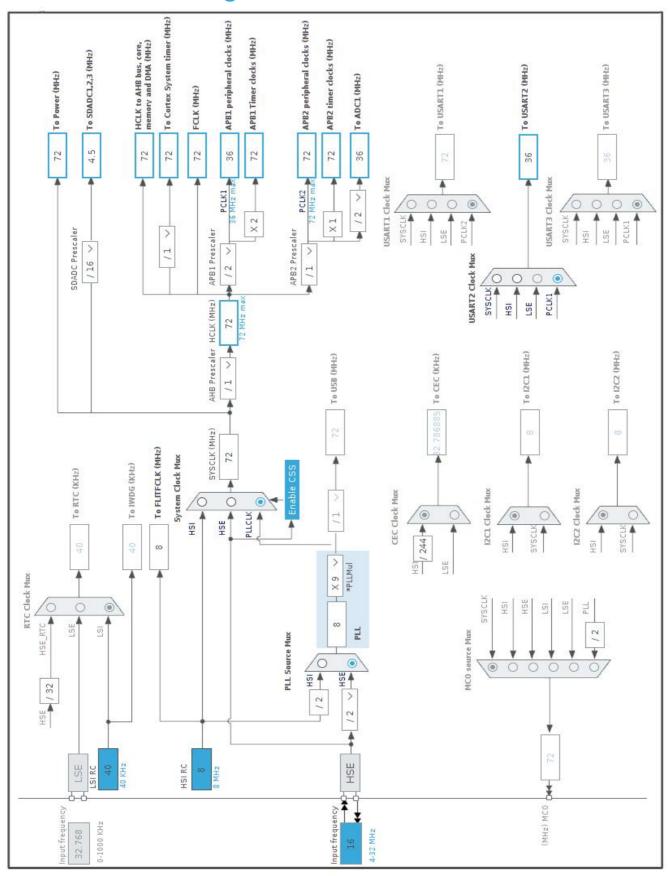
3. Pins Configuration

Pin Number	Pin Name	Pin Type	Alternate	Label
LQFP48	(function after		Function(s)	
4	reset)	Danie		
1	VBAT	Power	000 0 4 4	00 150#4
2	PC13 *	1/0	GPIO_Output	CC_LED#1
3	PC14-OSC32_IN	1/0	GPIO_EXTI14	CC#1
4	PC15-OSC32_OUT	I/O	GPIO_EXTI15	CC#2
5	PF0-OSC_IN	I/O	RCC_OSC_IN	
6	PF1-OSC_OUT	I/O	RCC_OSC_OUT	
7	NRST	Reset		
8	VSSA/VREF-	Power		
9	VDDA/VREF+	Power		
10	PA0	I/O	ADC1_IN0	TEMP#1
11	PA1 *	I/O	GPIO_Output	CC_LED#2
12	PA2	I/O	USART2_TX	
13	PA3	I/O	USART2_RX	
14	PA4 *	I/O	GPIO_Output	DAC_CS
15	PA5	I/O	SPI1_SCK	DAC_SCLK
16	PA6	I/O	ADC1_IN6	TEMP#2
17	VDD	Power		
18	PB0	I/O	SDADC1_AIN6P	U_MON#1
19	PB1	I/O	SDADC1_AIN5P	I_MON#1
20	PB2	I/O	SDADC1_AIN4P	U_MON#2
21	PE8	I/O	SDADC1_AIN8P	I_MON#2
23	VSSSD/VREFSD-	Power		
24	VDDSD	Power		
25	VREFSD+	Power		
29	PA8	I/O	SPI2_SCK	DIB_SCLK
30	PA9	I/O	SPI2_MISO	DIB_MISO
31	PA10	I/O	SPI2_MOSI	DIB_MOSI
32	PA11	I/O	SPI2_NSS	DIB_NSS
33	PA12 *	I/O	GPIO_Output	DIB_IRQ
34	PA13	I/O	SYS_JTMS-SWDIO	-
35	PF6	I/O	SPI1_MOSI	DAC_MOSI
36	PF7	I/O	GPIO_EXTI7	DIB_SYNC
37	PA14	I/O	SYS_JTCK-SWCLK	
39	PB3	I/O	SYS_JTDO-TRACESWO	
40	PB4 *	I/O	GPIO_Input	PWRGOOD
41	PB5 *	1/0	GPIO_Output	OE#1

Pin Number LQFP48	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
42	PB6 *	I/O	GPIO_Output	OE#2
44	воото	Boot		
45	PB8 *	I/O	GPIO_Input	Reserved (CV#2)
46	PB9 *	I/O	GPIO_Input	Reserved (CV#1)
47	VSS	Power		
48	VDD	Power		

^{*} The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	EEZ DIB DCM220 r2B2
Project Folder	/media/denis/9fcb6f91-68fe-4cc2-9835-
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.10.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F3
Line	STM32F373
MCU	STM32F373C8Tx
Datasheet	022691_Rev7

6.2. Parameter Selection

Temperature	25
Vdd	3.6

7. IPs and Middleware Configuration

7.1. ADC1

mode: IN0 mode: IN6

mode: Temperature Sensor Channel

7.1.1. Parameter Settings:

ADC_Settings:

Data Alignment

Scan Conversion Mode

Continuous Conversion Mode

Disabled

Discontinuous Conversion Mode

Disabled

Disabled

ADC_Regular_ConversionMode:

Enable Regular Conversions Enable
Number Of Conversion 1

External Trigger Conversion Source Regular Conversion launched by software

Rank 1

Channel Temperature Sensor *

Sampling Time 1.5 Cycles

 $ADC_Injected_ConversionMode:$

Number Of Conversions 0

WatchDog:

Enable Analog WatchDog Mode false

7.2. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

7.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 2 WS (3 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

7.3. SDADC1

IN4: IN4-Single-Ended zero reference IN5: IN5-Single-Ended zero reference IN6: IN6-Single-Ended zero reference IN8: IN8-Single-Ended zero reference mode: Conversion Configuration 0

7.3.1. Parameter Settings:

General Settings:

Low Power ModeNoneFast Conversion ModeDisableSlow Clock ModeDisable

Reference Voltage Forced externally using VREF pin

Conversion Configuration 0:

Input Mode Single-ended zero-volt reference mode *

Gain equal to 1

Common Mode SDADC VSSA

Offset 0

SDADC Regular Conversions Settings:

Enable Regular Conversion Disable

SDADC Injected Conversions Settings:

Enable Injected Conversion Disable

7.4. SPI1

Mode: Half-Duplex Master 7.4.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits *

First Bit MSB First

Clock Parameters:

Prescaler (for Baud Rate) 4 *

Baud Rate 18.0 MBits/s *

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled

NSSP Mode Enabled

NSS Signal Type Software

7.5. SPI2

Mode: Full-Duplex Slave

Hardware NSS Signal: Hardware NSS Input Signal

7.5.1. Parameter Settings:

Basic Parameters:

Frame Format Motorola

Data Size 8 Bits *

First Bit MSB First

Clock Parameters:

Clock Polarity (CPOL) Low
Clock Phase (CPHA) 1 Edge

Advanced Parameters:

CRC Calculation Disabled

NSS Signal Type Input Hardware

7.6. SYS

Debug: Trace Asynchronous Sw

Timebase Source: SysTick

7.7. **USART2**

Mode: Asynchronous

7.7.1. Parameter Settings:

Basic Parameters:

Baud Rate 38400

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

Auto Baudrate Disable TX Pin Active Level Inversion Disable RX Pin Active Level Inversion Disable Disable Data Inversion TX and RX Pins Swapping Disable Enable Overrun Enable DMA on RX Error MSB First Disable

^{*} User modified value

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
ADC1	PA0	ADC1_IN0	Analog mode	No pull up pull down	n/a	TEMP#1
	PA6	ADC1_IN6	Analog mode	No pull up pull down	n/a	TEMP#2
RCC	PF0-OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PF1- OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
SDADC1	PB0	SDADC1_AIN6P	Analog mode	No pull up pull down	n/a	U_MON#1
	PB1	SDADC1_AIN5P	Analog mode	No pull up pull down	n/a	I_MON#1
	PB2	SDADC1_AIN4P	Analog mode	No pull up pull down	n/a	U_MON#2
	PE8	SDADC1_AIN8P	Analog mode	No pull up pull down	n/a	I_MON#2
SPI1	PA5	SPI1_SCK	Alternate Function Push Pull	No pull up pull down	High *	DAC_SCLK
	PF6	SPI1_MOSI	Alternate Function Push Pull	No pull up pull down	High *	DAC_MOSI
SPI2	PA8	SPI2_SCK	Alternate Function Push Pull	No pull up pull down	High *	DIB_SCLK
	PA9	SPI2_MISO	Alternate Function Push Pull	No pull up pull down	High *	DIB_MISO
	PA10	SPI2_MOSI	Alternate Function Push Pull	No pull up pull down	High *	DIB_MOSI
	PA11	SPI2_NSS	Alternate Function Push Pull	No pull up pull down	High *	DIB_NSS
SYS	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO- TRACESWO	n/a	n/a	n/a	
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull up pull down	High *	
	PA3	USART2_RX	Alternate Function Push Pull	No pull up pull down	High *	
GPIO	PC13	GPIO_Output	Output Push Pull	No pull up pull down	Low	CC_LED#1
	PC14- OSC32_IN	GPIO_EXTI14	External Interrupt Mode with Rising/Falling edge	No pull up pull down	n/a	CC#1
	PC15- OSC32_OU T	GPIO_EXTI15	External Interrupt Mode with Rising/Falling edge	No pull up pull down	n/a	CC#2
	PA1	GPIO_Output	Output Push Pull	No pull up pull down	Low	CC_LED#2
	PA4	GPIO_Output	Output Push Pull	No pull up pull down	Low	DAC_CS
	PA12	GPIO_Output	Output Push Pull	No pull up pull down	Low	DIB_IRQ
	PF7	GPIO_EXTI7	External Interrupt Mode with Rising edge trigger detection	No pull up pull down	n/a	DIB_SYNC

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB4	GPIO_Input	Input mode	Pull-up *	n/a	PWRGOOD
	PB5	GPIO_Output	Output Push Pull	No pull up pull down	Low	OE#1
	PB6	GPIO_Output	Output Push Pull	No pull up pull down	Low	OE#2
	PB8	GPIO_Input	Input mode	No pull up pull down	n/a	Reserved (CV#2)
	PB9	GPIO_Input	Input mode	No pull up pull down	n/a	Reserved (CV#1)

8.2. DMA configuration

DMA request	Stream	Direction	Priority
SPI2_RX	DMA1_Channel4	Peripheral To Memory	Low
SPI2_TX	DMA1_Channel5	Memory To Peripheral	Low

SPI2_RX: DMA1_Channel4 DMA request Settings:

Normal Mode: Peripheral Increment: Disable Memory Increment: Enable * Peripheral Data Width: Byte Memory Data Width:

SPI2_TX: DMA1_Channel5 DMA request Settings:

Byte

Mode: Normal Peripheral Increment: Disable Memory Increment: Enable *

Byte Peripheral Data Width: Memory Data Width: Byte

8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority	
Non maskable interrupt	true	0	0	
Hard fault interrupt	true	0	0	
Memory management fault	true	0	0	
Prefetch fault, memory access fault	true	0	0	
Undefined instruction or illegal state	true	0	0	
System service call via SWI instruction	true	0	0	
Debug monitor	true	0	0	
Pendable request for system service	true	0	0	
System tick timer	true	0	0	
DMA1 channel4 global interrupt	true	0	0	
DMA1 channel5 global interrupt	true	0	0	
EXTI line[9:5] interrupts	true	0	0	
EXTI line[15:10] interrupts	true	0	0	
PVD interrupt through EXTI line16		unused		
Flash global interrupt		unused		
RCC global interrupt		unused		
ADC1 interrupt		unused		
SPI1 global interrupt	unused			
SPI2 global interrupt	unused			
USART2 global interrupt / USART2 wake-up interrupt through EXTI line 26	unused			
SDADC1 global interrupt	unused			
Floating point unit interrupt	unused			

^{*} User modified value

9. So	ftware	Pack	Re	port
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