1. Description

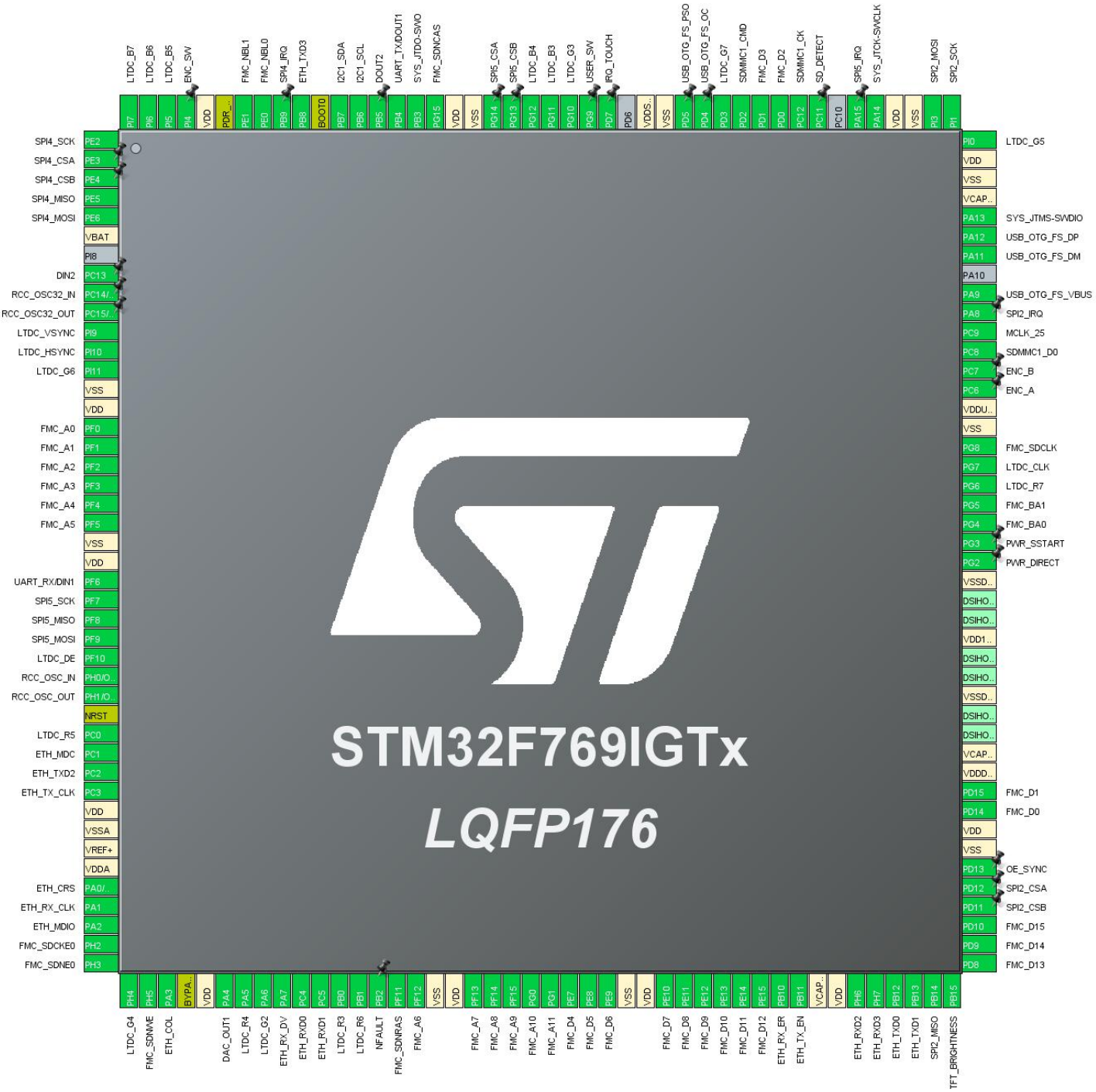
1.1. Project

Project Name	EEZ DIB STM32F7 r2B4
Board Name	EEZ BB3 MCU board v0.3
Generated with:	STM32CubeMX 5.6.1
Date	06/11/2020

1.2. MCU

MCU Series	STM32F7
MCU Line	STM32F7x9
MCU name	STM32F769IGTx
MCU Package	LQFP176
MCU Pin number	176

2. Pinout Configuration



3. Pins Configuration

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	PE2	I/O	SPI4_SCK	
2	PE3 *	I/O	GPIO_Output	SPI4_CSA
3	PE4 *	I/O	GPIO_Output	SPI4_CSB
4	PE5	I/O	SPI4_MISO	
5	PE6	I/O	SPI4_MOSI	
6	VBAT	Power		
8	PC13 *	I/O	GPIO_Input	DIN2
9	PC14/OSC32_IN	I/O	RCC_OSC32_IN	
10	PC15/OSC32_OUT	I/O	RCC_OSC32_OUT	
11	PI9	I/O	LTDC_VSYNC	
12	PI10	I/O	LTDC_HSYNC	
13	PI11	I/O	LTDC_G6	
14	VSS	Power		
15	VDD	Power		
16	PF0	I/O	FMC_A0	
17	PF1	I/O	FMC_A1	
18	PF2	I/O	FMC_A2	
19	PF3	I/O	FMC_A3	
20	PF4	I/O	FMC_A4	
21	PF5	I/O	FMC_A5	
22	VSS	Power		
23	VDD	Power		
24	PF6	I/O	UART7_RX	UART_RX/DIN1
25	PF7	I/O	SPI5_SCK	
26	PF8	I/O	SPI5_MISO	
27	PF9	I/O	SPI5_MOSI	
28	PF10	I/O	LTDC_DE	
29	PH0/OSC_IN	I/O	RCC_OSC_IN	
30	PH1/OSC_OUT	I/O	RCC_OSC_OUT	
31	NRST	Reset		
32	PC0	I/O	LTDC_R5	
33	PC1	I/O	ETH_MDC	
34	PC2	I/O	ETH_TXD2	
35	PC3	I/O	ETH_TX_CLK	
36	VDD	Power		
37	VSSA	Power		

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
38	VREF+	Power		
39	VDDA	Power		
40	PA0/WKUP	I/O	ETH_CRS	
41	PA1	I/O	ETH_RX_CLK	
42	PA2	I/O	ETH_MDIO	
43	PH2	I/O	FMC_SDCKE0	
44	PH3	I/O	FMC_SDNE0	
45	PH4	I/O	LTDC_G4	
46	PH5	I/O	FMC_SDNWE	
47	PA3	I/O	ETH_COL	
48	BYPASS_REG	Reset		
49	VDD	Power		
50	PA4	I/O	DAC_OUT1	
51	PA5	I/O	LTDC_R4	
52	PA6	I/O	LTDC_G2	
53	PA7	I/O	ETH_RX_DV	
54	PC4	I/O	ETH_RXD0	
55	PC5	I/O	ETH_RXD1	
56	PB0	I/O	LTDC_R3	
57	PB1	I/O	LTDC_R6	
58	PB2 *	I/O	GPIO_Input	NFAULT
59	PF11	I/O	FMC_SDNRAS	
60	PF12	I/O	FMC_A6	
61	VSS	Power		
62	VDD	Power		
63	PF13	I/O	FMC_A7	
64	PF14	I/O	FMC_A8	
65	PF15	I/O	FMC_A9	
66	PG0	I/O	FMC_A10	
67	PG1	I/O	FMC_A11	
68	PE7	I/O	FMC_D4	
69	PE8	I/O	FMC_D5	
70	PE9	I/O	FMC_D6	
71	VSS	Power		
72	VDD	Power		
73	PE10	I/O	FMC_D7	
74	PE11	I/O	FMC_D8	
75	PE12	I/O	FMC_D9	
76	PE13	I/O	FMC_D10	

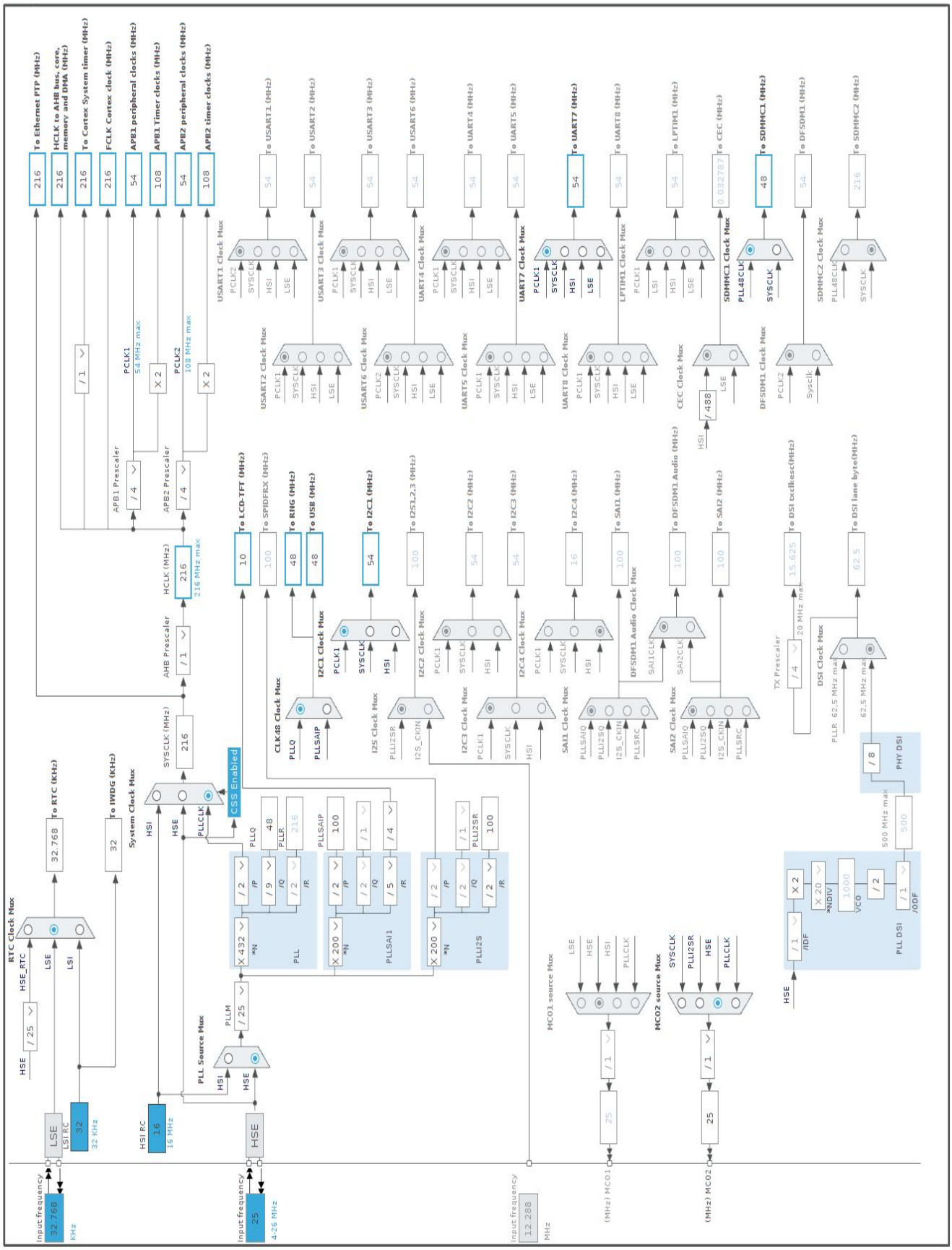
Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
77	PE14	I/O	FMC_D11	
78	PE15	I/O	FMC_D12	
79	PB10	I/O	ETH_RX_ER	
80	PB11	I/O	ETH_TX_EN	
81	VCAP_1	Power		
82	VDD	Power		
83	PH6	I/O	ETH_RXD2	
84	PH7	I/O	ETH_RXD3	
85	PB12	I/O	ETH_TXD0	
86	PB13	I/O	ETH_TXD1	
87	PB14	I/O	SPI2_MISO	
88	PB15	I/O	TIM12_CH2	TFT_BRIGHTNESS
89	PD8	I/O	FMC_D13	
90	PD9	I/O	FMC_D14	
91	PD10	I/O	FMC_D15	
92	PD11 *	I/O	GPIO_Output	SPI2_CSB
93	PD12 *	I/O	GPIO_Output	SPI2_CSA
94	PD13 *	I/O	GPIO_Output	OE_SYNC
95	VSS	Power		
96	VDD	Power		
97	PD14	I/O	FMC_D0	
98	PD15	I/O	FMC_D1	
99	VDDDSI	Power		
100	VCAPDSI	Power		
103	VSSDSI	Power		
106	VDD12DSI	Power		
109	VSSDSI	Power		
110	PG2 *	I/O	GPIO_Output	PWR_DIRECT
111	PG3 *	I/O	GPIO_Output	PWR_SSTART
112	PG4	I/O	FMC_BA0	
113	PG5	I/O	FMC_BA1	
114	PG6	I/O	LTDC_R7	
115	PG7	I/O	LTDC_CLK	
116	PG8	I/O	FMC_SDCLK	
117	VSS	Power		
118	VDDUSB	Power		
119	PC6	I/O	GPIO_EXTI6	ENC_A
120	PC7	I/O	GPIO_EXTI7	ENC_B
121	PC8	I/O	SDMMC1_D0	

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
122	PC9	I/O	RCC_MCO_2	MCLK_25
123	PA8	I/O	GPIO_EXTI8	SPI2_IRQ
124	PA9	I/O	USB_OTG_FS_VBUS	
126	PA11	I/O	USB_OTG_FS_DM	
127	PA12	I/O	USB_OTG_FS_DP	
128	PA13	I/O	SYS_JTMS-SWDIO	
129	VCAP_2	Power		
130	VSS	Power		
131	VDD	Power		
132	PI0	I/O	LTDC_G5	
133	PI1	I/O	SPI2_SCK	
134	PI3	I/O	SPI2_MOSI	
135	VSS	Power		
136	VDD	Power		
137	PA14	I/O	SYS_JTCK-SWCLK	
138	PA15	I/O	GPIO_EXTI15	SPI5_IRQ
140	PC11	I/O	GPIO_EXTI11	SD_DETECT
141	PC12	I/O	SDMMC1_CK	
142	PD0	I/O	FMC_D2	
143	PD1	I/O	FMC_D3	
144	PD2	I/O	SDMMC1_CMD	
145	PD3	I/O	LTDC_G7	
146	PD4 *	I/O	GPIO_Input	USB_OTG_FS_OC
147	PD5 *	I/O	GPIO_Output	USB_OTG_FS_PSO
148	VSS	Power		
149	VDDSDMMC	Power		
151	PD7 *	I/O	GPIO_Input	IRQ_TOUCH
152	PG9 *	I/O	GPIO_Input	USER_SW
153	PG10	I/O	LTDC_G3	
154	PG11	I/O	LTDC_B3	
155	PG12	I/O	LTDC_B4	
156	PG13 *	I/O	GPIO_Output	SPI5_CSB
157	PG14 *	I/O	GPIO_Output	SPI5_CSA
158	VSS	Power		
159	VDD	Power		
160	PG15	I/O	FMC_SDNCAS	
161	PB3	I/O	SYS_JTDO-SWO	
162	PB4	I/O	UART7_TX	UART_TX/DOUT1
163	PB5	I/O	TIM3_CH2	DOUT2

Pin Number LQFP176	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
164	PB6	I/O	I2C1_SCL	
165	PB7	I/O	I2C1_SDA	
166	BOOT0	Boot		
167	PB8	I/O	ETH_TXD3	
168	PB9	I/O	GPIO_EXTI9	SPI4_IRQ
169	PE0	I/O	FMC_NBL0	
170	PE1	I/O	FMC_NBL1	
171	PDR_ON	Reset		
172	VDD	Power		
173	PI4 *	I/O	GPIO_Input	ENC_SW
174	PI5	I/O	LTDC_B5	
175	PI6	I/O	LTDC_B6	
176	PI7	I/O	LTDC_B7	

* The pin is affected with an I/O function

4. Clock Tree Configuration



5. Software Project

5.1. Project Settings

Name	Value
Project Name	EEZ DIB STM32F7 r2B4
Project Folder	/home/denis/BACKUP/EEZ/Digital control/MCU/STM32/Projects/EEZ DIB
Toolchain / IDE	TrueSTUDIO
Firmware Package Name and Version	STM32Cube FW_F7 V1.16.0

5.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	Yes
Backup previously generated files when re-generating	No
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power consumption)	Yes

6. Power Consumption Calculator report

6.1. Microcontroller Selection

Series	STM32F7
Line	STM32F7x9
MCU	STM32F769IGTx
Datasheet	029041_Rev4

6.2. Parameter Selection

Temperature	25
Vdd	3.3

6.3. Battery Selection

Battery	Alkaline(9V)
Capacity	625.0 mAh
Self Discharge	0.3 %/month
Nominal Voltage	9.0 V
Max Cont Current	200.0 mA
Max Pulse Current	0.0 mA
Cells in series	1
Cells in parallel	1

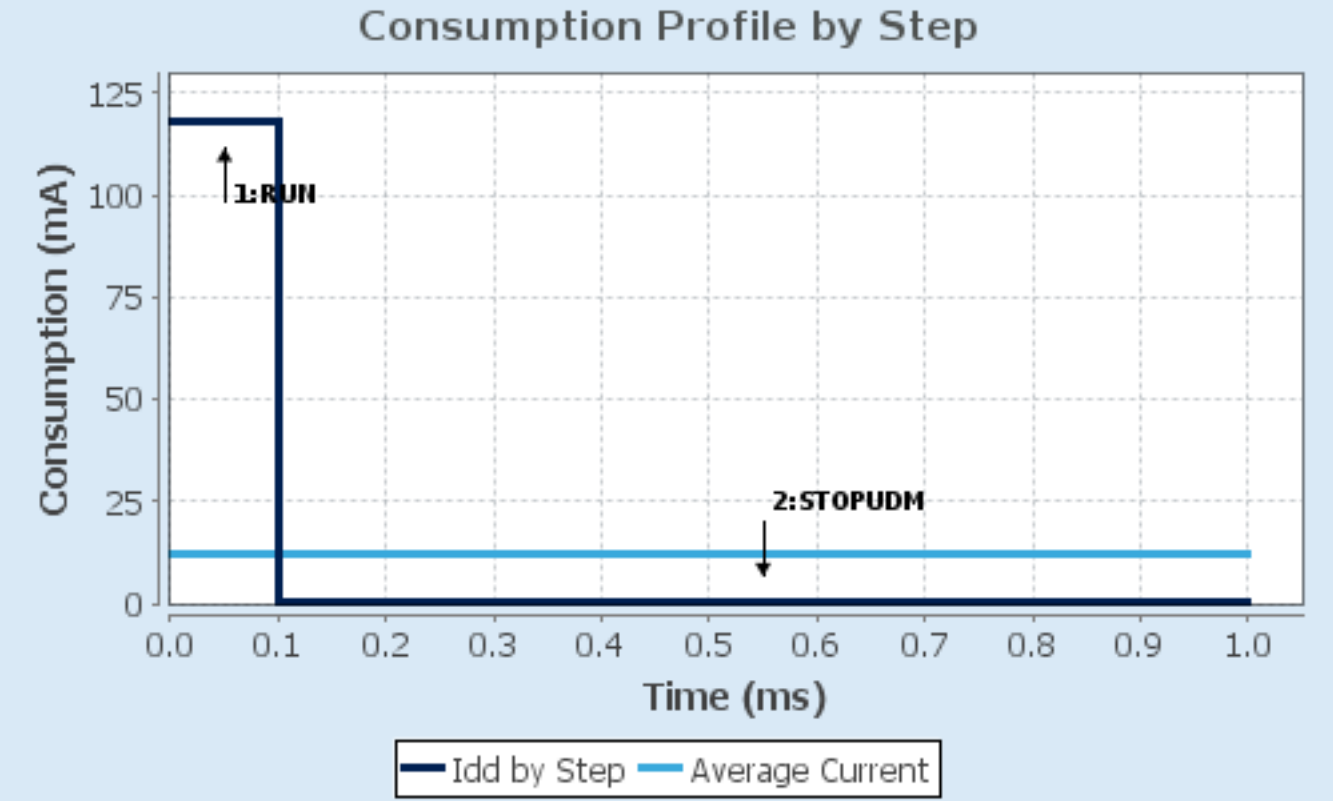
6.4. Sequence

Step	Step1	Step2
Mode	RUN	STOP_UDM (Under Drive)
Vdd	3.3	3.3
Voltage Source	Battery	Battery
Range	Scale1-High	No Scale
Fetch Type	ICTM FLASH-SingleBank REGON	n/a
CPU Frequency	216 MHz	0 Hz
Clock Configuration	HSE PLL	Regulator_LP Flash-PwrDwn
Clock Source Frequency	4 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	118 mA	130 µA
Duration	0.1 ms	0.9 ms
DMIPS	462.0	0.0
Ta Max	90.2	104.98
Category	In DS Table	In DS Table

6.5. RESULTS

Sequence Time	1 ms	Average Current	11.92 mA
Battery Life	2 days, 4 hours	Average DMIPS	462.24 DMIPS

6.6. Chart


Consumption Profile by Step
Consumption (mA)
125
100
75
50
25
0
1:RUN
2:STOPUDM
0.0
0.1
0.2
0.3
0.4
0.5
0.6
0.7
0.8
0.9
1.0
Time (ms)
Idd by Step
Average Current

7. IPs and Middleware Configuration

7.1. ADC1

mode: Vbat Channel

7.1.1. Parameter Settings:

ADCs_Common_Settings:

Mode	Independent mode

ADC_Settings:

Clock Prescaler	PCLK2 divided by 2
Resolution	12 bits (15 ADC Clock cycles)
Data Alignment	Right alignment
Scan Conversion Mode	Disabled
Continuous Conversion Mode	Disabled
Discontinuous Conversion Mode	Disabled
DMA Continuous Requests	Disabled
End Of Conversion Selection	EOC flag at the end of single channel conversion

ADC_Regular_ConversionMode:

Number Of Conversion	1
External Trigger Conversion Source	Regular Conversion launched by software
External Trigger Conversion Edge	None
Rank	1
Channel	Channel Vbat
Sampling Time	**15 Cycles ***

ADC_Injected_ConversionMode:

Number Of Conversions	0

WatchDog:

Enable Analog WatchDog Mode	false

7.2. CORTEX_M7

7.2.1. Parameter Settings:

Cortex Interface Settings:

Flash Interface	AXI Interface
ART ACCLERATOR	Disabled
Instruction Prefetch	Disabled
CPU ICache	Disabled
CPU DCache	Disabled

Cortex Memory Protection Unit Control Settings:

MPU Control Mode	MPU NOT USED

7.3. CRC

mode: Activated

7.3.1. Parameter Settings:

Basic Parameters:

Default Polynomial State	Enable
Default Init Value State	Enable

Advanced Parameters:

Input Data Inversion Mode	None
Output Data Inversion Mode	Disable
Input Data Format	Bytes

7.4. DAC

mode: OUT1 Configuration

7.4.1. Parameter Settings:

DAC Out1 Settings:

Output Buffer	Enable
Trigger	**Timer 6 Trigger Out event ***
Wave generation mode	Disabled

7.5. DMA2D

mode: Activated

7.5.1. Parameter Settings:

Basic Parameters:

Transfer Mode	Memory to Memory
Color Mode	**RGB565 ***
Output Offset	0
DMA2D Bytes Swap	Bytes in regular order in output FIFO
DMA2D Line Offset Mode	Line offsets expressed in pixels

Foreground layer Configuration:

DMA2D Input Color Mode	RGB565
DMA2D ALPHA MODE	No modification of the alpha channel value
Input Alpha	0
Input Offset	0
DMA2D ALPHA Inversion	Regular Alpha
DMA2D Red and Blue swap	Regular mode (RGB or ARGB)

7.6. ETH

Mode: MII

mode: Activate Rx Err signal

7.6.1. Parameter Settings:

Advanced : Ethernet Media Configuration:

Auto Negotiation	Enabled

General : Ethernet Configuration:

Ethernet MAC Address	00:80:E1:00:00:00
PHY Address	1

Ethernet Basic Configuration:

Rx Mode	Interrupt Mode
TX IP Header Checksum Computation	By hardware

7.6.2. Advanced Parameters:

External PHY Configuration:

PHY	DP83848_PHY_ADDRESS
PHY Address Value	1
PHY Reset delay these values are based on a 1 ms Systick interrupt	**0x000000FF ***
PHY Configuration delay	**0x00000FFF ***
PHY Read TimeOut	**0x0000FFFF ***
PHY Write TimeOut	**0x0000FFFF ***

Common : External PHY Configuration:

Transceiver Basic Control Register	**0x00 ***
Transceiver Basic Status Register	**0x01 ***
PHY Reset	**0x8000 ***
Select loop-back mode	**0x4000 ***

Set the full-duplex mode at 100 Mb/s	**0x2100 ***
Set the half-duplex mode at 100 Mb/s	**0x2000 ***
Set the full-duplex mode at 10 Mb/s	**0x0100 ***
Set the half-duplex mode at 10 Mb/s	**0x0000 ***
Enable auto-negotiation function	**0x1000 ***
Restart auto-negotiation function	**0x0200 ***
Select the power down mode	**0x0800 ***
Isolate PHY from MII	**0x0400 ***
Auto-Negotiation process completed	**0x0020 ***
Valid link established	**0x0004 ***
Jabber condition detected	**0x0002 ***

Extended : External PHY Configuration:

PHY special control/status register Offset	**0x1F ***
MII Interrupt Control Register	**0x11 ***
MII Interrupt Status and Misc. Control Register	**0x12 ***
PHY Link mask	**0x0001 ***
PHY Speed mask	**0x0004 ***
PHY Duplex mask	**0x0010 ***
PHY Enable interrupts	**0x0002 ***
PHY Enable output interrupt events	**0x0001 ***
Enable Interrupt on change of link status	**0x0020 ***
PHY link status interrupt mask	**0x2000 ***

7.7. FMC

SDRAM 1

Clock and chip enable: SDCKE0+SDNE0

Internal bank number: 4 banks

Address: 12 bits

Data: 16 bits

Byte enable: 16-bit byte enable

7.7.1. SDRAM 1:

SDRAM control:

Bank	SDRAM bank 1
Number of column address bits	8 bits

Number of row address bits	12 bits
CAS latency	**3 memory clock cycles ***
Write protection	Disabled
SDRAM common clock	**2 HCLK clock cycles ***
SDRAM common burst read	Disabled
SDRAM common read pipe delay	**1 HCLK clock cycle ***

SDRAM timing in memory clock cycles:

Load mode register to active delay	**2 ***
Exit self-refresh delay	**7 ***
Self-refresh time	**4 ***
SDRAM common row cycle delay	**7 ***
Write recovery time	**3 ***
SDRAM common row precharge delay	**2 ***
Row to column delay	**2 ***

7.8. GPIO

7.9. I2C1

I2C: I2C

7.9.1. Parameter Settings:

Timing configuration:

I2C Speed Mode	**Fast Mode ***
I2C Speed Frequency (KHz)	400
Rise Time (ns)	0
Fall Time (ns)	0
Coefficient of Digital Filter	0
Analog Filter	Enabled
Timing	**0x6000030D ***

Slave Features:

Clock No Stretch Mode	Disabled
General Call Address Detection	Disabled
Primary Address Length selection	7-bit
Dual Address Acknowledged	Disabled
Primary slave address	0

7.10. IWDG

mode: Activated

7.10.1. Parameter Settings:

Watchdog Clocking:

IWDG counter clock prescaler	**16 ***
IWDG window value	4095
IWDG down-counter reload value	4095

7.11. JPEG

mode: Activated

7.11.1. Parameter Settings:

Version:

JPEG version	jpeg1_v1_0

JPEG Software options:

ENCODE	Enabled
DECODE	Enabled
RGB_FORMAT	**JPEG_RGB565 ***
JPEG_SWAP_RG	0

7.12. LTDC

Display Type: RGB565 (16 bits)

7.12.1. Parameter Settings:

Synchronization for Width:

Horizontal Synchronization Width	**51 ***
Horizontal Back Porch	**43 ***
Active Width	**480 ***
Horizontal Front Porch	**8 ***
HSync Width	50
Accumulated Horizontal Back Porch Width	93
Accumulated Active Width	573
Total Width	581

Synchronization for Height:

Vertical Synchronization Height	**20 ***
Vertical Back Porch	**12 ***
Active Height	**272 ***
Vertical Front Porch	**8 ***
VSync Height	19
Accumulated Vertical Back Porch Height	31
Accumulated Active Height	303
Total Height	311

Signal Polarity:

Horizontal Synchronization Polarity	**Active High ***
Vertical Synchronization Polarity	Active Low
Not Data Enable Polarity	Active Low
Pixel Clock Polarity	Normal Input

BackGround Color:

Red	0
Green	0
Blue	0

7.12.2. Layer Settings:

BackGround Color:

Layer 0 - Blue	0
Layer 0 - Green	0
Layer 0 - Red	0

Windows Position:

Layer 0 - Window Horizontal Start	0
Layer 0 - Window Horizontal Stop	**480 ***
Layer 0 - Window Vertical Start	0
Layer 0 - Window Vertical Stop	**272 ***

Pixel Parameters:

Layer 0 - Pixel Format	**RGB565 ***

Blending:

Layer 0 - Alpha constant for blending	**255 ***
Layer 0 - Default Alpha value	**255 ***
Layer 0 - Blending Factor1	Alpha constant
Layer 0 - Blending Factor2	Alpha constant

Frame Buffer:

Layer 0 - Color Frame Buffer Start Adress	0

Layer 0 - Color Frame Buffer Line Length (Image Width)	**480 ***
Layer 0 - Color Frame Buffer Number of Lines (Image Height)	**272 ***

Number of Layers:

Number of Layers	**1 layer ***

7.13. RCC

High Speed Clock (HSE): Crystal/Ceramic Resonator

Low Speed Clock (LSE) : Crystal/Ceramic Resonator

mode: Master Clock Output 2

7.13.1. Parameter Settings:

System Parameters:

VDD voltage (V)	3.3
Flash Latency(WS)	7 WS (8 CPU cycle)

RCC Parameters:

HSI Calibration Value	16
TIM Prescaler Selection	Disabled
HSE Startup Timout Value (ms)	100
LSE Startup Timout Value (ms)	5000
LSE Drive Capability	LSE oscillator low drive capability

Power Parameters:

Power Over Drive	Enabled
Power Regulator Voltage Scale	Power Regulator Voltage Scale 1

7.14. RNG

mode: Activated

7.15. RTC

mode: Activate Clock Source

7.15.1. Parameter Settings:

General:

Hour Format	Hourformat 24
Asynchronous Predivider value	127

Synchronous Predivider value	255

7.16. SDMMC1

Mode: SD 1 bit

7.16.1. Parameter Settings:

SDMMC parameters:

Clock transition on which the bit capture is made	Rising transition
SDMMC Clock divider bypass	Disable
SDMMC Clock output enable when the bus is idle	Disable the power save for the clock
SDMMC hardware flow control	**The hardware control flow is enabled ***
SDMMCCLK clock divide factor	0

7.17. SPI2

Mode: Full-Duplex Master

7.17.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**3.375 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.18. SPI4

Mode: Full-Duplex Master

7.18.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**3.375 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.19. SPI5

Mode: Full-Duplex Master

7.19.1. Parameter Settings:

Basic Parameters:

Frame Format	Motorola
Data Size	**8 Bits ***
First Bit	MSB First

Clock Parameters:

Prescaler (for Baud Rate)	**16 ***
Baud Rate	**3.375 MBits/s ***
Clock Polarity (CPOL)	Low
Clock Phase (CPHA)	1 Edge

Advanced Parameters:

CRC Calculation	Disabled
NSSP Mode	Enabled
NSS Signal Type	Software

7.20. SYS

Debug: Trace Asynchronous Sw

Timebase Source: TIM10

7.21. TIM3

Channel2: PWM Generation CH2

7.21.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**100 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**1000 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

Trigger Output (TRGO) Parameters:

Master/Slave Mode (MSM bit)	Disable (Trigger input effect not delayed)
Trigger Event Selection TRGO	Reset (UG bit from TIMx_EGR)

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	0
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.22. TIM6

mode: Activated

7.22.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	0
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**2249 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	**Update Event ***

7.23. TIM7

mode: Activated

7.23.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**215 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**99 ***
auto-reload preload	**Enable ***

Trigger Output (TRGO) Parameters:

Trigger Event Selection	Reset (UG bit from TIMx_EGR)

7.24. TIM12

Channel2: PWM Generation CH2

7.24.1. Parameter Settings:

Counter Settings:

Prescaler (PSC - 16 bits value)	**3 ***
Counter Mode	Up
Counter Period (AutoReload Register - 16 bits value)	**999 ***
Internal Clock Division (CKD)	No Division
auto-reload preload	Disable

PWM Generation Channel 2:

Mode	PWM mode 1
Pulse (16 bits value)	**499 ***
Output compare preload	Enable
Fast Mode	Disable
CH Polarity	High

7.25. UART7

Mode: Asynchronous

7.25.1. Parameter Settings:

Basic Parameters:

Baud Rate	115200
Word Length	**9 Bits (including Parity) ***
Parity	**Even ***
Stop Bits	1

Advanced Parameters:

Data Direction	Receive and Transmit
Over Sampling	16 Samples
Single Sample	Disable

Advanced Features:

Auto Baudrate	Disable
TX Pin Active Level Inversion	Disable
RX Pin Active Level Inversion	Disable
Data Inversion	Disable
TX and RX Pins Swapping	Disable
Overrun	Enable
DMA on RX Error	Enable
MSB First	Disable

7.26. USB_OTG_FS

Mode: Device_Only

mode: Activate_VBUS

7.26.1. Parameter Settings:

Speed	Device Full Speed 12MBit/s
Low power	Disabled
Link Power Management	Disabled
VBUS sensing	Enabled
Signal start of frame	Disabled

7.27. FATFS

mode: SD Card

7.27.1. Set Defines:

Version:

FATFS version	R0.12c

Function Parameters:

FS_READONLY (Read-only mode)	Disabled

FS_MINIMIZE (Minimization level)	Disabled
USE_STRFUNC (String functions)	**Disabled ***
USE_FIND (Find functions)	**Enabled ***
USE_MKFS (Make filesystem function)	Enabled
USE_FASTSEEK (Fast seek function)	Enabled
USE_EXPAND (Use f_expand function)	Disabled
USE_CHMOD (Change attributes function)	Disabled
USE_LABEL (Volume label functions)	Disabled
USE_FORWARD (Forward function)	Disabled

Locale and Namespace Parameters:

CODE_PAGE (Code page on target)	Latin 1
USE_LFN (Use Long Filename)	**Enabled with dynamic working buffer on the STACK ***
MAX_LFN (Max Long Filename)	255
LFN_UNICODE (Enable Unicode)	ANSI/OEM
STRF_ENCODE (Character encoding)	UTF-8
FS_RPATH (Relative Path)	Disabled

Physical Drive Parameters:

VOLUMES (Logical drives)	1
MAX_SS (Maximum Sector Size)	512
MIN_SS (Minimum Sector Size)	512
MULTI_PARTITION (Volume partitions feature)	Disabled
USE_TRIM (Erase feature)	Disabled
FS_NOFSINFO (Force full FAT scan)	0

System Parameters:

FS_TINY (Tiny mode)	Disabled
FS_EXFAT (Support of exFAT file system)	Disabled
FS_NORTC (Timestamp feature)	Dynamic timestamp
FS_REENTRANT (Re-Entrancy)	Enabled
FS_TIMEOUT (Timeout ticks)	1000
USE_MUTEX	Disabled
SYNC_t (O/S sync object)	osSemaphoreId
FS_LOCK (Number of files opened simultaneously)	**0 ***

7.27.2. Advanced Settings:

SDIO/SDMMC:

SDMMC instance	SDMMC1
Use dma template	Enabled
BSP code for SD	Generic

7.28. FREERTOS

Interface: CMSIS_V1

7.28.1. Config parameters:

API:

FreeRTOS API	CMSIS v1

Versions:

FreeRTOS version	10.2.1
CMSIS-RTOS version	1.02

MPU/FPU:

ENABLE_MPU	Disabled
ENABLE_FPU	Disabled

Kernel settings:

USE_PREEMPTION	Enabled
CPU_CLOCK_HZ	SystemCoreClock
TICK_RATE_HZ	1000
MAX_PRIORITIES	7
MINIMAL_STACK_SIZE	**1024 ***
MAX_TASK_NAME_LEN	16
USE_16_BIT_TICKS	Disabled
IDLE_SHOULD_YIELD	Enabled
USE_MUTEXES	Enabled
USE_RECURSIVE_MUTEXES	Disabled
USE_COUNTING_SEMAPHORES	Disabled
QUEUE_REGISTRY_SIZE	8
USE_APPLICATION_TASK_TAG	Disabled
ENABLE_BACKWARD_COMPATIBILITY	Enabled
USE_PORT_OPTIMISED_TASK_SELECTION	Enabled
USE_TICKLESS_IDLE	Disabled
USE_TASK_NOTIFICATIONS	Enabled
RECORD_STACK_HIGH_ADDRESS	Disabled

Memory management settings:

Memory Allocation	Dynamic / Static
TOTAL_HEAP_SIZE	**131072 ***
Memory Management scheme	heap_4

Hook function related definitions:

USE_IDLE_HOOK	Disabled
USE_TICK_HOOK	Disabled

USE_MALLOC_FAILED_HOOK	Disabled
USE_DAEMON_TASK_STARTUP_HOOK	Disabled
CHECK_FOR_STACK_OVERFLOW	Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS	Disabled
USE_TRACE_FACILITY	Disabled
USE_STATS_FORMATTING_FUNCTIONS	Disabled

Co-routine related definitions:

USE_CO_ROUTINES	Disabled
MAX_CO_ROUTINE_PRIORITIES	2

Software timer definitions:

USE_TIMERS	Disabled

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY	15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY	5

Added with 10.2.1 support:

MESSAGE_BUFFER_LENGTH_TYPE	size_t
USE_POSIX_ERRNO	Disabled

7.28.2. Include parameters:

Include definitions:

vTaskPrioritySet	Enabled
uxTaskPriorityGet	Enabled
vTaskDelete	Enabled
vTaskCleanUpResources	Disabled
vTaskSuspend	Enabled
vTaskDelayUntil	Disabled
vTaskDelay	Enabled
xTaskGetSchedulerState	Enabled
xTaskResumeFromISR	Enabled
xQueueGetMutexHolder	Disabled
xSemaphoreGetMutexHolder	Disabled
pcTaskGetTaskName	Disabled
uxTaskGetStackHighWaterMark	Disabled
xTaskGetCurrentTaskHandle	Disabled
eTaskGetState	Disabled
xEventGroupSetBitFromISR	Disabled
xTimerPendFunctionCall	Disabled
xTaskAbortDelay	Disabled
xTaskGetHandle	Disabled

uxTaskGetStackHighWaterMark2	Disabled

7.28.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT	Disabled

Project settings (see parameter description first):

Use FW pack heap file	Enabled

7.29. LIBJPEG

mode: Enabled

7.29.1. Config parameters:

Version:

LIBJPEG version	8d

MW configuration:

Data Stream management type	**None ***
FREERTOS	Enabled

General Settings:

Use FREERTOS Memory Allocator	Enabled

7.30. LWIP

mode: Enabled

Advanced parameters are not listed except if modified by user.

7.30.1. General Settings:

LwIP Version:

LwIP Version (Version of LwIP supported by CubeMX ** CubeMX specific **)	2.1.2

IPv4 - DHCP Options:

LWIP_DHCP (DHCP Module)	Enabled

RTOS Dependency:

WITH_RTOS (Use FREERTOS ** CubeMX specific **)	Enabled
CMSIS_VERSION (CMSIS API Version used)	CMSIS v1

Protocols Options:

LWIP_ICMP (ICMP Module Activation)	Enabled

LWIP_IGMP (IGMP Module)	Disabled
LWIP_DNS (DNS Module)	**Enabled ***
LWIP_UDP (UDP Module)	Enabled
MEMP_NUM_UDP_PCB (Number of UDP Connections)	4
LWIP_TCP (TCP Module)	Enabled
MEMP_NUM_TCP_PCB (Number of TCP Connections)	5

7.30.2. Key Options:

Infrastructure - OS Awarness Option:

NO_SYS (OS Awarness)	OS Used

Infrastructure - Timers Options:

LWIP_TIMERS (Use Support For sys_timeout)	Enabled

Infrastructure - Core Locking and MPU Options:

SYS_LIGHTWEIGHT_PROT (Memory Functions Protection)	Enabled

Infrastructure - Heap and Memory Pools Options:

MEM_SIZE (Heap Memory Size)	1600

Infrastructure - Internal Memory Pool Sizes:

MEMP_NUM_PBUF (Number of Memory Pool struct Pbufs)	16
MEMP_NUM_RAW_PCB (Number of Raw Protocol Control Blocks)	4
MEMP_NUM_TCP_PCB_LISTEN (Number of Listening TCP Connections)	8
MEMP_NUM_TCP_SEG (Number of TCP Segments simultaneously queued)	16
MEMP_NUM_LOCALHOSTLIST (Number of Host Entries in the Local Host List)	1

Pbuf Options:

PBUF_POOL_SIZE (Number of Buffers in the Pbuf Pool)	16
PBUF_POOL_BUFSIZE (Size of each pbuf in the pbuf pool)	592

IPv4 - ARP Options:

LWIP_ARP (ARP Functionality)	Enabled

Callback - TCP Options:

TCP_TTL (Number of Time-To-Live Used by TCP Packets)	255
TCP_WND (TCP Receive Window Maximum Size)	2144
TCP_QUEUE_OOSEQ (Allow Out-Of-Order Incoming Packets)	Enabled
LWIP_TCP_SACK_OUT (Allow Sending Selective Acknowledgements)	Disabled
TCP_MSS (Maximum Segment Size)	536
TCP_SND_BUF (TCP Sender Buffer Space)	1072
TCP_SND_QUEUELEN (Number of Packet Buffers Allowed for TCP Sender)	9

Network Interfaces Options:

LWIP_NETIF_STATUS_CALLBACK (Callback Function on Interface Status Changes)	**Enabled ***
LWIP_NETIF_EXT_STATUS_CALLBACK (Extended Callback Function for several netif)	Disabled
LWIP_NETIF_LINK_CALLBACK (Callback Function on Interface Link Changes)	**Enabled ***

NETIF - Loopback Interface Options:

LWIP_NETIF_LOOPBACK (NETIF Loopback)	Disabled

Infrastructure - Threading Options:

TCPIP_THREAD_NAME (TCPIP Thread Name)	"tcpip_thread"
TCPIP_THREAD_STACKSIZE (TCPIP Thread Stack Size)	1024
TCPIP_THREAD_PRIO (TCPIP Thread Priority Level)	3
TCPIP_MBOX_SIZE (TCPIP Mailbox Size)	6
DEFAULT_THREAD_NAME (Default LwIP Thread Name)	"lwIP"
DEFAULT_THREAD_STACKSIZE (Default LwIP Thread Stack Size)	1024
DEFAULT_THREAD_PRIO (Default LwIP Thread Priority Level)	3
DEFAULT_RAW_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN Raw)	0
DEFAULT_TCP_RECVMBOX_SIZE (Default Mailbox Size on a NETCONN TCP)	6
DEFAULT_ACCEPTMBOX_SIZE (Default Mailbox Size for Incoming Connections)	6

Thread Safe APIs - Netconn Options:

LWIP_NETCONN (NETCONN API)	Enabled

Thread Safe APIs - Socket Options:

LWIP_SOCKET (Socket API)	Enabled
LWIP_COMPAT_SOCKETS (BSD-style Socket Functions Names)	1
LWIP_SOCKET_OFFSET (Socket Offset Number)	0
LWIP_SOCKET_SELECT (Select for Socket)	Enabled
LWIP_SOCKET_POLL (Poll for Socket)	Enabled

7.30.3. PPP:

PPP Options:

PPP_SUPPORT (PPP Module)	Disabled

7.30.4. IPv6:

IPv6 Options:

LWIP_IPV6 (IPv6 Protocol)	Disabled

7.30.5. HTTPD:

HTTPD Options:

LWIP_HTTPD (LwIP HTTPD Support ** CubeMX specific **)	Disabled

7.30.6. SNMP:

SNMP Options:

LWIP_SNMP (LwIP SNMP Agent)	Disabled

7.30.7. SNTP/SMTP:

SNTP Options:

LWIP_SNTP (LWIP SNTP Support ** CubeMX specific **)	**Enabled ***

SMTP Options:

LWIP_SMTP (LWIP SMTP Support ** CubeMX specific **)	Disabled

7.30.8. MDNS/TFTP:

MDNS Options:

LWIP_MDNS (Multicast DNS Support ** CubeMX specific **)	Disabled

TFTP Options:

LWIP_TFTP (TFTP Support ** CubeMX specific **)	Disabled

7.30.9. Perf/Checks:

Sanity Checks:

LWIP_DISABLE_TCP_SANITY_CHECKS (TCP Sanity Checks)	Disabled
LWIP_DISABLE_MEMP_SANITY_CHECKS (MEMP Sanity Checks)	Disabled

Performance Options:

LWIP_PERF (Performace Testing for LwIP)	Disabled

7.30.10. Statistics:

Debug - Statistics Options:

LWIP_STATS (Statictics Collection)	Disabled

7.30.11. Checksum:

Infrastructure - Checksum Options:

CHECKSUM_BY_HARDWARE (Hardware Checksum ** CubeMX specific **)	Disabled
LWIP_CHECKSUM_CTRL_PER_NETIF (Generate/Check Checksum per Netif)	Disabled
CHECKSUM_GEN_IP (Generate Software Checksum for Outgoing IP Packets)	Disabled
CHECKSUM_GEN_UDP (Generate Software Checksum for Outgoing UDP Packets)	Disabled

CHECKSUM_GEN_TCP (Generate Software Checksum for Outgoing TCP Packets)	Disabled
CHECKSUM_GEN_ICMP (Generate Software Checksum for Outgoing ICMP Packets)	Disabled
CHECKSUM_GEN_ICMP6 (Generate Software Checksum for Outgoing ICMP6 Packets)	Disabled
CHECKSUM_CHECK_IP (Generate Software Checksum for Incoming IP Packets)	Disabled
CHECKSUM_CHECK_UDP (Generate Software Checksum for Incoming UDP Packets)	Disabled
CHECKSUM_CHECK_TCP (Generate Software Checksum for Incoming TCP Packets)	Disabled
CHECKSUM_CHECK_ICMP (Generate Software Checksum for Incoming ICMP Packets)	Disabled
CHECKSUM_CHECK_ICMP6 (Generate Software Checksum for Incoming ICMP6 Packets)	Disabled

7.30.12. Debug:

LwIP Main Debugging Options:

LWIP_DBG_MIN_LEVEL (Minimum Level)	All

7.31. USB_DEVICE

Class For FS IP: Communication Device Class (Virtual Port Com)

7.31.1. Parameter Settings:

Basic Parameters:

USBD_MAX_NUM_INTERFACES (Maximum number of supported interfaces)	1
USBD_MAX_NUM_CONFIGURATION (Maximum number of supported configuration)	1
USBD_MAX_STR_DESC_SIZ (Maximum size for the string descriptors)	512
USBD_SELF_POWERED (Enabled self power)	Enabled
USBD_DEBUG_LEVEL (USBD Debug Level)	0: No debug message
USBD_LPM_ENABLED (Link Power Management)	1: Link Power Management supported

Class Parameters:

USB CDC Rx Buffer Size	2048
USB CDC Tx Buffer Size	2048

7.31.2. Device Descriptor:

Device Descriptor:

VID (Vendor IDentifier)	**4617 ***
LANGID_STRING (Language Identifier)	English(United States)
MANUFACTURER_STRING (Manufacturer Identifier)	**EEZ ***

Device Descriptor FS:

PID (Product IDentifier)	**8216 ***
PRODUCT_STRING (Product Identifier)	**MCU Virtual ComPort ***

CONFIGURATION_STRING (Configuration Identifier)	CDC Config
INTERFACE_STRING (Interface Identifier)	CDC Interface

*** User modified value**

8. System Configuration

8.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
DAC	PA4	DAC_OUT1	Analog mode	No pull-up and no pull-down	n/a	
ETH	PC1	ETH_MDC	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC2	ETH_TXD2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC3	ETH_TX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA0/WKUP	ETH_CRS	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA1	ETH_RX_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA2	ETH_MDIO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA3	ETH_COL	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PA7	ETH_RX_DV	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC4	ETH_RXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PC5	ETH_RXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB10	ETH_RX_ER	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB11	ETH_TX_EN	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PH6	ETH_RXD2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PH7	ETH_RXD3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB12	ETH_TXD0	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	
	PB13	ETH_TXD1	Alternate Function Push Pull	No pull-up and no pull-down	**Very High** *	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PB8	ETH_TXD3	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
FMC	PF0	FMC_A0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF1	FMC_A1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF2	FMC_A2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF3	FMC_A3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF4	FMC_A4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF5	FMC_A5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH2	FMC_SDCKE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH3	FMC_SDNE0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PH5	FMC_SDNWE	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF11	FMC_SDNRAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF12	FMC_A6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF13	FMC_A7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF14	FMC_A8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PF15	FMC_A9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG0	FMC_A10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG1	FMC_A11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE7	FMC_D4	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE8	FMC_D5	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE9	FMC_D6	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE10	FMC_D7	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE11	FMC_D8	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE12	FMC_D9	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE13	FMC_D10	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE14	FMC_D11	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE15	FMC_D12	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD8	FMC_D13	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD9	FMC_D14	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD10	FMC_D15	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD14	FMC_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD15	FMC_D1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG4	FMC_BA0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG5	FMC_BA1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG8	FMC_SDCLK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD0	FMC_D2	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD1	FMC_D3	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PG15	FMC_SDNCAS	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE0	FMC_NBL0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PE1	FMC_NBL1	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	Pull-up	**Very High ***	
	PB7	I2C1_SDA	Alternate Function Open Drain	Pull-up	**Very High ***	
LTDC	PI9	LTDC_VSYNC	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PI10	LTDC_HSYNC	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PI11	LTDC_G6	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PF10	LTDC_DE	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PC0	LTDC_R5	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PH4	LTDC_G4	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA5	LTDC_R4	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PA6	LTDC_G2	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB0	LTDC_R3	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PB1	LTDC_R6	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PG6	LTDC_R7	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PG7	LTDC_CLK	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PI0	LTDC_G5	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PD3	LTDC_G7	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PG10	LTDC_G3	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PG11	LTDC_B3	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PG12	LTDC_B4	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PI5	LTDC_B5	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PI6	LTDC_B6	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
	PI7	LTDC_B7	Alternate Function Push Pull	No pull-up and no pull-down	**High ***	
RCC	PC14/OSC32_IN	RCC_OSC32_IN	n/a	n/a	n/a	
	PC15/OSC32_OUT	RCC_OSC32_OUT	n/a	n/a	n/a	
	PH0/OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	
	PH1/OSC_OUT	RCC_OSC_OUT	n/a	n/a	n/a	
	PC9	RCC_MCO_2	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	MCLK_25
SDMMC1	PC8	SDMMC1_D0	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PC12	SDMMC1_CK	Alternate Function Push Pull	No pull-up and no pull-down	Very High	
	PD2	SDMMC1_CMD	Alternate Function Push Pull	No pull-up and no pull-down	Very High	

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
SPI2	PB14	SPI2_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PI1	SPI2_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PI3	SPI2_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI4	PE2	SPI4_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE5	SPI4_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PE6	SPI4_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SPI5	PF7	SPI5_SCK	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF8	SPI5_MISO	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PF9	SPI5_MOSI	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
SYS	PA13	SYS_JTMS-SWDIO	n/a	n/a	n/a	
	PA14	SYS_JTCK-SWCLK	n/a	n/a	n/a	
	PB3	SYS_JTDO-SWO	n/a	n/a	n/a	
TIM3	PB5	TIM3_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	DOUT2
TIM12	PB15	TIM12_CH2	Alternate Function Push Pull	No pull-up and no pull-down	Low	TFT_BRIGHTNESS
UART7	PF6	UART7_RX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	UART_RX/DIN1
	PB4	UART7_TX	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	UART_TX/DOUT1
USB_OTG_FS	PA9	USB_OTG_FS_VBUS	Input mode	No pull-up and no pull-down	n/a	
	PA11	USB_OTG_FS_DM	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
	PA12	USB_OTG_FS_DP	Alternate Function Push Pull	No pull-up and no pull-down	**Very High ***	
GPIO	PE3	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SPI4_CSA
	PE4	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SPI4_CSB

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
	PC13	GPIO_Input	Input mode	No pull-up and no pull-down	**n/a**	DIN2
	PB2	GPIO_Input	Input mode	**Pull-up ***	**n/a**	NFAULT
	PD11	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SPI2_CSB
	PD12	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SPI2_CSA
	PD13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	OE_SYNC
	PG2	GPIO_Output	Output Push Pull	**Pull-down ***	Low	PWR_DIRECT
	PG3	GPIO_Output	Output Push Pull	**Pull-down ***	Low	PWR_SSTART
	PC6	GPIO_EXTI6	**External Interrupt Mode with Rising/Falling edge**	No pull-up and no pull-down	n/a	ENC_A
	PC7	GPIO_EXTI7	**External Interrupt Mode with Rising/Falling edge**	No pull-up and no pull-down	n/a	ENC_B
	PA8	GPIO_EXTI8	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	n/a	SPI2_IRQ
	PA15	GPIO_EXTI15	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	n/a	SPI5_IRQ
	PC11	GPIO_EXTI11	**External Interrupt Mode with Falling edge trigger detection**	**Pull-up ***	n/a	SD_DETECT
	PD4	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	USB_OTG_FS_OC
	PD5	GPIO_Output	Output Push Pull	No pull-up and no pull-down	Low	USB_OTG_FS_PSO
	PD7	GPIO_Input	Input mode	No pull-up and no pull-down	n/a	IRQ_TOUCH
	PG9	GPIO_Input	Input mode	**Pull-up ***	n/a	USER_SW
	PG13	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SPI5_CSB
	PG14	GPIO_Output	Output Push Pull	No pull-up and no pull-down	**High ***	SPI5_CSA
	PB9	GPIO_EXTI9	External Interrupt Mode with Rising edge trigger detection	**Pull-up ***	**n/a**	SPI4_IRQ
	PI4	GPIO_Input	Input mode	**Pull-up ***	**n/a**	ENC_SW

8.2. DMA configuration

DMA request	Stream	Direction	Priority
DAC1	DMA1_Stream5	Memory To Peripheral	Low
SDMMC1_RX	DMA2_Stream3	Peripheral To Memory	Low
SDMMC1_TX	DMA2_Stream6	Memory To Peripheral	Low

DAC1: DMA1_Stream5 DMA request Settings:

Mode:	Normal
Use fifo:	Disable
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Byte ***
Memory Data Width:	**Byte ***

SDMMC1_RX: DMA2_Stream3 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	**4 Increment ***
Memory Burst Size:	4 Increment

SDMMC1_TX: DMA2_Stream6 DMA request Settings:

Mode:	**Peripheral Flow Control ***
Use fifo:	**Enable ***
FIFO Threshold:	Full
Peripheral Increment:	Disable
Memory Increment:	**Enable ***
Peripheral Data Width:	**Word ***
Memory Data Width:	Word
Peripheral Burst Size:	

	4 Increment *
Memory Burst Size:	4 Increment

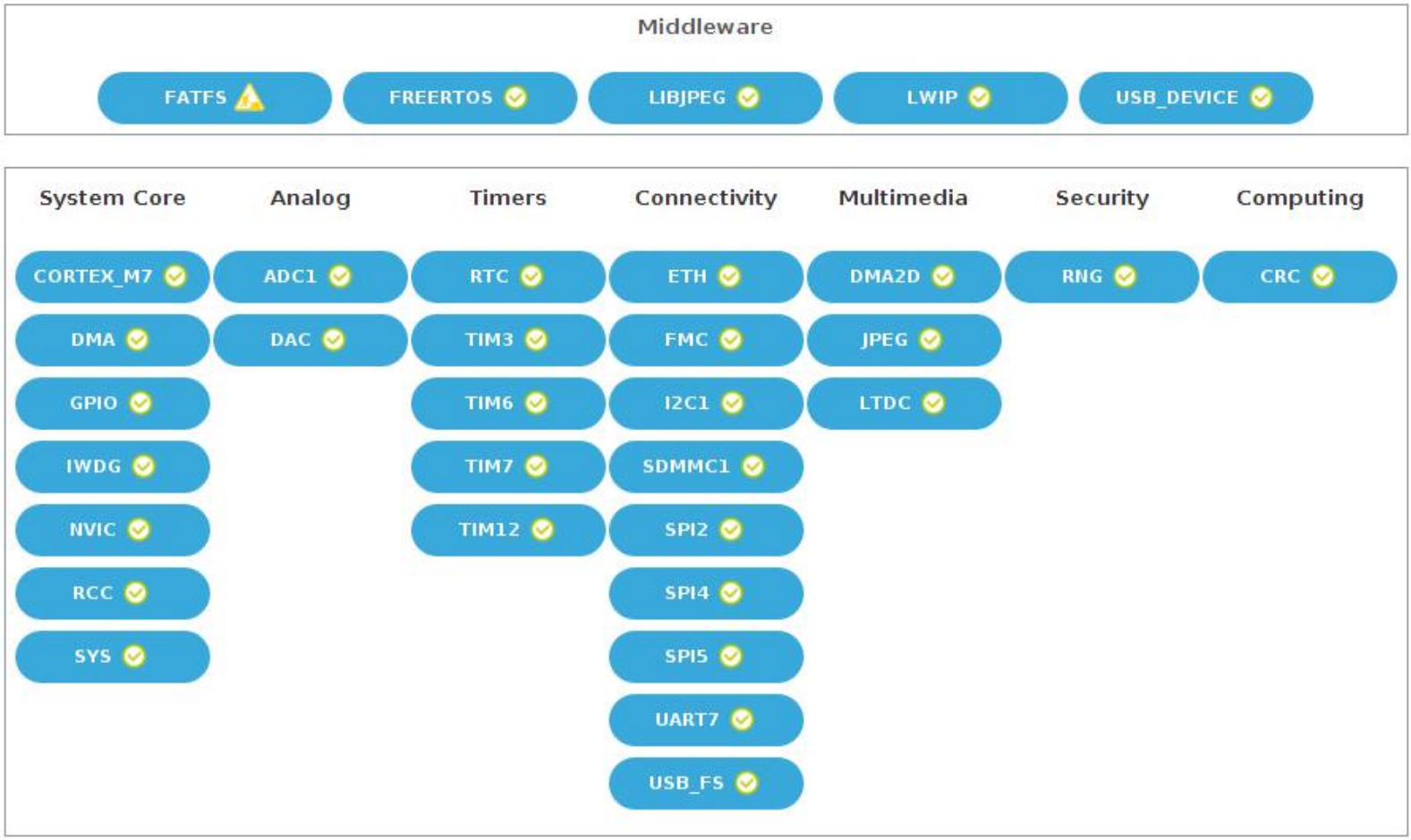
8.3. NVIC configuration

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
DMA1 stream5 global interrupt	true	5	0
ADC1, ADC2 and ADC3 global interrupts	true	5	0
EXTI line[9:5] interrupts	true	5	0
TIM1 update interrupt and TIM10 global interrupt	true	0	0
EXTI line[15:10] interrupts	true	5	0
SDMMC1 global interrupt	true	5	0
TIM7 global interrupt	true	5	0
DMA2 stream3 global interrupt	true	5	0
Ethernet global interrupt	true	5	0
USB On The Go FS global interrupt	true	5	0
DMA2 stream6 global interrupt	true	5	0
UART7 global interrupt	true	5	0
PVD interrupt through EXTI line 16	unused		
Flash global interrupt	unused		
RCC global interrupt	unused		
TIM3 global interrupt	unused		
I2C1 event interrupt	unused		
I2C1 error interrupt	unused		
SPI2 global interrupt	unused		
TIM8 break interrupt and TIM12 global interrupt	unused		
FMC global interrupt	unused		
TIM6 global interrupt, DAC1 and DAC2 underrun error interrupts	unused		
Ethernet wake-up interrupt through EXTI line 19	unused		
HASH and RNG global interrupts	unused		
FPU global interrupt	unused		
SPI4 global interrupt	unused		
SPI5 global interrupt	unused		
LTDC global interrupt	unused		

Interrupt Table	Enable	Preenmption Priority	SubPriority
LTDC global error interrupt	unused		
DMA2D global interrupt	unused		
JPEG global interrupt	unused		

*** User modified value**

9. Predefined Views - Category view : Current



10. Software Pack Report

10.1. Software Pack selected

Vendor	Name	Version	Component
STMicroelectronics	FreeRTOS	0.0.1	Class : CMSIS Group : RTOS SubGroup : FreeRTOS Version : 10.2.0 Class : RTOS Group : Core Version : 10.2.0