

PE 1	O	O	2 PE
+12V 3	O	O	4 +12V
+5V 5	O	O	6 +5V
Gnd 7	O	O	8 Gnd
Gnd 9	O	O	10 +VAUX
PWR_SSTART 11	O	O	12 PWR_DIRECT
SSCL 13	O	O	14 SSDA
FAULT 15	O	O	16 +3V3

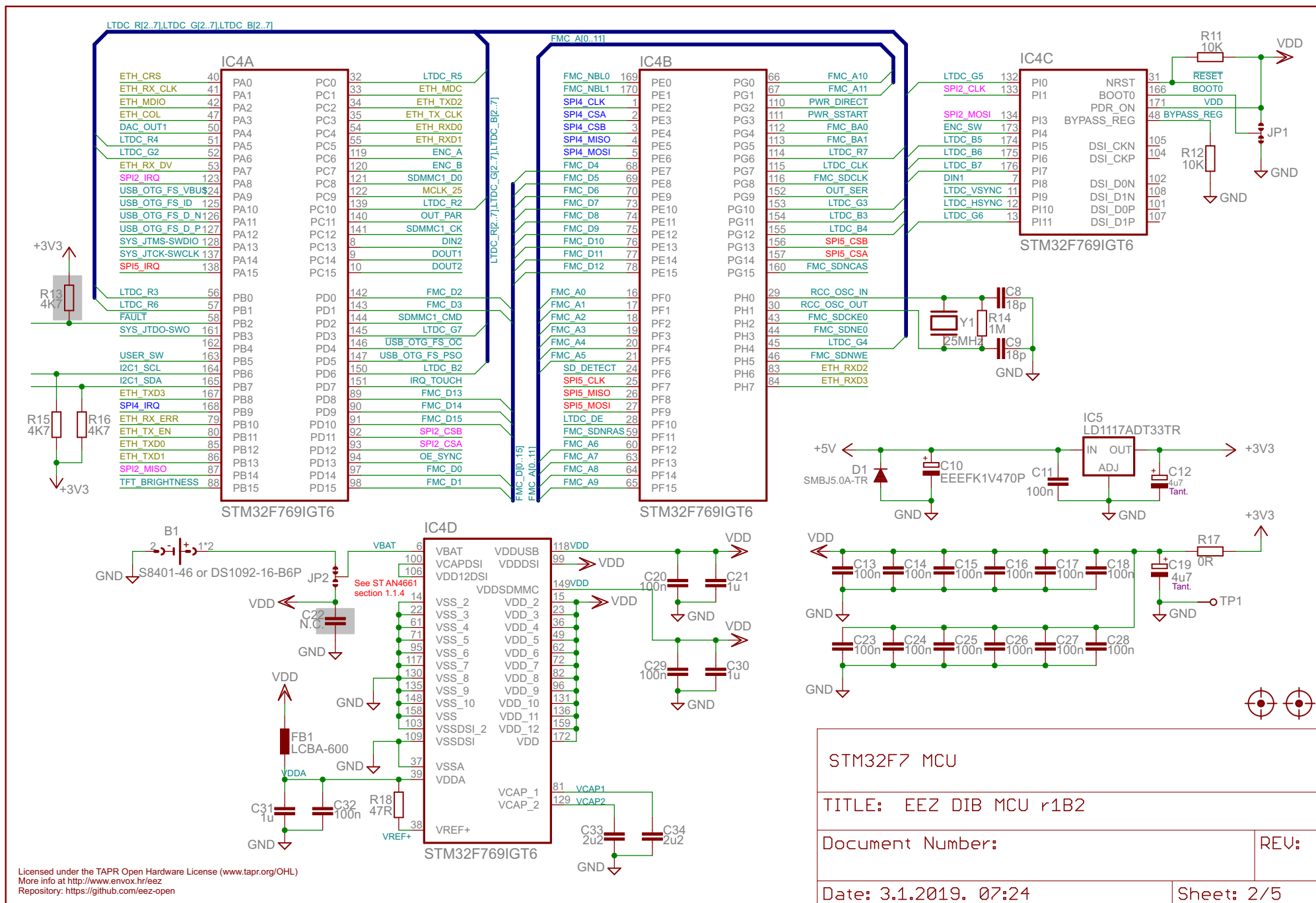
Pin connection diagram for the ZL263-40DG component. The diagram shows two columns of pins, X1-1 to X1-39 on the left and X1-2 to X1-40 on the right. Various signals are connected to these pins, including OUT_SER, +VAUX, SPI5_IRQ, SPI5_CSA, SPI5_CSB, SPI5_CLK, SPI4_IRQ, SPI4_CSB, SPI4_CLK, SPI2_IRQ, SPI2_CSB, SPI2_MISO, SPI2_MOSI, OUT_PAR, RESET, FAULT, OE_SYNC, I2C1_SCL, I2C1_SDA, SPI5_MISO, SPI5_MOSI, SPI4_CSA, SPI4_MISO, SPI4_MOSI, SPI2_CSA, and SPI2_CLK. Power connections are shown for +3V3, +5V, +12V, and GND.

Gnd 1	○	○	2 Gnd
OUT_SER 3	○	○	4 OUT_PAR
+Vaux 5	○	○	6 NRESET
+3V3 7	○	○	8 NFAULT
CH3_IRQ 9	○	○	10 OE_SYNC
CH3_CSA 11	○	○	12 I2C_SCL
CH3_CSB 13	○	○	14 I2C_SDA
Gnd 15	○	○	16 Gnd
CH3_SCLK 17	○	○	18 CH3_MISO
CH2_IRQ 19	○	○	20 CH3_MOSI
CH2_CSB 21	○	○	22 CH2_CSA
CH2_SCLK 23	○	○	24 CH2_MISO
CH1_IRQ 25	○	○	26 CH2_MOSI
CH1_CSB 27	○	○	28 CH1_CSA
Gnd 29	○	○	30 Gnd
CH1_MISO 31	○	○	32 CH1_SCLK
CH1_MOSI 33	○	○	34 Gnd
+5V 35	○	○	36 +5V
+12V 37	○	○	38 +12V
Gnd 39	○	○	40 Gnd

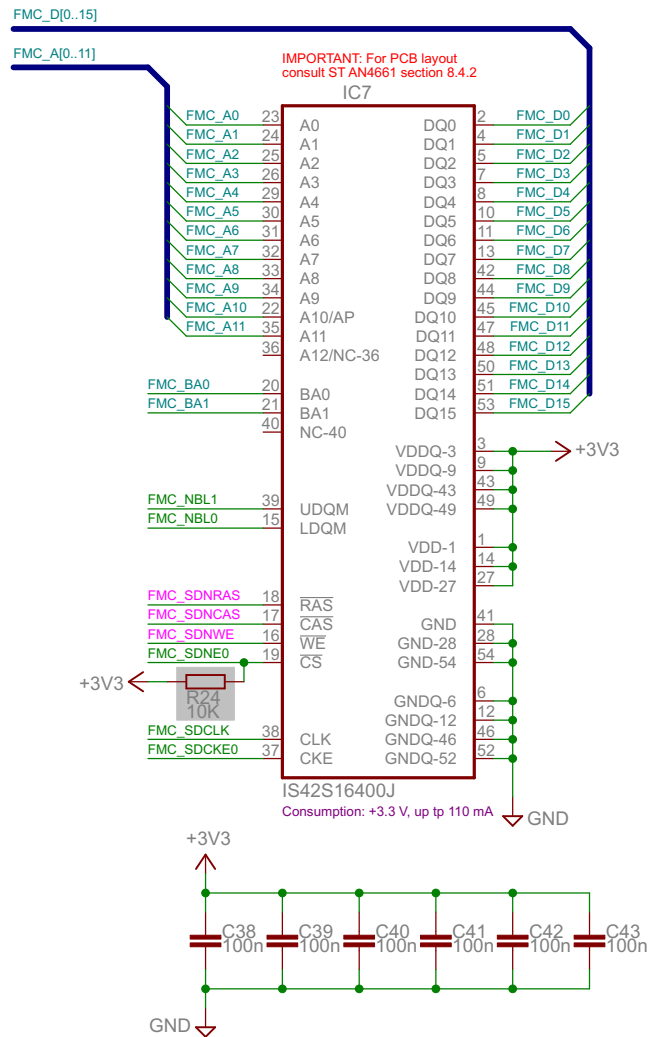
The diagram illustrates a digital I/O interface circuit with various protection features. It includes a TPD4E001DRLR (IC1) for input protection, two SN74LVC2G34DBVR (IC2A, IC2B) inverters, and a BTS3408G (IC3) for output protection. The circuit is powered by +5V and +3V3 rails. Key components include resistors (R2, R3, R4, R6, R7, R8), capacitors (C1, C4, C7), fuses (F1, F2), and diodes (ZD1, ZD2). The input lines are X3-1 to X3-5, and the output lines are DOUT1, DOUT2, FAULT, and RESET.

[illegible]

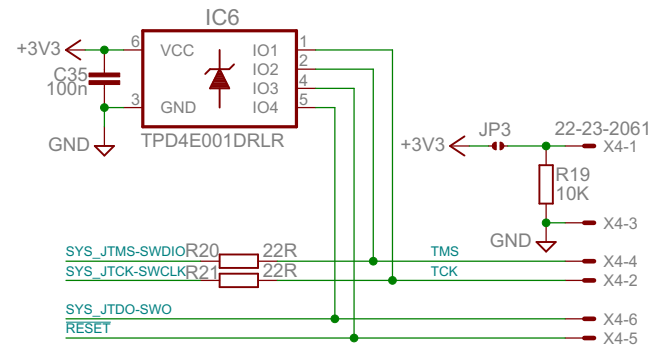
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SDRAM



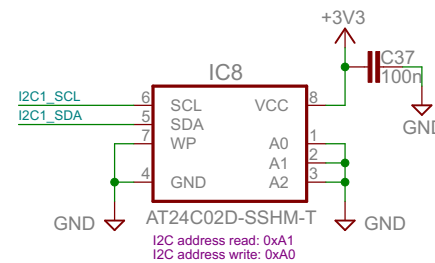
JTAG (SWD)



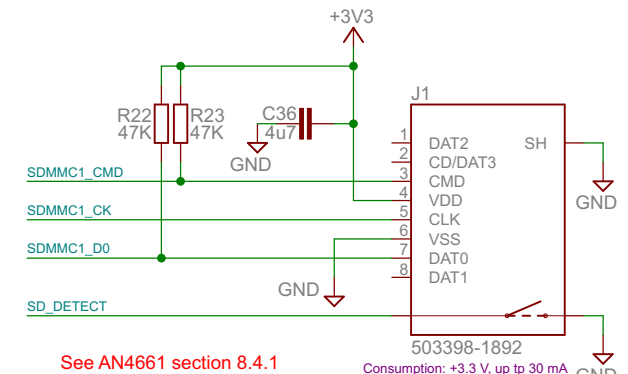
STM-32 board SWD header



I2C EEPROM



Micro SD card socket



SDRAM, JTAG, I2C EEPROM, SD Card

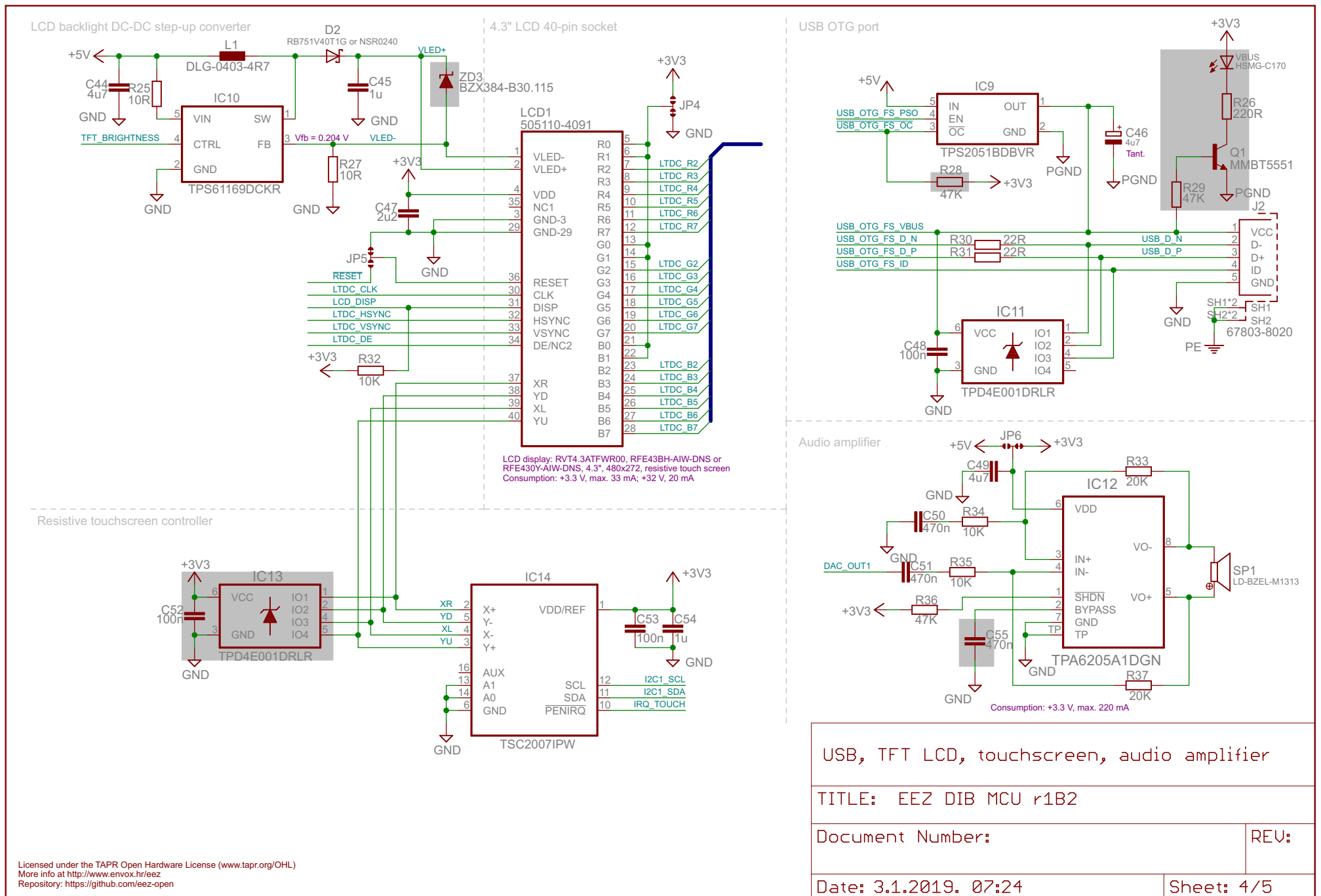
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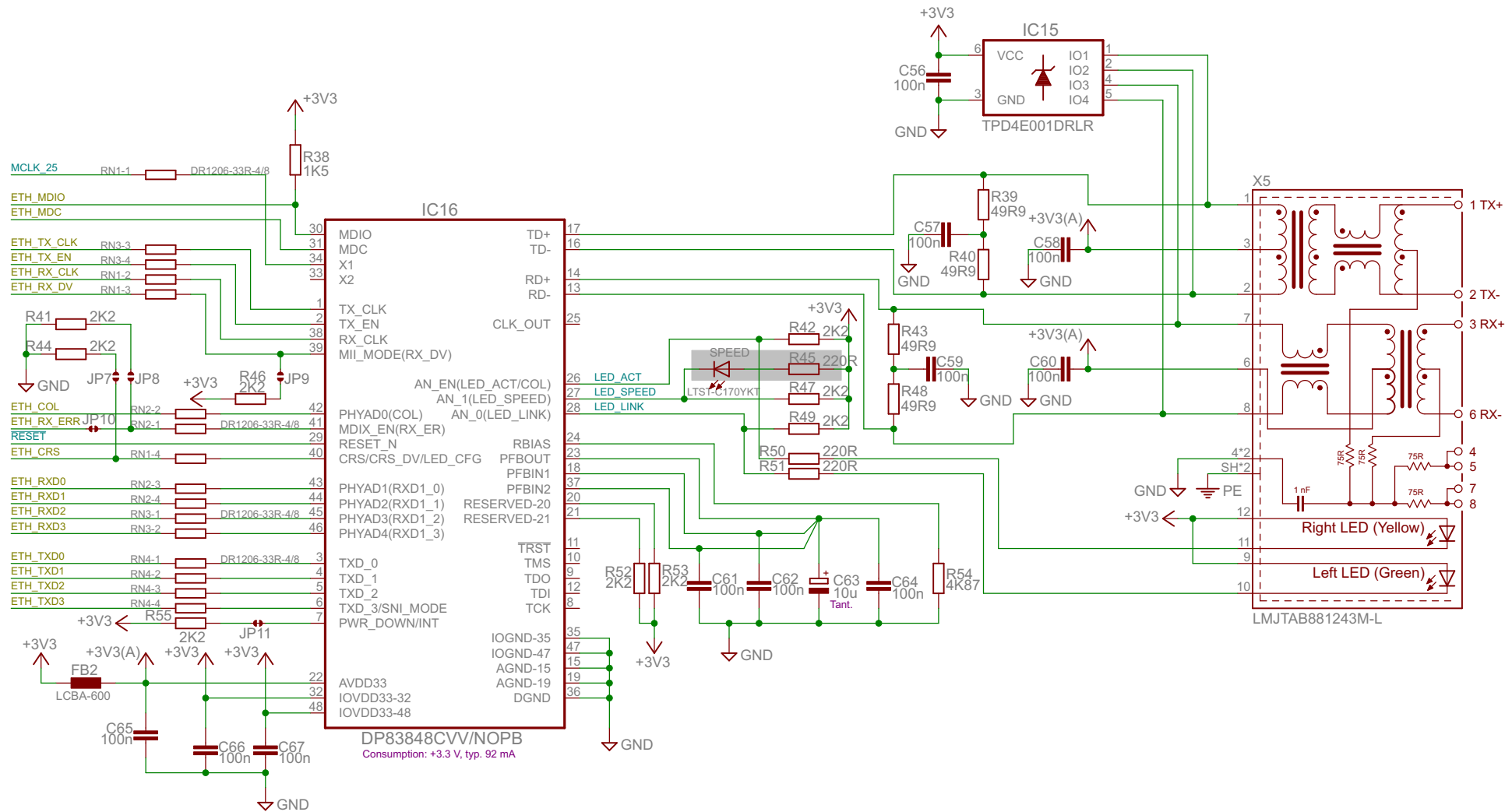
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