	MCU module (2 x 20-pin)						Status: Mandatory
	Α	Dir			В	Dir	_
1	GND			2	GND		
3	UART_RX	ı	Shared UART RX	4	UART_TX	0	Shared UART TX
5	+VAUX	I/O	• •	6	NRESET	0	Master reset (active low)
7	+3V3	0	DC power	8	NFAULT	I	Fault (active low)
9	CH3_IRQ	- 1	#3 IRQ	10	SYNC	0	Sync output
11	CH3_CSA	0	#3 Chip select A	12	SSCL	0	Shared I ² C SCL
13	CH3_CSB	0	#3 Chip select B	14	SSDA	I/O	Shared I ² C SDA
15	GND		-	16	GND		
17	CH3 SCLK	0	#3 SPI CLK	18	CH3 MISO	ı	#3 MISO
19	CH2_IRQ	ı	#2 IRQ	20	CH3 MOSI	0	#3 MOSI
21	CH2 CSB	0	#2 Chip select B	22	CH2 CSA	0	#2 Chip select A
23	CH2_SCLK	0	#2 SPI CLK	24	CH2 MISO	ı	#2 MISO
25	CH1 IRQ	ı	#1 IRQ	26	CH2 MOSI	0	#2 MOSI
27	CH1_CSB	0	#1 Chip select B	28	CH1 CSA	0	#1 Chip select A
29	GND			30	GND		- I
31	CH1_MISO	1	#1 MISO	32	CH1 SCLK	0	#1 SPI CLK
33	CH1_MOSI	0	#1 MOSI	34	GND	Ŭ	
35	+5V	Ī	DC power	36	+5V	1	DC power
37	+12V	i	DC power	38	+12V	i	DC power
39	GND		20 power	40	GND		20 power
33	SILD			-7-0			
	Peripheral modules (2 x 14-pin) Status: Mandatory						
	Α	Dir			В	Dir	
1	+3V3	ı	DC power	2	+VAUX	ı	Backup DC power
3	NFAULT	I/O	Fault (active low)	4	NRESET	I	Master reset (active low)
5	SSCL	- 1	Shared I ² C SCL	6	SYNC	- 1	Sync input
7	GND			8	SSDA	I/O	Shared I ² C SDA
9	CSA	ı	Module Chip select A	10	IRQ	0	Module IRQ
11	GND		·	12	CSB	ı	Module Chip select B
13	SCLK	ı	Module SPI CLK	14	MISO	0	Module MISO
15	MOSI	ı	Module MOSI	16	GND		
17	A0	ı	I ² C Address 0	18	A2	1	I ² C Address 2
19	A1	i	I ² C Address 1	20	GND		
21	+12V	i	DC power	22	+12V	1	DC power
23	+5V	i	DC power	24	+5V	i	DC power
25	GND		DO porto:	26	BOOT	i	Module bootloader select
	CIVE				БООТ		Status: Optional*
27	UART TX	0	Shared UART TX	28	UART RX	-	Shared UART RX
	<u> </u>				9 7 1. <u>_</u> . 1. 7.		
AUX PS module (2 x 8-pin) Status: Recommended							
	Α	Dir			В	Dir	
1	PE			2	MBOOT	0	Master bootloader select
3	+12V	0	DC power	4	+12V	0	DC power
5	+5V	0	DC power	6	+5V	0	DC power
7	GND			8	GND		
9	GND			10	+VAUX	I/O	Backup DC power
11	PWR_SSTART	I	AC soft-start	12	PWR_DIRECT	I	AC power on
13	SSCL	I	Shared I ² C SCL	14	SSDA	I/O	Shared I ² C SDA
15	NFAULT	I/O	Fault (active low)	16	+3V3	I	DC power
D							
	A	Dir	wer source module (2 :	х тО-	pin) B	Dir	Status: Optional
1	IN+	ااط	Power positive input	2	IN+	اات	Power positive input
3	IN+	i	Power positive input	4	IN+	i	Power positive input
5	IN+	i	Power positive input	6	OUT+	0	Power positive output
7	OUT+	0	Power positive input Power positive output	8	OUT+	0	Power positive output
9	OUT+	0	Power positive output Power positive output	10	OUT+	0	Power positive output Power positive output
11	OUT-	0	Power negative output	12	OUT-	0	Power negative output
13	OUT-	0	Power negative output	14	OUT-	0	Power negative output Power negative output
15 15	OUT-	0	Power negative output	16	IN-	l	Power negative output Power negative input
15 17	IN-	li	Power negative input	18	IN-	H	Power negative input
17 19	IN-		Power negative input	20	IN-		Power negative input
TA	II.A.	' '	i owei negative input	20	IIV-	' '	i owei negative tilput

^{*)} The first 26-pin of peripheral module connector is mandatory and last two pin are optional. New versions of DIB specification could introduce even more features but that will require also introduction of larger MCU connector or additional connector for the MCU