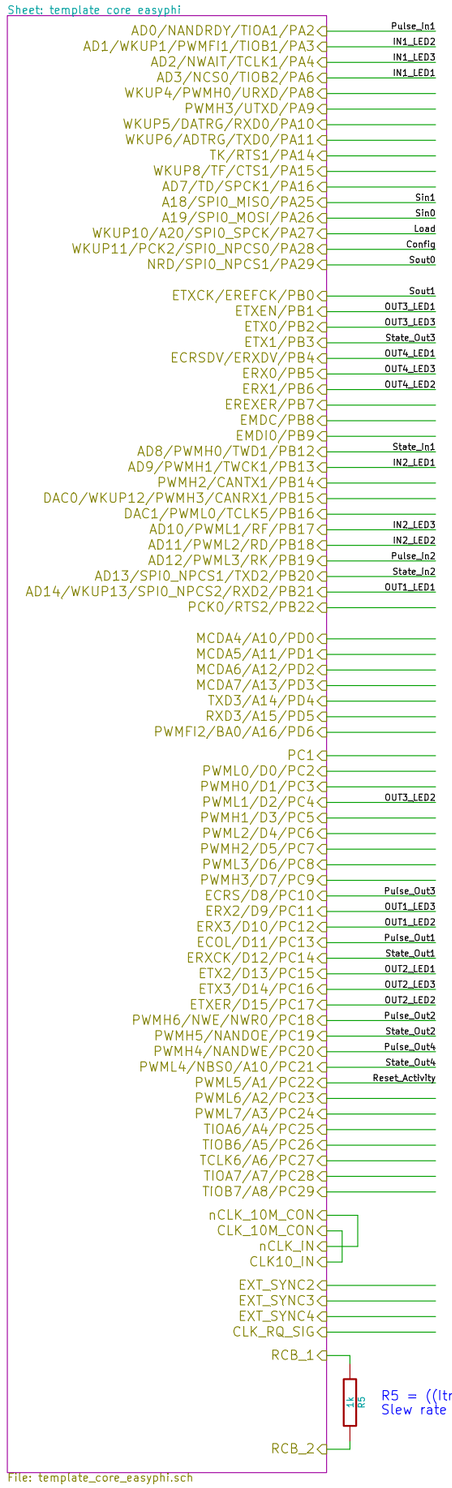

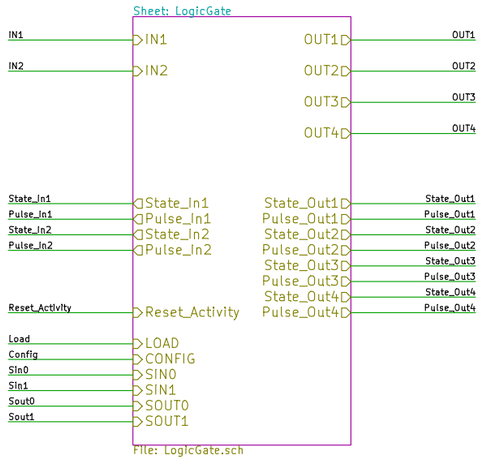

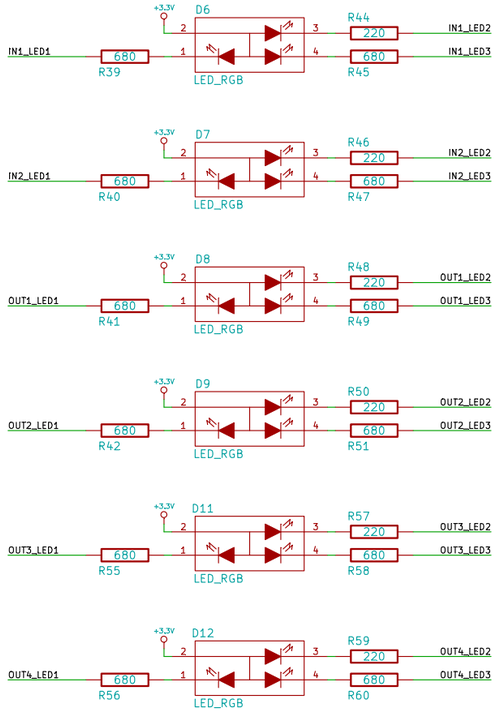

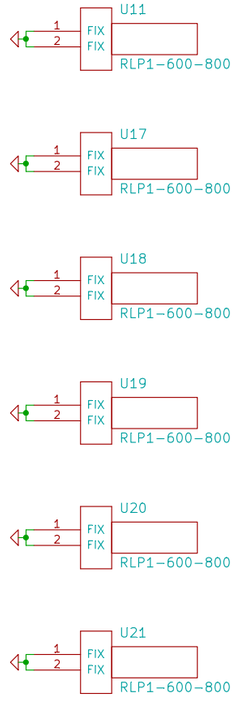

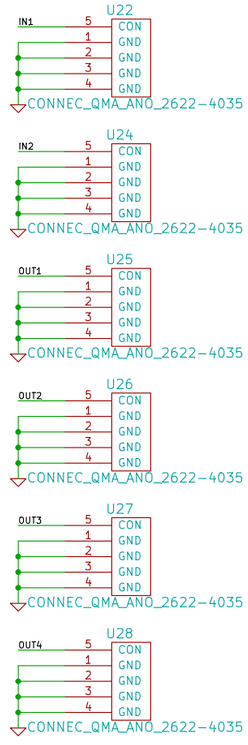

ABOUT THE POWER SUPPLY SYMBOLS	
+12V	is the 12V filtered coming from the backplane (MAX 4A) set R5 according to the max current you'll have
+5V	is the 5V filtered coming from the backplane (MAX 0.5A)
+3.3V	is a 3.3V generated from this 5V by a stepdown used by template_core chips
+3.3VADC	is a 3.3V generated from the 5V by a LDO used by the uC ADC

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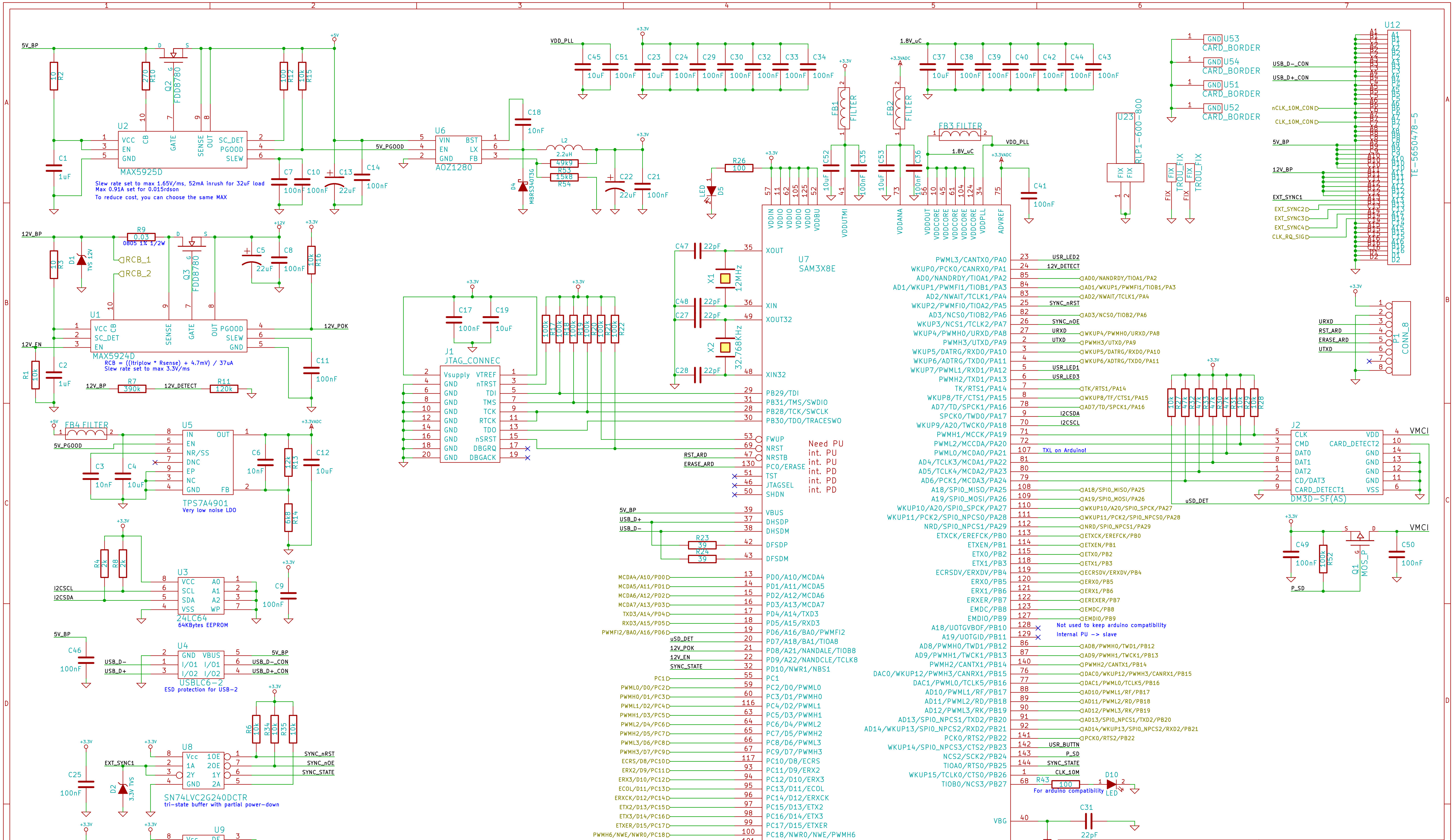
File: top_level_easyphi.sch	
Sheet: /	
Title: High-speed Logic Gate	
Size: A3	Date: 6 dec 2013 — **Rev: 1.0**
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable	Id: 1/9



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File: template_core_easyphi.sch

Sheet: /template core easyphi/

Title: High-speed Logic Gate

Size: A3 — Date: 6 dec 2013 — **Rev: 1.0**

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Input 1

IN1

U29
SY89854U

U13
LM7321MF

U31
MC100LVEP05DTG
AND

U32
MC100LVEP05DTG
OR

Sheet: ActivityDetector_In1
File: ActivityDetector.sch

U34
SY89540U

Sheet: ActivityDetector_Out1
File: ActivityDetector.sch
U35
SY89850U

Sheet: ActivityDetector_Out2
File: ActivityDetector.sch
U36
SY89850U

Sheet: ActivityDetector_Out3
File: ActivityDetector.sch
U37
SY89850U

Sheet: ActivityDetector_Out4
File: ActivityDetector.sch
U38
SY89850U

Input 2

IN2

U30
SY89854U

U14
LM7321MF

Sheet: ActivityDetector_In2
File: ActivityDetector.sch

U33
A0Z1280

FB5
FILTER_ELKE333FA

RP1
RP2
R_PACK8

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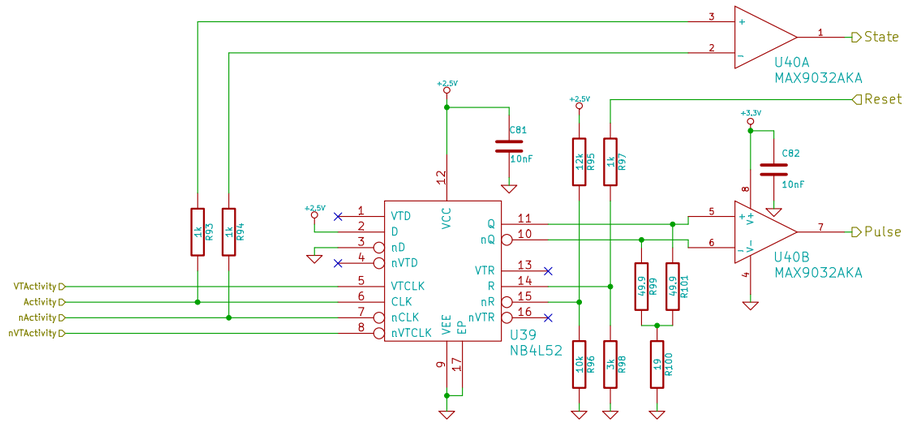
File: LogicGate.sch		
Sheet: /LogicGate/		
Title: High-speed Logic Gate		
Size: A3	Date: 6 dec 2013	**Rev: 1.0**
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable		Id: 3/9



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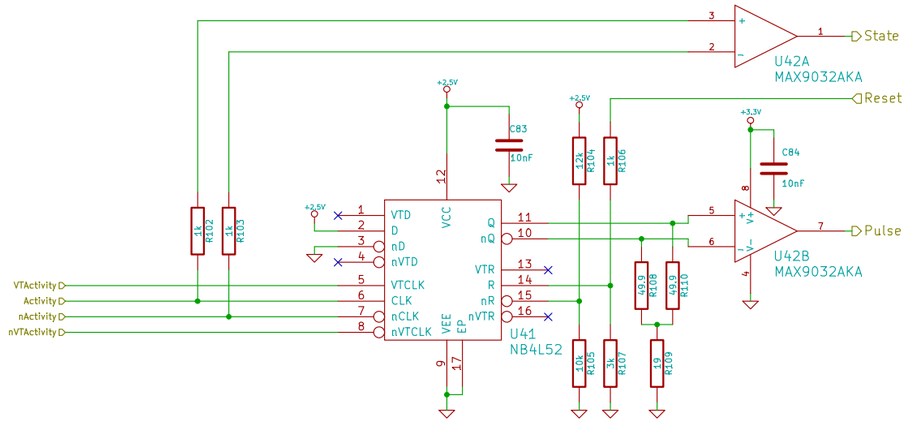
File: ActivityDetector.sch

Sheet: /LogicGate/ActivityDetector_In1/

Title: High-speed Logic Gate

Size: A3	Date: 6 dec 2013	**Rev: 1.0**
KiCad E.D.A.	eeschema (2013-07-07 BZR 4022)-stable	Id: 4/9



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File: ActivityDetector.sch

Sheet: /LogicGate/ActivityDetector_Out4/

Title: High-speed Logic Gate

Size: A3	Date: 6 dec 2013	**Rev: 1.0**
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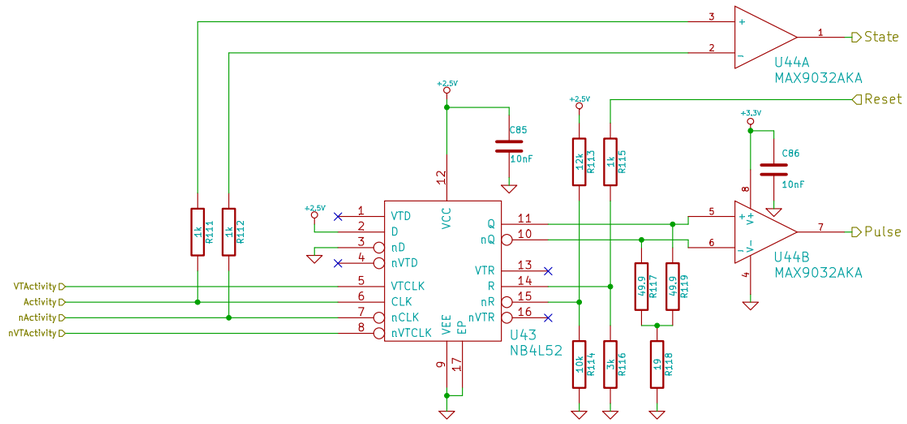

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File: ActivityDetector.sch

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Title: High-speed Logic Gate

Size: A3	Date: 6 dec 2013	**Rev: 1.0**
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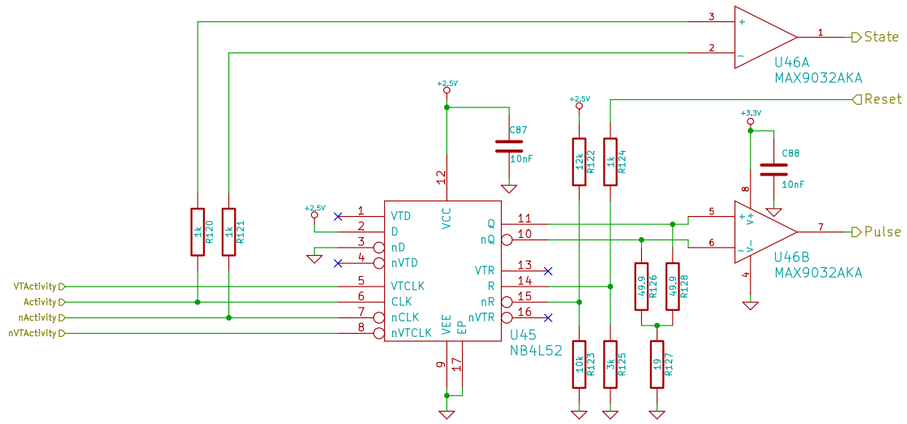

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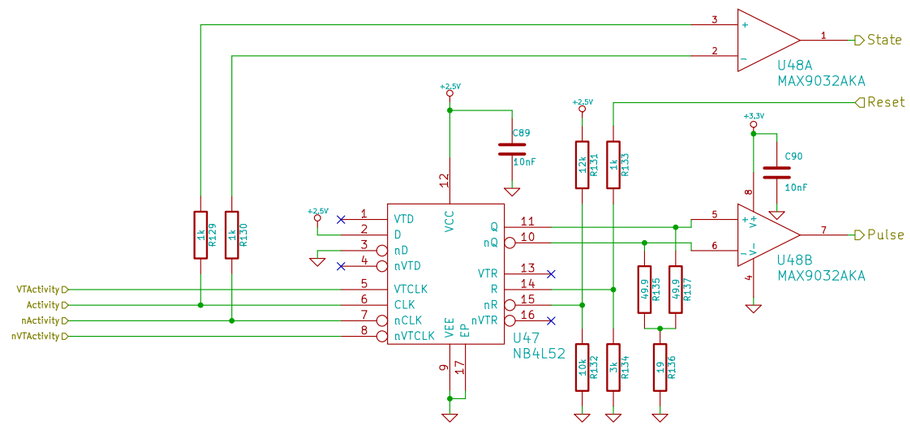
File: ActivityDetector.sch

Sheet: /LogicGate/ActivityDetector_Out2/

Title: High-speed Logic Gate

Size: A3	Date: 6 dec 2013	**Rev: 1.0**
KiCad E.D.A.	eeschema (2013-07-07 BZR 4022)-stable	Id: 7/9



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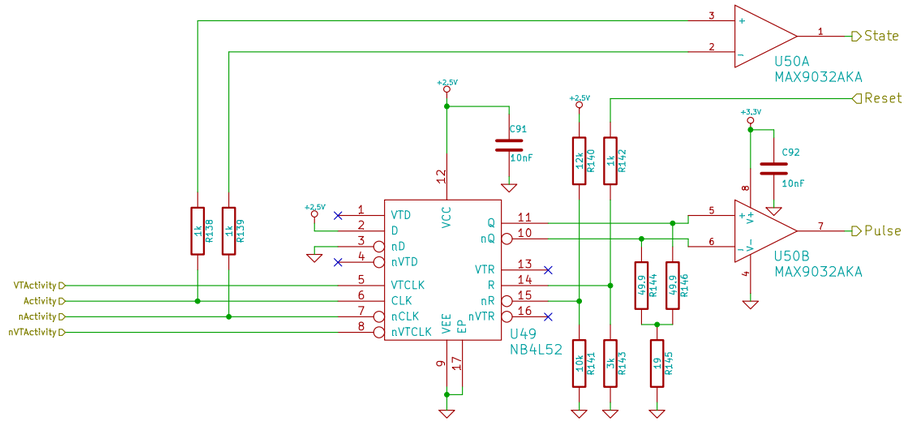
File: ActivityDetector.sch

Sheet: /LogicGate/ActivityDetector_Out1/

Title: High-speed Logic Gate

Size: A3	Date: 6 dec 2013	**Rev: 1.0**
KiCad E.D.A.	eeschema (2013-07-07 BZR 4022)-stable	Id: 8/9



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File: ActivityDetector.sch

Sheet: /LogicGate/ActivityDetector_In2/

Title: High-speed Logic Gate

Size: A3	Date: 6 dec 2013	**Rev: 1.0**
KiCad E.D.A.	eeschema (2013-07-07 BZR 4022)-stable	Id: 9/9