Sheet: template_core_easyphi

AD0/NANDRDY/TIOA1/PA2
AD1/WKUP1/PWMFI1/TIOB1/PA3
AD2/NWAIT/TCLK1/PA4
AD3/NCS0/TIOB2/PA6
WKUP4/PWMH0/URXD/PA8
PWMH3/UTXD/PA9
WKUP5/DATRG/RXD0/PA10
WKUP6/ADTRG/TXD0/PA11
TK/RTS1/PA14
WKUP8/TF/CTS1/PA15
AD7/TD/SPCK1/PA16
A18/SPI0_MISO/PA25
A19/SPI0_MOSI/PA26 — SPI_DAT
WKUP10/A20/SPI0_SPCK/PA27 — SPI_SCK
WKUP11/PCK2/SPI0_NPCS0/PA28 — SPI_nS
NRD/SPI0_NPCS1/PA29 — DELB_EN

ETXCK/EREFCK/PB0 — DELA_EN
ETXEN/PB1 — DELB_STATE
ETX0/PB2 — DELB_PULSE
ETX1/PB3 — IN_B_LED2
ECRSDV/ERXDV/PB4 — DELB_RES
ERX0/PB5 — OUT1_CHB_LED1
ERX1/PB6 — OUT1_CHB_LED3
EREXER/PB7 — OUT1_CHB_LED2
EMDC/PB8
EMDIO/PB9
AD8/PWMH0/TWD1/PB12
AD9/PWMH1/TWCK1/PB13
PWMH2/CANTX1/PB14
DAC0/WKUP12/PWMH3/CANRX1/PB15
DAC1/PWML0/TCLK5/PB16
AD10/PWML1/RF/PB17
AD11/PWML2/RD/PB18
AD12/PWML3/RK/PB19
AD13/SPI0_NPCS1/TXD2/PB20
AD14/WKUP13/SPI0_NPCS2/RXD2/PB21
PCK0/RTS2/PB22

MCDA4/A10/PD0
MCDA5/A11/PD1
MCDA6/A12/PD2
MCDA7/A13/PD3
TXD3/A14/PD4
RXD3/A15/PD5
PWMFI2/BA0/A16/PD6

PC1
PWML0/D0/PC2
PWMH0/D1/PC3
PWML1/D2/PC4 — IN_B_LED1
PWMH1/D3/PC5
PWML2/D4/PC6
PWMH2/D5/PC7
PWML3/D6/PC8
PWMH3/D7/PC9
ECRS/D8/PC10 — IN_B_LED3
ERX2/D9/PC11 — INA_LED1
ERX3/D10/PC12 — INA_LED3
ECOL/D11/PC13 — INA_LED2
ERXCK/D12/PC14 — DELA_STATE
ETX2/D13/PC15 — DELA_PULSE
ETX3/D14/PC16 — DELA_RES
ETXER/D15/PC17 — OUT1_CHA_LED1
PWMH6/NWE/NWR0/PC18 — OUT1_CHA_LED3
PWMH5/NANDOE/PC19 — OUT1_CHA_LED2
PWMH4/NANDWE/PC20
PWML4/NBS0/A10/PC21
PWML5/A1/PC22
PWML6/A2/PC23
PWML7/A3/PC24
TIOA6/A4/PC25
TIOB6/A5/PC26
TCLK6/A6/PC27
TIOA7/A7/PC28
TIOB7/A8/PC29

nCLK_10M_CON
CLK_10M_CON
nCLK_IN
CLK10_IN

EXT_SYNC2
EXT_SYNC3
EXT_SYNC4
CLK_RQ_SIG

RCB_1
R5 4k
RCB_2

R5 = ((Itriplow * 0.03) + 4.7mV) / 37uA
Slew rate set to max 3.3V/ms

File: template_core_easyphi.sch

D6 — LED_RGB — R39 680 (INA_LED1) — R44 220 (INA_LED2) — R45 680 (INA_LED3)
D7 — LED_RGB — R40 680 (OUT1_CHA_LED1) — R46 220 (OUT1_CHA_LED2) — R47 680 (OUT1_CHA_LED3)
D8 — LED_RGB — R41 680 (OUT1_CHA_LED1) — R48 220 (OUT1_CHA_LED2) — R49 680 (OUT1_CHA_LED3)
D9 — LED_RGB — R42 680 (IN_B_LED1) — R50 220 (IN_B_LED2) — R51 680 (IN_B_LED3)
D11 — LED_RGB — R55 680 (OUT1_CHB_LED1) — R57 220 (OUT1_CHB_LED2) — R58 680 (OUT1_CHB_LED3)
D12 — LED_RGB — R56 680 (OUT1_CHB_LED1) — R59 220 (OUT1_CHB_LED2) — R60 680 (OUT1_CHB_LED3)

U11 — U17 — U18 — U19 — U20 — U21 — RLP1-600-800 (FIX, FIX)

U22 — U24 — U25 — U26 — U27 — U28 — CONNEC_QMA_ANO_2622-4035 (CON, GND, GND, GND, GND, GND)
U22: IN_A
U24: OUT1_CHA
U25: OUT2_CHA
U26: IN_B
U27: OUT1_CHB
U28: OUT2_CHB

Sheet: DelayLineGenerator

SPI_nS
SPI_SCK
SPI_DAT
DELA_EN
DELB_EN
DELA_RES
DELB_RES
DELA_STATE
DELA_PULSE
DELB_STATE
DELB_PULSE
IN_A
IN_B

SLOAD
SCLK
SDATA
EnableA
EnableB
ResetA
ResetB
StateA
PulseA
StateB
PulseB
IN_CHA
IN_CHB

OUT1_CHA
OUT1_CHB
OUT2_CHA
OUT2_CHB

OUT2_CHA
OUT2_CHB
OUT1_CHA
OUT1_CHB

File: DelayLineGenerator.sch

ABOUT THE POWER SUPPLY SYMBOLS

+12V	is the 12V filtered coming from the backplane (MAX 4A) set R5 according to the max current you'll have
+5V	is the 5V filtered coming from the backplane (MAX 0.5A)
+3.3V	is a 3.3V generated from this 5V by a stepdown used by template_core chips
+3.3VADC	is a 3.3V generated from the 5V by a LDO used by the uC ADC

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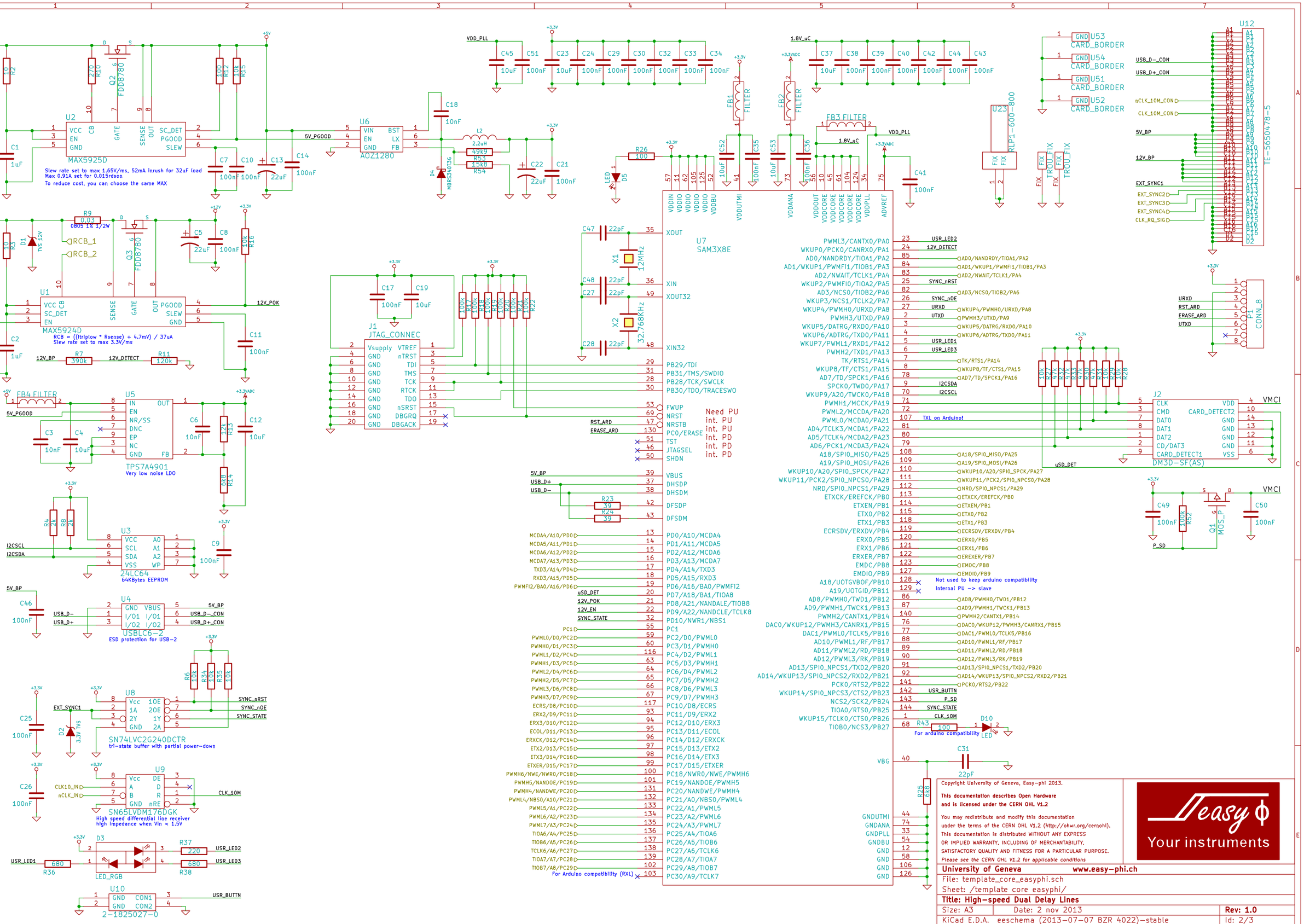
File: top_level_easyphi.sch
Sheet: /

Title: High-speed Dual Delay Lines

Size: A3	Date: 2 nov 2013	**Rev: 1.0**
KiCad E.D.A.	eeschema (2013-07-07 BZR 4022)-stable	Id: 1/3



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File: template_core_easyphi.sch
Sheet: /template core easyphi/

Title: High-speed Dual Delay Lines

Size: A3	Date: 2 nov 2013	**Rev: 1.0**
KiCad E.D.A.	eeschema (2013-07-07 BZR 4022)-stable	Id: 2/3

Input Channel A

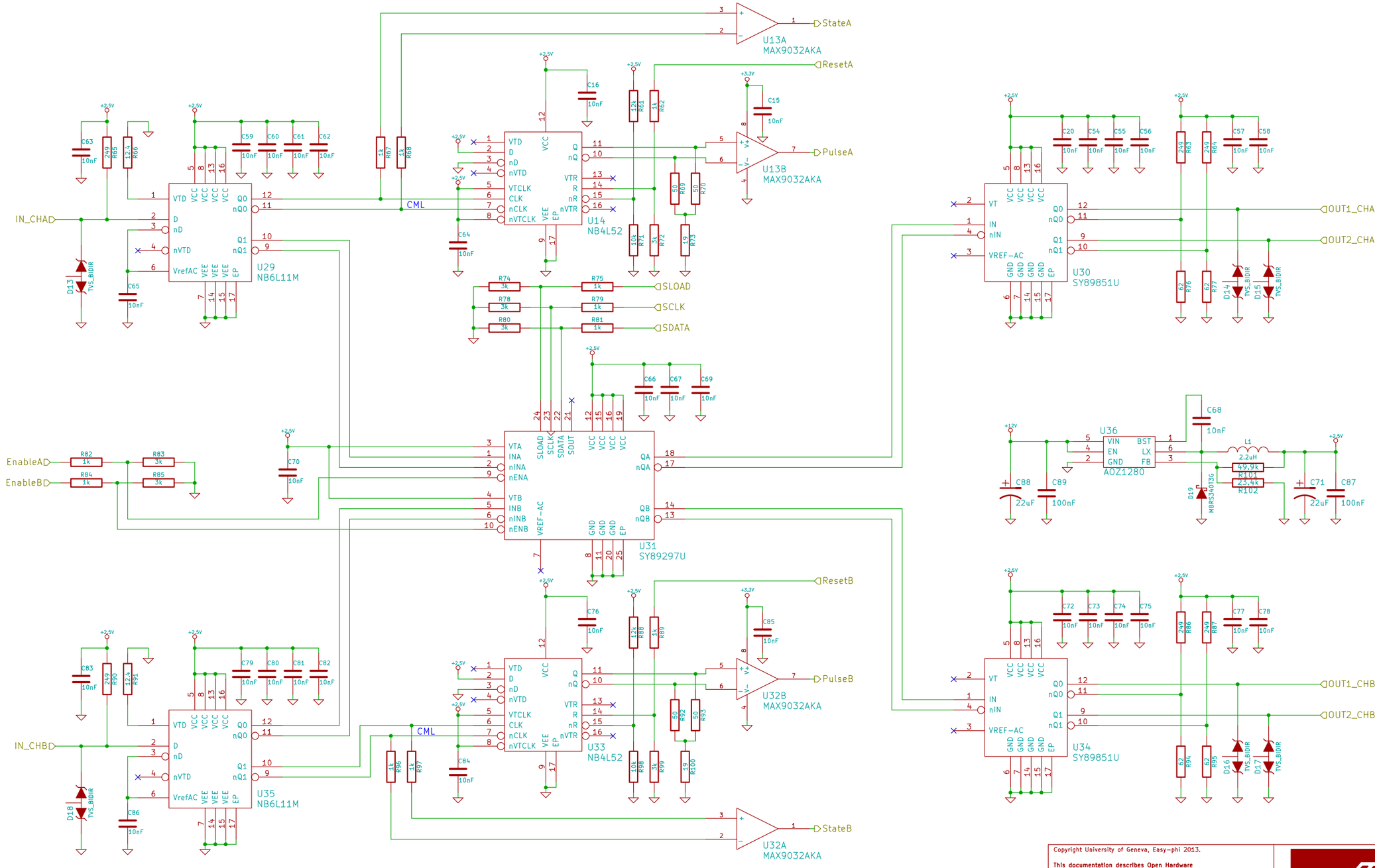
Input Channel B

Output 1 Channel A

Output 2 Channel A

Output 1 Channel B

Output 2 Channel B



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File: DelayLineGenerator.sch

Sheet: /DelayLineGenerator/

Title: High-speed Dual Delay Lines

Size: A3	Date: 2 nov 2013	**Rev: 1.0**
KiCad E.D.A.	eeschema (2013-07-07 BZR 4022)-stable	Id: 3/3