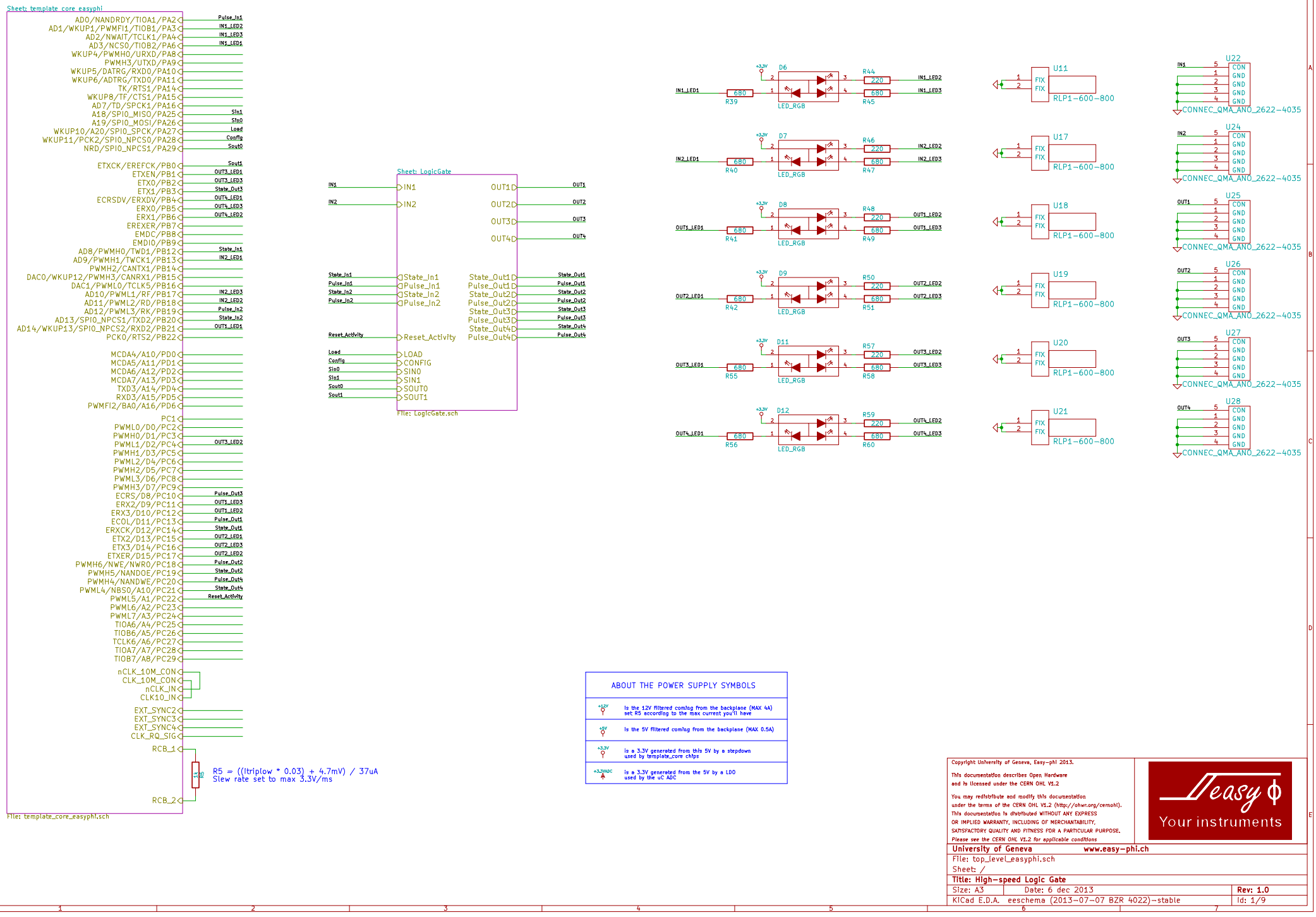
Sheet: template_core_easyphi
AD0/NANDRDY/TIOA1/PA2
AD1/WKUP1/PWMFI1/TIOB1/PA3
AD2/NWAIT/TCLK1/PA4
AD3/NCS0/TIOB2/PA6
WKUP4/PWMH0/URXD/PA8
PWMH3/UTXD/PA9
WKUP5/DATRG/RXD0/PA10
WKUP6/ADTRG/TXD0/PA11
TK/RTS1/PA14
WKUP8/TF/CTS1/PA15
AD7/TD/SPCK1/PA16
A18/SPI0_MISO/PA25
A19/SPI0_MOSI/PA26
WKUP10/A20/SPI0_SPCK/PA27
WKUP11/PCK2/SPI0_NPCS0/PA28
NRD/SPI0_NPCS1/PA29
ETXCK/EREFCK/PB0
ETXEN/PB1
ETX0/PB2
ETX1/PB3
ECRSDV/ERXDV/PB4
ERX0/PB5
ERX1/PB6
EREXER/PB7
EMDC/PB8
EMDIO/PB9
AD8/PWMH0/TWD1/PB12
AD9/PWMH1/TWCK1/PB13
PWMH2/CANTX1/PB14
DAC0/WKUP12/PWMH3/CANRX1/PB15
DAC1/PWML0/TCLK5/PB16
AD10/PWML1/RF/PB17
AD11/PWML2/RD/PB18
AD12/PWML3/RK/PB19
AD13/SPI0_NPCS1/TXD2/PB20
AD14/WKUP13/SPI0_NPCS2/RXD2/PB21
PCK0/RTS2/PB22
MCDA4/A10/PD0
MCDA5/A11/PD1
MCDA6/A12/PD2
MCDA7/A13/PD3
TXD3/A14/PD4
RXD3/A15/PD5
PWMFI2/BA0/A16/PD6
PC1
PWML0/D0/PC2
PWMH0/D1/PC3
PWML1/D2/PC4
PWMH1/D3/PC5
PWML2/D4/PC6
PWMH2/D5/PC7
PWML3/D6/PC8
PWMH3/D7/PC9
ECRS/D8/PC10
ERX2/D9/PC11
ERX3/D10/PC12
ECOL/D11/PC13
ERXCK/D12/PC14
ETX2/D13/PC15
ETX3/D14/PC16
ETXER/D15/PC17
PWMH6/NWE/NWR0/PC18
PWMH5/NANDOE/PC19
PWMH4/NANDWE/PC20
PWML4/NBS0/A10/PC21
PWML5/A1/PC22
PWML6/A2/PC23
PWML7/A3/PC24
TIOA6/A4/PC25
TIOB6/A5/PC26
TCLK6/A6/PC27
TIOA7/A7/PC28
TIOB7/A8/PC29
nCLK_10M_CON
CLK_10M_CON
nCLK_IN
CLK10_IN
EXT_SYNC2
EXT_SYNC3
EXT_SYNC4
CLK_RQ_SIG
RCB_1
RCB_2
R5 = ((Itriplow * 0.03) + 4.7mV) / 37uA
Slew rate set to max 3.3V/ms
File: template_core_easyphi.sch
Sheet: LogicGate
IN1
IN2
OUT1
OUT2
OUT3
OUT4
State_In1
Pulse_In1
State_In2
Pulse_In2
Reset_Activity
Load
Config
Sin0
Sin1
Sout0
Sout1
State_Out1
Pulse_Out1
State_Out2
Pulse_Out2
State_Out3
Pulse_Out3
State_Out4
Pulse_Out4
LOAD
CONFIG
SIN0
SIN1
SOUT0
SOUT1
File: LogicGate.sch
D6
D7
D8
D9
D11
D12
R44
R45
R46
R47
R48
R49
R50
R51
R57
R58
R59
R60
R39
R40
R41
R42
R55
R56
680
220
LED_RGB
IN1_LED1
IN1_LED2
IN1_LED3
IN2_LED1
IN2_LED2
IN2_LED3
OUT1_LED1
OUT1_LED2
OUT1_LED3
OUT2_LED1
OUT2_LED2
OUT2_LED3
OUT3_LED1
OUT3_LED2
OUT3_LED3
OUT4_LED1
OUT4_LED2
OUT4_LED3
U11
U17
U18
U19
U20
U21
FIX
RLP1-600-800
U22
U24
U25
U26
U27
U28
CON
GND
CONNEC_QMA_ANO_2622-4035
ABOUT THE POWER SUPPLY SYMBOLS
+12V
Is the 12V filtered comlog from the backplane (MAX 4A) set R5 according to the max current you'll have
+5V
Is the 5V filtered comlog from the backplane (MAX 0.5A)
+3.3V
Is a 3.3V generated from this 5V by a stepdown used by template_core chips
+3.3VADC
Is a 3.3V generated from the 5V by a LDO used by the uC ADC
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Easy ϕ
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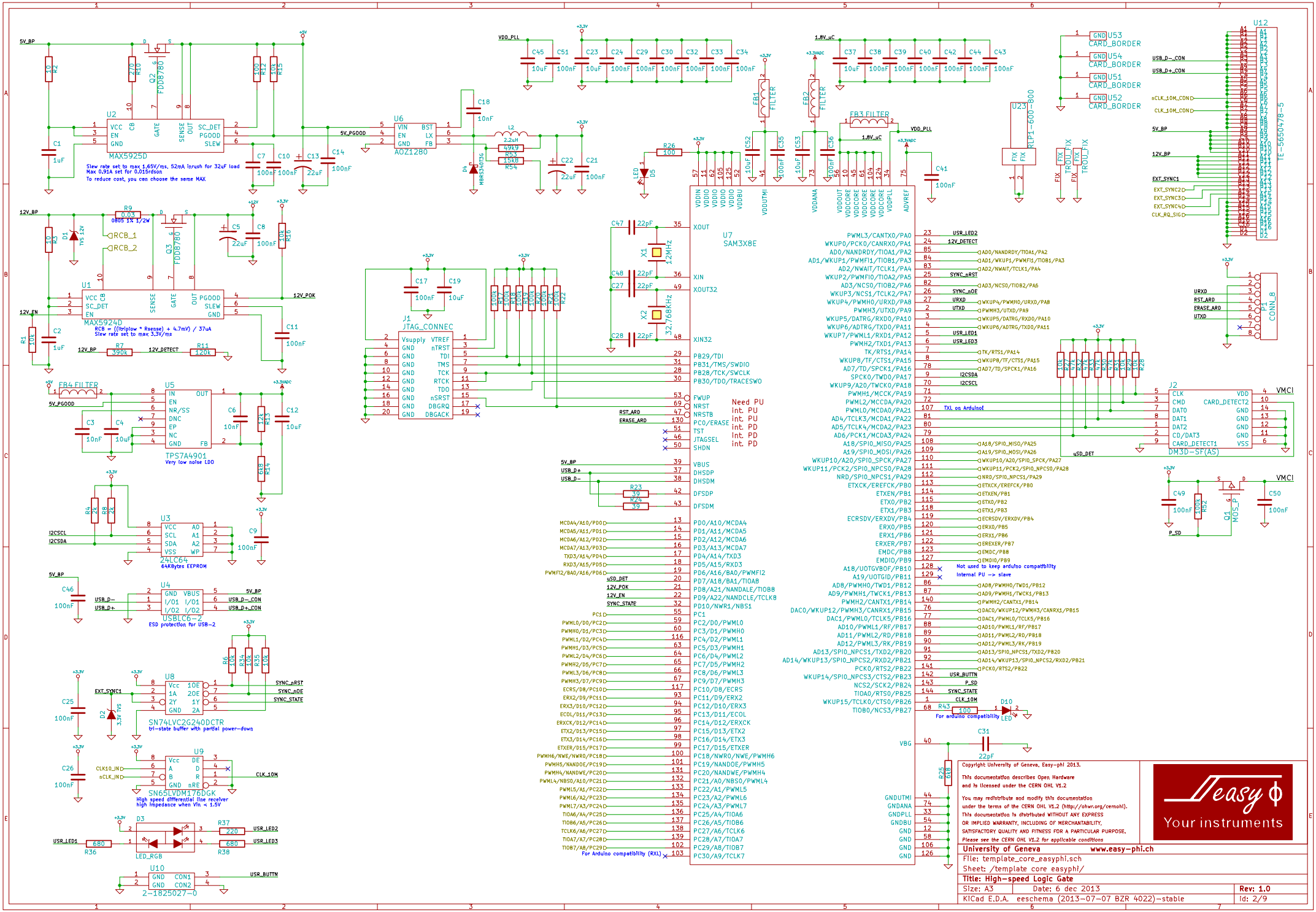
File: top_level_easyphi.sch
Sheet: /
Title: High-speed Logic Gate
Size: A3
Date: 6 dec 2013
Rev: 1.0
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable
Id: 1/9


MAX5925D
Slew rate set to max 1.65V/ms, 52mA inrush for 32uF load
Max 0.91A set for 0.015rdson
To reduce cost, you can choose the same MAX
AOZ1280
MAX5924D
RCB = ((Vinplow * Rsense) + 4.7mV) / 37uA
Slew rate set to max 3.3V/ms
TPS7A4901
Very low noise LDO
24LC64
64KBytes EEPROM
USBLC6-2
ESD protection for USB-2
SN74LVC2G240DCTR
tri-state buffer with partial power-down
SN65LVDM176DGK
High speed differential line receiver
high impedance when Vin < 1.5V
LED_RGB
2-1825027-0
SAM3X8E
JTAG_CONNEC
12MHz
32.768KHz
Need PU
int. PU
int. PU
int. PD
int. PD
int. PD
RLP1-600-800
CARD_BORDER
TE-5650478-5
DM3D-SF(AS)
CONN_8
MOS_P
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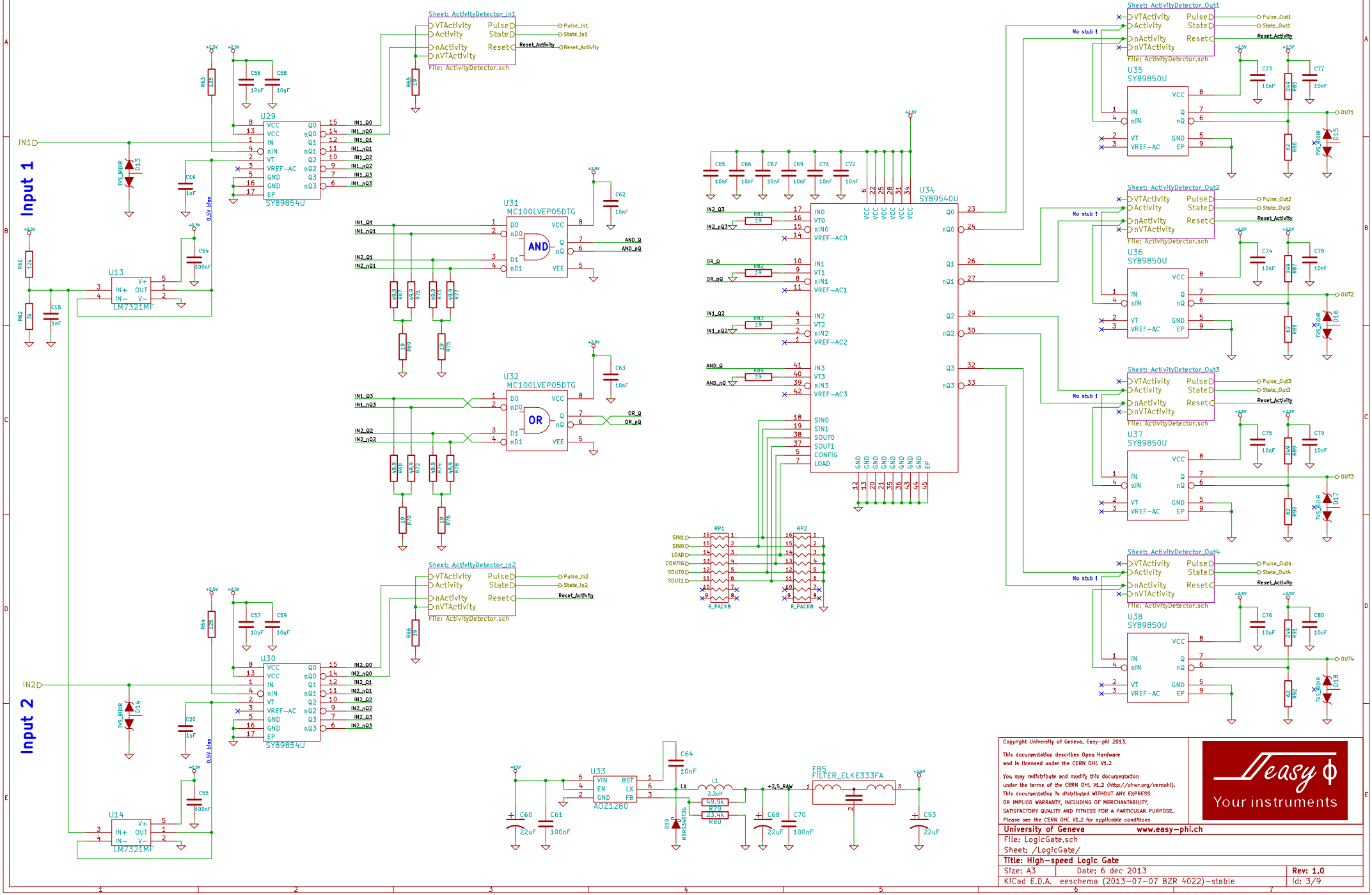
File: template_core_easyphi.sch
Sheet: /template core easyphi/
Title: High-speed Logic Gate
Size: A3
Date: 6 dec 2013
Rev: 1.0
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable
Id: 2/9


Input 1
Input 2
IN1
IN2
U29
U30
U31
U32
U33
U34
U35
U36
U37
U38
SY89854U
SY89540U
MC100LVEP05DTG
AND
OR
LM7321MF
A0Z1280
FILTER_ELKE333FA
Sheet: ActivityDetector_In1
Sheet: ActivityDetector_In2
Sheet: ActivityDetector_Out1
Sheet: ActivityDetector_Out2
Sheet: ActivityDetector_Out3
Sheet: ActivityDetector_Out4
File: ActivityDetector.sch
VTActivity
Activity
nActivity
nVTActivity
Pulse
State
Reset
Reset_Activity
No stub !
+2.5V
+2.5_RAW
0.5V bias
TVS_BIDIR
MBRS340T3G
R_PACK8
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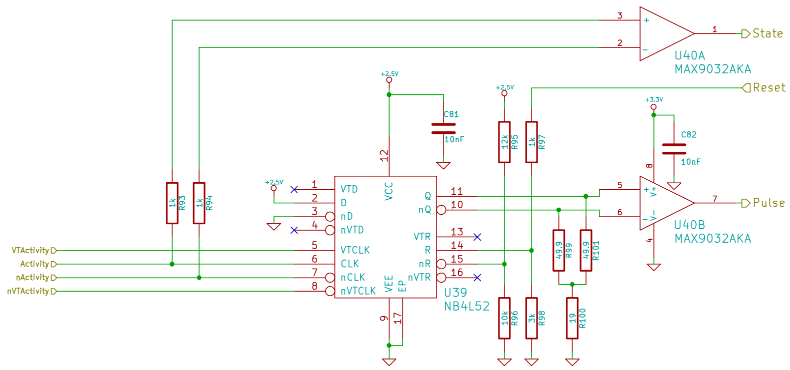
File: LogicGate.sch
Sheet: /LogicGate/
Title: High-speed Logic Gate
Size: A3
Date: 6 dec 2013
Rev: 1.0
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable
Id: 3/9



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File: ActivityDetector.sch

Sheet: /LogicGate/ActivityDetector_In1/

Title: High-speed Logic Gate

Size: A3	Date: 6 dec 2013	**Rev: 1.0**
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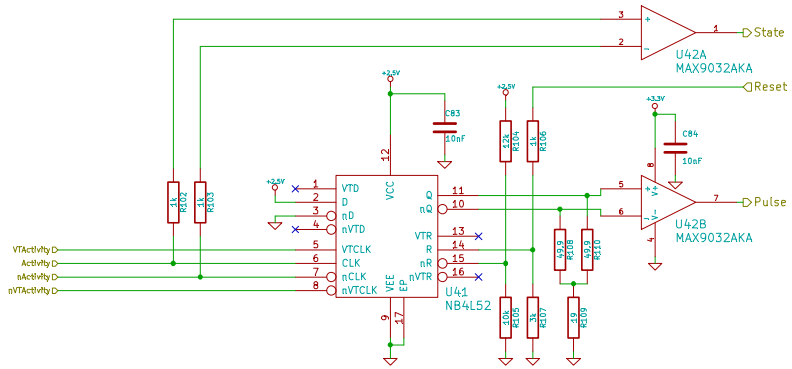

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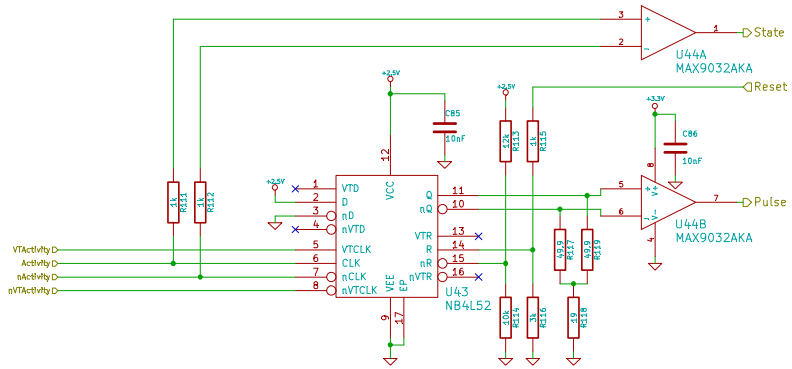
File: ActivityDetector.sch		
Sheet: /LogicGate/ActivityDetector_Out4/		
Title: High-speed Logic Gate		
Size: A3	Date: 6 dec 2013	**Rev: 1.0**
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable		Id: 5/9



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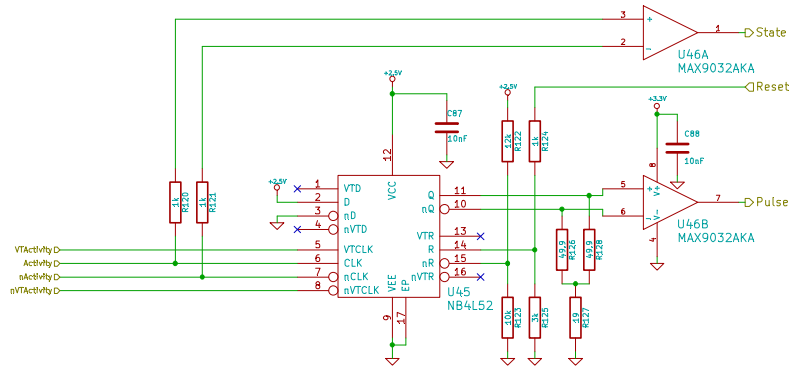
File: ActivityDetector.sch		
Sheet: /LogicGate/ActivityDetector_Out3/		
Title: High-speed Logic Gate		
Size: A3	Date: 6 dec 2013	**Rev: 1.0**
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable		Id: 6/9



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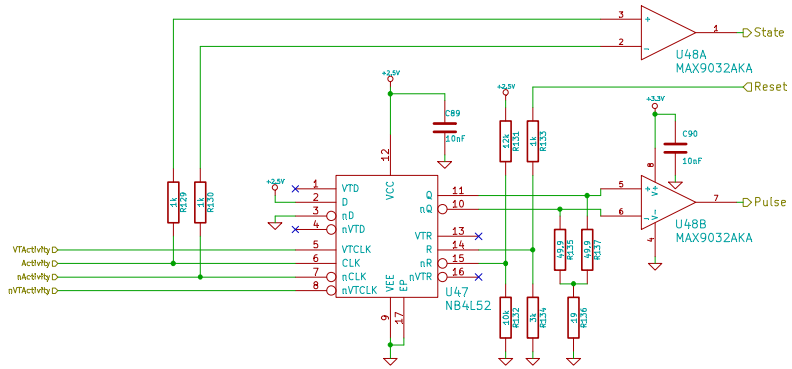
File: ActivityDetector.sch	
Sheet: /LogicGate/ActivityDetector_Out2/	
Title: High-speed Logic Gate	
Size: A3	Date: 6 dec 2013
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable	Id: 7/9

Rev: 1.0



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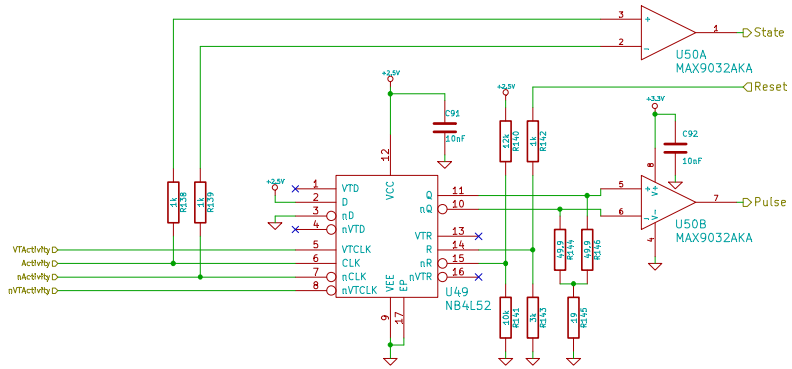
File: ActivityDetector.sch		
Sheet: /LogicGate/ActivityDetector_Out1/		
Title: High-speed Logic Gate		
Size: A3	Date: 6 dec 2013	**Rev: 1.0**
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable		Id: 8/9



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File: ActivityDetector.sch		
Sheet: /LogicGate/ActivityDetector_In2/		
Title: High-speed Logic Gate		
Size: A3	Date: 6 dec 2013	**Rev: 1.0**
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable		Id: 9/9