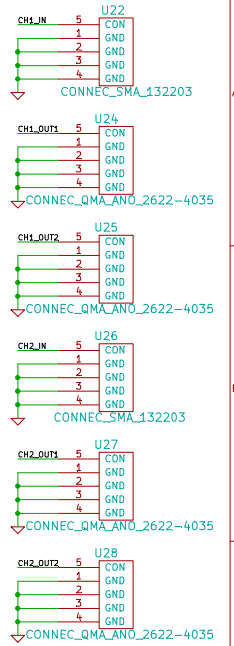
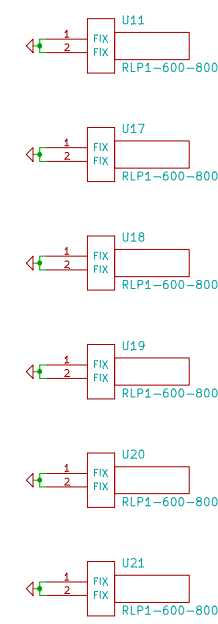
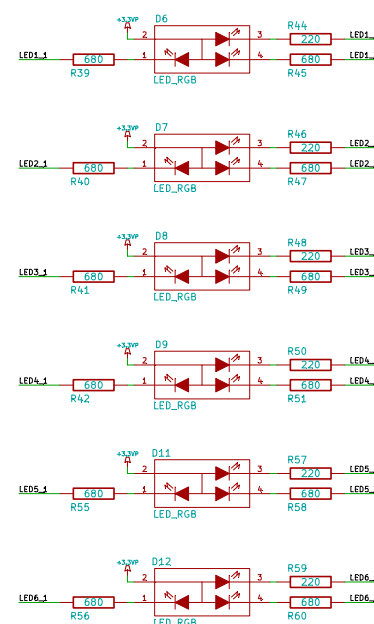
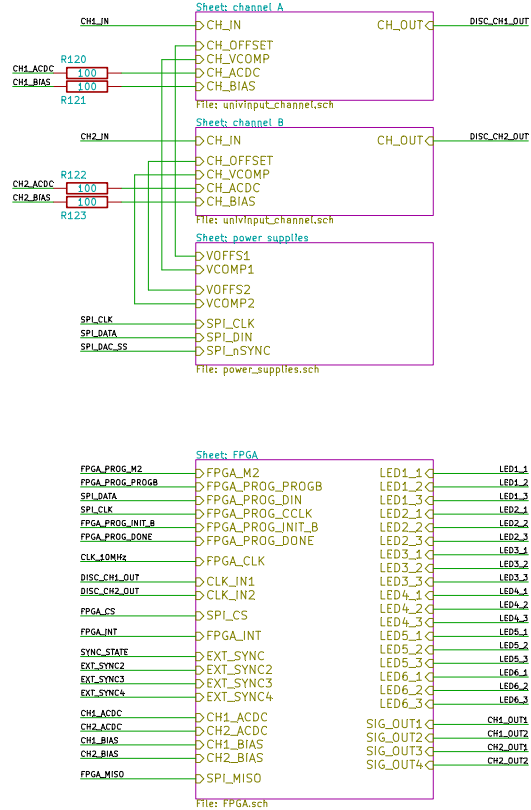


Sheet: template\_core\_easyphi

ADO/NANDRDY/TIOA1/PA2C  
 AD1/WKUP1/PWMF1/TIOB1/PA3C  
 AD2/NWAI/TCLK1/PA4C  
 AD3/NC50/TIOB2/PA6C  
 WKUP4/PWMH0/URX0/PA8C  
 PWMH3/UTX0/PA9C  
 WKUP5/DATRG/RXD0/PA10C  
 WKUP6/ADTRG/TXD0/PA11C  
 TK/RTS1/PA14C  
 WKUP8/TF/CTS1/PA15C  
 AD7/TD/SPCK1/PA16C  
 A18/SPIO\_MISO/PA26C  
 A19/SPIO\_MOSI/PA28C  
 WKUP10/A20/SPIO\_SPCK/PA27C  
 WKUP11/PCK2/SPIO\_NPCS0/PA28C  
 NRD/SPIO\_NPCS1/PA29C  
 ETXCK/EREFCK/PB0C  
 ETXEN/PB1C  
 ETX0/PB2C  
 ETX1/PB3C  
 ECRSDV/ERXDV/PB4C  
 ERX0/PB5C  
 ERX1/PB6C  
 EREXER/PB7C  
 EMDC/PB8C  
 EMDIO/PB9C  
 AD8/PWMH0/TWD1/PB12C  
 AD9/PWMH1/TWCK1/PB13C  
 PWMH2/CANTX1/PB14C  
 DAC0/WKUP12/PWMH3/CANRX1/PB15C  
 DAC1/PWML0/TCLK5/PB16C  
 AD10/PWML1/RF/PB17C  
 AD11/PWML2/RD/PB18C  
 AD12/PWML3/RK/PB19C  
 AD13/SPIO\_NPCS1/TXD2/PB20C  
 AD14/WKUP13/SPIO\_NPCS2/RXD2/PB21C  
 PCK0/RTS2/PB22C  
 MCD4/A10/PD0C  
 MCD4/A11/PD1C  
 MCD6/A12/PD2C  
 MCD7/A13/PD3C  
 TXD3/A14/PD4C  
 RXD3/A15/PD5C  
 PWMF12/BA0/A16/PD6C  
 PC1C  
 PWML0/D0/PC2C  
 PWMH0/D1/PC3C  
 PWML1/D2/PC4C  
 PWMH1/D3/PC5C  
 PWML2/D4/PC6C  
 PWMH2/D5/PC7C  
 PWML3/D6/PC8C  
 PWMH3/D7/PC9C  
 ECR5/D8/PC10C  
 ERX2/D9/PC11C  
 ERX3/D10/PC12C  
 ECOL/D11/PC13C  
 ERXCK/D12/PC14C  
 ETX2/D13/PC15C  
 ETX3/D14/PC16C  
 ETXER/D15/PC17C  
 PWMH6/NWE/NWRO/PC18C  
 PWMH5/NANDOE/PC19C  
 PWMH4/NANDWE/PC20C  
 PWML4/NBS0/A10/PC21C  
 PWML5/A1/PC22C  
 PWML6/A2/PC23C  
 PWML7/A3/PC24C  
 TIOA6/A4/PC25C  
 TIOB6/A5/PC26C  
 TCLK6/A6/PC27C  
 TIOA7/A7/PC28C  
 TIOB7/A8/PC29C  
 nCLK\_10M\_CONC  
 CLK\_10M\_CONC  
 nCLK\_INQ  
 CLK10\_INQ  
 EXT\_SYNC2C  
 EXT\_SYNC3C  
 EXT\_SYNC4C  
 CLK\_RQ\_SIGC  
 RCB\_1C  
 RCB\_2C  
 CLK\_10MHzC  
 CLK\_10MHz\_nEN  
 SYNC\_STATEC



# ABOUT THE POWER SUPPLY SYMBOLS

+12V	Is the 12V filtered coming from the backplane (MAX 4A) set R5 according to the max current you'll have
+5V	Is the 5V filtered coming from the backplane (MAX 0.5A)
+3.3V	Is a 3.3V generated from this 5V by a stepdowns used by template_core chips
+3.3VADC	Is a 3.3V generated from the 5V by a LDO used by the uC ADC

Universal input specs:  
max input frequency: 100MHz

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File: top\_level\_easyphi.sch

Sheet: /

Title: Low cost Dual 100MHz Universal Input

Size: A3 Date: 20 dec 2013

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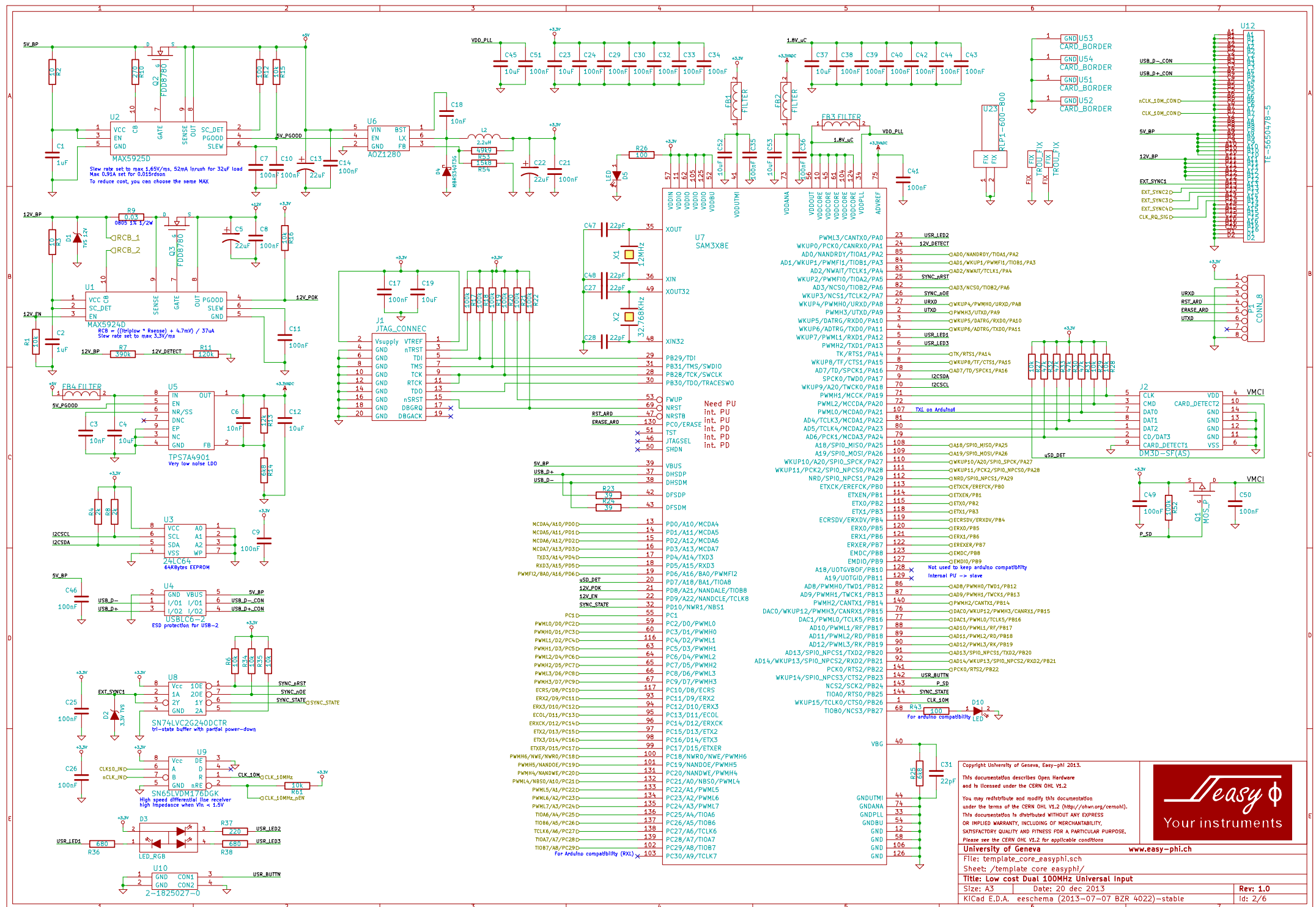
Rev: 1.0

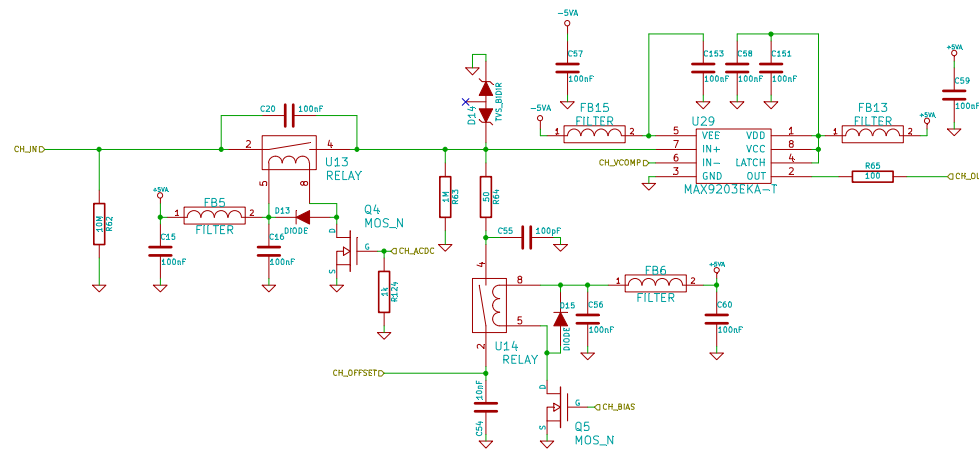
Id: 1/6

File: template\_core\_easyphi.sch

$$R5 = ((Itripow * 0.03) + 4.7mV) / 37uA$$

Slew rate set to max 3.3V/ms





YES, WE NEED A WHOLE PAGE FOR THAT.

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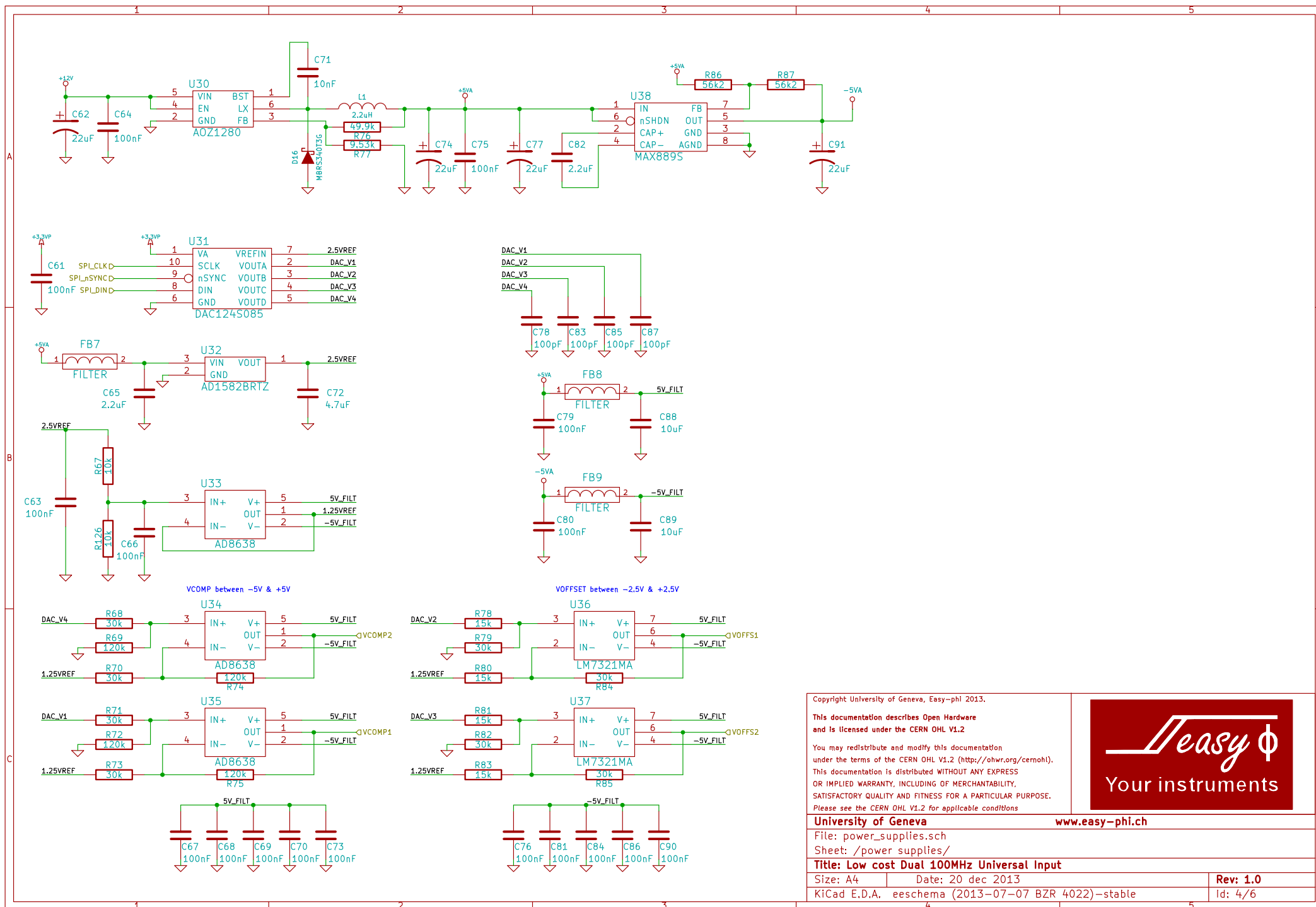
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Size: A3 Date: 20 dec 2013

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Rev: 1.0

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File: power\_supplies.sch

Sheet: /power\_supplies/

Title: Low cost Dual 100MHz Universal Input

Size: A4 Date: 20 dec 2013

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Rev: 1.0

Id: 4/6





