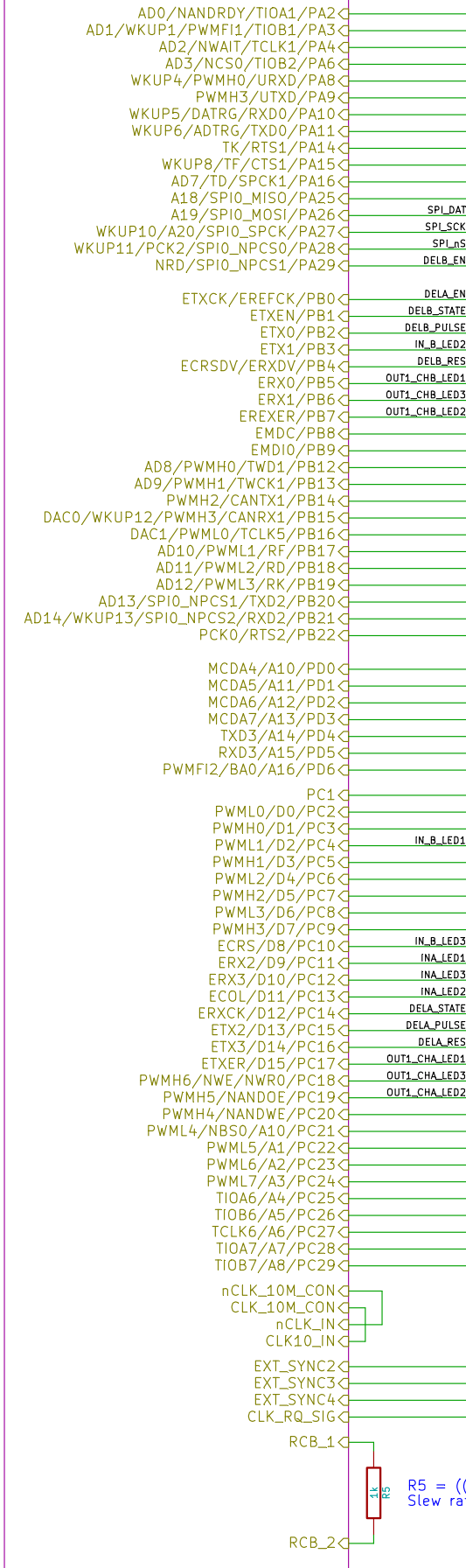
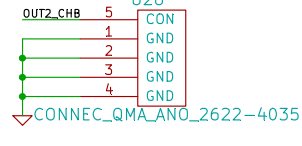
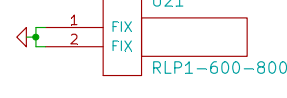
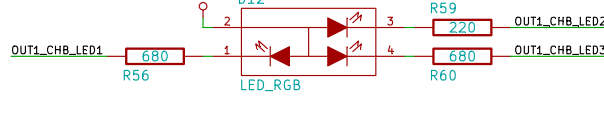
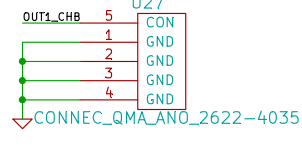
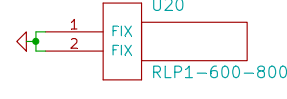
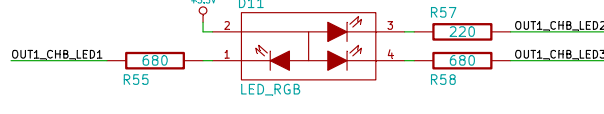
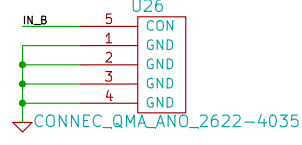
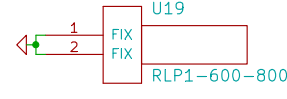
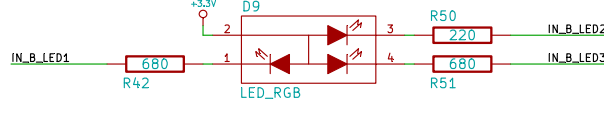
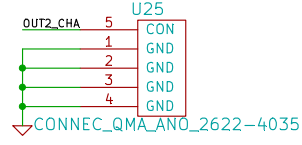
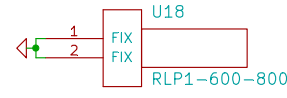
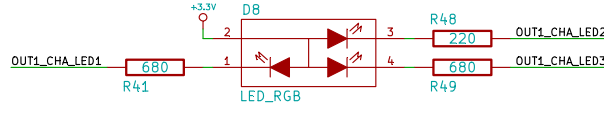
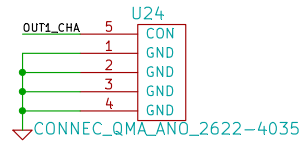
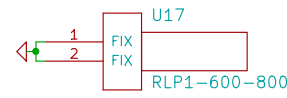
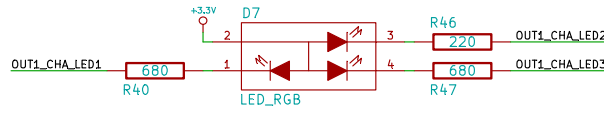
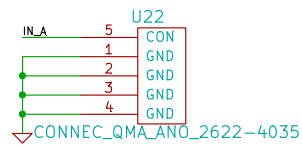
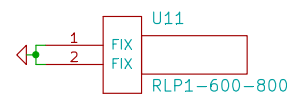
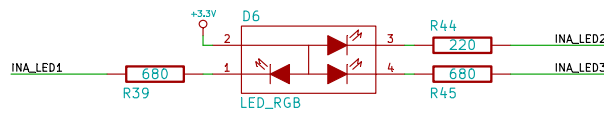


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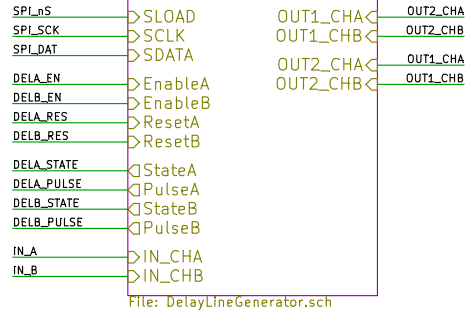


$R5 = ((I_{triplow} * 0.03) + 4.7mV) / 37\mu A$
Slew rate set to max 3.3V/ms

File: template_core_easyphi.sch



Sheet: DelayLineGenerator



ABOUT THE POWER SUPPLY SYMBOLS

+12V	is the 12V filtered coming from the backplane (MAX 4A) set R5 according to the max current you'll have
+5V	is the 5V filtered coming from the backplane (MAX 0.5A)
+3.3V	is a 3.3V generated from this 5V by a stepdown used by template_core chips
+3.3VADC	is a 3.3V generated from the 5V by a LDO used by the uc ADC

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File: top_level_easyphi.sch

Sheet: /

Title: High-speed Dual Delay Lines

Size: A3 Date: 2 nov 2013

Rev: 1.0

KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable

Id: 1/3



