

nCLK_10M_CONC CLK_10M_CONC nCLK_INC CLK10_INC

EXT_SYNC2C EXT_SYNC3C EXT_SYNC4C CLK_RQ_SIGC

RCB_1

RCB_2<

File: template_core_easyphi.sch

R5 = ((Itriplow * 0.03) + 4.7mV) / 37uASlew rate set to max 3.3V/ms

Al	BOUT THE POWER SUPPLY SYMBOLS
+12V	is the 12V filtered coming from the backplane (MAX 4A) set R5 according to the max current you'll have
+5∨ •	is the 5V filtered coming from the backplane (MAX 0.5A)
+3.3V	is a 3.3V generated from this 5V by a stepdown used by template_core chips
+3.3VADC	is a 3.3V generated from the 5V by a LDO used by the uC ADC



File: top_level_easyphi.sch Sheet: /			
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