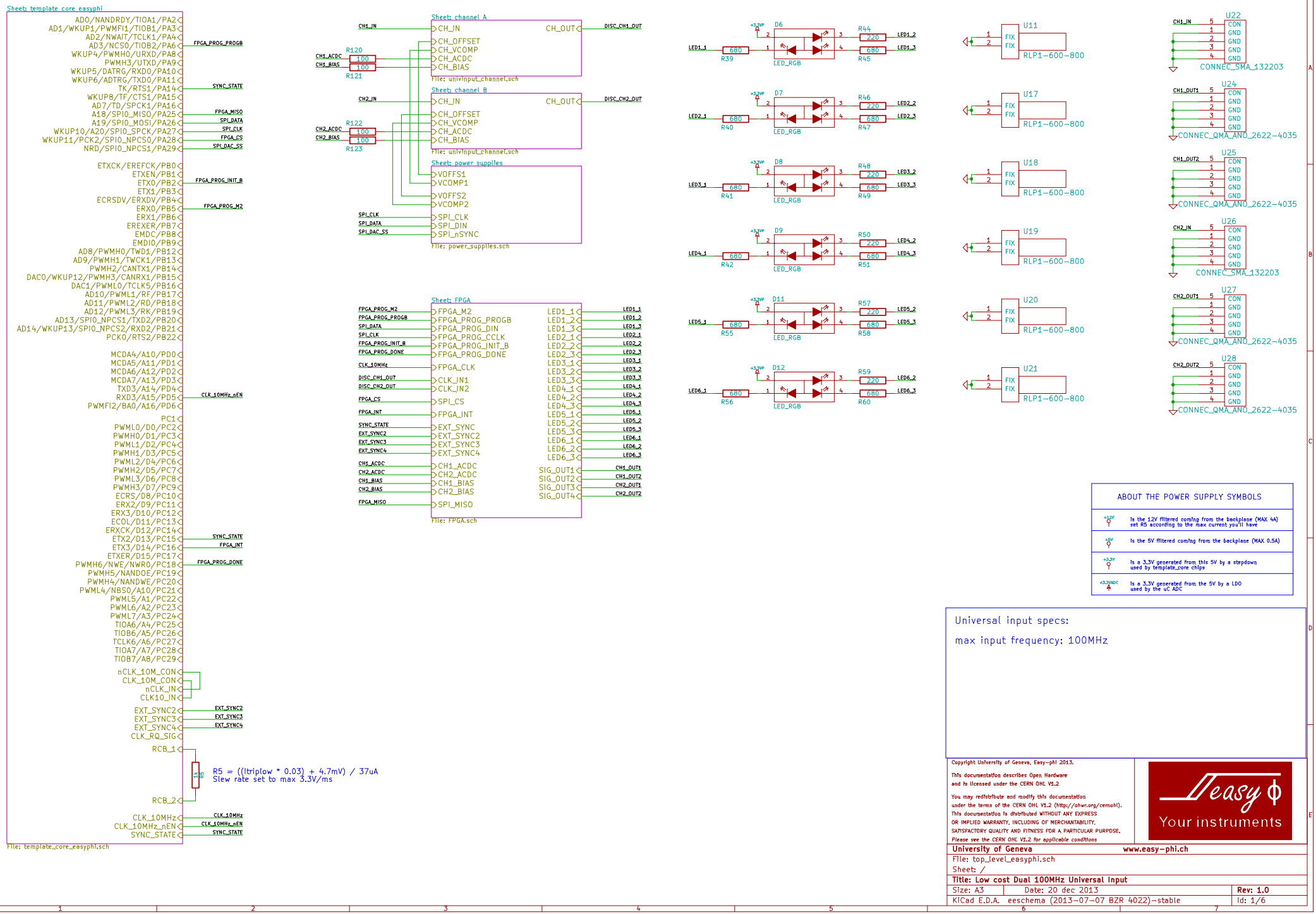
Sheet: template_core_easyphi
AD0/NANDRDY/TIOA1/PA2
AD1/WKUP1/PWMFI1/TIOB1/PA3
AD2/NWAIT/TCLK1/PA4
AD3/NCS0/TIOB2/PA6
WKUP4/PWMH0/URXD/PA8
PWMH3/UTXD/PA9
WKUP5/DATRG/RXD0/PA10
WKUP6/ADTRG/TXD0/PA11
TK/RTS1/PA14
WKUP8/TF/CTS1/PA15
AD7/TD/SPCK1/PA16
A18/SPI0_MISO/PA25
A19/SPI0_MOSI/PA26
WKUP10/A20/SPI0_SPCK/PA27
WKUP11/PCK2/SPI0_NPCS0/PA28
NRD/SPI0_NPCS1/PA29
ETXCK/EREFCK/PB0
ETXEN/PB1
ETX0/PB2
ETX1/PB3
ECRSDV/ERXDV/PB4
ERX0/PB5
ERX1/PB6
EREXER/PB7
EMDC/PB8
EMDIO/PB9
AD8/PWMH0/TWD1/PB12
AD9/PWMH1/TWCK1/PB13
PWMH2/CANTX1/PB14
DAC0/WKUP12/PWMH3/CANRX1/PB15
DAC1/PWML0/TCLK5/PB16
AD10/PWML1/RF/PB17
AD11/PWML2/RD/PB18
AD12/PWML3/RK/PB19
AD13/SPI0_NPCS1/TXD2/PB20
AD14/WKUP13/SPI0_NPCS2/RXD2/PB21
PCK0/RTS2/PB22
MCDA4/A10/PD0
MCDA5/A11/PD1
MCDA6/A12/PD2
MCDA7/A13/PD3
TXD3/A14/PD4
RXD3/A15/PD5
PWMFI2/BA0/A16/PD6
PC1
PWML0/D0/PC2
PWMH0/D1/PC3
PWML1/D2/PC4
PWMH1/D3/PC5
PWML2/D4/PC6
PWMH2/D5/PC7
PWML3/D6/PC8
PWMH3/D7/PC9
ECRS/D8/PC10
ERX2/D9/PC11
ERX3/D10/PC12
ECOL/D11/PC13
ERXCK/D12/PC14
ETX2/D13/PC15
ETX3/D14/PC16
ETXER/D15/PC17
PWMH6/NWE/NWR0/PC18
PWMH5/NANDOE/PC19
PWMH4/NANDWE/PC20
PWML4/NBS0/A10/PC21
PWML5/A1/PC22
PWML6/A2/PC23
PWML7/A3/PC24
TIOA6/A4/PC25
TIOB6/A5/PC26
TCLK6/A6/PC27
TIOA7/A7/PC28
TIOB7/A8/PC29
nCLK_10M_CON
CLK_10M_CON
nCLK_IN
CLK10_IN
EXT_SYNC2
EXT_SYNC3
EXT_SYNC4
CLK_RQ_SIG
RCB_1
RCB_2
CLK_10MHz
CLK_10MHz_nEN
SYNC_STATE
FPGA_PROG_PROGB
SYNC_STATE
FPGA_MISO
SPI_DATA
SPI_CLK
FPGA_CS
SPI_DAC_SS
FPGA_PROG_INIT_B
FPGA_PROG_M2
CLK_10MHz_nEN
SYNC_STATE
FPGA_INT
FPGA_PROG_DONE
File: template_core_easyphi.sch
R5 = ((Itriplow * 0.03) + 4.7mV) / 37uA
Slew rate set to max 3.3V/ms
Sheet: channel A
CH1_IN
CH_IN
CH_OUT
DISC_CH1_OUT
CH_OFFSET
CH_VCOMP
CH_ACDC
CH_BIAS
CH1_ACDC
CH1_BIAS
R120
100
R121
File: univinput_channel.sch
Sheet: channel B
CH2_IN
CH2_ACDC
CH2_BIAS
R122
R123
DISC_CH2_OUT
Sheet: power supplies
VOFFS1
VCOMP1
VOFFS2
VCOMP2
SPI_CLK
SPI_DIN
SPI_nSYNC
File: power_supplies.sch
Sheet: FPGA
FPGA_M2
FPGA_PROG_PROGB
FPGA_PROG_DIN
FPGA_PROG_CCLK
FPGA_PROG_INIT_B
FPGA_PROG_DONE
FPGA_CLK
CLK_IN1
CLK_IN2
SPI_CS
FPGA_INT
EXT_SYNC
EXT_SYNC2
EXT_SYNC3
EXT_SYNC4
CH1_ACDC
CH2_ACDC
CH1_BIAS
CH2_BIAS
SPI_MISO
LED1_1
LED1_2
LED1_3
LED2_1
LED2_2
LED2_3
LED3_1
LED3_2
LED3_3
LED4_1
LED4_2
LED4_3
LED5_1
LED5_2
LED5_3
LED6_1
LED6_2
LED6_3
SIG_OUT1
SIG_OUT2
SIG_OUT3
SIG_OUT4
CH1_OUT1
CH1_OUT2
CH2_OUT1
CH2_OUT2
File: FPGA.sch
D6
D7
D8
D9
D11
D12
R44
R45
R46
R47
R48
R49
R50
R51
R57
R58
R59
R60
R39
R40
R41
R42
R55
R56
680
220
LED_RGB
U11
U17
U18
U19
U20
U21
FIX
RLP1-600-800
U22
U24
U25
U26
U27
U28
CON
GND
CONNEC_SMA_132203
CONNEC_QMA_ANO_2622-4035
ABOUT THE POWER SUPPLY SYMBOLS
+12V
Is the 12V filtered coming from the backplane (MAX 4A) set R5 according to the max current you'll have
+5V
Is the 5V filtered coming from the backplane (MAX 0.5A)
+3.3V
Is a 3.3V generated from this 5V by a stepdown used by template_core chips
+3.3VADC
Is a 3.3V generated from the 5V by a LDO used by the uC ADC
Universal input specs:
max input frequency: 100MHz
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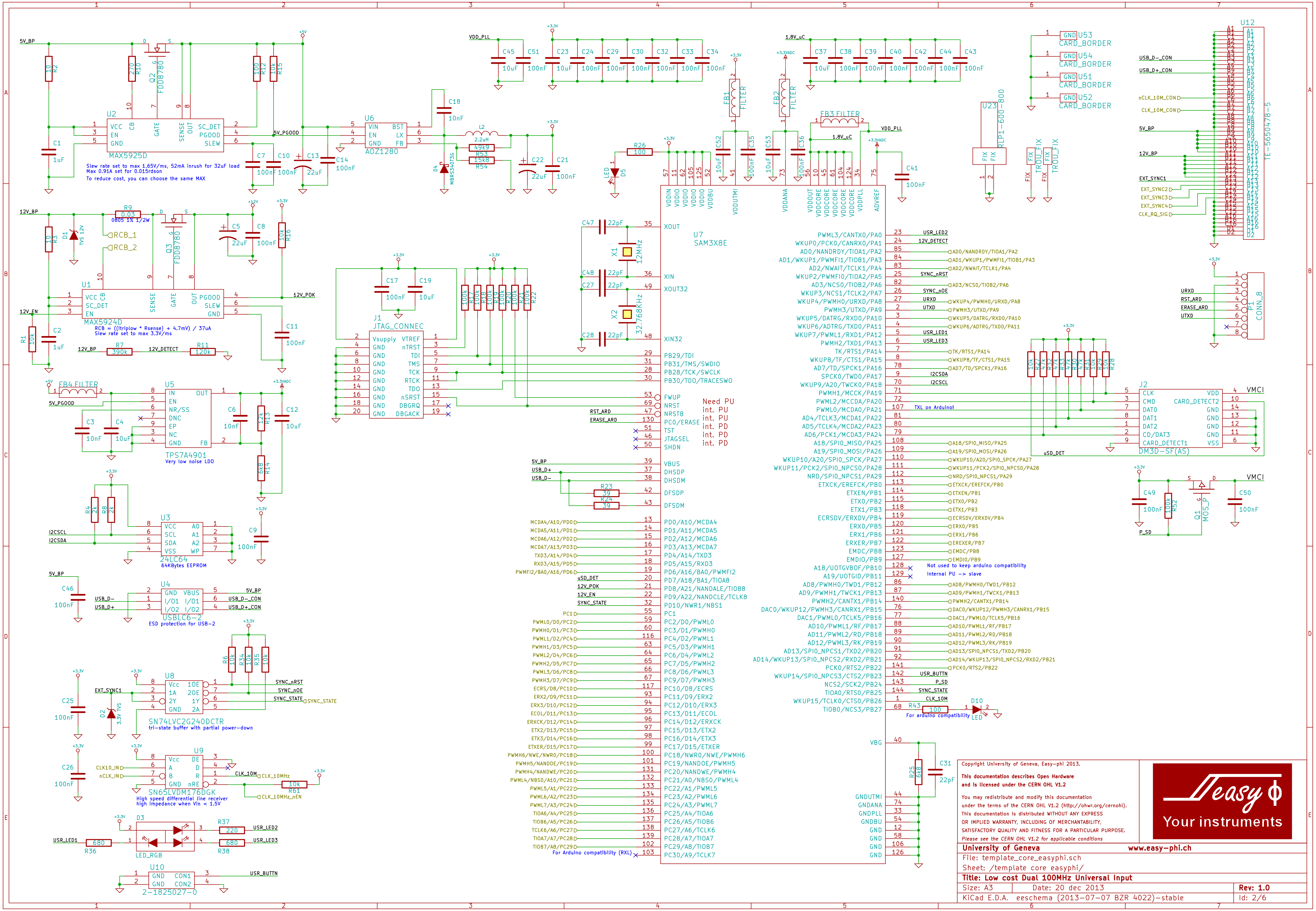
Easy ϕ
Your instruments
University of Geneva
www.easy-phi.ch
File: top_level_easyphi.sch
Sheet: /
Title: Low cost Dual 100MHz Universal Input
Size: A3
Date: 20 dec 2013
Rev: 1.0
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable
Id: 1/6



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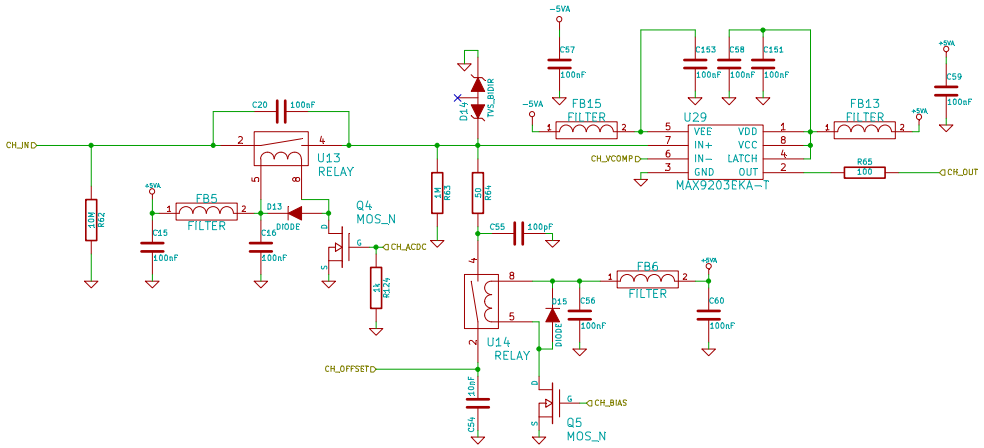
File: template_core_easyphi.sch

Sheet: /template core easyphi/

Title: Low cost Dual 100MHz Universal Input

Size: A3 | Date: 20 dec 2013 | **Rev: 1.0**

KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable | Id: 2/6



YES, WE NEED A WHOLE PAGE FOR THAT.

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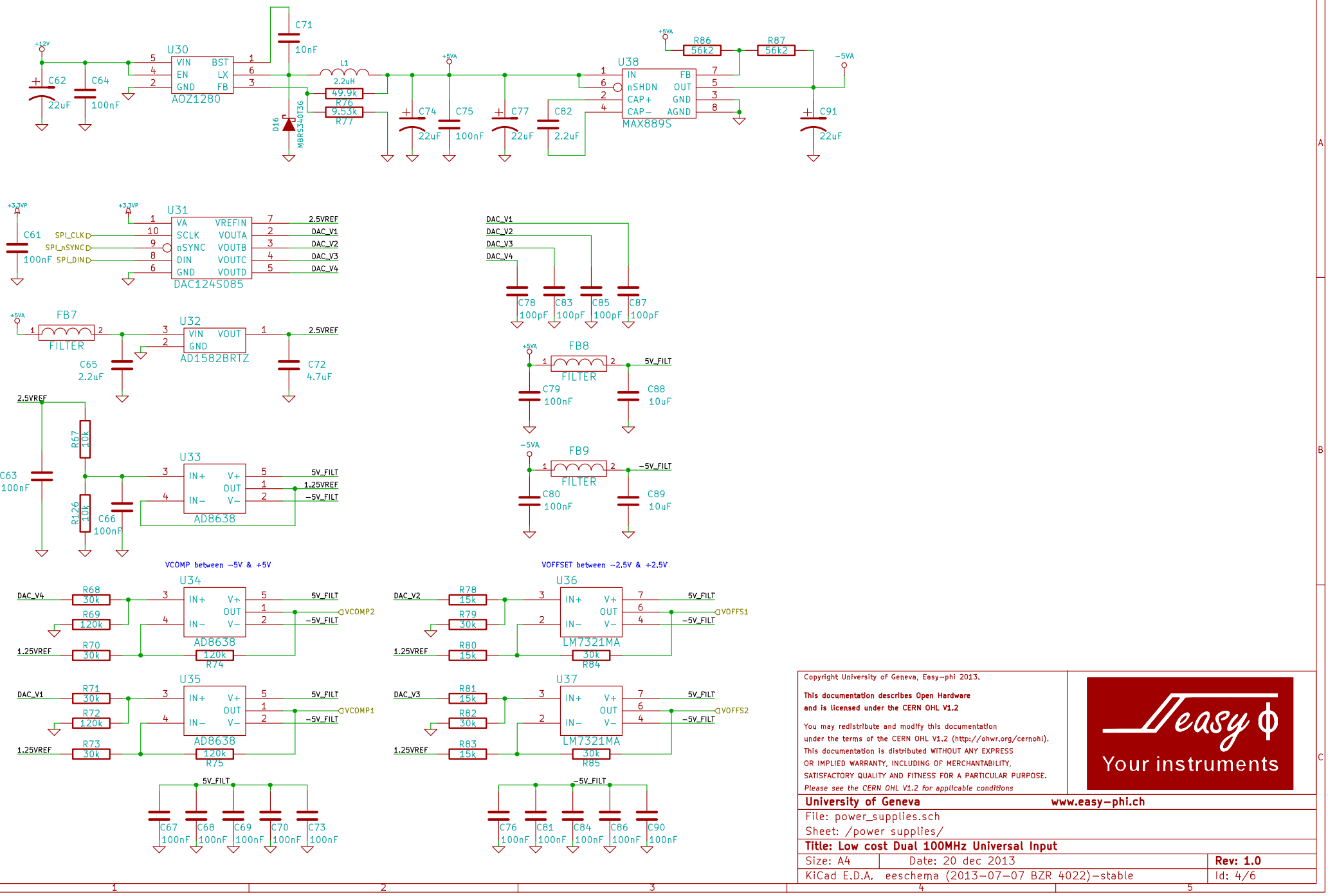
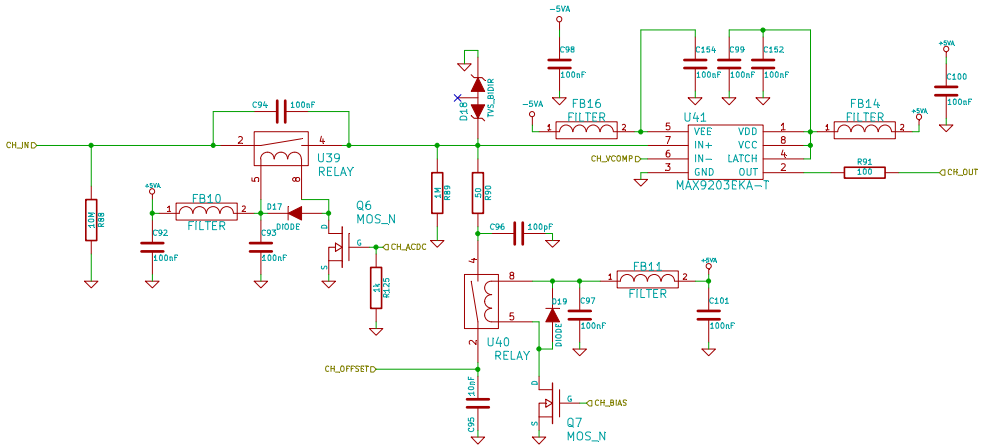
File: univinput_channel.sch	
Sheet: /channel A/	
Title: Low cost Dual 100MHz Universal Input	
Size: A3	Date: 20 dec 2013
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable	Id: 3/6

Rev: 1.0



Easy Φ Your instruments

University of Geneva	**www.easy−phi.ch**	
File: power_supplies.sch		
Sheet: /power supplies/		
Title: Low cost Dual 100MHz Universal Input		
Size: A4	Date: 20 dec 2013	**Rev: 1.0**
KiCad E.D.A. eeschema (2013−07−07 BZR 4022)−stable		Id: 4/6

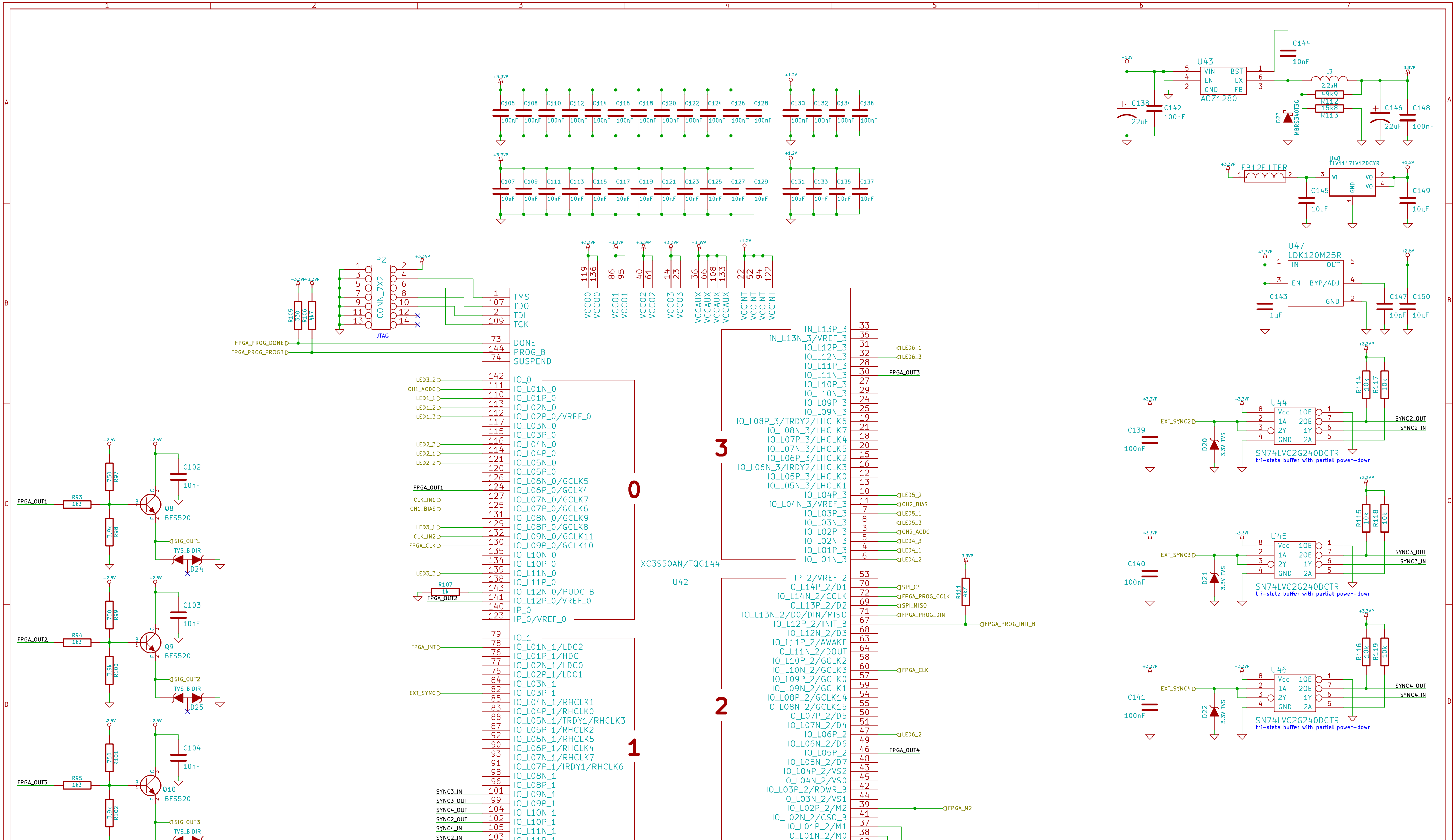


YES, WE NEED A WHOLE PAGE FOR THAT.

Easy ϕ Your instruments

University of Geneva	www.easy-phi.ch
File: univinput_channel.sch	
Sheet: /channel B/	
Title: Low cost Dual 100MHz Universal Input	
Size: A3	Date: 20 dec 2013
KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable	Id: 5/6

Rev: 1.0



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File: FPGA.sch

Sheet: /FPGA/

Title: Low cost Dual 100MHz Universal Input

Size: A3 Date: 20 dec 2013 Rev: 1.0

KiCad E.D.A. eeschema (2013-07-07 BZR 4022)-stable Id: 6/6