CMOS Image Sensor

HV7131R

MagnaChip Semiconductor Ltd

Version 1.7

Revision History

Revision	Issue Date	Comments
1.0	2001-November-6	Initial Creation
1.1	2002-April-12	Replaced ADC to 10-bit resolution Changed Package Specification Changed Pin Configuration
1.2	2002-December-24	Review datasheet & release
1.3	2002-December-30	Add I/R Reflow Condition added
1.4	2003-March-12	40 pin PKG. Drawing Revision
1.5	2003.May-29	Register Revision
1.6	2004 March-26	Electro-Optical Characteristic Revision
1.7	2004 June-18	Add Spectral Characteristics

CONTENTS

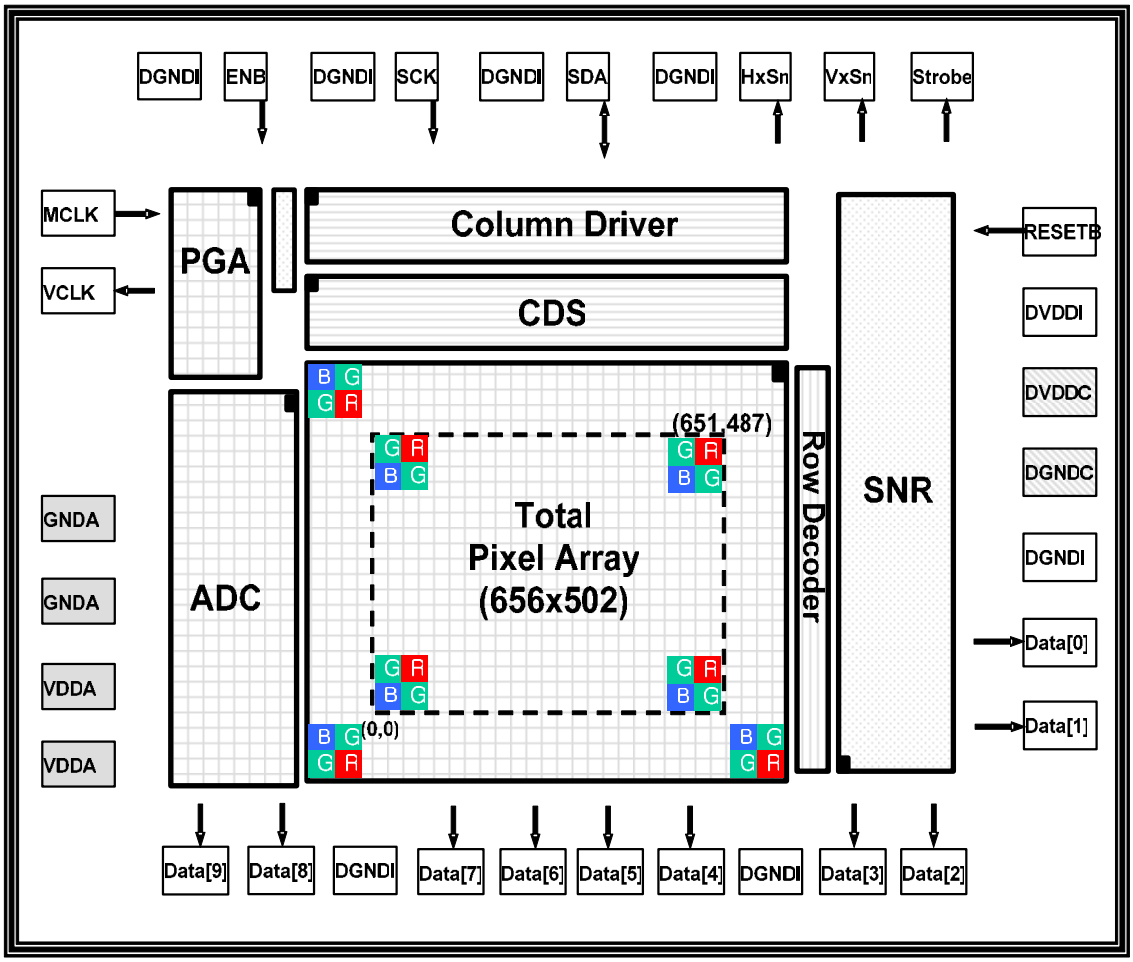
General Description

HV7131R is a highly integrated single chip CMOS color image sensor implemented by proprietary MagnaChip 0.30um CMOS sensor process realizing high sensitivity and wide dynamic range. Total pixel array size is 656x502, and 640x480 pixels are active. Each active pixel composed of 4 transistors, it has a micro-lens to enhance sensitivity. and it converts photon energy to analog pixel voltage. On-chip 10-bit Analog to Digital Converter (ADC) are configured to digitize analog pixel voltage, and on-chip Correlated Double Sampling (CDS) scheme reduces Fixed Pattern Noise (FPN) dramatically. Auto Black Level Compensation (ABLC) is using light blocking shield pixels which is placed top and bottom at core pixel to measure the black level and compensation.

Features

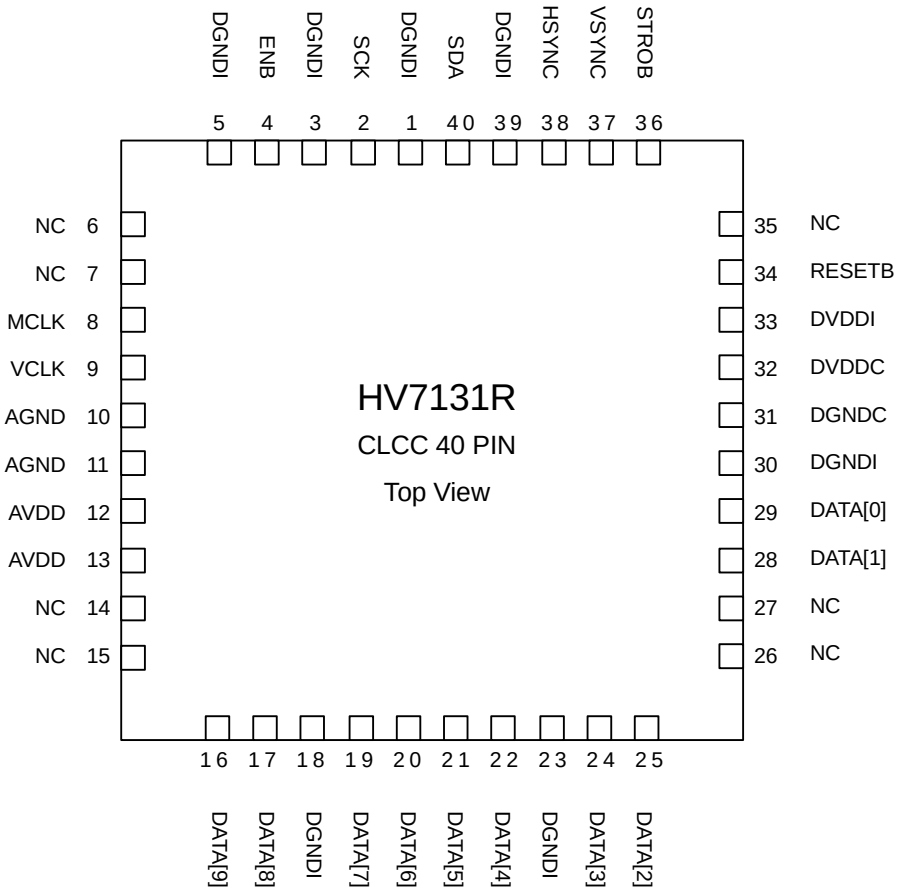
- VGA resolution
- 5.04μm x 5.04μm active square pixel
- 1/4.5 inch optical format
- Total Pixel Array : 656x502 / Active Pixel Array : 640x480
- Bayer RGB color filter array
- Micro-lens for high sensitivity
- Low Power Operation : Voltage Range : 2.6V - 3.0V
- Max Frame rate : 30 frame/s at 25Mhz Master Clock (VGA)
- Package Types : CLCC 40LD, COB(Chip-on-Board), COF(Chip-on-Flex)
- 10-bit Digital Image Signal Data Bus
- Low Fixed Pattern Noise by Correlated Double Sampling
- Controllable full function through standard IIC bus
- External Power Down
- Programmable Power Down mode
- Auto Black level compensation
- Flexible exposure time control
- Strobe Control Signal generation for frame capture mode
- Programmable Video Windowing
- Integrated 10bit Analog to Digital Conversion
- Programmable Frame Rate up to 30frame/sec

Block Diagram

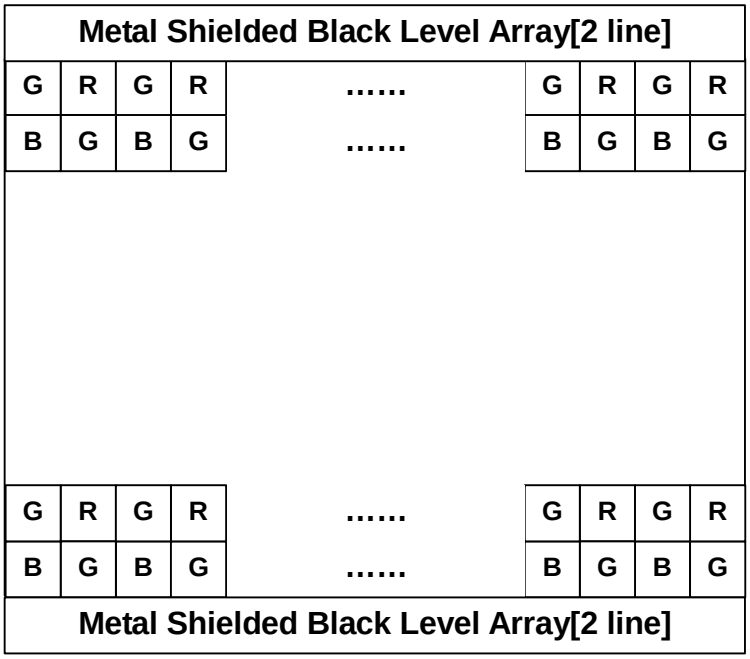


1. PGA : Programmable Gain Amplifier.
2. ADC : Analog to Digital Converter.
3. CDS : Correlated Double Sampling.
4. SNR : Sensor Control Digital Logic.

Pin Diagram



Pixel Array Structure



Pin Description

Pin	Type	Symbol	Description
1	G	DGNDI	Ground for I/O Buffer.
2	I	SCK	I2C Clock Input.
3	G	DGNDI	Ground for I/O Buffer.
4	I	ENB	ENB signal enables Sensor : High(Sensor Enabled), Low(Sensor Disabled, External Power Down)
5	G	DGNDI	Ground for I/O Buffer.
6~7	N	NC	No Connection.
8	I	MCLK	Master Input Clock.
9	O	VCLK	Video Output Clock.
10~11	G	AGND	Ground for Analog Block.
12~13	P	AVDD	Power for Analog Block.
14~15	N	NC	No Connection.
16	O	DATA[9]	Image Output Data Bit 9.
17	O	DATA[8]	Image Output Data Bit 8.
18	G	DGNDI	Ground for I/O Buffer.
19	O	DATA[7]	Image Output Data Bit 7.
20	O	DATA[6]	Image Output Data Bit 6.
21	O	DATA[5]	Image Output Data Bit 5.
22	O	DATA[4]	Image Output Data Bit 4.
23	G	DGNDI	Ground for I/O Buffer.
24	O	DATA[3]	Image Output Data Bit 3.
25	O	DATA[2]	Image Output Data Bit 2.
26~27	N	NC	No Connection.
28	O	DATA[1]	Image Output Data Bit 1.
29	O	DATA[0]	Image Output Data Bit 0.
30	G	DGNDI	Ground for I/O Buffer.
31	G	DGNDC	Ground for Internal Digital Block.
32	P	DVDDC	Power for Internal Digital Block.
33	P	DVDDI	Power for I/O Buffer.
34	I	RESETB	Sensor Reset, Low Active.
35	N	NC	No Connection.
36	O	STROBE	Strobe Signal Output.
37	O	VSYNC	Video Frame Synchronization signal. / Frame Start output VSYNC is active at start of image data frame.
38	O	HSYNC	Video Horizontal Line Synchronization signal. / Data is valid, when HSYNC is High.
39	G	DGNDI	Ground for I/O Buffer.
40	B	SDA	I2C Standard data I/O port.

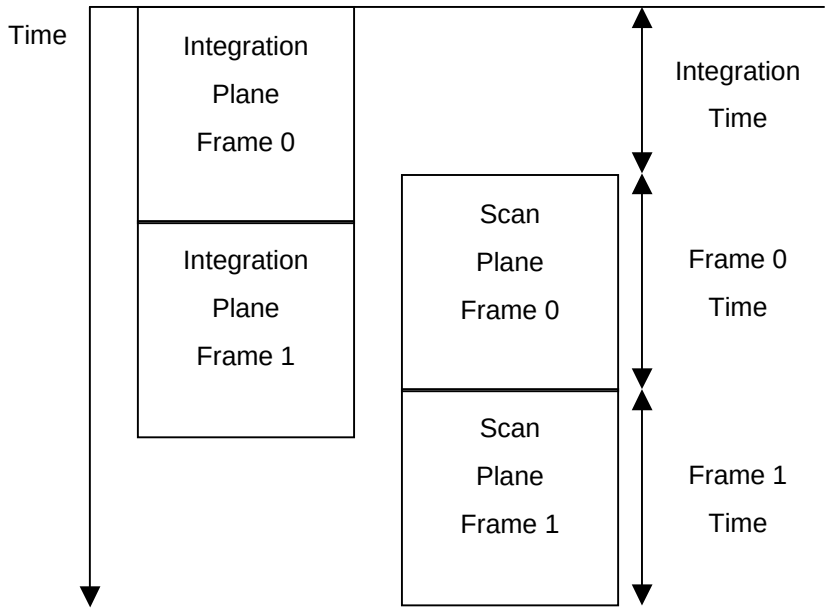
Functional Description

Pixel Architecture

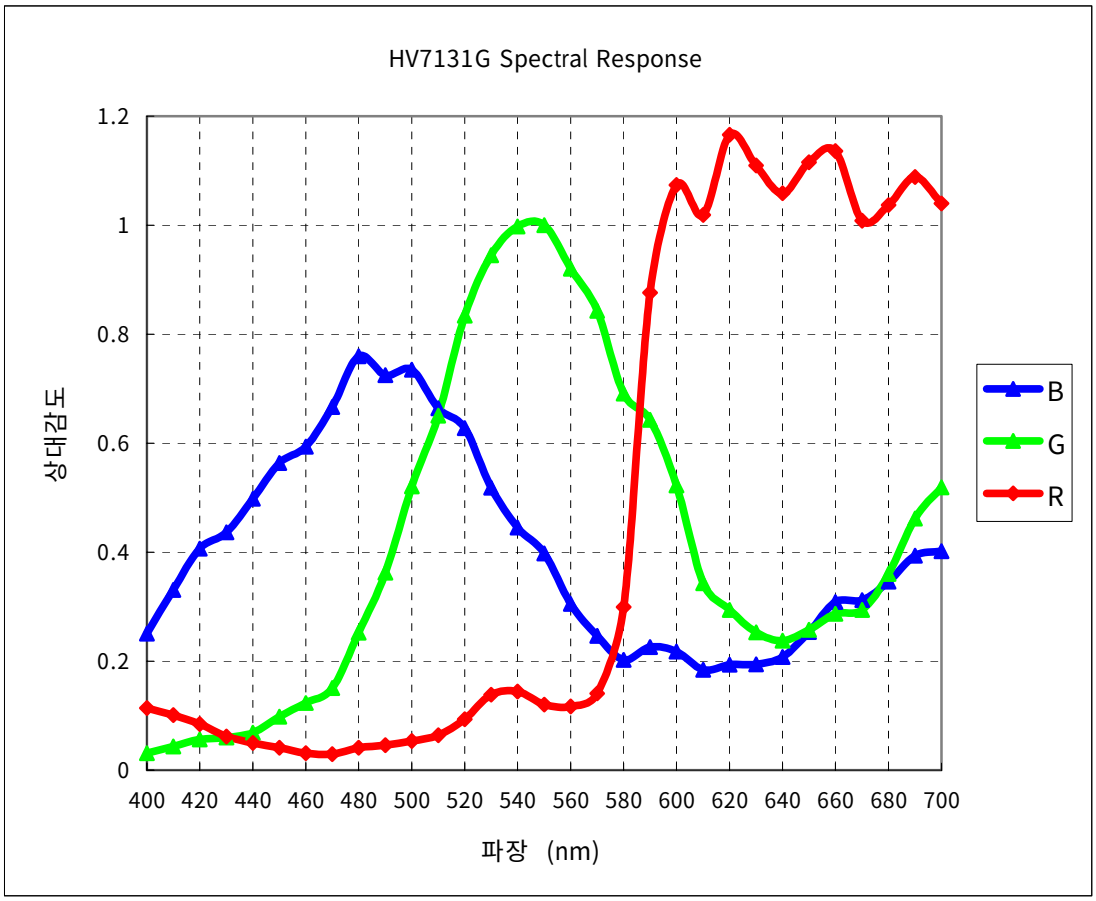
Pixel architecture is a 4-transistor NMOS pixel design. The additional use of a dedicated transfer transistor in the architecture reduces most of reset level noise so that fixed pattern noise is not visible. Furthermore, micro-lens is placed upon each pixel in order to increase fill factor so that high pixel sensitivity is achieved.

Sensor Imaging Operation

Imaging operation is implemented by the offset mechanism of integration domain and scan domain(rolling shutter scheme). First integration plane is initiated, and after the programmed integration time is elapsed, scan plane is initiated, then image data start being produced.



Spectral Characteristics



Register Description

Register	Symbol	Address	Default	Description
Device ID	DEVID	00h	02h	Product Identification, Revision Number.
Sensor Control A	SCTRA	01h	09h	ClkDiv[6:4], ABLCEn[3], PxlVs[2], XFlip[1], YFlip[0]
Sensor Control B	SCTRB	02h	01h	VCLK Disable[6], ADCPwDn[5], Black Mode[4], Sleep[3], VsHsEn[2], BLDataEn[1], StrobeEn[0]
Output Inversion	OUTIV	03h	00h	ByrDpcEn[6], ByrDpcTh[5:4], ClkHSC[3], InvVSC[2], InvHSC[1], InvVCLK[0]
Row Start Add Upper	RSAU	10h	00h	Row Start Address Upper Byte[8]
Row Start Add Lower	RSAL	11h	02h	Row Start Address Lower Byte[7:0]
Col. Start Add Upper	CSAU	12h	00h	Column Start Address Upper Byte[9:8]
Col. Start Add Lower	CSAL	13h	02h	Column Start Address Lower Byte[7:0]
Window Height Upper	WIHU	14h	01h	Window Height Upper Byte[8]
Window Height Lower	WIHL	15h	e2h	Window Height Lower Byte[7:0]
Window Width Upper	WIWU	16h	02h	Window Width Upper Byte[9:8]
Window Width Lower	WIWL	17h	82h	Window Width Lower Byte[7:0]
HBLANK Time Upper	HBLU	20h	00h	HBLANK Time Upper Byte[15:8].
HBLANK Time Lower	HBLL	21h	d0h	HBLANK Time Lower Byte[7:0].
VBLANK Time Upper	VBLU	22h	00h	VBLANK Time Upper Byte[15:8].
VBLANK Time Lower	VBLL	23h	08h	VBLANK Time Lower Byte[7:0].
Integration Time High	INTH	25h	06h	Integration Time [23:16]
Integration Time Middle	INTM	26h	5Bh	Integration Time [15:8]
Integration Time Low	INTL	27h	9ah	Integration Time [7:0]
Pre-amp Gain	PAG	30h	10h	Gain for Pre-amp (0.5~16.5 times with 8bit resolution) [7:0]
Red Color Gain	RCG	31h	10h	Gain for Red Pixel Read-out (0.5~2 times with 6bit resolution) [5:0]
Green Color Gain	GCG	32h	10h	Gain for Green Pixel Read-out (0.5~2 times with 6bit resolution [5:0]
Blue Color Gain	BCG	33h	10h	Gain for Blue Pixel Read-out (0.5~2 times with 6bit resolution [5:0]
Analog Bias Control A	ACTRA	34h	17h	CDS Bias [6:4], PGA Bias [3:0]
Analog Bias Control B	ACTRB	35h	7fh	Reset Clamp [7:4], ADC Bias [3:0]
Black Level Threshold	BLCTH	40h	ffh	Auto Black Level Pixel Threshold Value
Initial ADC Offset Red	ORedI	41h	7fh	Initial ADC Offset Red
Initial ADC Offset Green	OGrnI	42h	7fh	Initial ADC Offset Green
Initial ADC Offset Blue	OBluI	43h	7fh	Initial ADC Offset Blue

Device ID [DEVID : 00h : 02h]

7	6	5	4	3	2	1	0
Product ID				Revision Number			
0	0	0	0	0	0	1	0

High nibble represents Sensor Array Resolution, Low nibble represents Revision Number.

Sensor Control A [SCTRA : 01h : 09h]

7	6	5	4	3	2	1	0
Reserved	ClkDiv			ABLC En	PxlVs	X Flip	Y Flip
-	0	0	0	1	0	0	1

Clock Division

Device Input Master Clock(IMC) for internal use. Internal Divided Clock Frequency(DCF) is defined as Master Clock Frequency(MCF) divided by specified clock divisor. DCF is as follows

000 : DCF = MCLK, 001 : DCF = MCLK/2, 010 : DCF = MCLK/4

011 : DCF = MCLK/8, 100 : DCF = MCLK/16, 101 : DCF = MCLK/32

110 : DCF = MCLK/64, 111 : DCF = MCLK/128,

ABLC En

0 : Auto Black Level Compensation Disable

1 : Auto Black Level Compensation Enable

PxlVs

VBLANK unit : VBLANK Time value

0 : LCF unit

1 : SCF unit

X-Flip

0 : Normal.

1 : Image is horizontally flipped.

Y-Flip

0 : Normal.

1 : Image is vertically flipped.

Sensor Control B [SCTRB : 02h : 01h]

7	6	5	4	3	2	1	0
Reserved	VCLK	ADC PwDn	Black Mode	Sleep Mode	VsHsEn	BLDataEn	StrobeEn
-	0	0	0	0	0	0	1

VCLK

When this bit is high Video Output Clock(VCLK) Disable

ADCPwDn

When this bit is high ADC Block goes to Power Down

Black Mode

Black and White Mode : Red and Blue gain use the Green gain when this bit is set to high.

0 : Color Mode

1 : Black and White Mode

Sleep Mode

Software Power Down

0 : Software power down mode off.

1 : Software power down mode on.

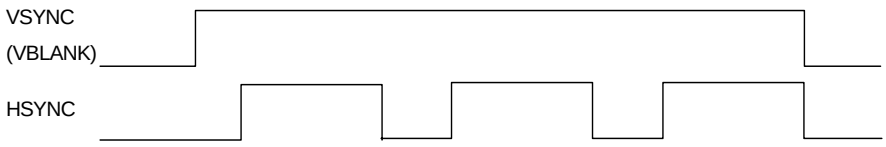
All internal digital block goes to sleep mode with this bit set to high

VsHsEn

HSYNC in VBLANK : VBLANK is equivalent to VSYNC, and HSYNC is the inversion of HBLANK, and this signal control whether HSYNC is active or not when VBLANK unit is LCF.

0 : There are no valid HSYNC signals during valid VSYNC signal.

1 : There are valid HSYNC signals during valid VSYNC signal. Number of valid HSYNC is same as number of VBLANK register when VSYNC unit is line unit. Do not use this mode when VSYNC unit is pixel unit



BLDataEn

Black Level Data Enable : HSYNC is generated for light-shielded pixels in 4 lines.

StrobeEn

Strobe Enable : When StrobEn is high STROBE pin will indicates when strobe light should be splashed in dark environment to get adequate lighted image

Output Inversion [OUTIV : 03h : X0h]

7	6	5	4	3	2	1	0
Reserved				Clocked HSYNC	VSYNC Inversion	HSYNC Inversion	VCLK Inversion
-	-	-	-	0	0	0	0

Clocked HSYNC

In HSYNC, VCLK is embedded, that is, HSYNC is toggling at VCLK rate during normal HSYNV time

VSYNC Inversion

VSYNC output polarity is inverted

HSYNC Inversion

HSYNC output polarity is inverted

VCLK Inversion

HSYNC output polarity is inverted

Row Start Address Upper [RSAU : 10h : X0h]

7	6	5	4	3	2	1	0

Reserved							RSA[8]
-	-	-	-	-	-	-	0

Row Start Address Low [RSAL : 11h : 02h]

7	6	5	4	3	2	1	0
RSA[7:0]							
0	0	0	0	0	0	1	0

Row Start Address register defines the row start address of image read out operation.

Column Start Address Upper [CSAU : 12h : X0h]

7	6	5	4	3	2	1	0
Reserved						CSA[9:8]	
-	-	-	-	-	-	0	0

Column Start Address Low [CSAL : 13h : 02h]

7	6	5	4	3	2	1	0
CSA[7:0]							
0	0	0	0	0	0	1	0

Column Start Address register defines the column start address of image read out operation.

Window Height Upper [WIHU : 14h : X1h]

7	6	5	4	3	2	1	0
Reserved							WIH[8]
-	-	-	-	-	-	-	1

Window Height Low [WIHL : 15h : e2h]

7	6	5	4	3	2	1	0
WIH[7:0]							
1	1	1	0	0	0	1	0

Window Height register defines the height of image read out operation.

Window Width Upper [WIWU : 16h : X2h]

7	6	5	4	3	2	1	0
Reserved						WIW[9:8]	
-	-	-	-	-	-	1	0

Window Width Low [WIWL : 17h : 82h]

7	6	5	4	3	2	1	0
WIW[7:0]							
1	0	0	0	0	0	1	0

Window Width register defines the width of image read out operation.

Horizontal Blanking Time Upper [HBLU : 20h : 00h]

7	6	5	4	3	2	1	0
HBLANK Time [15:8]							
0	0	0	0	0	0	0	0

Horizontal Blanking Time Low [HBLL : 21h : d0h]

7	6	5	4	3	2	1	0
HBLANK Time [7:0]							
1	1	0	1	0	0	0	0

HBLANK Time register defines data blank time between current line and next line by using Sensor Clock Period unit (1/SCF), and should larger then 208(d0h)

Vertical Blanking Time High [VBLU : 22h : 00h]

7	6	5	4	3	2	1	0
VBLANK Time[15:8]							
0	0	0	0	0	0	0	0

Vertical Blanking Time Low [VBLL : 23h : 08h]

7	6	5	4	3	2	1	0
VBLANK Time[7:0]							
0	0	0	0	1	0	0	0

VBLANK Time register defines active high duration of VSYNC output. Active high VSYNC indicates frame boundary between continuous frames For VSYNC-HSYNC timing relation in the frame transition, please refer to Frame Timing section

Integration Time High [INTH: 25h : 06h]

7	6	5	4	3	2	1	0
Integration Time [23:16]							
0	0	0	0	0	1	1	0

Integration Time Middle [INTM: 26h: 5bh]

7	6	5	4	3	2	1	0
Integration Time [15:8]							
0	1	0	1	1	0	1	1

Integration Time Low [INTL: 27h: 9ah]

7	6	5	4	3	2	1	0
Integration Time [7:0]							
1	0	0	1	1	0	1	0

Integration time value register defines the time during which active pixel element evaluates photon energy that is converted to digital data output by internal ADC processing. Integration time is equivalent to exposure time of general camera. So that integration time need to be increased in dark environment and decreased in bright environment. Maximum value of integration time is $(2^{24}-1)$ x sensor clock period (80ns, SCF 12.5MHz @ DCF 25MHz) = 1.34sec

Preamp Gain [PAG : 30h : 10h]

7	6	5	4	3	2	1	0
Preamp Gain							
0	0	0	1	0	0	0	0

Preamp Gain is common gain for R, G, B channel and used for auto exposure control. Programmable range is from 0.5X ~ 16.5X. Default gain is 1.5X.

Gain = 0.5 + B<7:0>/16

Red Color Gain [RCG : 31h : 10h]

7	6	5	4	3	2	1	0
Reserved		Red Color Gain					
-	-	0	1	0	0	0	0

Green Color Gain [GCG : 32h : 10h]

7	6	5	4	3	2	1	0
Reserved		Green Color Gain					
-	-	0	1	0	0	0	0

Blue Color Gain [BCG : 33h : 10h]

7	6	5	4	3	2	1	0
Reserved		Blue Color Gain					
-	-	0	1	0	0	0	0

There are three color gain registers for R, G, B pixels, respectively.
R, G, B color gain are used to amplify R, G, B channel. Programmable range is from 0.5X ~ 2.5X.

Default gain is 1X.

Gain = 0.5 + B<5:0>/32

Analog Bias Control A [ACTRA : 34h : 17h]

7	6	5	4	3	2	1	0
Reserved	CDS Bias			PGA Bias			
-	0	0	1	0	1	1	1

PGA Bias

Controls the amount of current in internal amplifier bias circuit to amplify pixel output effectively. The larger register value increases the amount of current

CDS Bias

Controls the amount of current in internal CDS bias circuit to amplify pixel output effectively. The larger register value increases the amount of current

Analog Bias Control B [ACTRB : 35h : 7fh]

7	6	5	4	3	2	1	0
Reset Clamp				ADC Bias			
0	1	1	1	1	1	1	1

Reset Level Clamp

Because extremely bright image like sun affects reset data voltage of pixel to lower, bright image is captured as black image in image sensor regardless of correlated double sampling. To solve this extraordinary phenomenon, we adopt the method to clamp reset data voltage. Reset Level Clamp controls the reset data voltage to prevent inversion of extremely bright image. The larger register value clamps the reset data level at highest voltage level. Default value is 7 to clamp the reset data level at appropriate voltage level.

ADC Bias

ADC Bias controls the amount of current in ADC bias circuit to operate ADC effectively. The larger register value increase the amount of current

Black Level Threshold [BLCTH : 40h : ffh]

7	6	5	4	3	2	1	0
Black Level Threshold							
1	1	1	1	1	1	1	1

The register specifies the maximum value, which determines whether light shielded pixel output, is valid. When light shielded pixel output exceeds this limit, the pixel is not accounted for black level calculation.

Initial ADC Offset Red [ORedI : 41h : 7fh]

7	6	5	4	3	2	1	0
Initial ADC Offset Red							
0	1	1	1	1	1	1	1

Initial ADC Offset Green [OGrnI : 42h : 7fh]

7	6	5	4	3	2	1	0
Initial ADC Offset Green							
0	1	1	1	1	1	1	1

Initial ADC Offset Blue [OBluI : 43h : 7fh]

7	6	5	4	3	2	1	0
Initial ADC Offset Blue							
0	1	1	1	1	1	1	1

* Update ADC Offset = - (Average – Initial ADC Offset)

These values are using black level compensation in active pixel.

Average value is measured and calculated at light shielded pixel with ABLCEn is active.

Frame Timing

For clear description of frame timing, clocks' acronym and relation are reminded in here again.

< Clock Acronym Definition >

MCF(Master Clock Frequency) : MCLK	DCF(Divided Clock Frequency) : MCF/Clock Division
SCF(Sensor Clock Frequency) : DCF/2	
VCF(Video Clock Frequency) : SCF	LCF(Line Clock Frequency) : 1/(HBLANJ Period + HSYNC Period (HBLANK Time + Video Width Time)

SCP(Sensor Clock Period) = 1/SCF, LCP(Line Clock Period) = 1/LCF

< Frame Time Calculation >

ABLC Time = 4LCP * (HBLANK + 512 SCP)

Core Frame Time = IDLE Slot + Video Height * LCP

Real Frame Time = Integration Time + VBLANK * LCP for Integration Time > Core Frame Time

= Core Frame Time + VBLANK * LCP for Integration Time <= Core Frame Time

HOLD Slot Time = Integration Time - Core Frame Time for Integration Time > Core Frame Time

= 0 for Integration Time <= Core Frame Time

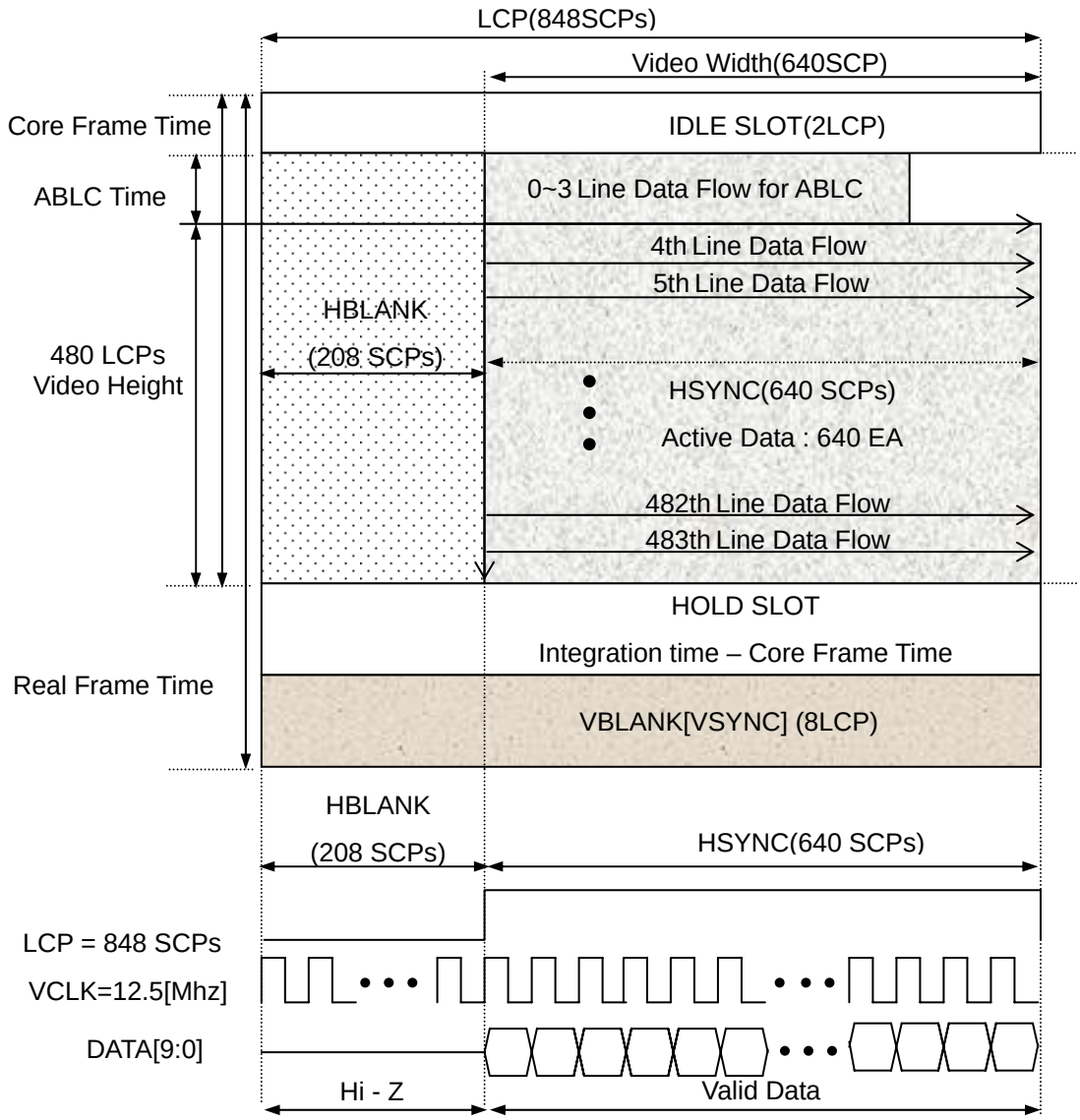
where IDLE Slot is 1LCP.

1. VGA size when Programmable Window is disabled and ABLC enable

VGA Frame Timing Related Parameters			
Master Clock Frequency(MCF)	25Mhz	Clock Division	MCF/1 = 25Mhz
Sensor Clock Frequency(SCF)	DCF/2 =12.5Mhz	Sensor Clock Period(SCP)	1/12.5Mhz = 80ns
HBLANK Value	208	VBLANK Value	8
VSYNC Mode	Line Mode	Line Clock Period(LCP)	848 SCPs
ABLC	Enable	Programmable Window	OFF

If Integration Time < Core Frame Time, Real Frame Time is
2(208 + 640)SCPs + 4(208 + 512)SCPs + 480(208 + 640)SCPs + 8(208 + 640)SCPs
= 418400 SCPs =418400 X 80ns = 33.47msec = 29.87fps
else Real Frame Time is
Integration Time * SCPs + 8 * (208 +640) SCPs.

HOLD SLOT in frame timing appears only if integration time is larger then core frame time

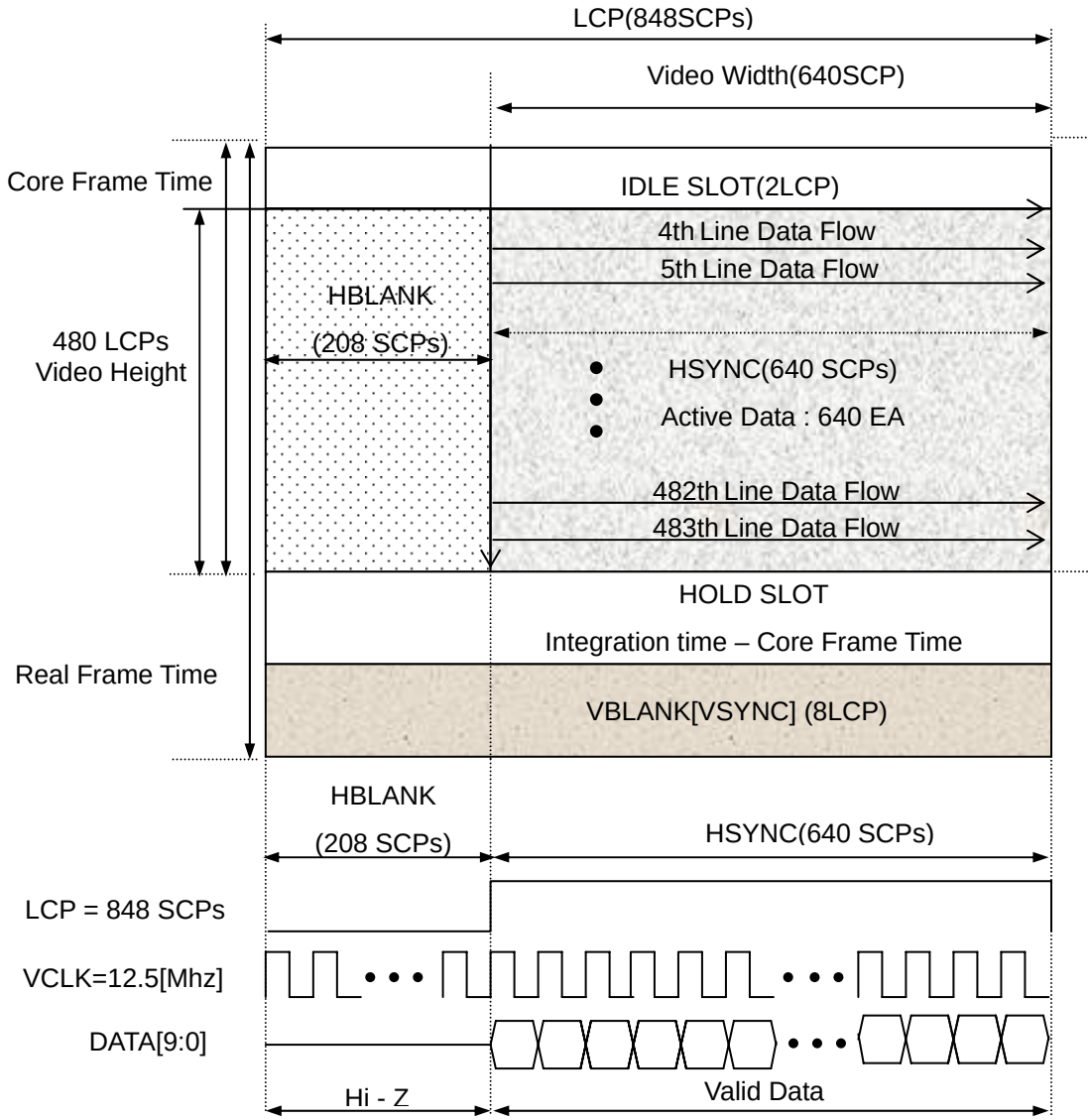


2. VGA size when Programmable Window is disabled and ABLC disable

VGA Frame Timing Related Parameters			
Master Clock Frequency(MCF)	25Mhz	Clock Division	MCF/1 = 25Mhz
Sensor Clock Frequency(SCF)	DCF/2 =12.5Mhz	Sensor Clock Period(SCP)	1/12.5Mhz = 80ns
HBLANK Value	208	VBLANK Value	8
VSYNC Mode	Line Mode	Line Clock Period(LCP)	848 SCPs
ABLC	Disable	Programmable Window	OFF

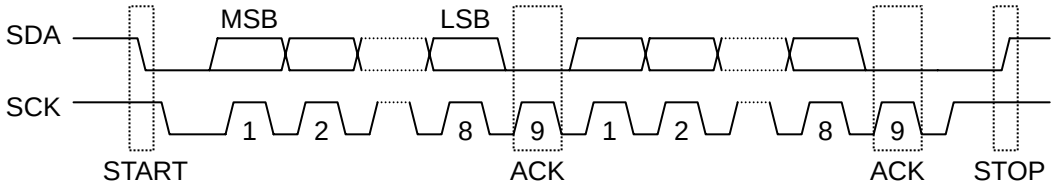
If Integration Time < Core Frame Time, Real Frame Time is
2(208 + 640)SCPs + 480(208 + 640)SCPs + 8(208 + 640)SCPs
= 415520 SCPs =415520 X 80ns = 33.24msec = 30fps
else Real Frame Time is
Integration Time * SCPs + 8 * (208 +640) SCPs.

HOLD SLOT in frame timing appears only if integration time is larger then core frame time



I2C Chip Interface

The serial bus interface consists of the SDA(serial data) and SCK(serial clock) pins. HV7131GR sensor can operate only as a slave. The SCK only controls the serial interface. However, MCLK should be supplied and RESET should be high signal during controlling the serial interface. The Start condition is that logic transition (High to Low) on the SDA pin while the SCK pin is at high. The Stop condition is that logic transition (Low to High) on the SDA pin while the SCK pin is at high. To generate Acknowledge signal, the Sensor drives the SDA low when the SCK is high. Every byte consists of 8 bits. Each byte transferred on the bus must be followed by an Acknowledge. The most significant bit of the byte should always be transmitted first.



Register Write Sequences

One Byte Write

S	22H	A	01H	A	03H	A	P
*1	*2	*3	*4	*5	*6	*7	*8

Set "Sensor Control A" register into Window mode

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 03H [Video Mode : CIF]

*7. Read: acknowledge from sensor

*8. Drive: I2C stop condition

Multiple Byte Write using Auto Address Increment

S	22H	A	10H	A	00H	A	64H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10

Set "HSYNC Blanking High/Low" register as 0064H with auto address increment

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit]

*3. Read: acknowledge from sensor

*4. Drive: 10H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: 00H [HSYNC Blanking High]

*7. Read: acknowledge from sensor

*8. Drive: 64H [HSYNC Blanking Low]

*9. Read: acknowledge from sensor

*10. Drive: I2C stop condition

Register Read Sequence

S	22H	A	01H	A	S	23H	A	13H	A	P
*1	*2	*3	*4	*5	*6	*7	*8	*9	*10	*11

Read "Sensor Control A" register from HV7131GR

*1. Drive: I2C start condition

*2. Drive: 22H(001_0001 + 0) [device address + R/W bit(be careful. R/W=0)]

*3. Read: acknowledge from sensor

*4. Drive: 01H [sub-address]

*5. Read: acknowledge from sensor

*6. Drive: I^2C start condition

*7. Drive: 23H(001_0001 + 1) [device address + R/W bit(be careful. R/W=1)]

*8. Read: acknowledge from sensor

*9. Read: Read “13H(Value of Sensor Control A) ” from sensor

*10. Drive: acknowledge to sensor. If there is more data bytes to read, SDA should be driven to low and data read states(*9, *10) is repeated. Otherwise SDA should be driven to high to prepare for the read transaction end.

*11. Drive: I2C stop condition

AC/DC Characteristics

Absolute Maximum Ratings

Symbol	Parameter	Units	Min.	Max.
Vdpp	Digital supply voltage	Volts	-0.3	7.0
Vapp	Analog supply voltage	Volts	-0.3	7.0
Vipp	Input signal voltage	Volts	-0.3	7.0
Top	Operating Temperature	°C	-10	50
Tst	Storage Temperature	°C	-30	80

Caution: Stresses exceeding the absolute maximum ratings may induce failure.

DC Operating Conditions

Symbol	Parameter	Units	Min.	Max.	Load[pF]	Notes
V_{dd}	Internal operation supply voltage	Volt	2.6	3.0		
V_{ih}	Input voltage logic "1"	Volt	2.0	3.0	6.5	
V_{il}	Input voltage logic "0"	Volt	0	0.8	6.5	
V_{oh}	Output voltage logic "1"	Volt	2.15		60	at Ioh = -1mA
V_{ol}	Output voltage logic "0"	Volt		0.4	60	
I_{oh}	Output High Current	mA		-4	60	
I_{ol}	Output Low Current	mA		4	60	
T_a	Ambient operating temperature	Celsius	-10	50		

AC Operating Conditions

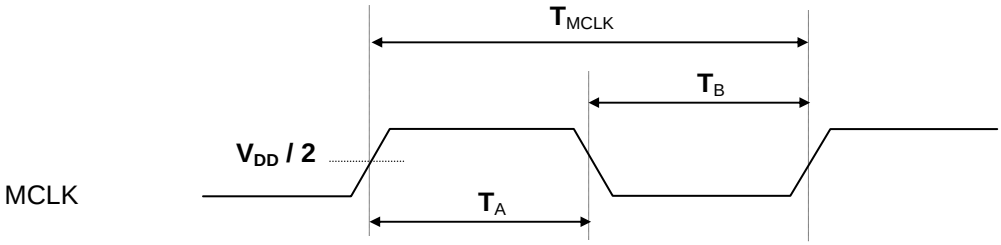
Symbol	Parameter	Max Operation Frequency	Units	Notes
MCLK	Main clock frequency	25	MHz	1
SCK	I^2C clock frequency	400	KHz	2
I_{NORMAL}	Power Consumption in Normal mode	30.953 @ 30fps, 25MHz	mA	
I_{DOWN_HARD}	Power Consumption in Hard Power Down mode	0.095 @ 25MHz	uA	
I_{DOWN_SOFT}	Power Consumption in Soft Power Down mode	208.815 @ 25MHz	uA	

1. MCLK may be divided by internal clock division logic for easy integration with high speed video codec.

2. SCK is driven by host processor. For the detail serial bus timing, refer to I2C chip interface section

Input AC Characteristics

MCLK Duty Cycle

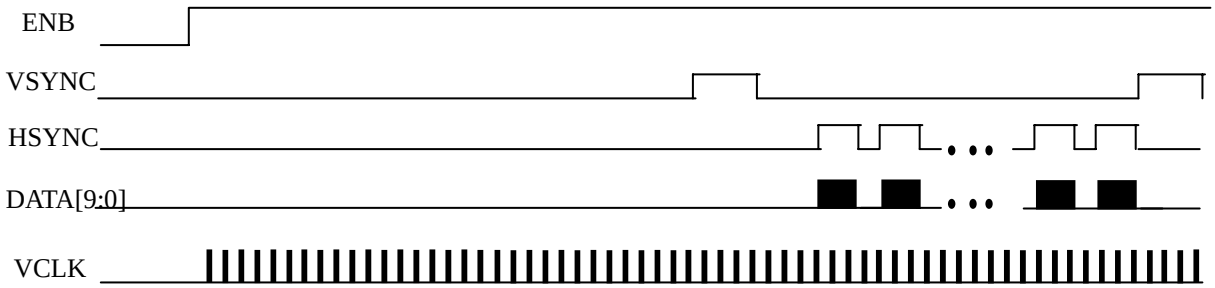


T_A = 40% ~ 60% of T_{MCLK}, T_B = 40% ~ 60% of T_{MCLK} , $T_A + T_B = T_{MCLK}$

ENB Timing

ENB pin enables sensor. If you set ENB pin to low, sensor goes to power down. Though sensor remains power down, you can program the registers by above IIC protocol. After ENB is changed to high, the registers that you set in power down are newly updated.

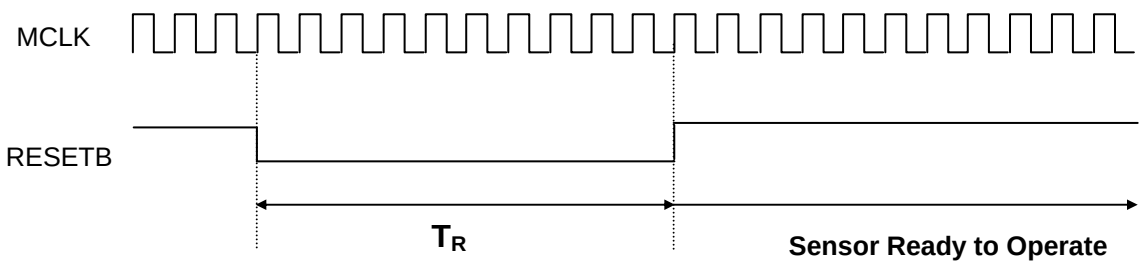
If you want software power down with ENB pin high, set sleep mode in SCTRB(02H)register.



RESETB Timing

RESETB pin initializes the registers to default value. When RESETB pin is low, initialization is done. HV7131GR is automatically reset the chip when power on.

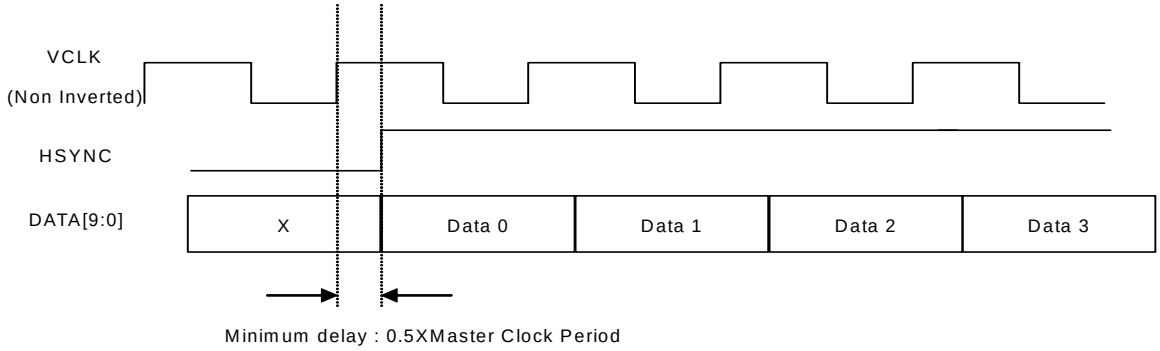
We recommend to initialize the registers by using RESETB pin. T_R: RESETB valid minimum time: 10 MCLK periods.



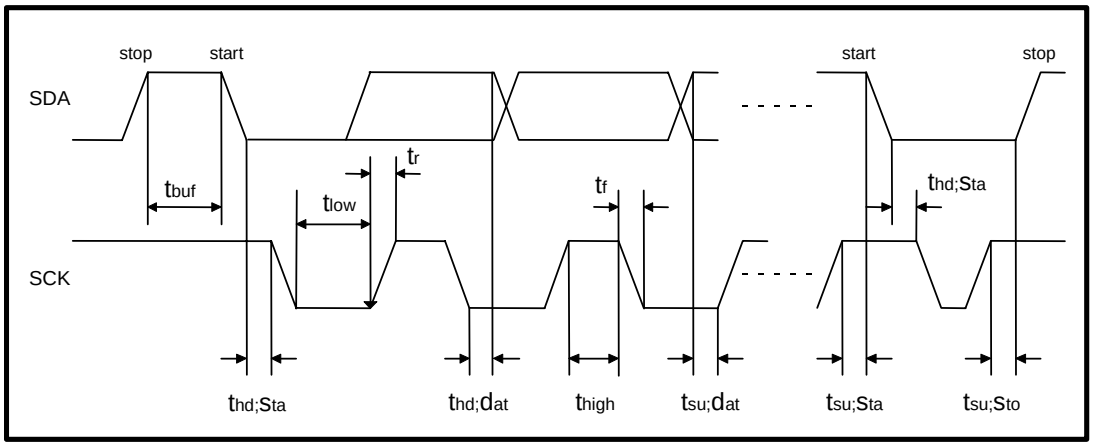
Output AC Characteristics

All output timing delays are measured with output load 60[pF]. Output delay includes the internal

clock path delay and output driving delay that changes in respect to the output load, the operating environment, and a board design. Due to the variable valid time delay of the output, RGB output signals DATA[9:0], HSYNC, and VSYNC may be latched in the negative edge of VCLK for the stable data transfer between the image sensor and video codec.



I2C Bus Timing



Parameter	Symbol	Min.	Max.	Unit
SCK clock frequency	f_{sck}	0	400	KHz
Time that I^2C bus must be free before a new transmission can start	t_{buf}	1.2	-	us
Hold time for a START	$t_{hd};s_{ta}$	1.0	-	us
LOW period of SCK	t_{low}	1.2	-	us
HIGH period of SCK	t_{high}	1.0	-	us
Setup time for START	$t_{su};s_{ta}$	1.2	-	us
Data hold time	$t_{hd};d_{at}$	1.3	-	us
Data setup time	$t_{su};d_{at}$	250	-	ns
Rise time of both SDA and SCK	t_r	-	250	ns
Fall time of both SDA and SCK	t_f	-	300	ns
Setup time for STOP	$t_{su};s_{to}$	1.2	-	us
Capacitive load of SCK/SDA	C_b	-	-	pf

Electro-Optical Characteristics

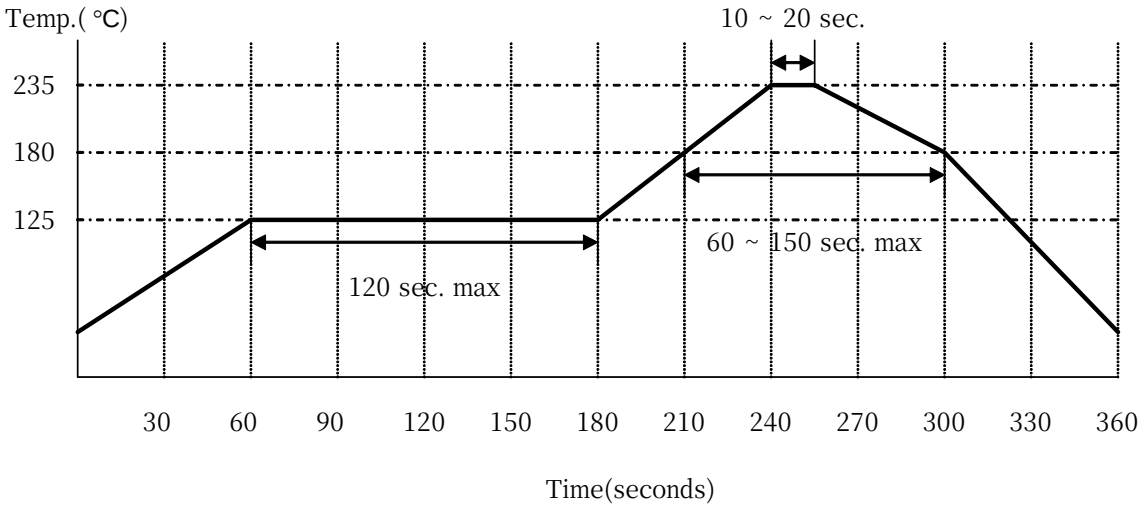
Parameter	Units	Min.	Typical	Max.	Note
Sensitivity	mV / lux·sec	2053.9	2480.482	3121.600	Green
		1356	1657.460	2093.500	Red
		1362.3	1656.700	2074.100	Blue
Dark Signal	code	0.000	10.728	31.990	
Output Saturation Signal	mV	1022.980	1023.000	1023.000	Green
		1022.990	1023.000	1023.000	Red
		1023.000	1023.000	1023.000	Blue
Power Consumption	mA	4.428	6.627	11.861	Dynamic DVDD
		19.572	24.326	30.009	Dynamic AVDD
Power Consumption	uA	0.000	0.005	27.130	Static DVDD
		0.000	0.090	29.610	Static AVDD
Power Consumption	uA	182.160	208.806	259.660	Sleep DVDD
		0.00	0.009	17.580	Sleep AVDD

- Color temperature of light source: 3200K / IR cut-off filter (CM-500S, 1mm thickness) is used.

Soldering

Infrared(IR) / Convection solder reflow condition

Parameter	Convection or IR/Convection
Average ramp-up rate(183°C to Peak)	3 °C / second max.
Preheat temperature 125(±25) °C	120 second max.
Temperature maintained above 183°C	60 – 150 second
Time within 235°C of actual peak temperature	10 – 20 second
Peak temperature range	(220 +5/-0) °C or (235 +5/-0) °C
Ramp-down rat	6°C / second max.
Time 25°C to peak temperature	6 minute



Package Specification

- **40 PIN CLCC**
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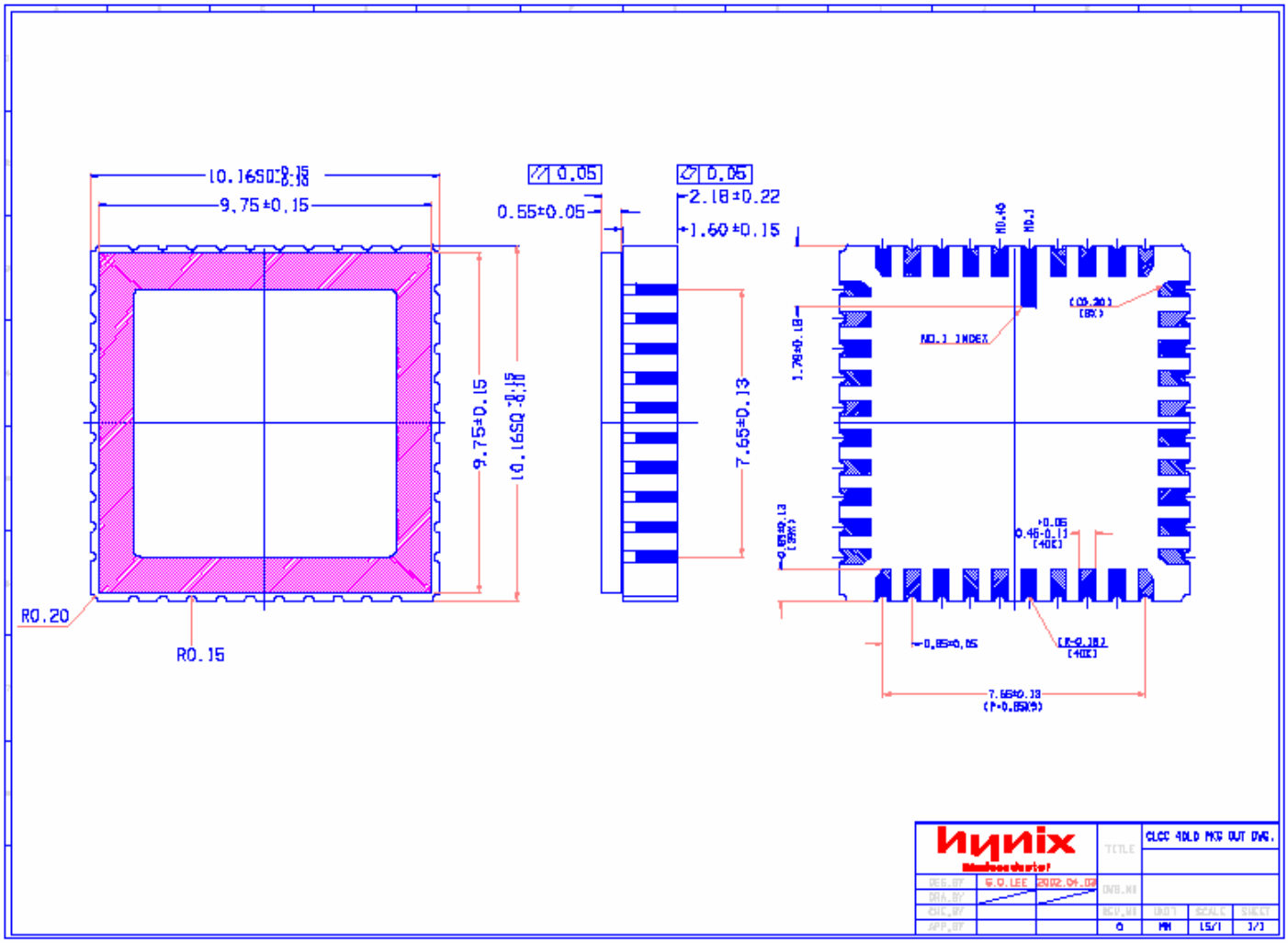

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MEMO

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