Ramaiah Institute of Technology (Autonomous Institute, Affiliated to VTU)

Department of CSE

Programme: B.E Term: Jan to May 2019
Course: Computer Organization Course Code: CS45

Activity V: Designing an ALU to perform arithmetic and logical functions using Logisim simulator.

Name: N.Sai Sanjith	Marks: /10	Date:
USN: 1MS18CS079	Signature of the Faculty:	

Objective: To simulate the working of Arithmetic and Logical Unit using simulator.

Simulator Description: Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolbar interface and simulation of circuits as you build them, it is simple enough to facilitate learning the most basic concepts related to logic circuits. With the capacity to build larger circuits from smaller sub circuits, and to draw bundles of wires with a single mouse drag, Logisim can be used (and is used) to design and simulate entire CPUs for educational purposes.

Activity to be performed by students:

```
List out the steps in designing ALU
  Nam: N Sai Sanjith
  PF 022812MI -: U2U
    LAB 5
     Steps in desiring ALU
     Step 1 Add 2 input pins
           Drop two East- Faving input is on the 4 bits each Label A and B. and ensure that each input is 4 bits
      Meps Add the adder subhator and
             Now we add the sub circuits cardier. Select the
                Circuits under the main project folder
       Nep 3:- Add the multipleners
         Thus bake on or more data injuly and generate a right output In Cogissim, multiplem icon and drop two of them into
          step 4: add controls
              Drop two pins on the colonies north-facing with I date bit Label othern O and I respectively
             Skps: add a splitter
               over, we add splitter in our corcuit that takes on the from the second multipleaser and gliller
                  to firmult to an DR gets for a 4 bit ALU
```

Now we add an OR gate after the gliter, which has a inputer. To the right of the OR gate add a NoT gate.

This averangement account by Jevo. The NoT gate following the OR gate actives their.

Finally add a single bit I'm after NoT gate to stove the Yexult. Lated It sero.

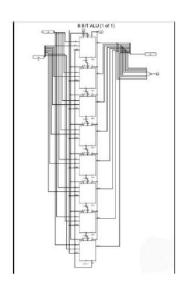
Step 7 Add a result pin for the MUN

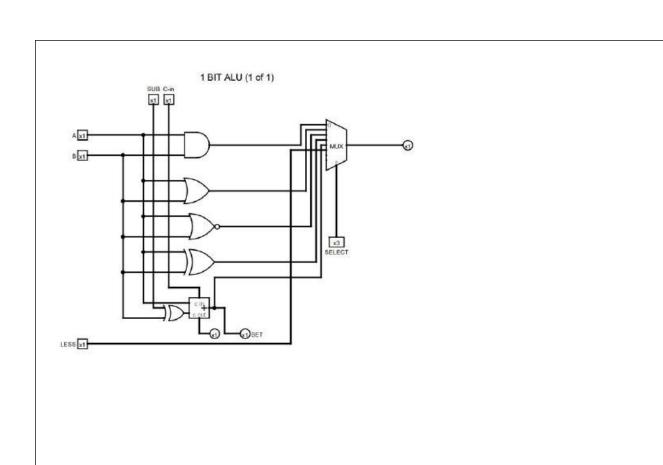
Luc handled the 32-005 coming ho on MUX, but we also

med to account for valid combination imputs from

A1B and the control Inputs.

Snapshots:





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Activity VI: Designing memory system using Logisim simulator.

Name: N.Sai Sanjith	Marks: /10	Date:
USN: 1MS18CS079	Signature of the Faculty:	

Objective: To simulate the writing operation on memory.

Simulator Description: Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolbar interface and simulation of circuits as you build them, it is simple enough to facilitate learning the most basic concepts related to logic circuits. With the capacity to build larger circuits from smaller sub circuits, and to draw bundles of wires with a single mouse drag, Logisim can be used (and is used) to design and simulate entire CPUs for educational purposes.

Activity to be performed by students:

List out the steps in designing memory system				

```
Name: N. Sai Sanjilly

USN: IMSIRCSO 79

Lab 6

Shep 1 add RAM

Celut a seperate load and slow operation for RAM

Shep 2: Add Counter

Correct Counter, clock and controller Badjer to the RAM

Step 3 Add TTY

To display the data

Shep 4 Add Randons Crementor

To generate different address Cacation Add in table and another Controller Duffer its the Random generator

Shep 5: Add Button

Connect Button to Cacater
```

Observations and Snapshots:

