Ramaiah Institute of Technology
(Autonomous Institute, Affiliated to VTU)

Department of CSE

Programme: B.E **Term: Jan to May 2019**
Course: Computer Organization **Course Code: CS45**

Activity V: Designing an ALU to perform arithmetic and logical functions using Logisim simulator.

Name: Laveesh Gupta	**Marks: /10**	**Date: 22/05/20**
USN: 1MS18CS062	**Signature of the Faculty:**	

Objective: To simulate the working of Arithmetic and Logical Unit using simulator.

Simulator Description: Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolbar interface and simulation of circuits as you build them, it is simple enough to facilitate learning the most basic concepts related to logic circuits. With the capacity to build larger circuits from smaller sub circuits, and to draw bundles of wires with a single mouse drag, Logisim can be used (and is used) to design and simulate entire CPUs for educational purposes.

Activity to be performed by students:

List out the steps in designing ALU

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Section – 4 'B'

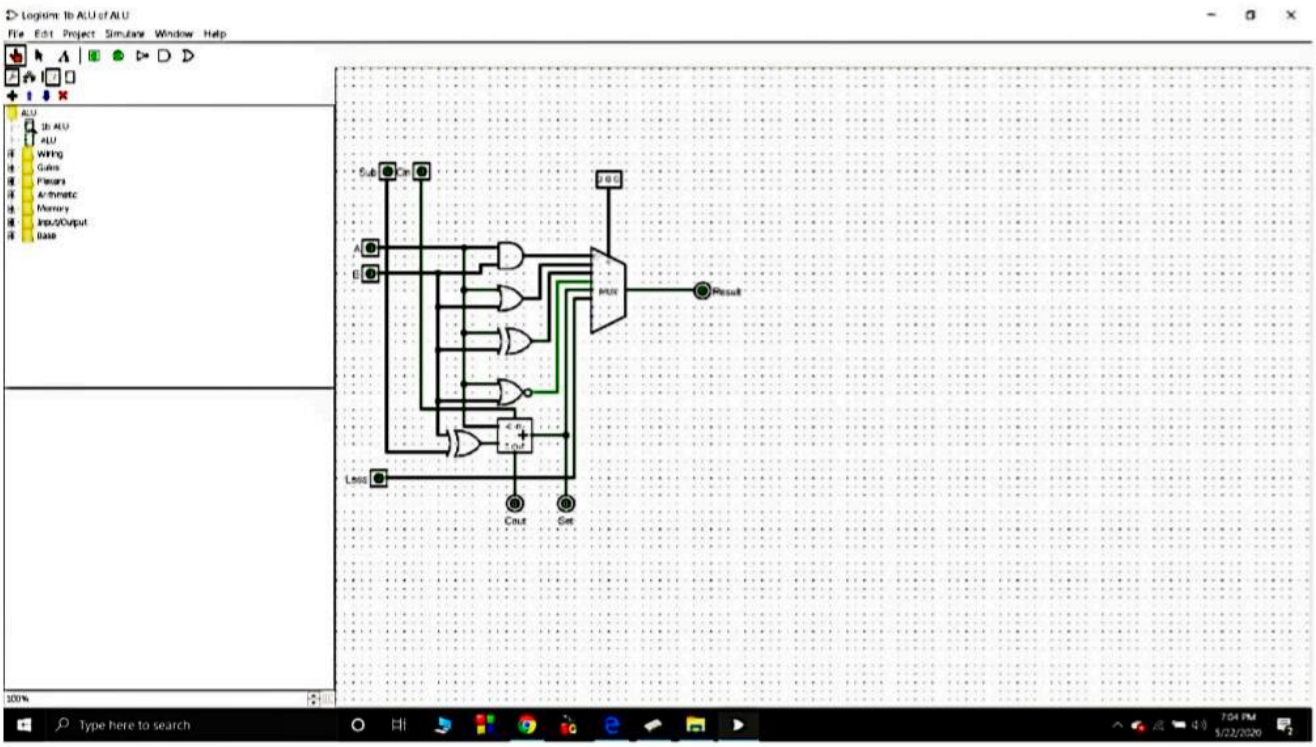
Computer Organization Lab

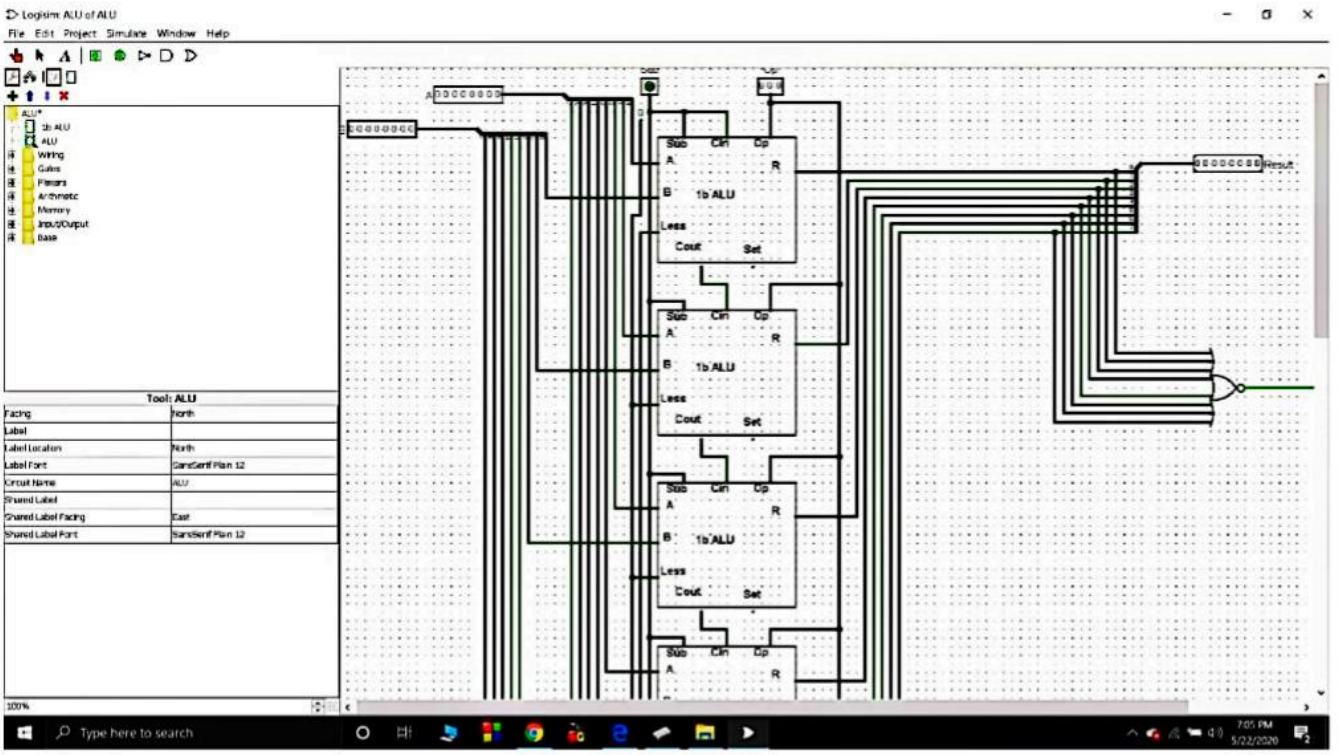
Activity V : Designing an ALU to perform arithmetic and logical functions using Logisim simulator.

List out the steps in designing ALU.

1. Add the two i/p pins. Name them A and B.
2. Add or, and, ex-or, nor gates and a 1-bit adder.
3. Connect the A's and B's of all the gates to their respective pins.
4. Add an output pin and name it Result.
5. Add a 1-bit multiplexer with select bits.
6. Connect outputs of all the gates to the mux.
7. Connect 3-bit input pin to mux.
8. Add i/p pin to C_{in}, and output pin to Cout.
9. Add an ex-or gate. Connect its o/p to Cout. The first i/p must be connected to B and the second to another i/p pin sub.
10. Add another i/p and name is Less. Connect it to the mux.
11. Add an ~~in~~ output pin and name it Set. Connect it to the multiplexer o/p of adder unit.

Snapshots :


Logisim: 1b ALU of ALU
File Edit Project Simulate Window Help
ALU
1b ALU
ALU
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Sub
Cin
A
B
MUX
Result
Less
Cout
Set
100%
Type here to search
7:04 PM
5/22/2020


Logisim: ALU of ALU
File Edit Project Simulate Window Help
ALU*
1b ALU
ALU
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Tool: ALU
Facing
North
Label
Label Location
North
Label Font
SansSerif Plain 12
Circuit Name
ALU
Shared Label
Shared Label Facing
East
Shared Label Font
SansSerif Plain 12
100%
Sub
Cin
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Cout
Set
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5/22/2020

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Activity VI: Designing memory system using Logisim simulator.

Name: Laveesh Gupta	**Marks: /10**	**Date: 22/05/20**
USN: 1MS18CS062	**Signature of the Faculty:**	

Objective: To simulate the writing operation on memory.

Simulator Description: Logisim is an educational tool for designing and simulating digital logic circuits. With its simple toolbar interface and simulation of circuits as you build them, it is simple enough to facilitate learning the most basic concepts related to logic circuits. With the capacity to build larger circuits from smaller sub circuits, and to draw bundles of wires with a single mouse drag, Logisim can be used (and is used) to design and simulate entire CPUs for educational purposes.

Activity to be performed by students:

List out the steps in designing memory system

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Section — 4 'B'

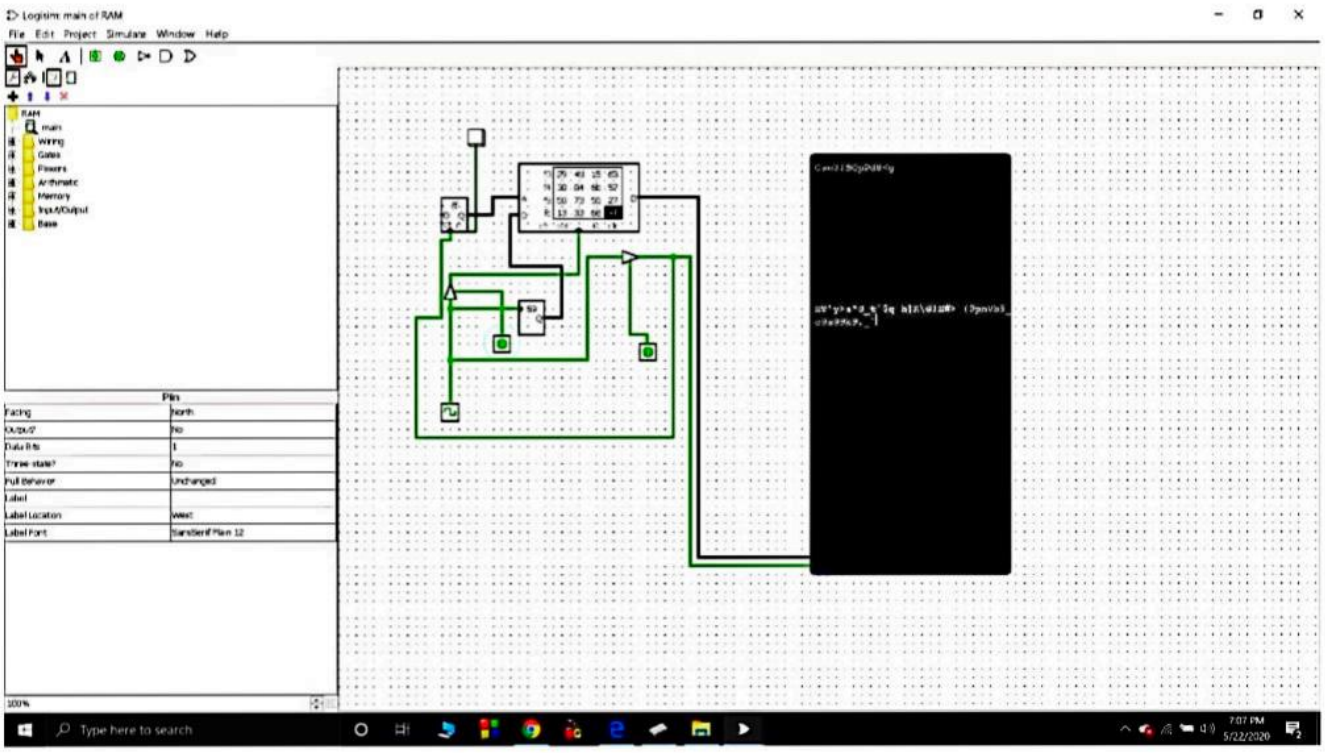
Computer Organization Lab

Activity VI : Designing memory system using Logisim simulator.

List out the steps in designing memory system.

1. Add a RAM with separate load and store selected.
2. Add a counter and connect Q to A of the RAM.
3. Add a controller buffer and connect its o/p to the RAM.
4. Add a clock and connect to the i/p of the buffer.
5. Add a TTY unit and with 32 rows and columns. Make the connections with RAM.
6. Add a 7-bit random number generator, connect Q to D.
7. Add another controlled buffer, connect to TTY. Also add an i/p pin to the buffer.
8. Connect the output of the second buffer to ~~its~~ the counter.
9. Connect a button to the counter.

Snapshot :


Logisim main of RAM
File Edit Project Simulate Window Help
RAM
main
Wiring
Gates
Plexers
Arithmetic
Memory
Input/Output
Base
Pin
Facing
north
Output?
no
Data Bits
1
Three-state?
no
Pull Behavior
Unchanged
Label
Label Location
west
Label Font
SansSerif Plain 12
100%
Type here to search
7:07 PM
5/22/2020

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Activity VII: To simulate advantages of using pipeline technique in executing a program.

Name: Laveesh Gupta	**Marks: /10**	**Date: 22/05/20**
USN: 1MS18CS062	**Signature of the Faculty:**	

Objective: To learn and analyze the performance of the CPU by overlapping of instructions using CPUOS-SIM simulator.

Simulator Used: CPUOS-SIM is a software development environment for the simulation of simple computers. It was developed by Dale Skrien to help users to understand computer architectures.

Modern CPU's contain several semi-independent circuits involved in decoding and executing each machine instruction. Separate circuit elements perform each of these typical steps:

- Fetch the next instruction from memory into an internal CPU register.
- Decode the instruction to determine which function sub-circuits it requires.
- Read any input operands required from high-speed registers or directly from memory.
- Execute the operation using the selected sub-circuits.
- Write any output results to high-speed registers or directly to memory.

Separate sections of the CPU circuitry are used for each of these steps. This allows these circuit sections to be arranged into a sequential pipeline, with the output of one step feeding into the next step.

Activity to be performed by students:

With diagram demonstrate the execution of the following instructions using pipelining technique.

```
lw   $10,20($1)
sub   $11, 42, $3
add  $12, $3, $4
lw   $13, 24($1)
add  $14, $5, $6
```

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USN - 1MS18CS062

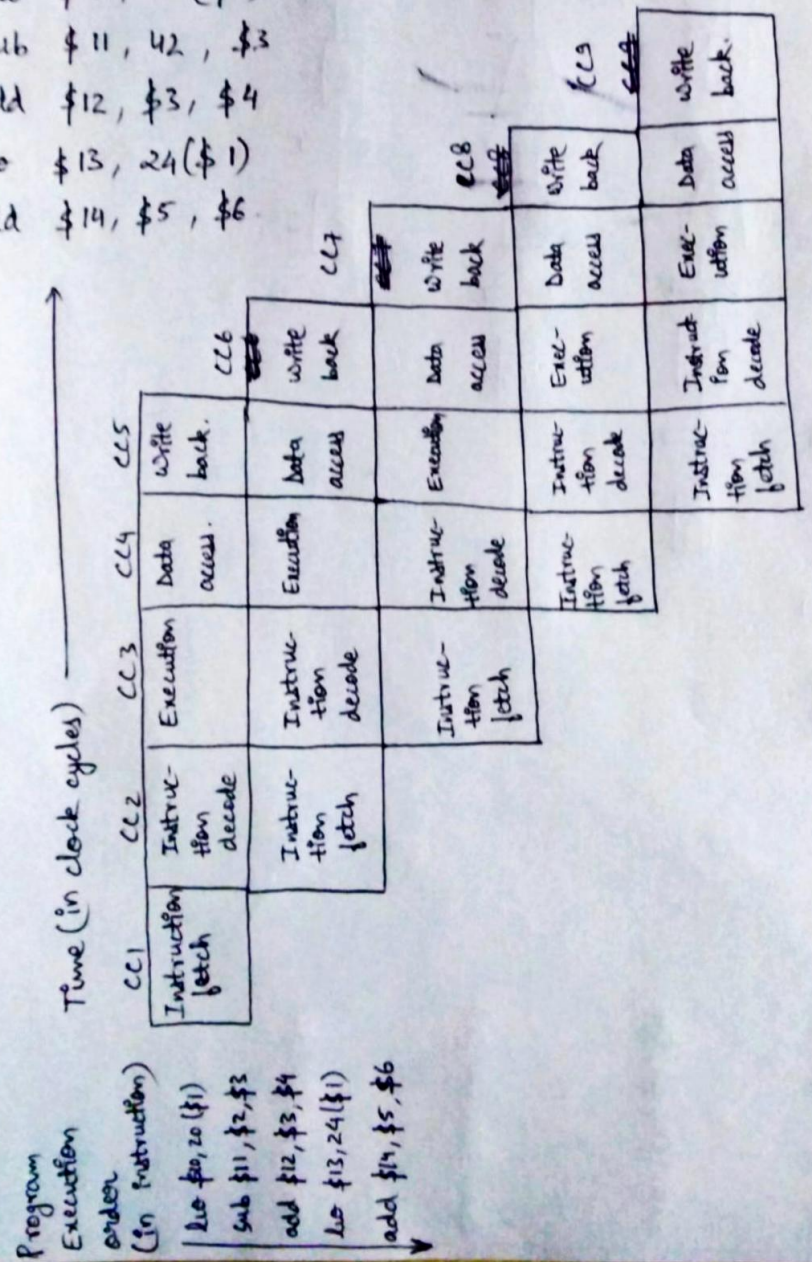
Section - 4 'B'

Computer Organization Lab

Activity VII : To simulate advantages of using pipeline technique in executing a program.

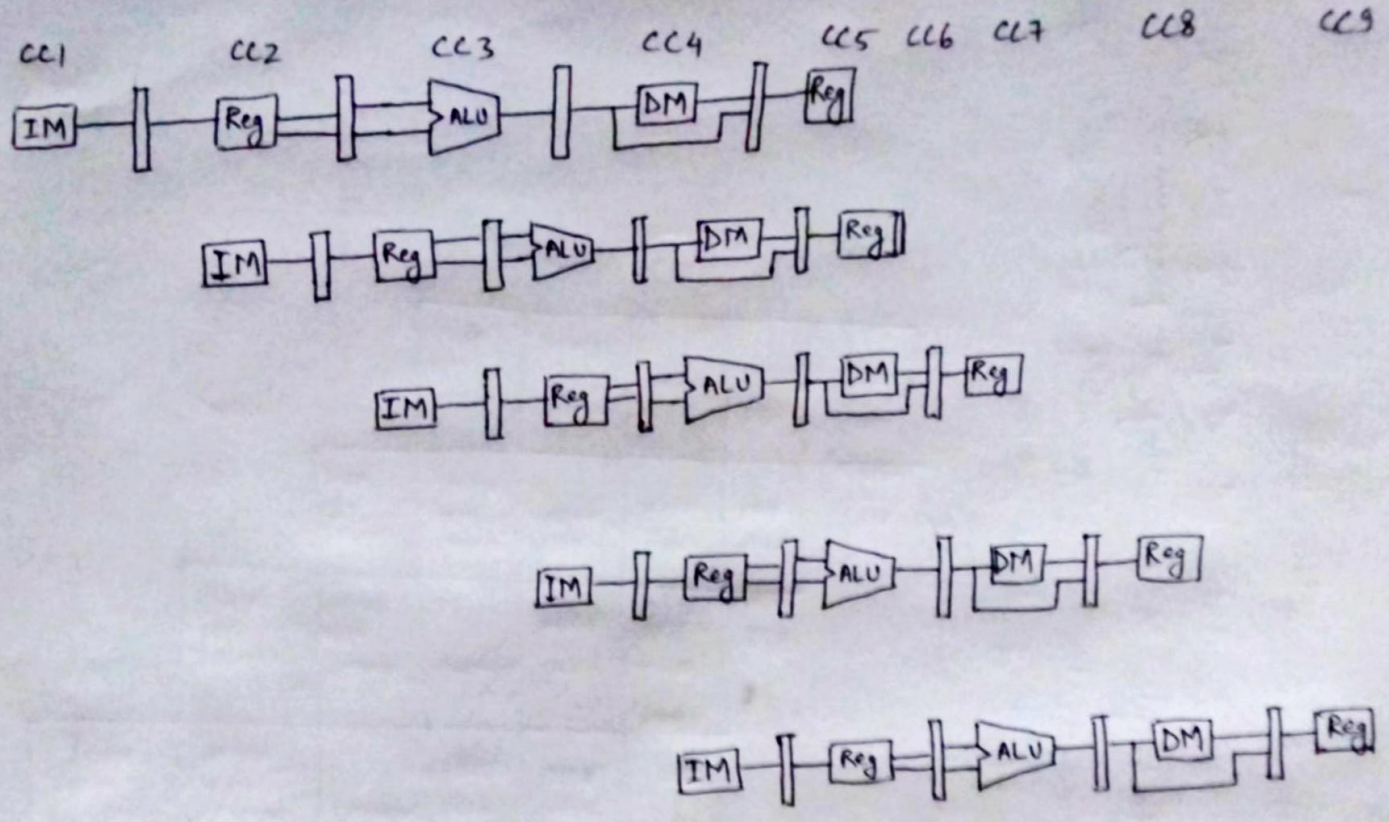
With diagram demonstrate the execution of the following instructions using pipelining technique.

lw $10, 20($1)
sub $11, 42, $3
add $12, $3, $4
lw $13, 24($1)
add $14, $5, $6



Program Execution order (in instruction)

Time (in clock cycles) →



Observations and Snapshots: Take the snap shot of CPU statistics and pipeline design.