Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name: TUSHAR Y S	SRN: PES1UG19CS545	Section I

Week#____1_____Program Number: ____1___

Title of the Program

Write an ALP using ARM instruction set to add and subtract two 32 bit numbers .Both numbers are in registers.

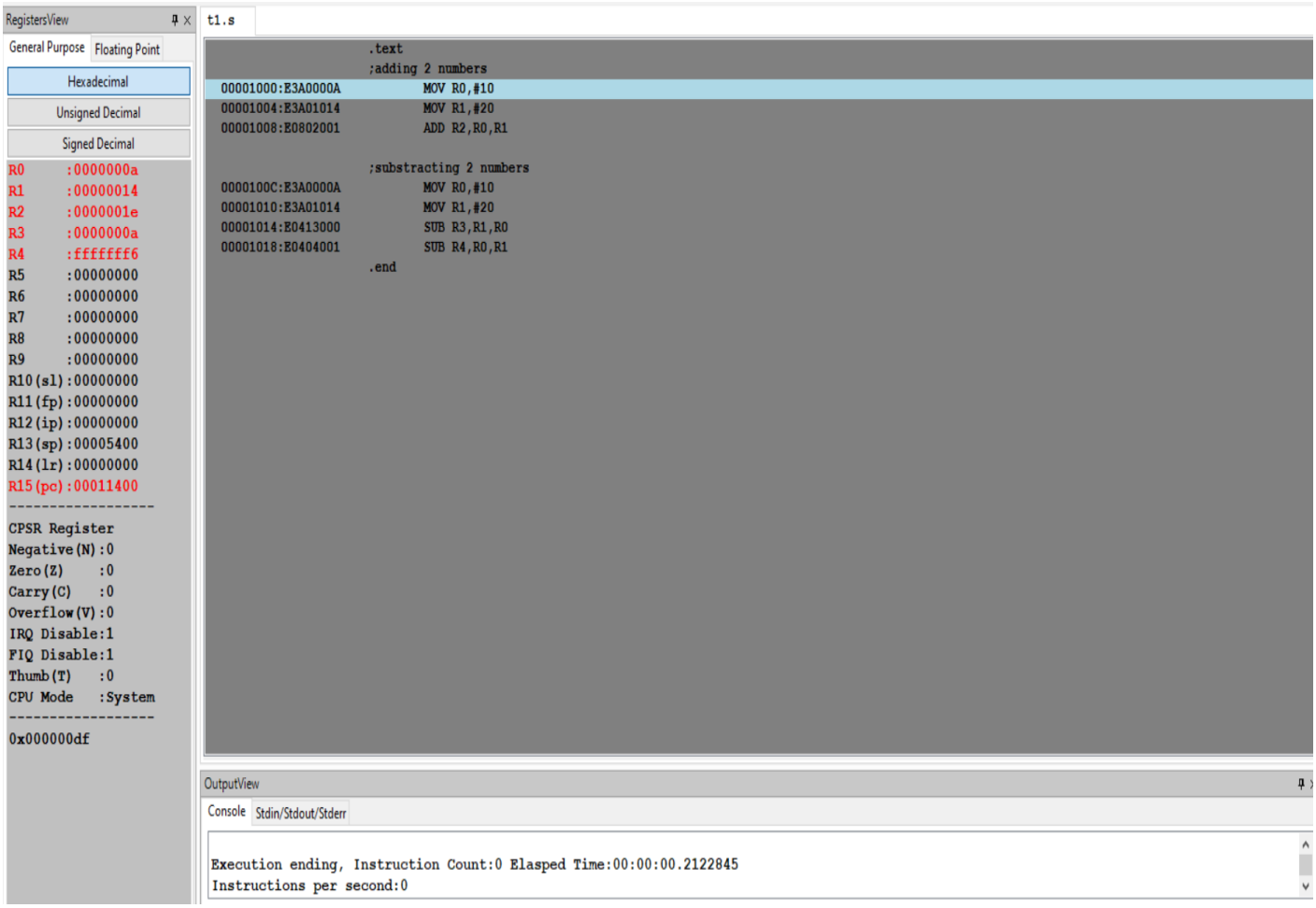
ARM Assembly code:

```
.text
;adding 2 numbers
    MOV R0,#10
    MOV R1,#20
    ADD R2,R0,R1

;substracting 2 numbers
```

```
        MOV R0,#10
        MOV R1,#20
        SUB R3,R1,R0
        SUB R4,R0,R1
.end
```

Output:

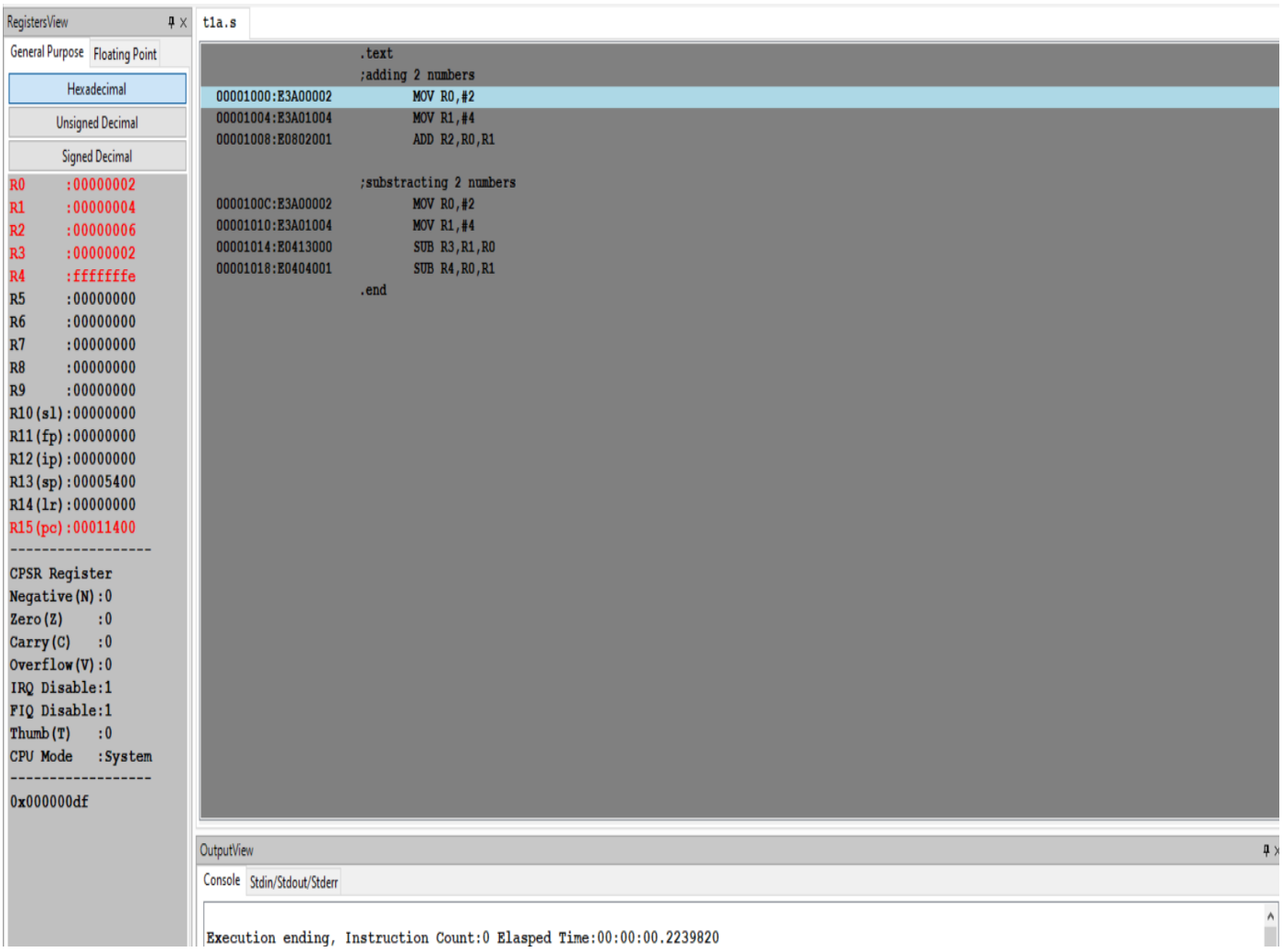


Test case:

```
.text
;adding 2 numbers
        MOV R0,#2
        MOV R1,#4
        ADD R2,R0,R1

;substracting 2 numbers
        MOV R0,#2
        MOV R1,#4
        SUB R3,R1,R0
        SUB R4,R0,R1
.end
```

Output:


RegistersView
General Purpose
Floating Point
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :00000002
R1 :00000004
R2 :00000006
R3 :00000002
R4 :fffffffe
R5 :00000000
R6 :00000000
R7 :00000000
R8 :00000000
R9 :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00011400
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
t1a.s
.text
;adding 2 numbers
00001000:E3A00002 MOV R0,#2
00001004:E3A01004 MOV R1,#4
00001008:E0802001 ADD R2,R0,R1
;substracting 2 numbers
0000100C:E3A00002 MOV R0,#2
00001010:E3A01004 MOV R1,#4
00001014:E0413000 SUB R3,R1,R0
00001018:E0404001 SUB R4,R0,R1
.end
OutputView
Console
Stdin/Stdout/Stderr
Execution ending, Instruction Count:0 Elasped Time:00:00:00.2239820

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4th Semester, Academic Year 2020-21

Date:

Name: TUSHAR Y S	SRN: PES1UG19CS545	Section I

Week#____1_____ Program Number: ____2___

Title of the Program

Write an ALP to demonstrate logical operations. All operands are in registers.

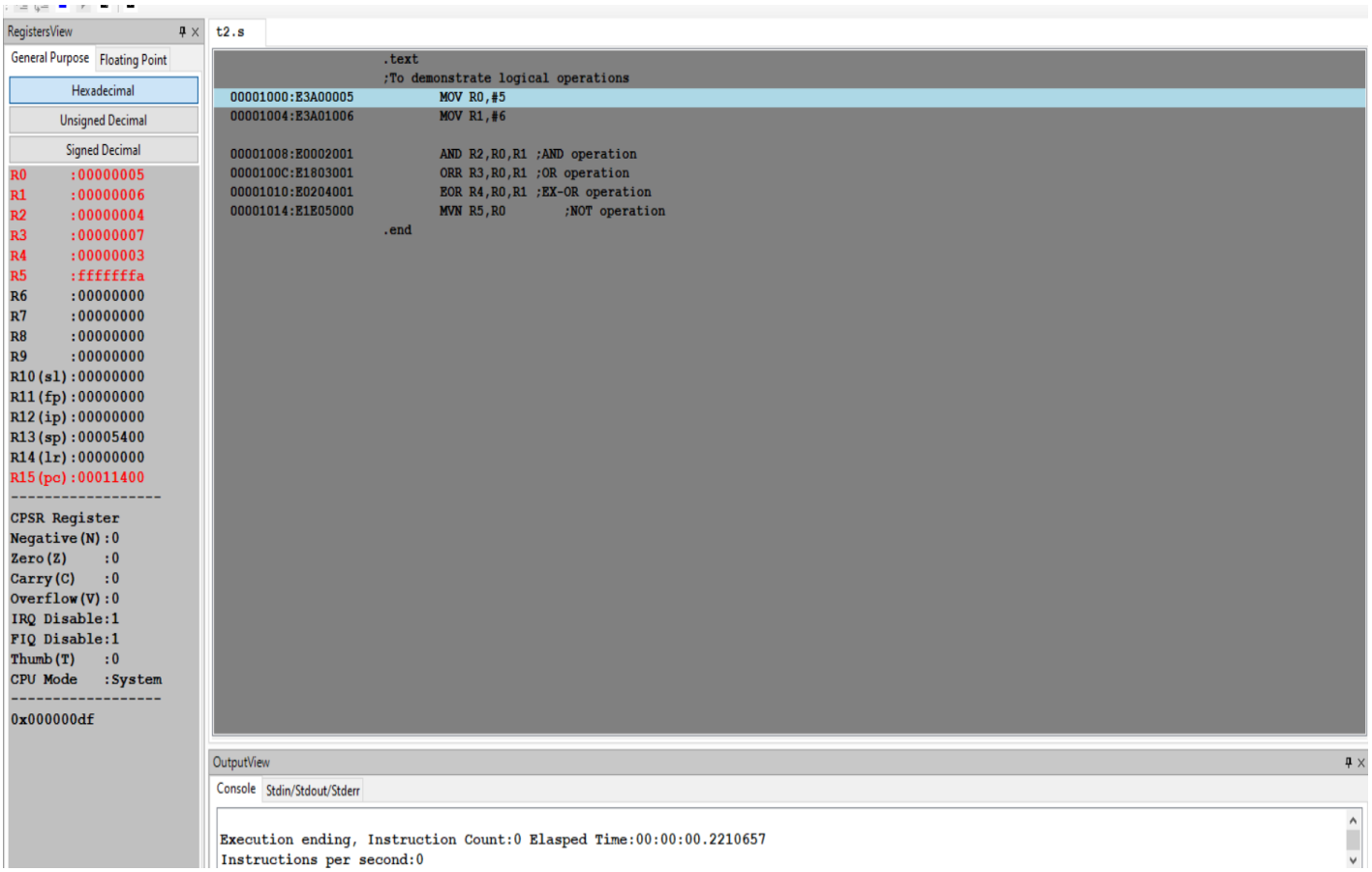
ARM Assembly Code:

```
.text
;To demonstrate logical operations
    MOV R0,#5
    MOV R1,#6

    AND R2,R0,R1 ;AND operation
    ORR R3,R0,R1 ;OR operation
    EOR R4,R0,R1 ;EX-OR operation
```

```
        MVN R5,R0      ;NOT operation
.end
```

Output:

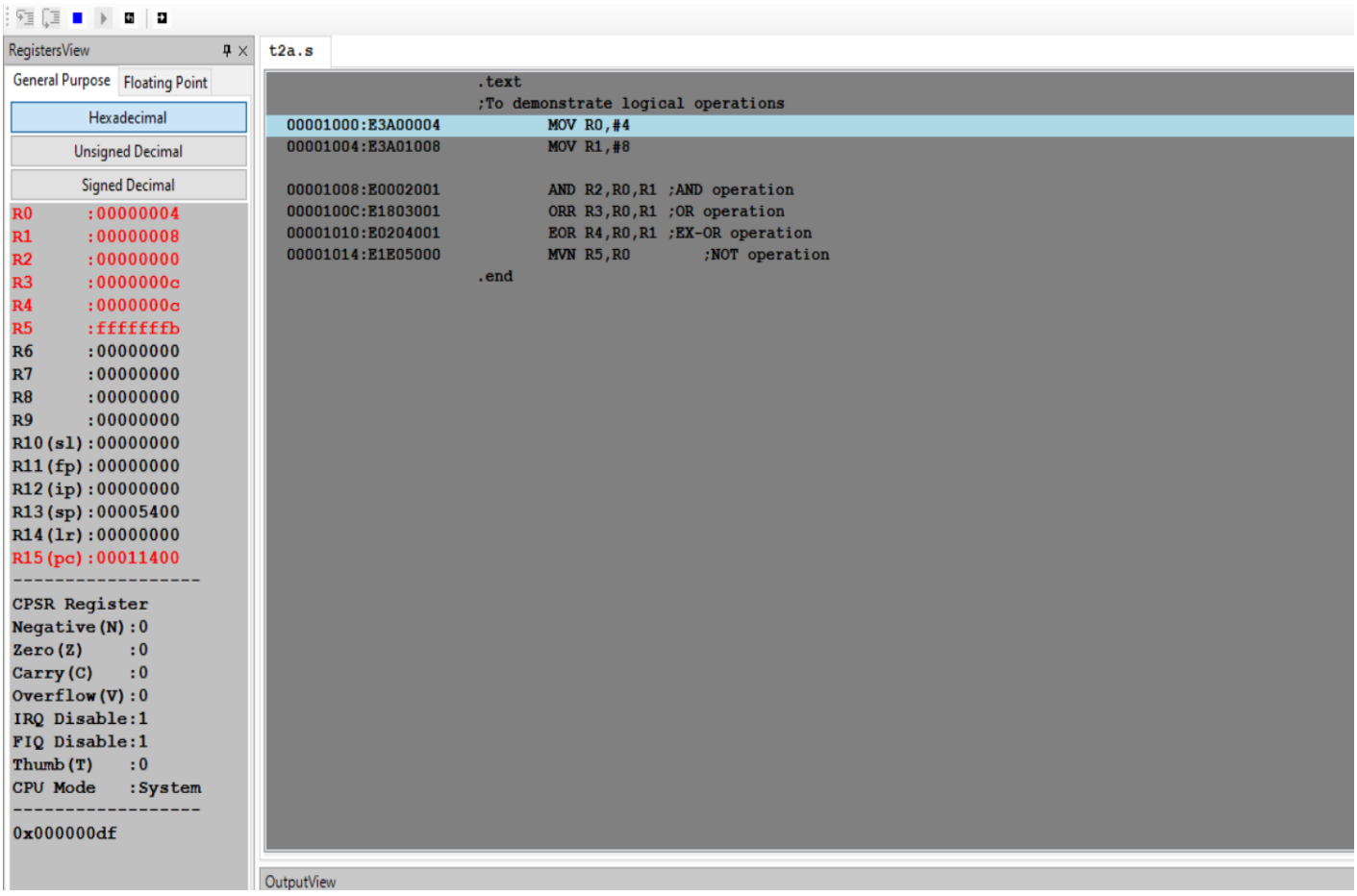


Test case:

```
.text
;To demonstrate logical operations
        MOV R0,#4
        MOV R1,#8
```

```
        AND R2,R0,R1 ;AND operation
        ORR R3,R0,R1 ;OR operation
        EOR R4,R0,R1 ;EX-OR operation
        MVN R5,R0    ;NOT operation
.end
```

Output:



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4th Semester, Academic Year 2020-21

Date:

Name: TUSHAR Y S	SRN: PES1UG19CS545	Section I

Week#____1_____ Program Number: ____3___

Title of the Program

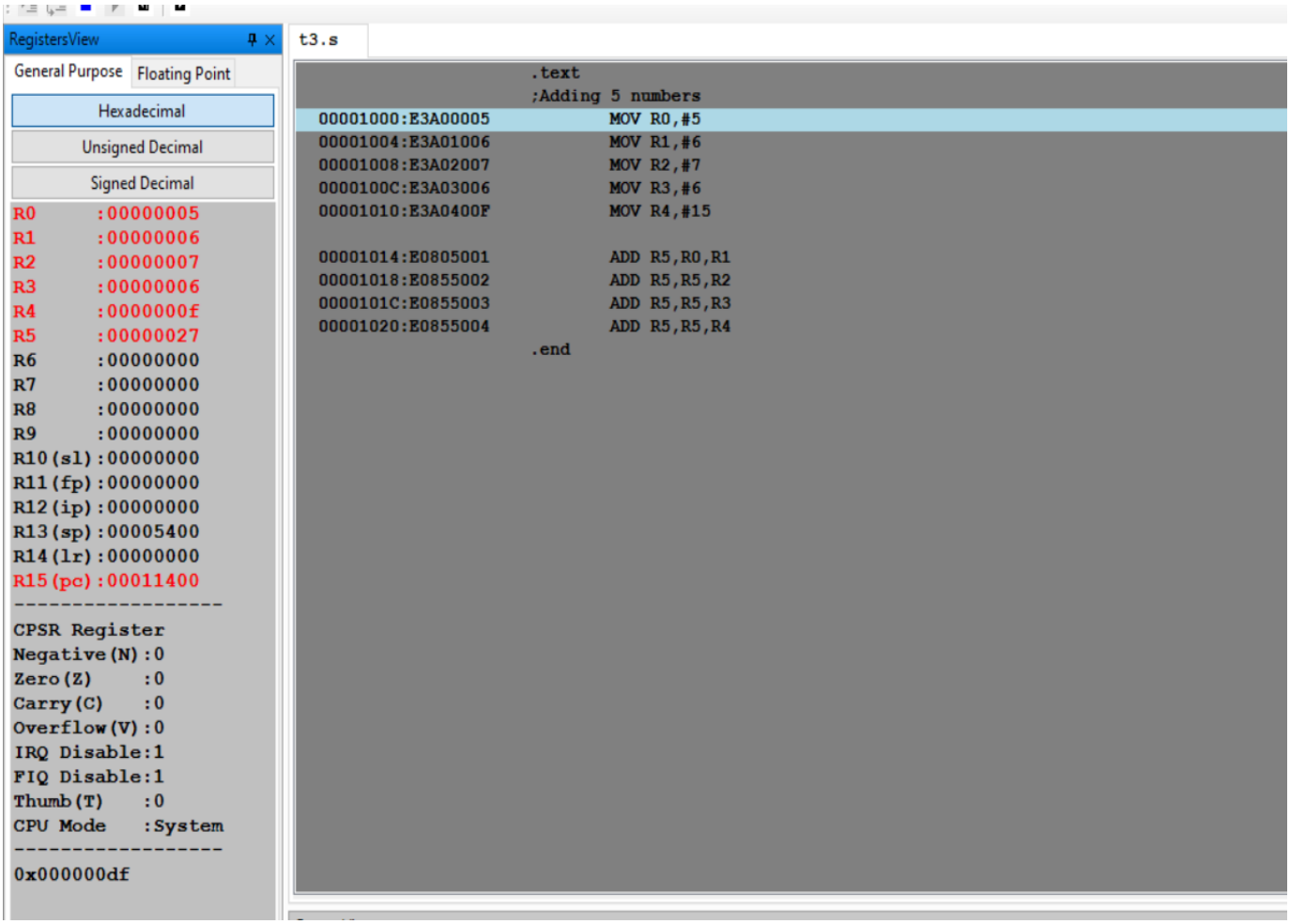
Write an ALP to add 5 numbers where values are present in registers.

ARM Assembly Code:

```
.text
;Adding 5 numbers
    MOV R0,#5
    MOV R1,#6
    MOV R2,#7
    MOV R3,#6
    MOV R4,#15
```

```
        ADD R5,R0,R1
        ADD R5,R5,R2
        ADD R5,R5,R3
        ADD R5,R5,R4
.end
```

Output:

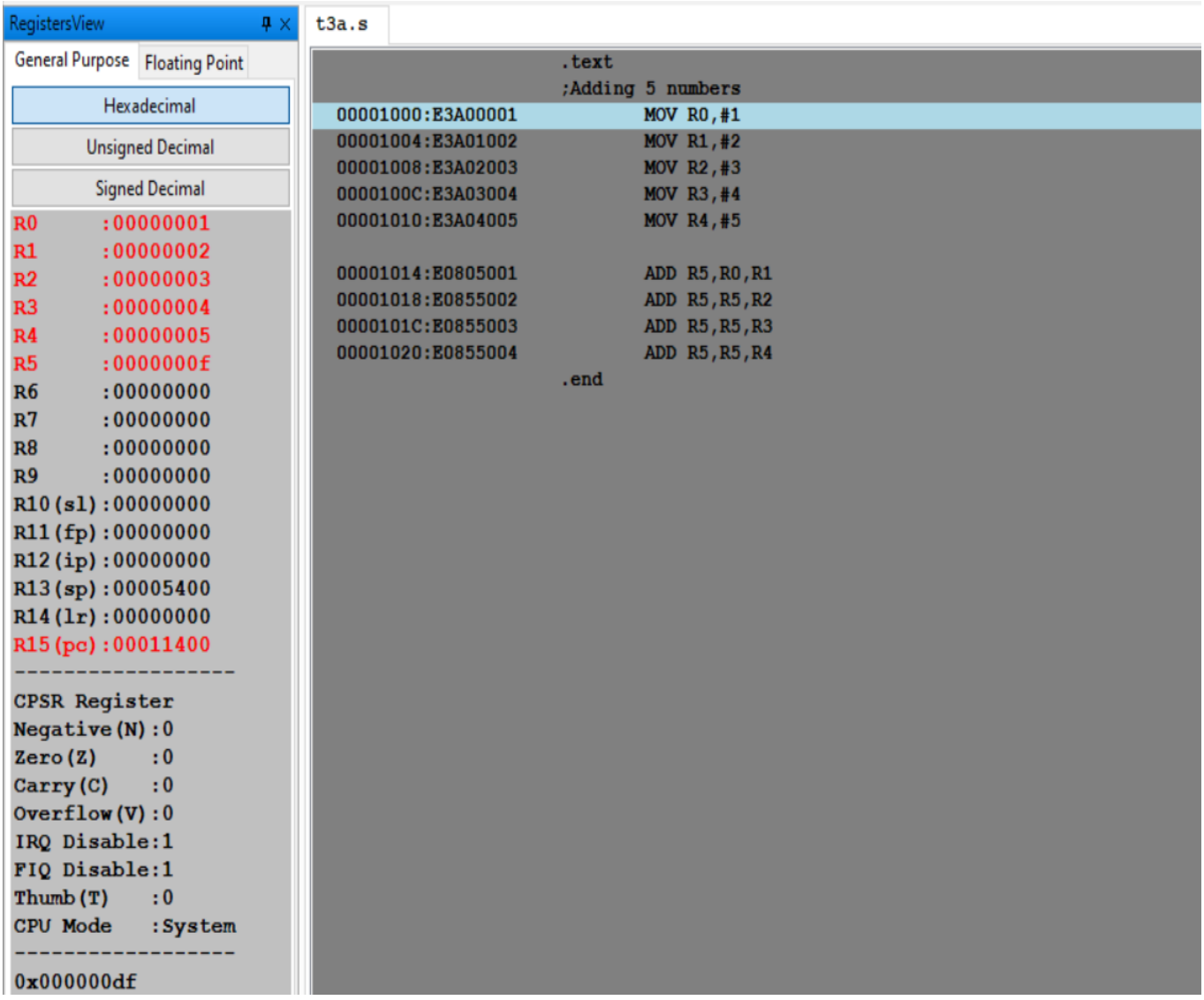


Test Case:

```
.text
;Adding 5 numbers
        MOV R0,#1
        MOV R1,#2
        MOV R2,#3
        MOV R3,#4
        MOV R4,#5

        ADD R5,R0,R1
        ADD R5,R5,R2
        ADD R5,R5,R3
        ADD R5,R5,R4
.end
```

Output:


RegistersView
General Purpose
Floating Point
Hexadecimal
Unsigned Decimal
Signed Decimal
R0 :00000001
R1 :00000002
R2 :00000003
R3 :00000004
R4 :00000005
R5 :0000000f
R6 :00000000
R7 :00000000
R8 :00000000
R9 :00000000
R10(sl):00000000
R11(fp):00000000
R12(ip):00000000
R13(sp):00005400
R14(lr):00000000
R15(pc):00011400
CPSR Register
Negative(N):0
Zero(Z) :0
Carry(C) :0
Overflow(V):0
IRQ Disable:1
FIQ Disable:1
Thumb(T) :0
CPU Mode :System
0x000000df
t3a.s
.text
;Adding 5 numbers
00001000:E3A00001 MOV R0,#1
00001004:E3A01002 MOV R1,#2
00001008:E3A02003 MOV R2,#3
0000100C:E3A03004 MOV R3,#4
00001010:E3A04005 MOV R4,#5
00001014:E0805001 ADD R5,R0,R1
00001018:E0855002 ADD R5,R5,R2
0000101C:E0855003 ADD R5,R5,R3
00001020:E0855004 ADD R5,R5,R4
.end

Microprocessor and Computer Architecture Laboratory

UE19CS256

4th Semester, Academic Year 2020-21

Date:

Name: TUSHAR Y S	SRN: PES1UG19CS545	Section I

Week#____1_____ Program Number: ____4___

Title of the Program

Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0

ARM Assembly Code:

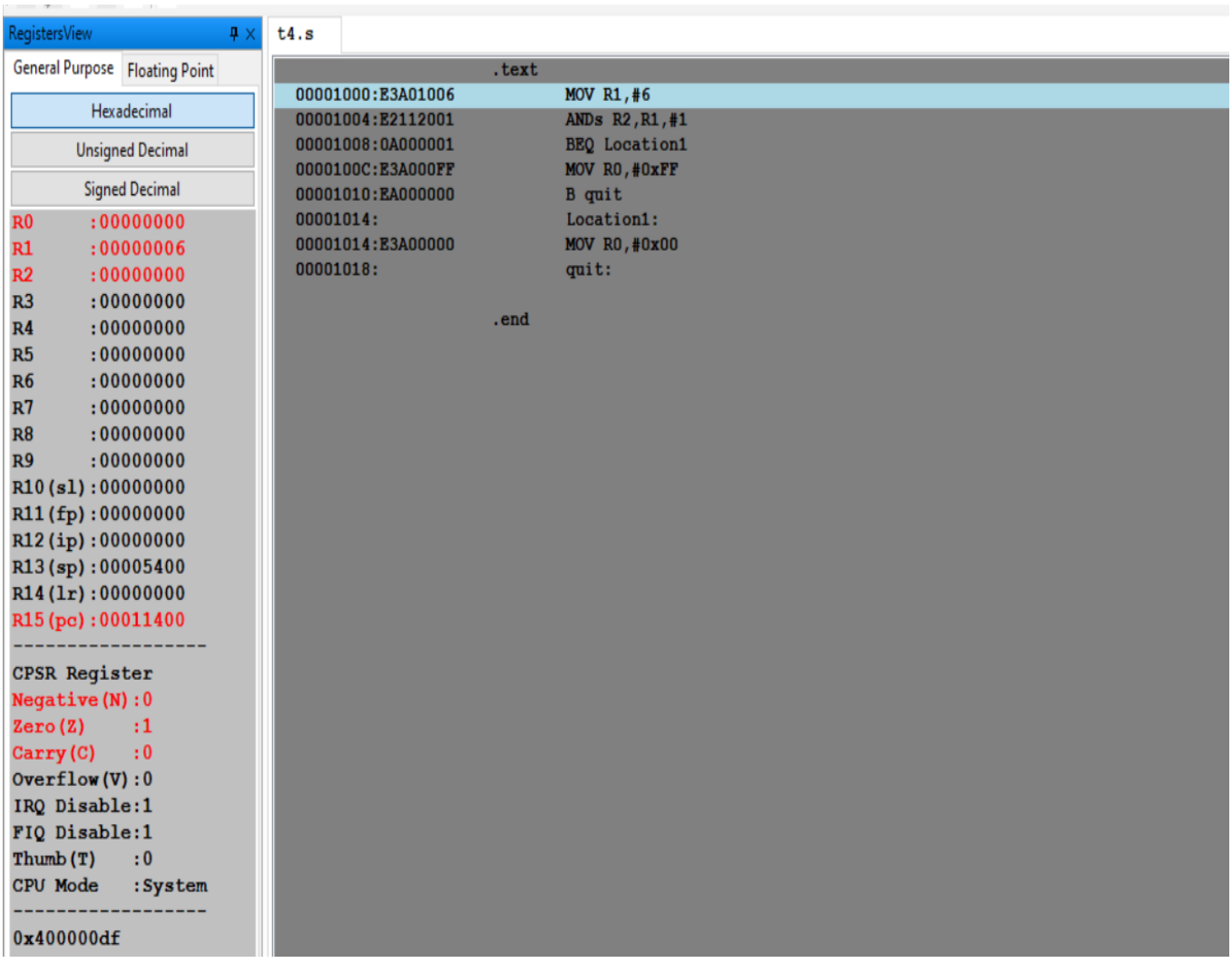
Case 1:

```
.text
    MOV R1,#6
    ANDs R2,R1,#1
    BEQ Location1
    MOV R0,#0xFF
    B quit
```

```
Location1:
MOV R0,#0x00
quit:


.end
```

Output:

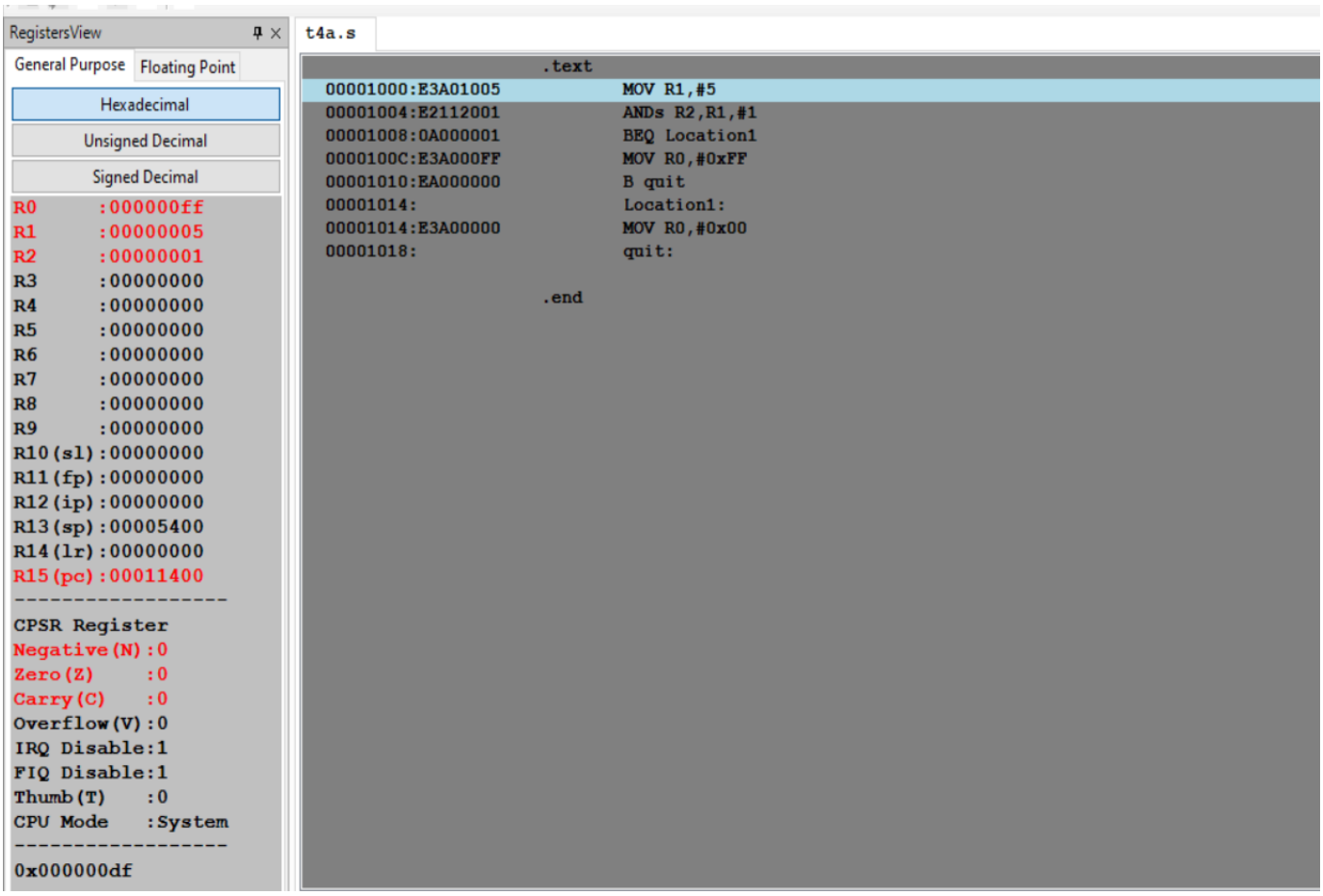


Case 2:

```
.text
        MOV R1,#5
        ANDs R2,R1,#1
        BEQ Location1
        MOV R0,#0xFF
        B quit
        Location1:
        MOV R0,#0x00
        quit:

.end
```

Output:



Test cases:

Case 1:

.text

MOV R1,#10

ANDs R2,R1,#1

BEQ Location1

MOV R0,#0xFF

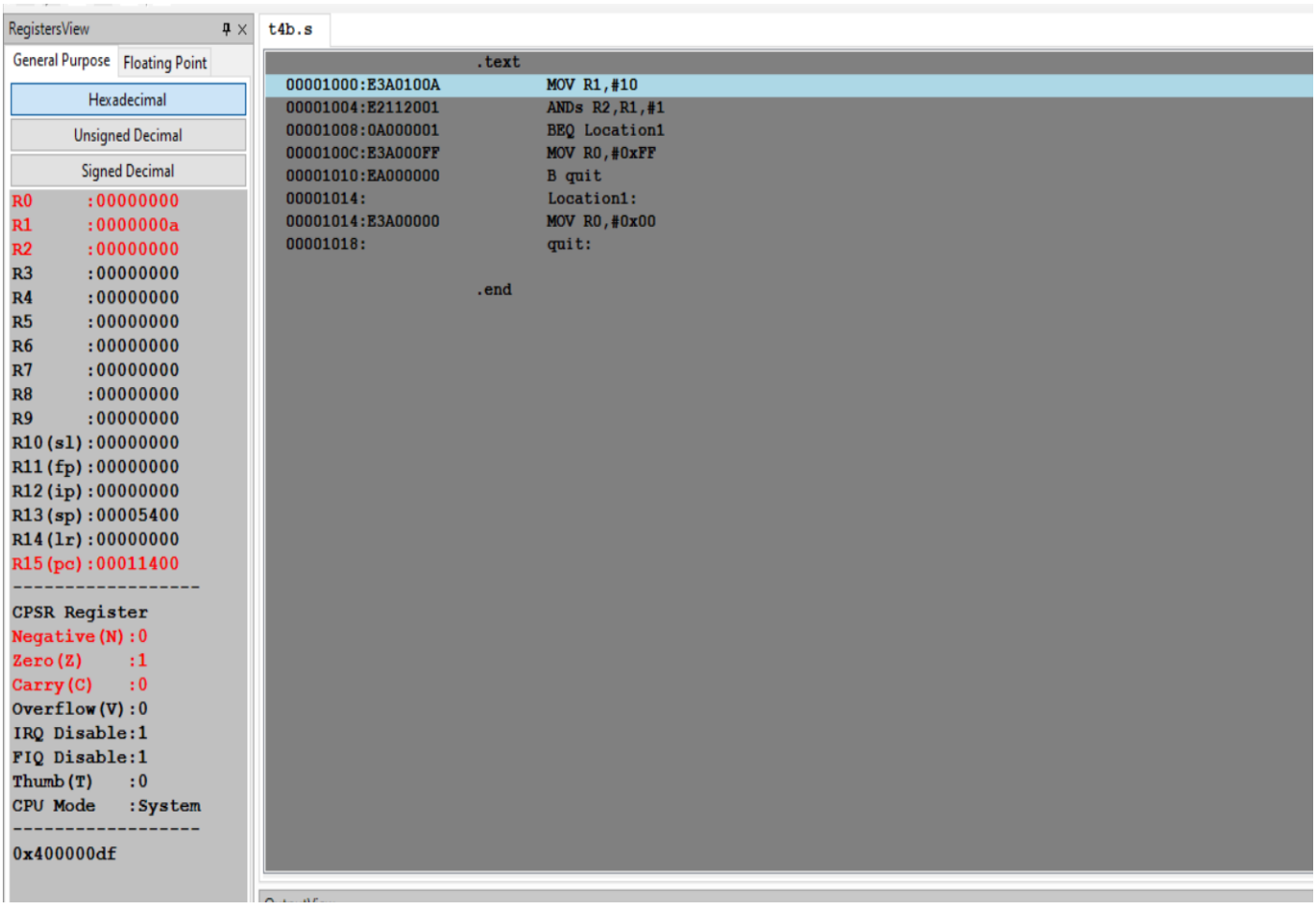
B quit

Location1:

```
        MOV R0,#0x00
        quit:


.end
```

Output:



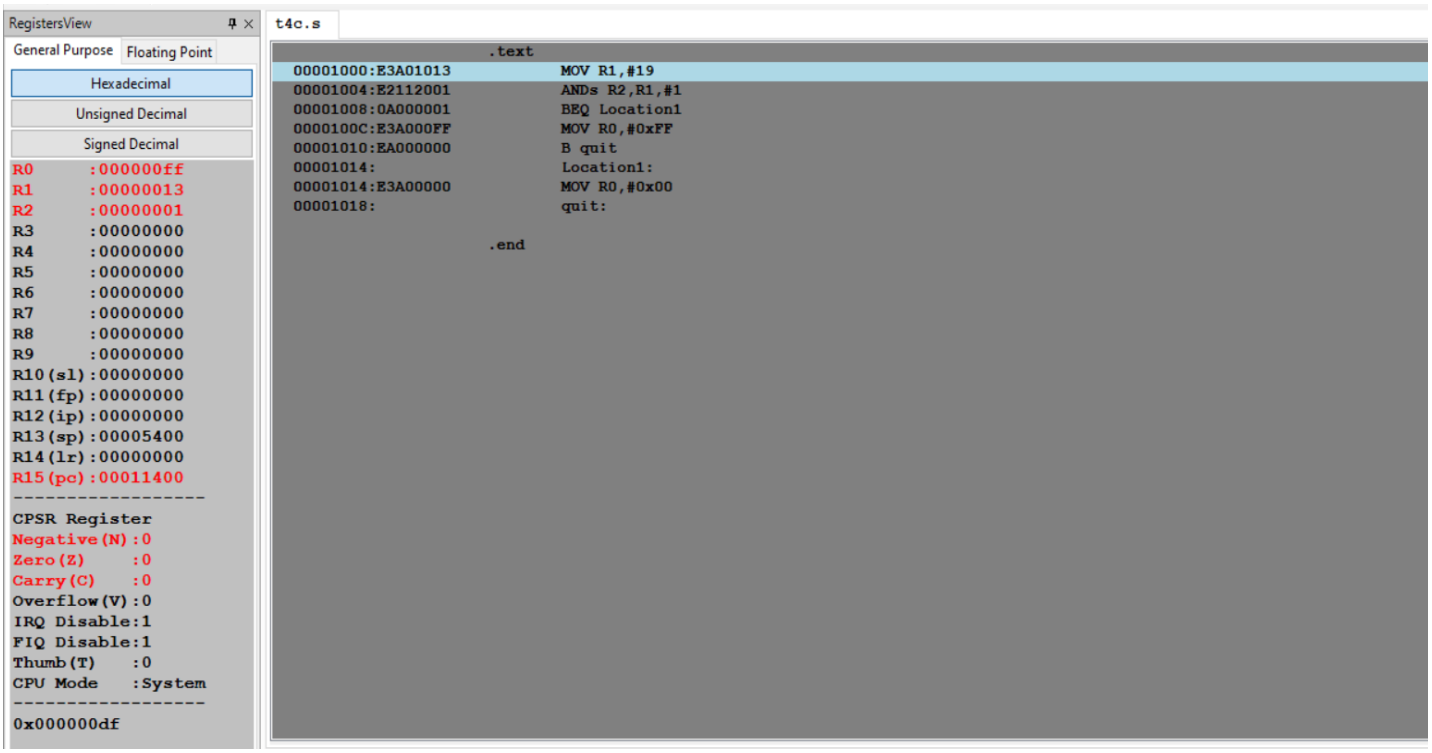
Case 2:

```
.text
        MOV R1,#19
```

```
ANDs R2,R1,#1
BEQ Location1
MOV R0,#0xFF
B quit
Location1:
MOV R0,#0x00
quit:
```

```
.end
```

Output:



Disclaimer:

- The programs and output submitted is duly written, verified and executed by me.
- I have not copied from any of my peers nor from the external resource such as internet.
- If found plagiarized, I will abide with the disciplinary action of the University.

Signature: Tushar
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SRN: PES1UG19CS545
Section: I
Date: 26/1/2021