**Microprocessor and Computer Architecture Laboratory**

**UE19CS256**

**4th Semester, Academic Year 2020-21**

Date:

|  |  |  |
| --- | --- | --- |
| Name: TUSHAR Y S | SRN:  PES1UG19CS545 | Section  I |

Week#\_\_\_\_1\_\_\_\_\_\_\_Program Number: \_\_\_\_1\_\_\_

Title of the Program

**Write an ALP using ARM instruction set to add and subtract two 32 bit numbers .Both numbers are in registers.**

ARM Assembly code:

.text

;adding 2 numbers

MOV R0,#10

MOV R1,#20

ADD R2,R0,R1

;substracting 2 numbers

MOV R0,#10

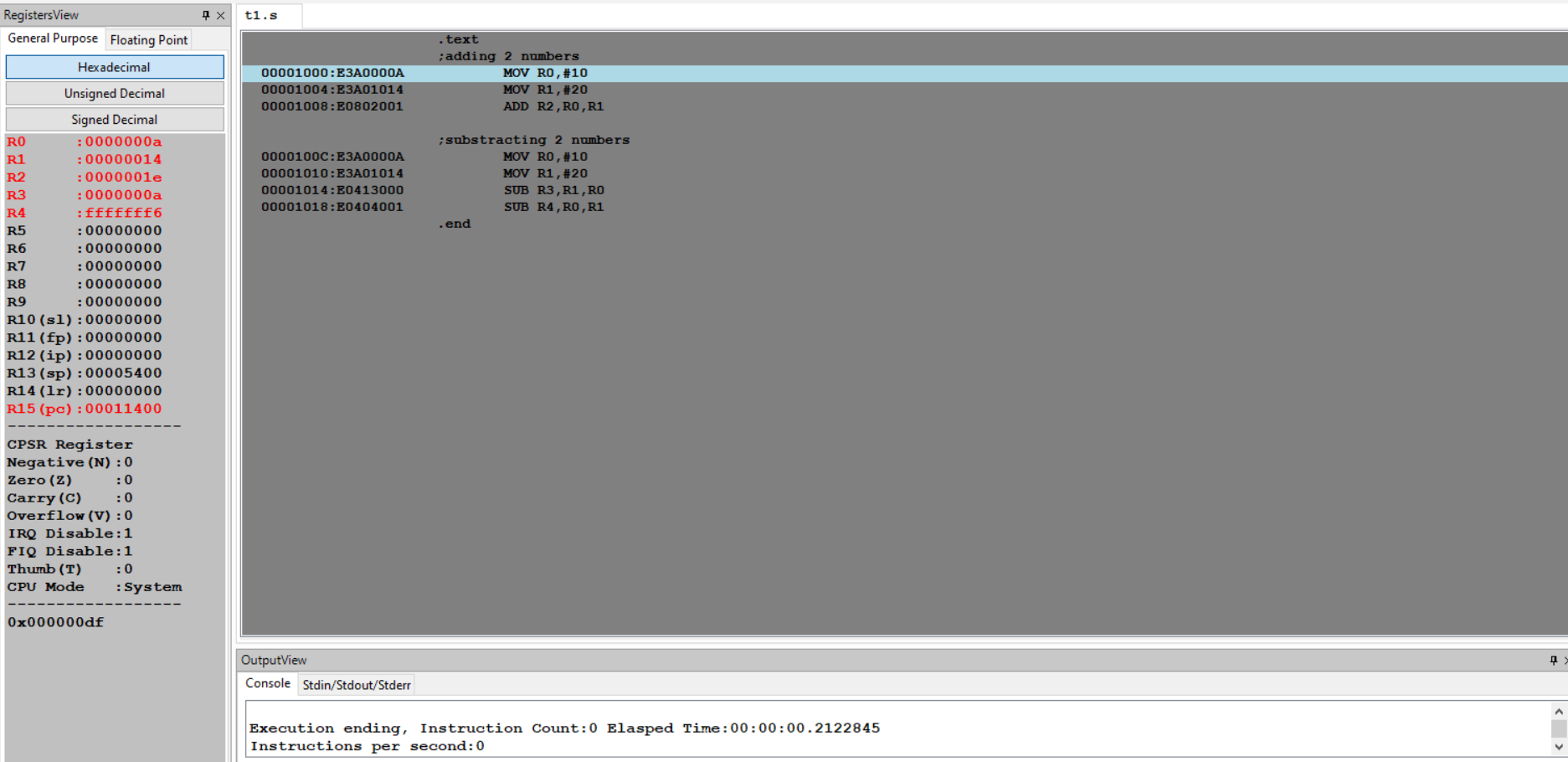
MOV R1,#20

SUB R3,R1,R0

SUB R4,R0,R1

.end

Output:



Test case:

.text

;adding 2 numbers

MOV R0,#2

MOV R1,#4

ADD R2,R0,R1

;substracting 2 numbers

MOV R0,#2

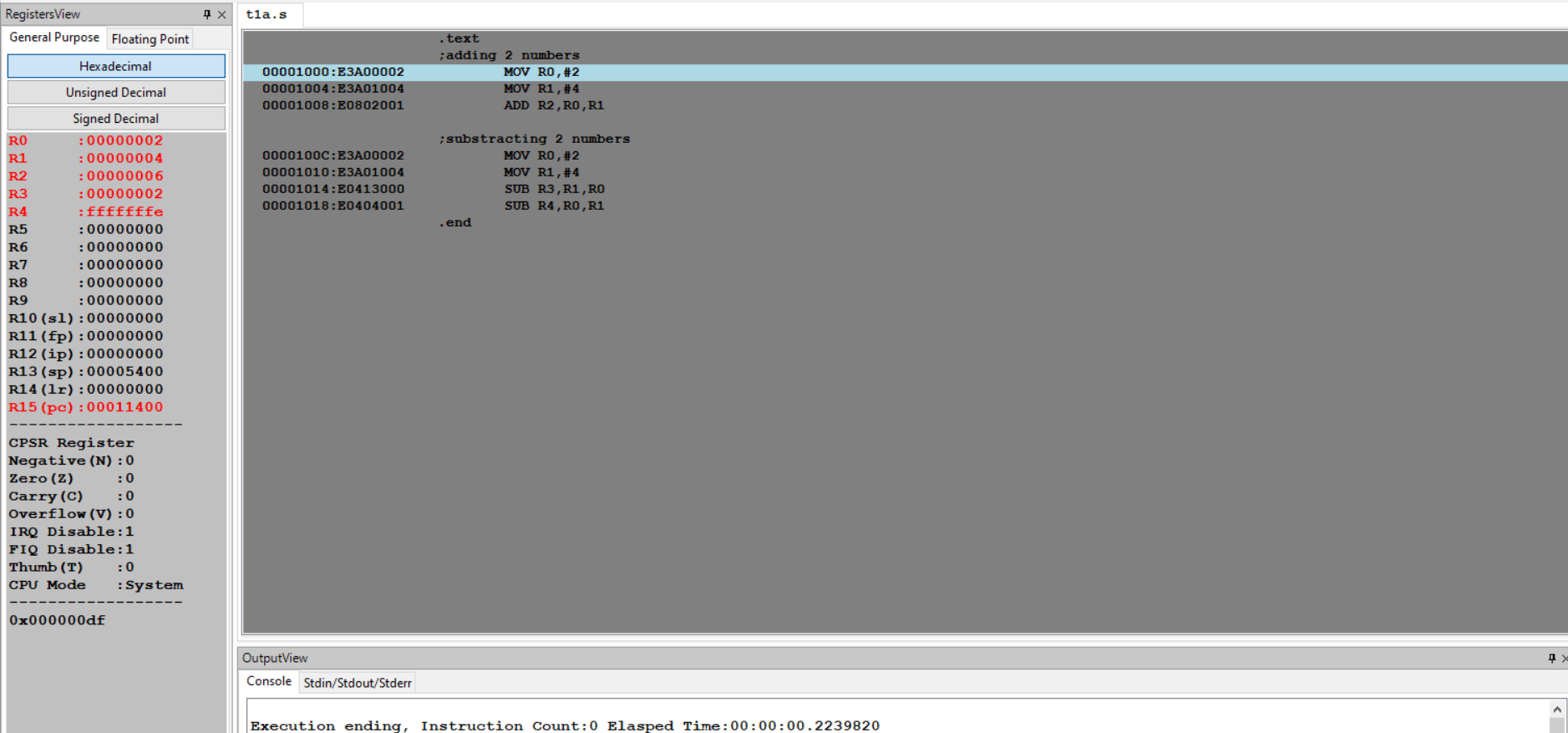
MOV R1,#4

SUB R3,R1,R0

SUB R4,R0,R1

.end

Output:



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Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_2\_\_\_

Title of the Program

**Write an ALP to demonstrate logical operations. All operands are in registers.**

ARM Assembly Code:

.text

;To demonstrate logical operations

MOV R0,#5

MOV R1,#6

AND R2,R0,R1 ;AND operation

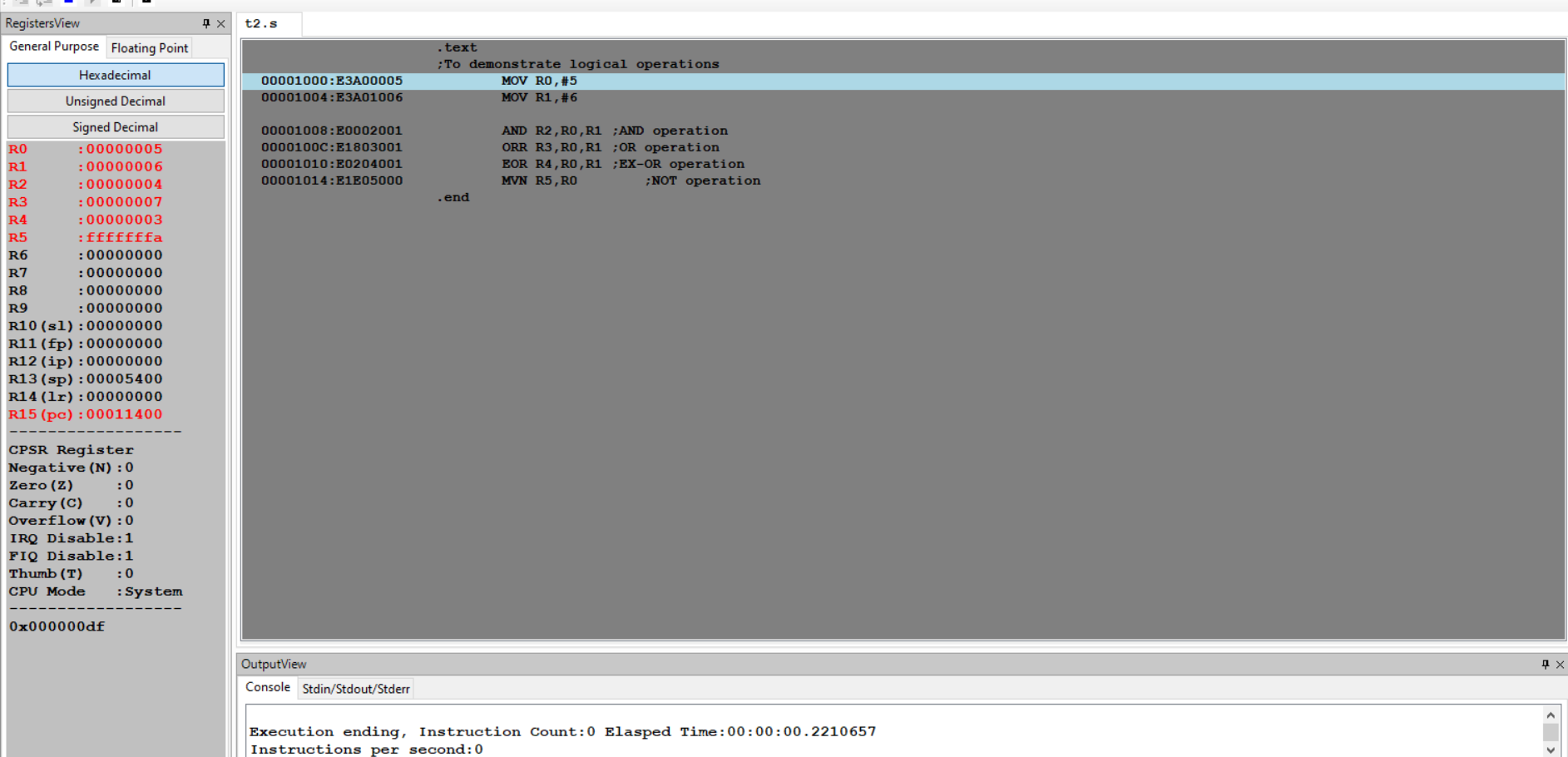
ORR R3,R0,R1 ;OR operation

EOR R4,R0,R1 ;EX-OR operation

MVN R5,R0 ;NOT operation

.end

Output:



Test case:

.text

;To demonstrate logical operations

MOV R0,#4

MOV R1,#8

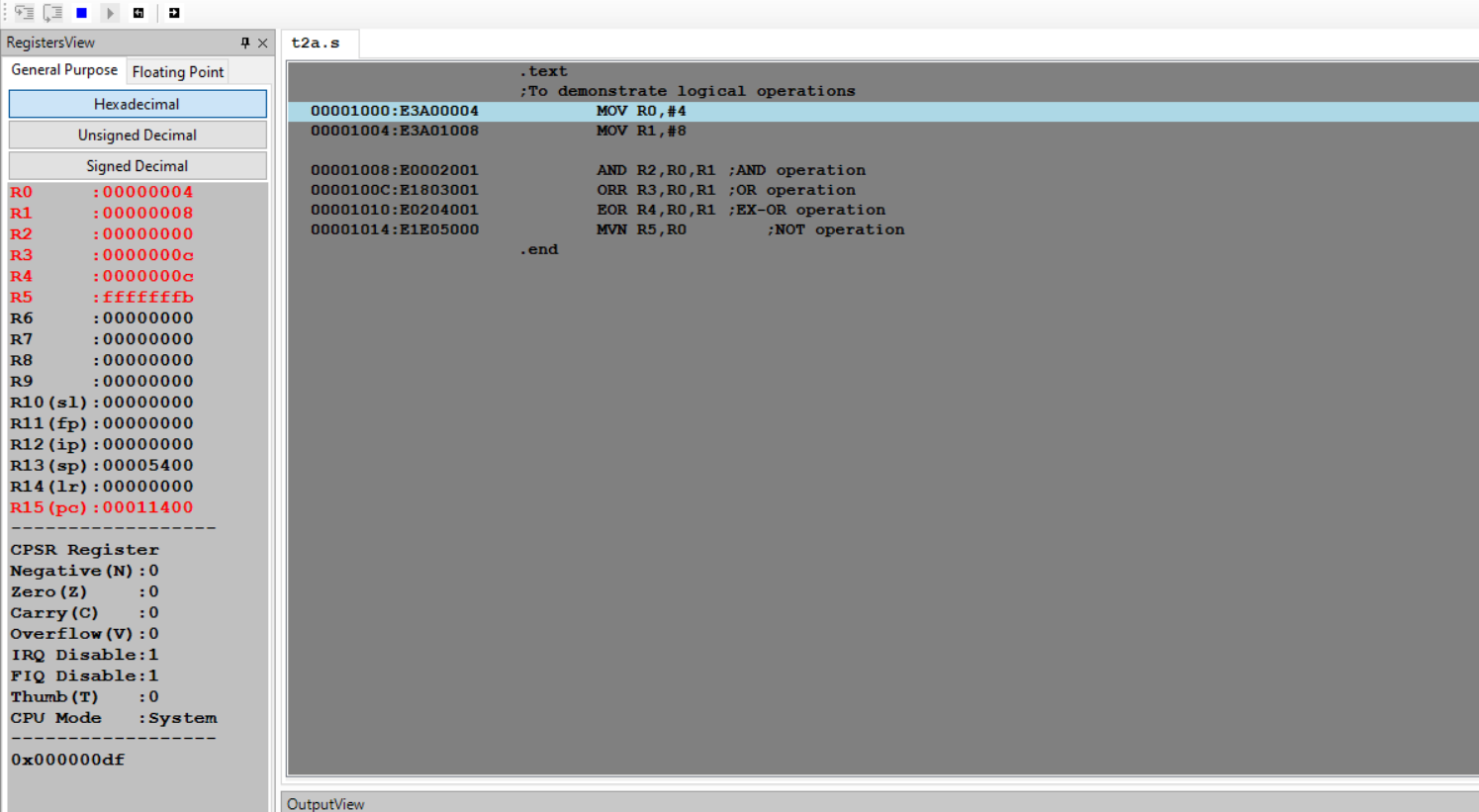
AND R2,R0,R1 ;AND operation

ORR R3,R0,R1 ;OR operation

EOR R4,R0,R1 ;EX-OR operation

MVN R5,R0 ;NOT operation

.end

Output:  


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Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_3\_\_\_

Title of the Program

**Write an ALP to add 5 numbers where values are present in registers.**

ARM Assembly Code:

.text

;Adding 5 numbers

MOV R0,#5

MOV R1,#6

MOV R2,#7

MOV R3,#6

MOV R4,#15

ADD R5,R0,R1

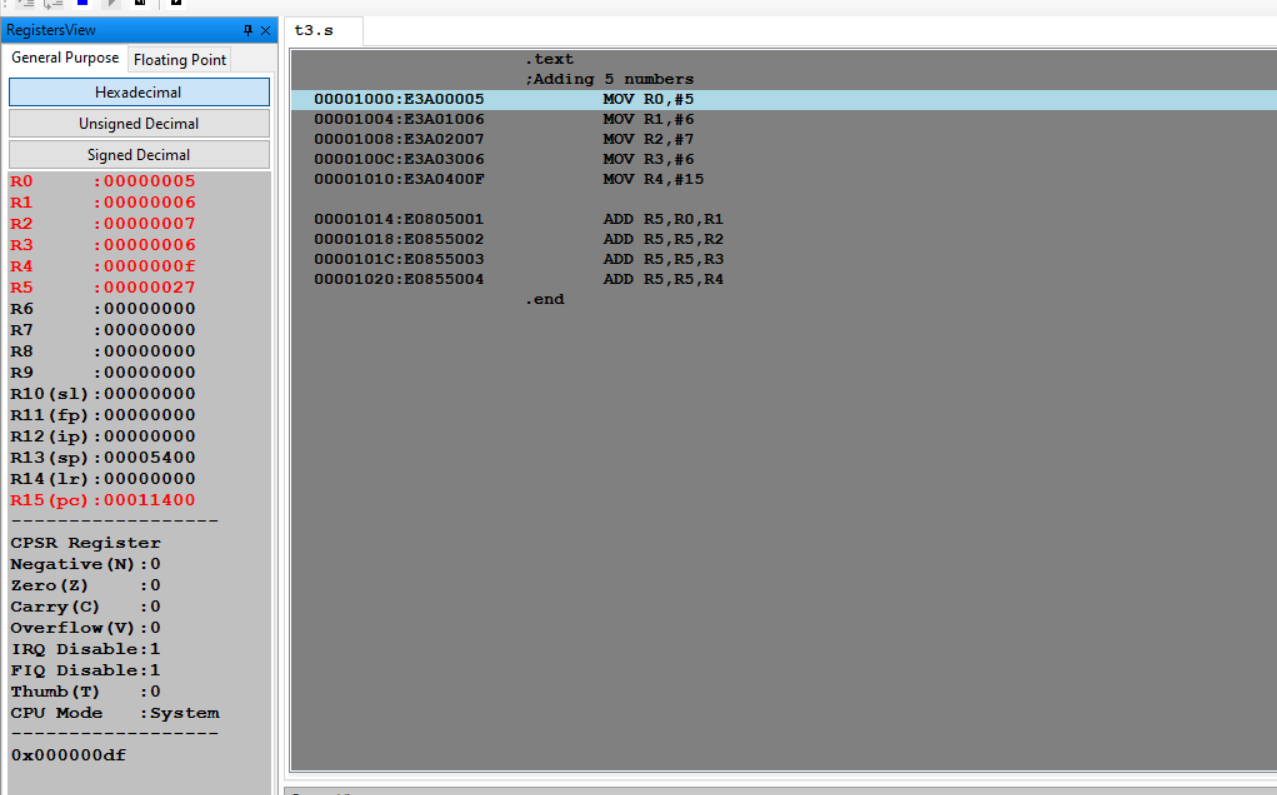
ADD R5,R5,R2

ADD R5,R5,R3

ADD R5,R5,R4

.end

Output:



Test Case:  
.text

;Adding 5 numbers

MOV R0,#1

MOV R1,#2

MOV R2,#3

MOV R3,#4

MOV R4,#5

ADD R5,R0,R1

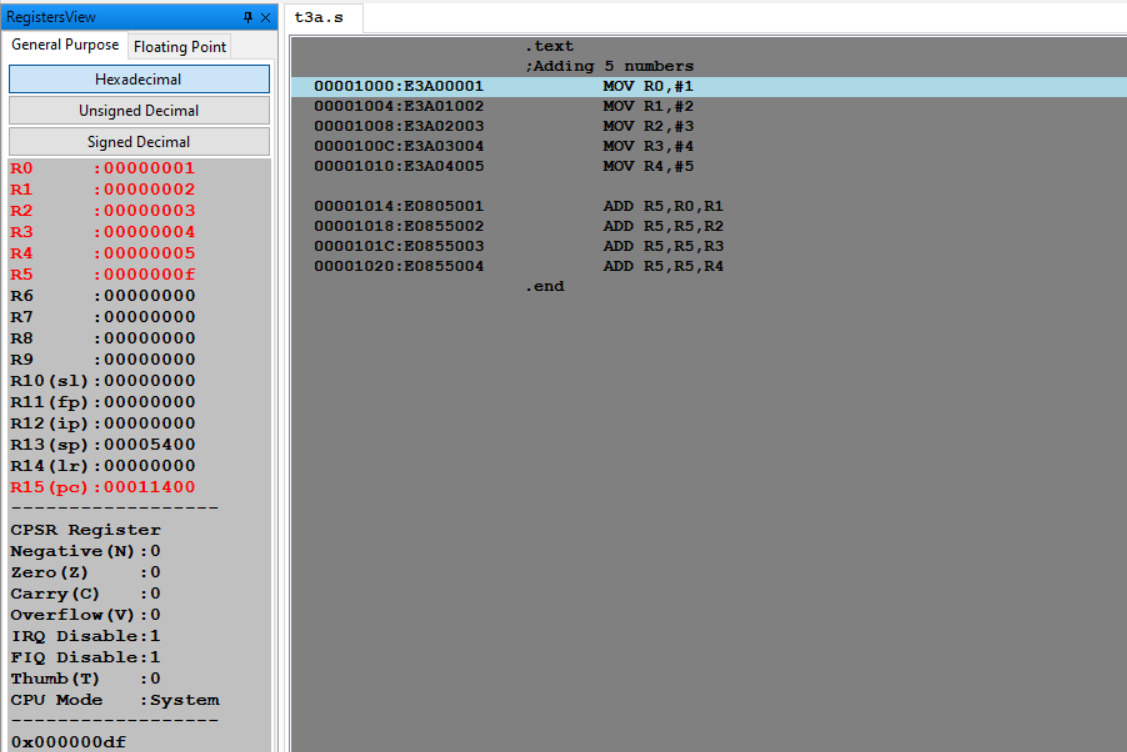
ADD R5,R5,R2

ADD R5,R5,R3

ADD R5,R5,R4

.end

Output:



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Week#\_\_\_\_1\_\_\_\_\_\_\_ Program Number: \_\_\_\_4\_\_\_

Title of the Program

**Write an ALP using ARM instruction set to check if a number stored in a register is even or odd. If even, store 00 in R0, else store FF in R0**

ARM Assembly Code:

Case 1:

.text

MOV R1,#6

ANDs R2,R1,#1

BEQ Location1

MOV R0,#0xFF

B quit

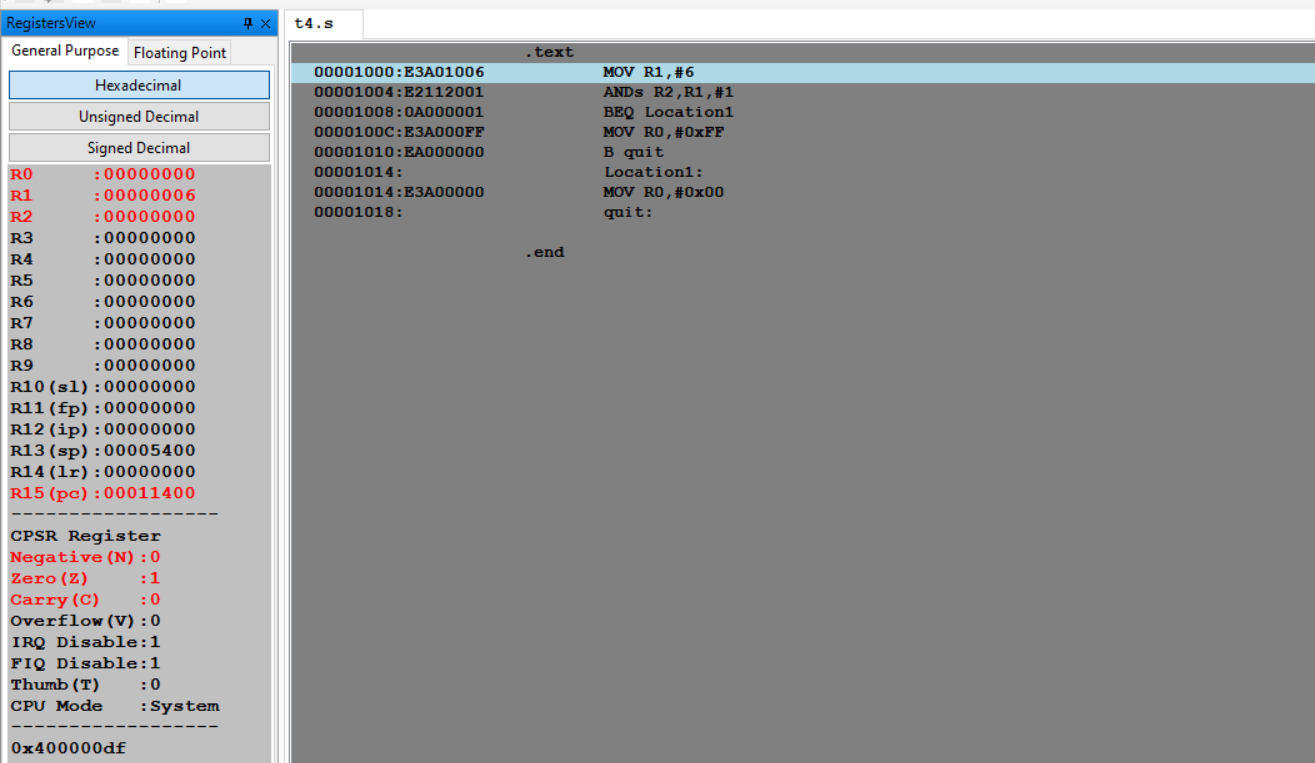
Location1:

MOV R0,#0x00

quit:

.end

Output:



Case 2:

.text

MOV R1,#5

ANDs R2,R1,#1

BEQ Location1

MOV R0,#0xFF

B quit

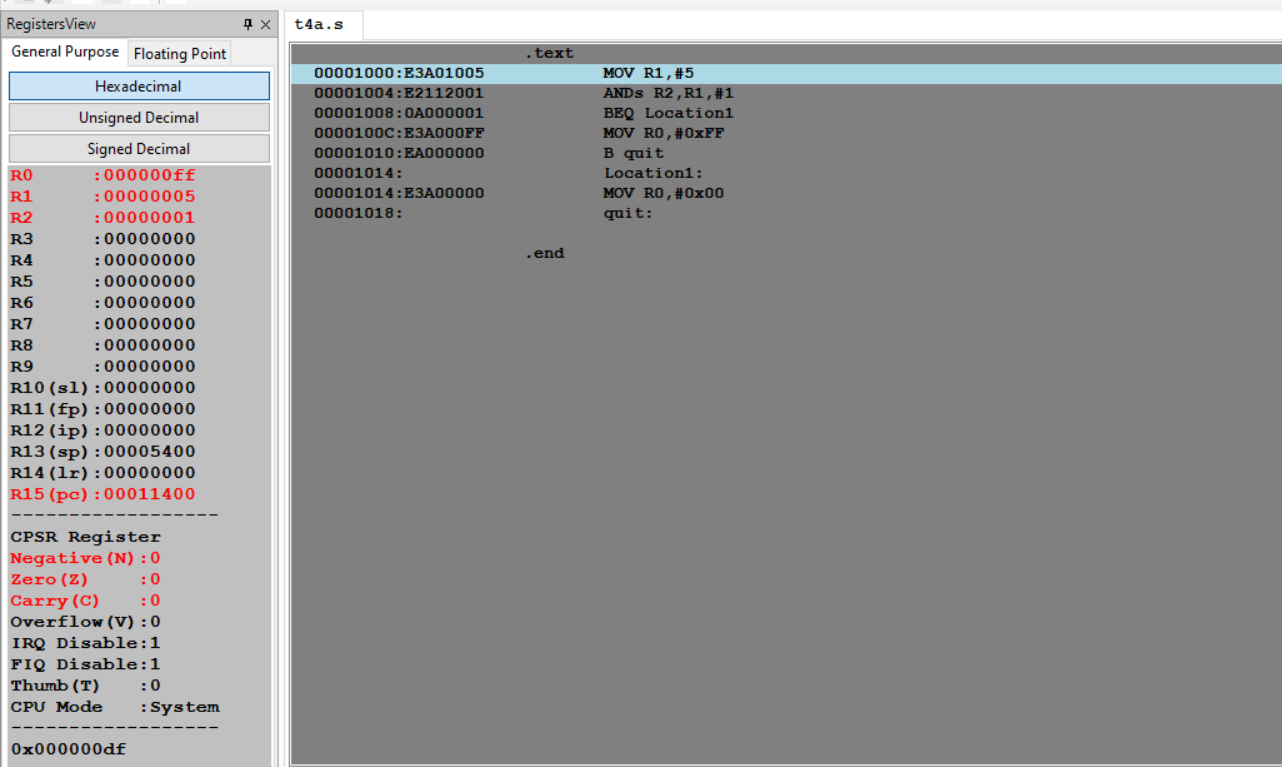
Location1:

MOV R0,#0x00

quit:

.end

Output:



Test cases:

Case 1:

.text

MOV R1,#10

ANDs R2,R1,#1

BEQ Location1

MOV R0,#0xFF

B quit

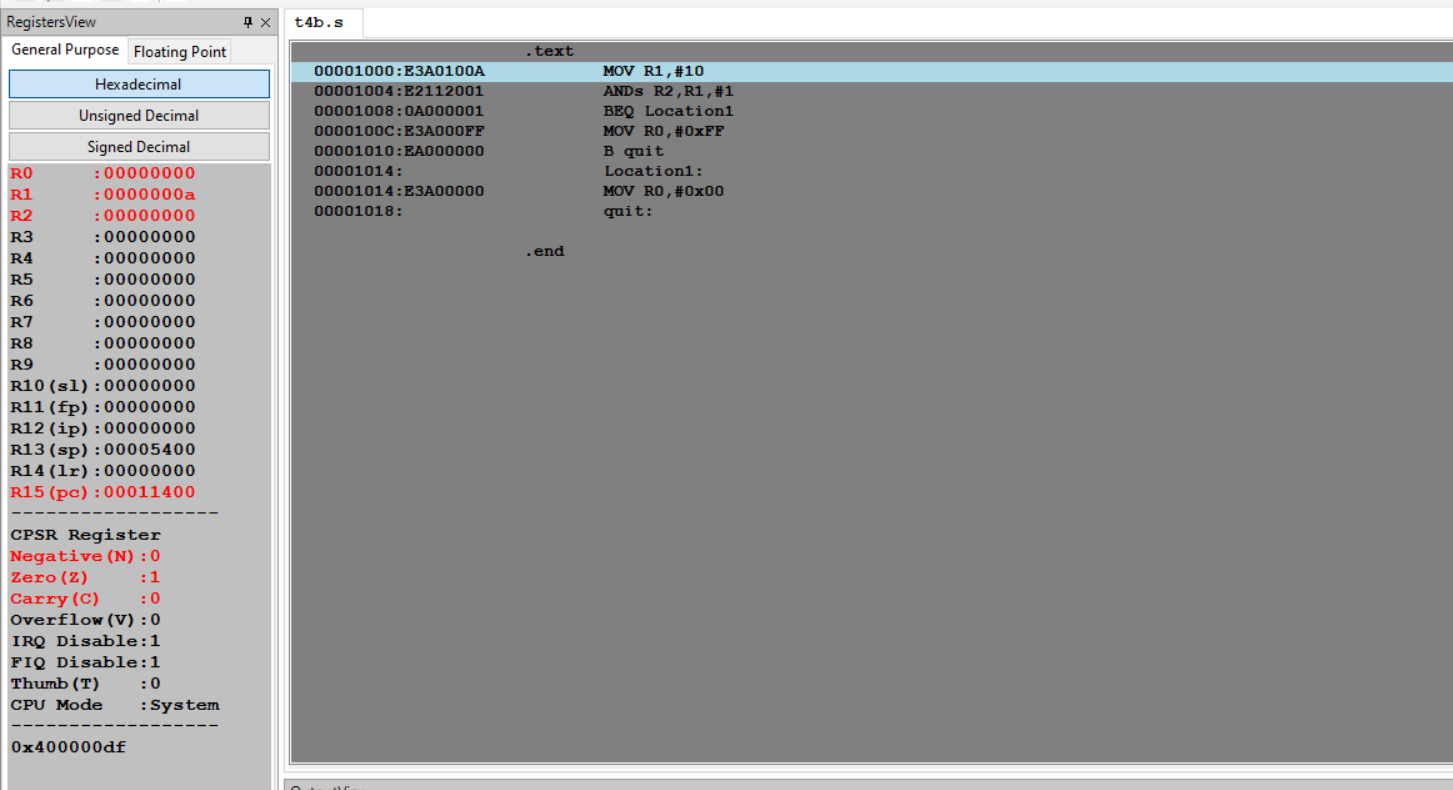
Location1:

MOV R0,#0x00

quit:

.end

Output:



Case 2:

.text

MOV R1,#19

ANDs R2,R1,#1

BEQ Location1

MOV R0,#0xFF

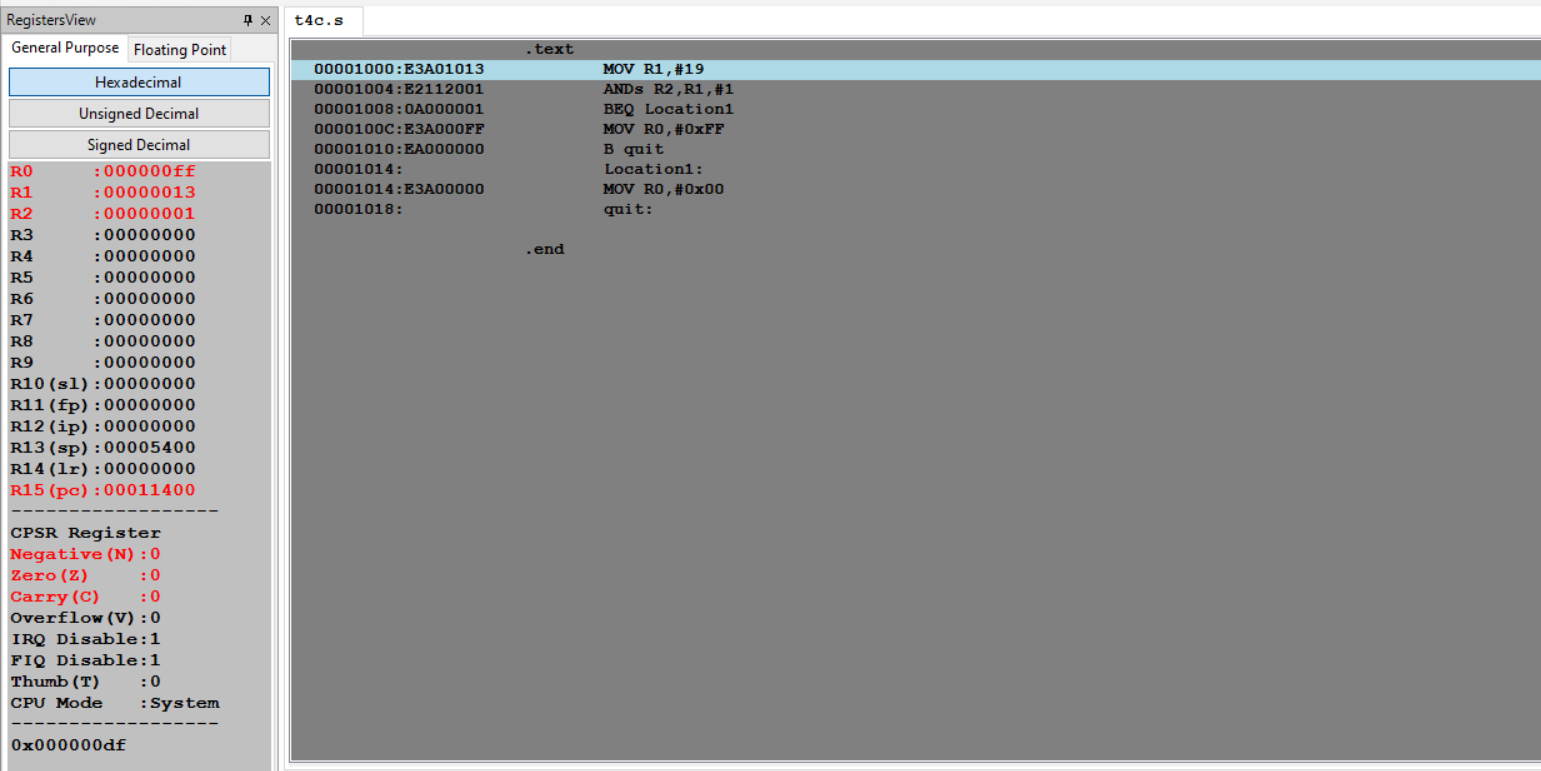
B quit

Location1:

MOV R0,#0x00

quit:

.end

Output:  
****

**Disclaimer:**

* The programs and output submitted is duly written, verified and executed by me.
* I have not copied from any of my peers nor from the external resource such as internet.
* If found plagiarized, I will abide with the disciplinary action of the University.

Signature: Tushar

Name: TUSHAR Y S

SRN: PES1UG19CS545

Section: I

Date: 26/1/2021