

Supplementary Materials for
**Harnessing spatiotemporal transformation in magnetic domains for
nonvolatile physical reservoir computing**

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Movies S1 to S3

Supplementary Note S1. Impacts of small device inhomogeneity.

In physical reservoir computing, device inhomogeneity creates diverse neuron responses that enrich reservoir dynamics – a favourable property not accessible in software-based approaches (1,22,39). In spatial multiplexing, device inhomogeneity causes the same input to generate vastly different outputs in multiple devices of nominally the same physical characteristics. This causes the reservoir to be more sensitive to small changes in input and to recognize more distinct states, leading to better separability and lower risk of overfitting. In ferroelectrics-based physical reservoir, device-to-device variations of more than 60% have been claimed to be favourable for enhancing the reservoir performance (25).

However, when the spread in device readout becomes sufficiently large and random, the system is compromised by reduced signal-to-noise ratio, damaging the accuracy. Therefore, the computing performance is expected to first increase with device-to-device variations and then fall off. Furthermore, from the perspectives of circuit design, excessively large device-to-device variations are disastrous when the network size grows. Large and unrepeatable readout range makes it difficult to have a well-defined working window with sufficient resolution.

Therefore, reservoir dynamics cannot be indefinitely enriched by device inhomogeneity. This is one of our motivations to build a dynamic reservoir from the VNs of fairly homogeneous devices (fig. S1) rather than relying on stochastically inhomogeneous devices. In our approach, the diverse neuron responses are more controllable and repeatable (fig. S3), leading to enhanced separability without compromising the practicability on analogue circuits and the adaptability to larger network sizes. We have spent considerable efforts to minimize the device inhomogeneity, partially by preparing our samples using an industry-graded 200-mm fabrication line. Nevertheless, we still expect the very small device-to-device variations in our devices to enrich the reservoir dynamics since they slightly spread the readouts of the already-diversified VNs.

Supplementary Note S2. Additional discussions domain wall motion.

In Fig. 2C, the seemingly stagnant portions near $L_{RD} \approx 7 \mu\text{m}$ for $\tau_p = 120 \text{ ns}$ and $\tau_p = 80 \text{ ns}$ are completely accidental. These step-like features are not due to pinning. Instead, they arise from the way we define L_{RD} .

Figure S2a shows the frame-by-frame MOKE images for $\tau_p = 80 \text{ ns}$. L_{RD} remains roughly unchanged from $N_p = 71$ to $N_p = 77$ because we define L_{RD} as the maximum horizontal span of remaining domains, and the central part of the right domain wall did not move for a few pulses. However, the domain wall front actually moves with addition pulses, which is highlighted in the right column by the contours for $N_p = 71$. In contrast, the step-like feature for $\tau_p = 120 \text{ ns}$ is caused by domain wall at a different horizontal position, as shown in fig. S2c. Furthermore, the domain wall front near the upper edge did not move for a few pulses, rather than the centre. Therefore, we conclude that the step-like features near $L_{RD} \approx 7 \mu\text{m}$ in Fig. 2C are accidental as they are not caused by pinning, which usually happens at the same position.

It is expected to observe a portion of the domain wall being unmoved after a few pulses, especially for small τ_p . This is because a pulse of small τ_p inputs a small amount of energy, which is insufficient to move the entire domain wall front. A portion of the domain wall front always move first and the rest follows. For the same reason, we seldom observe the step-like features for large τ_p .

We repeat the measurement for $\tau_p = 80 \text{ ns}$ on exactly the same device (fig. S2b). We identify the same horizontal position, which is marked by the dotted line passing through sub-figure (a)-(c). We observe the same overall pattern, where the central part of the domain wall front did not move for a few pulses. Furthermore, the lower part of the red contour in (a) matches well with domain in (b). These agree with the highly repeatable electrical readouts in our devices. However, we must emphasize that the domain wall fronts **are not exactly the same** at the same position in repeated measurement. This is seen from the different contours and domain evolution in the right columns of fig. S2a and fig. S2b. Therefore, despite having an overall pattern for a given τ_p , the domain wall motion is associated with stochastic processes. Notably, the fact that τ_p can alter the pattern of domain wall motion is the basis of the rich dynamics in our spintronic reservoir.

Supplementary Note S3. Repeatability, endurance and thermal stability of device.

Figure S3 demonstrates the excellent repeatability of our device. Using the experimental approach by Liao *et al* (45), we evaluate the retention of our device by calculating the thermal stability factor (Δ , in units of $k_B T$). We first measure the R_H - V_p response for $50 \mu s \leq \tau_p \leq 0.1$ s (fig. S4a). Then, we extract the critical switching current from the ‘coercive voltage’ of R_H - V_p curves by treating them as hysteresis loops. Next, we fit I_c against $\ln(\tau_p/\tau_0)$ using $I_c = I_{c0}[1 - \frac{1}{\Delta} \ln(\frac{\tau}{\tau_0})]$ (fig. S4b). Here, I_{c0} is the thermal-free critical switching current and τ_0 (assumed to be 1 ns) is the inverse of intrinsic attempt frequency. From the gradient of the linear fit, we get $\Delta = 243.3$ and 211.2 for the up-to-down and down-to-up switching. These values, though much larger than those ($\Delta=22-39$) in Liao’s work, are rationalized by stronger perpendicular magnetic anisotropy from the much thinner CoFeB in our work. Based on extracted values of Δ , we conclude excellent data retention in our devices. We stress that the above calculation only provides a rough estimation since the equation in Liao’s work is derived from an analytical model on single-domain nanomagnet, which differs from the multi-domain structure in our work.

We estimate the endurance of our device by checking the magnetic hysteresis loop after applying a large number of pulses with $\tau_p = 200$ ns (fig. S4c). For $V_p = 3.0$ V, which is the maximum amplitude used during training, the R_H - H_z curve shows negligible changes after 10^{11} pulses. For $V_p = 3.3$ V, the R_H - H_z curve is deteriorated severely only after 10^{11} pulses. The reduced coercive field, reduced R_H range and shifted R_H offset all indicate that the device has been irreversibly damaged. These results show that our device has an endurance of at least 10^{11} in its operating conditions (i.e. $V_p \leq 3$ V, $\tau_p \leq 200$ ns).

We also examine the data retention time of our device using the following experiment. To mimic the electrical disturbance during reading, the probing current has a base value of $50 \mu A$ and a 100-ms pulse of additional $50 \mu A$ every 5 seconds. The Hall voltage (V_H) was read during the pulse (fig. S5a), i.e. the probing current is $100 \mu A$, doubling the value in the main text. The V_H measurement was run continuously for more than 10 days with minimal drifting observed (fig. S5b-d). The standard deviation is $1.2 m\Omega$, which is constrained by the resolution of measurement equipment.

Supplementary Note S4. Performance of device and circuit.

A. Energy consumption of single device

The reading (E_R) the writing energies (E_W) in this work is estimated using a simple relation of $E_{R,W} = \frac{V^2}{R}t = I^2Rt$, where V and I are current and voltage input, t is the duration of inputs and R ($= 262 \text{ Ohm}$) is the resistance.

For reading, $I = 50 \text{ } \mu\text{A}$, $t = 1/(65\text{MHz})$. Therefore, $E_R = 10.1 \text{ fJ}$ per read.

For writing, $V = 2.2 \text{ V}$, $t = 50 \text{ ns}$. Therefore, $E_W = 0.92 \text{ nJ}$ per input.

The writing energy is mainly limited by the large device size of Hall bars. Figure S8 shows the electrical switching of a 240-nm perpendicularly magnetized SOT-MTJ built on the stack in the main text. The write energy is lowered to 37 pJ at 10 ns.

B. System speed

The operating speed of our circuit is constrained by the hardware delay times summarized in table S3. Summing up the values, the total time per operation – pulsing once followed by reading once – is roughly 10 μs . Most of the time is consumed by the amplifier (AMP) because the electronic components are connected by metallic tracks of the PCB, demanding additional efforts to peg the noise and to stabilize the reading. If integrated on a chiplet, our circuit is expected to be at least 10 to 100 times faster.

Given a 10- μs delay, we estimate the data acquisition time for each task. In written digit recognition with 6 NVs, there are 20000 samples per trial, each passing 196 pulses but executing in parallel by 14 devices, leading to a total time of $(10 \text{ } \mu\text{s}) \times 20000 \times 196 \times 6 / 14 = 16.8 \text{ s}$. In Mackey-Glass prediction task with 57 NVs, there are 1400 data points per trial, each passing 1 pulse but executing in parallel by 14 devices, leading to a total time of $(10 \text{ } \mu\text{s}) \times 1400 \times 57 / 14 = 57 \text{ ms}$.

Beside the data acquisition, the total time for each task also includes the computation of the output weight matrix W_{out} , which depends on the size of reservoir state matrix thus number of neurons. We used a build-in timer in Python to monitor the real-time task duration. For written digit recognition with $N_s = 20000$ and $N_{VN} = 6$, the computation time is 0.918-1.058 s. For Mackey-Glass prediction with $N_s = 1400$ and $N_{VN} = 57$, the computation time is 30-35 ms. Therefore, the total time per trial for written digit recognition and Mackey-glass prediction are roughly 18 s and 90 ms, respectively.

C. System power

We adopt the method reported by Zhong *et al* to estimate the power consumption (24). Basically, the total power consumption P_t for each component is $P_t = V \times I \times N \times t \times f$. Here, V and I are the voltage and current of power supply, where $V \times I$ are sometimes replaced by the commercial power rating P_0 in our estimation. N is the total number of hardware. t is the active duration of the component (e.g. pulse width). f is the frequency (100kHz) of the input waveform. Table S4 summarizes the power consumption for read and write per operation.

Finally, we compare in table S5 our approach with prior implementation of RC. Overall, our system has promising operating speed and power budget based on two types of comparison with prior works. First, our system has much lower power than the digital implementation by FPGA (62-64). We attribute this power saving to the fact that PRC involves much less matrix multiplication, which is energetically costly. Second, the power of our system is comparable with the circuit-level implementation of PRCs (65, 66), much smaller than the photonics but significantly larger than Zhong’s work (24). In Zhong’s work, the record-low power is based on highly optimized circuit structure, which is not a focus of the present work.

We emphasize that table S5 only provides rough evaluation of the standard of our system since RC performance depends on optimization of both hardware network and algorithms. Therefore, the major innovation of this work – PRC based on spatiotemporal transformation in spintronics – should not be compromised by the hardware-constrained circuit performance.

D. Energy consumption

We attempted to compare the energy consumption of our PRC with the state-of-the-art implementation using CPU or GPU only. Selected prior works are summarized in table S6. As expected, the reported energy consumption exhibits a wide distribution. This is because the energy consumption depends strongly on (a) the number of input or samples, (b) the network size/structure, and (c) the model of CPU or GPU. The task speed is even more scattered for the same reasons (a-c). Some take a few milliseconds(69) or a few seconds(70) while others take 78 hours(71).

Therefore, given the difficulty in having apple-to-apple comparison with prior works, we estimate the energy consumption of our PRC and compare it with those of all-software implementations using the same computer. The energy consumption of our spintronic network consists of two parts. The first part includes spintronic memristors and peripheral circuits on PCB, which are estimated using the powers and times taken for writing and reading (see table S3 and S4). The per-sample and per-task energy consumption are only 1.16 μJ and 23.1 mJ for devices. The second part is the energy required to compute the output weight matrix W_{out} . Using two Python libraries (*psutil* and *threading*), we monitored accurately the live CPU usages during task computation (U_{task}) and idle status (U_0) and task time (t_{task}). We also find the thermal design power (P_{TDP}) of our CPU (Intel i7-11370H) from the manufacturer. Then the energy consumed by CPU is estimated as $(U_{task} - U_0) \times P_{TDP} \times t_{task}$, giving 0.212 mJ per sample and 4.25 J per task. Although the total energy consumption per sample is dominated by the CPU, it is still fairly low in table S6. Next, we perform the digit recognition task using the classic echo state network (Fig. 3A, red arrow) with the **same reservoir size** and **same number of samples** on the **same computer**. The per-sample and per-task energy are 51.0 mJ and 1.02 kJ, respectively, which are two orders of magnitude higher than the spintronic approach. In addition, we also perform the digit recognition task using the state-of-the-art feedforward neural network and backpropagation (3 layers with 10 neurons in the hidden layer)(41). The energy consumption is lower than software implementation of RC (due to a smaller network size) but 19 times higher than our spintronic approach. Such a huge gap is expected since there are far more matrix manipulations in software-based approaches.

Figures S1-S8

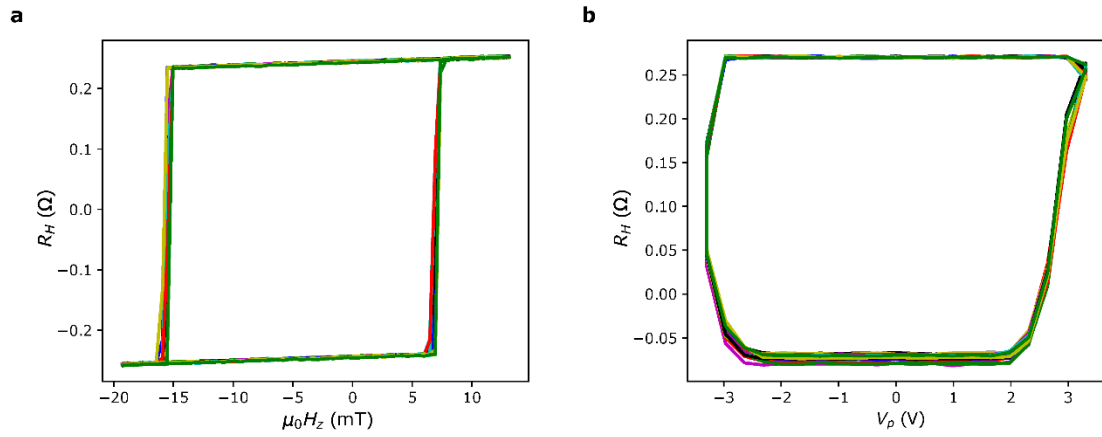


Figure S1. Switching behaviour of 14 Hall bars. (a) R_H - H_z with a field step of 0.5 mT. (b) Field-free switching (R_H - V_p) with $\tau_p = 200$ ns and maximum amplitude of V_p is 3.3 V.

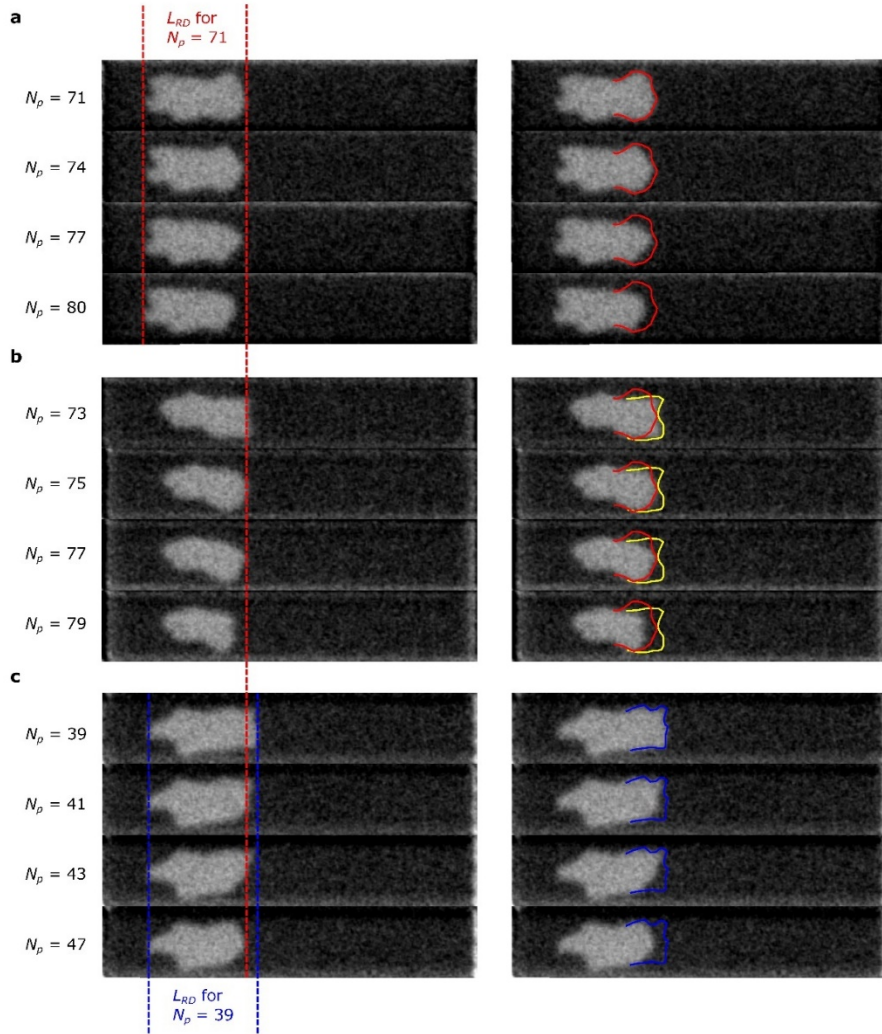


Figure S2. MOKE image frames. (a) $\tau_p = 80$ ns. (b) Repeated measurement for $\tau_p = 80$ ns on the same device as in (a). (c) $\tau_p = 120$ ns. Dotted lines mark the domain wall positions for $N_p = 71$ in (a)(red) and $N_p = 39$ in (c)(blue). The coloured contours in the right column highlight the shape of the domain walls for $N_p = 71$ in (a)(red), $N_p = 73$ in (b)(yellow) and $N_p = 39$ in (c)(blue).

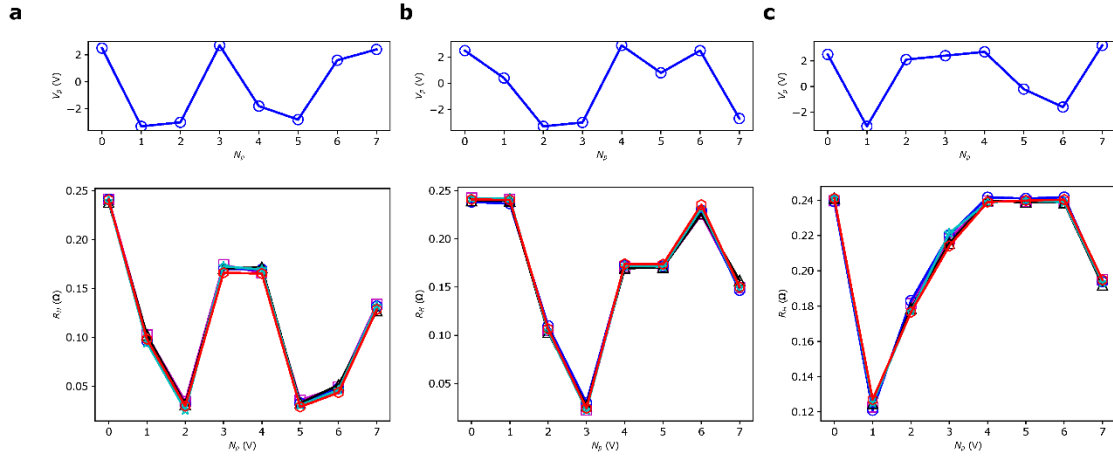


Figure S3. Highly repeatable readout from spintronic memristor. Readout (bottom) of a single device from 5 repeats of the same pulse sequence (top). (a) Sequence 1: maximum $V_p = 2.7$ V, minimum $V_p = -3.3$ V (b) Sequence 2: maximum $V_p = 2.9$ V, minimum $V_p = -3.3$ V. (c) Sequence 3: maximum $V_p = 3.2$ V, minimum $V_p = -3.1$ V.

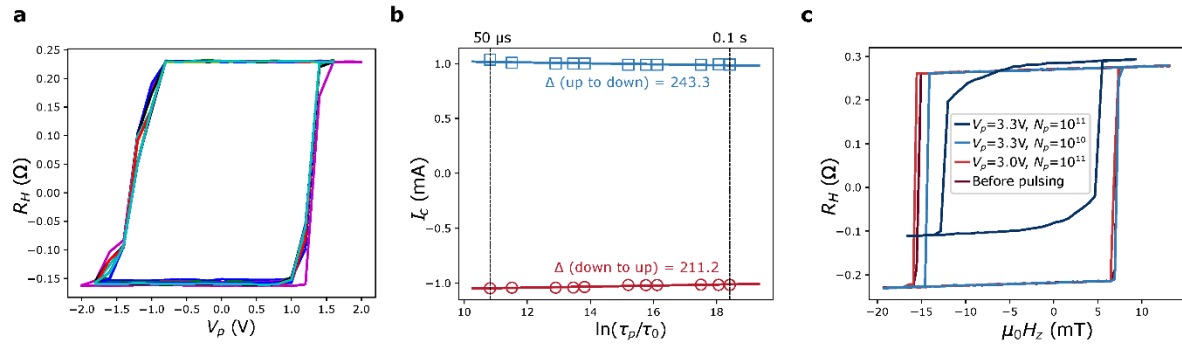


Figure S4. Estimation of thermal stability and endurance. (a) Pulsed switching with $50 \mu s \leq \tau_p \leq 0.1$ s. (b) Critical switching current (I_c) extracted from (a) as a function of $\ln(\tau_p/\tau_0)$. Lines are linear fits. (c) Magnetic hysteresis loop measured before pulsing and after different pulse trains. $\tau_p = 200$ ns.

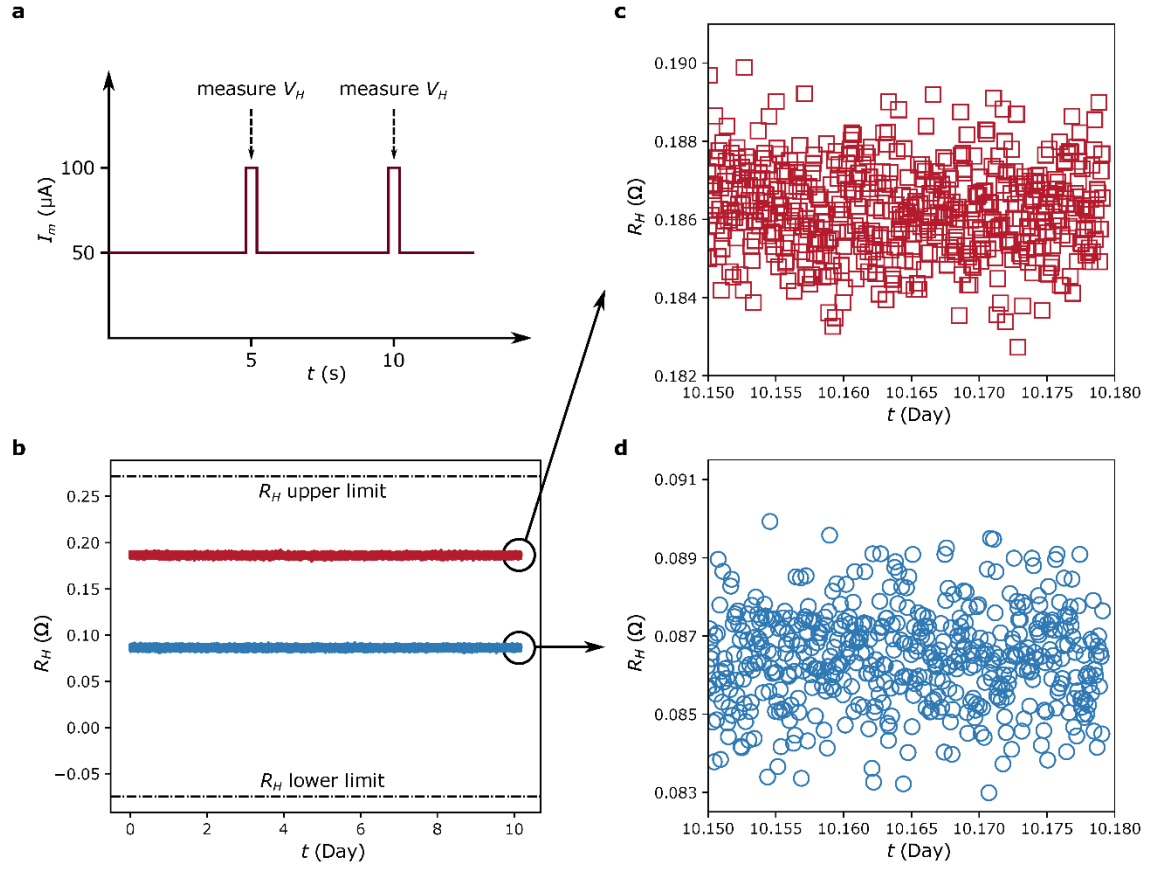


Figure S5. Data retention of Hall bar devices. (a) Schematic illustration of measurement procedures. (b) Continuous measurement of two intermediate R_H states over 10 days. (c-d) Enlarged view of the two states in (b) after 10 days.

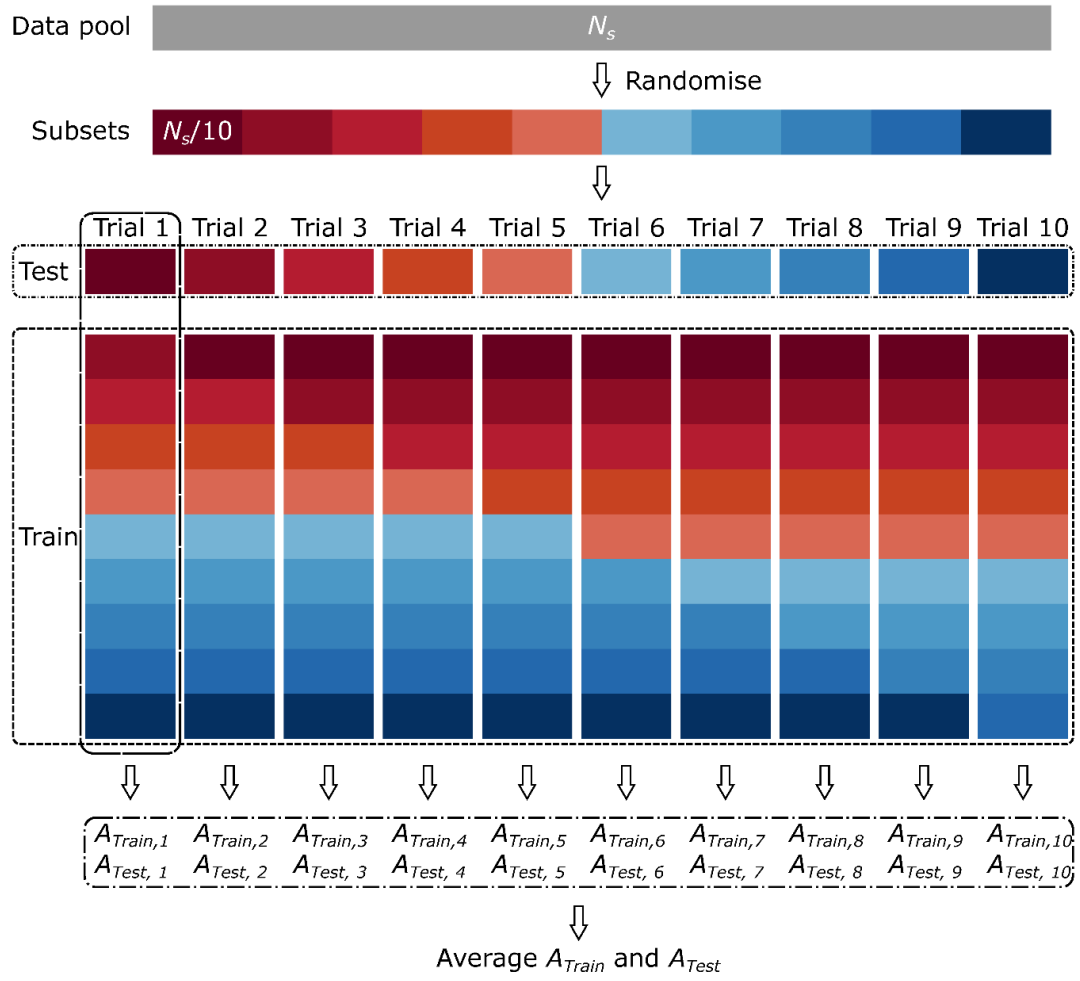


Figure S6. Illustration of 10-fold cross validation.

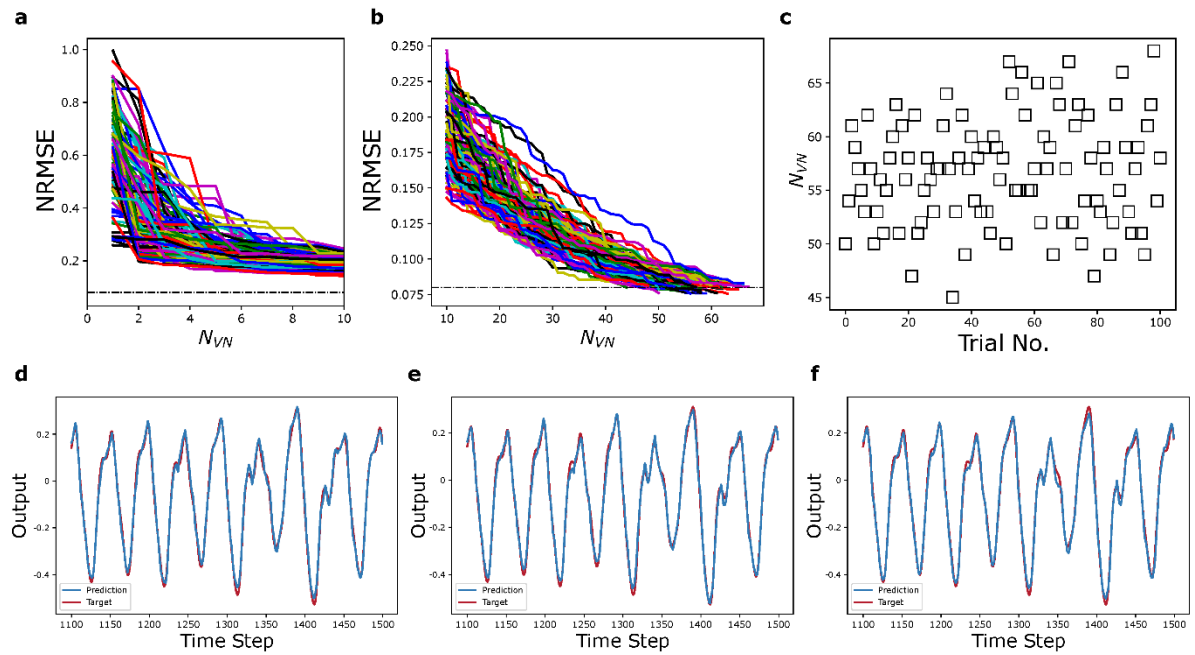


Figure S7. Additional results on Mackey-Glass time series prediction. (a-b) Reduction in NRMSE as number of VNs increases in all 100 trials. (c) Final number of VNs in all trials. (d-f) Final prediction in trial 10, 54 and 85.

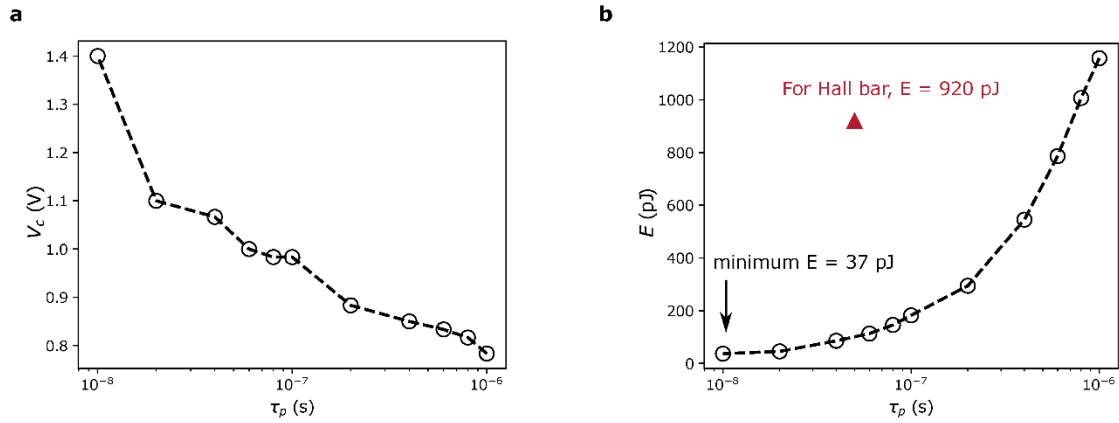


Figure S8. Switching in 240-nm SOT-MTJ. (a) Dependence of critical switching voltage (V_c) on pulse width (τ_p) in SOT-MTJ. (b) Dependence of switching energy on τ_p .

Tables S1-S6

Table S1. Illustration of linear mapping. It is assumed the raw inputs are between 1 and -1.

Input	DR1 (100 ns < τ_p < 200 ns)		DR2 (50 ns < τ_p < 100 ns)	
	V_p (V)	τ_p (ns)	V_p (V)	τ_p (ns)
0.1	2.8	110	2.8	55
0.5	2.8	150	2.8	75
-0.3	-3.0	130	-3.0	65
-0.5	-3.0	150	-3.0	75

Table S2. Comparison of task performance in our work with prior reports.

S/N	hardware	MNIST written digit classification					Mackey-Glass time series prediction				Ref
		Physical Node	Train size	Test size	Binarize	A_{test}	Physical Node	Train size	Test size	NRMSE	
1	Metal oxide	88	14k	2k	Yes	0.881	-	-	-	-	22
2	Ferroelectrics	22	60k	10k	Yes	0.895	-	-	-	-	25
3	Optics	-	-	-	-	-	1	2400	800	0.4	23
4	Ag nanowire	196	60k	10k	Yes	0.900	98	900	100	0.00884*	67
5	Metal oxide	-	-	-	-	-	20	450	300	N.A.	39
6	Circuitry	-	-	-	-	-	64	1440	1440	0.03-0.17	66
7	Spin vortex ice	-	-	-	-	-	397	393	271	0.00275*	68
8	Spintronic memristor	14	18k	2k	No	0.903	14	1000	400	0.076	This work

*These are the MSE values. The NRMSE scores were not reported. The lowest MSE in our work is 2.67×10^{-4} , which is one order of magnitude smaller.

Table S3. Speed of circuit components

Decoder	MUX	AMP	ADC	Total
200 ns	100 ns	9.5 μ s	15 ns	9.815 μ s

Table S4. Power consumption per operation of circuit.

Module	Write	Read	Remarks
DAC	0.225 mW	7.5 μ W	Write I (9 mA) is much larger than read I (1 mA)
MUX	12.04 mW	25.48 μ W	Total power includes the dynamic and static contribution. The dynamic I (8.4 mA or 60 μ A) is much larger than static I (1 nA). $N = 56$ based on number of transmission gate.
DUT	1.20 mW	0.98 nW	$N = 14$
AMP	16.00 μ W	250 μ W	$P_o = 400 \mu$ W, $N = 8$
ADC	0.25 mW	2.625 mW	Only static contribution for write ($I = 50 \mu$ A). Both dynamic ($I = 95 \mu$ A) and static contribution for read.
Total	13.73 mW	2.91 mW	Total power for one write-read operation is 16.64 mW

Table S5. Speed and power of different implementations RC.

Hardware	No. of neurons	Processing rate	Power	Ref.
ASIC	1000	926	11 mW	65
Metal oxide memristor	192	5000	22.2 μ W	24
Analogue circuits	64	10^7	4.7 mW	66
FPGA	48	10^6	1.5 W	62
FPGA	50	763	1.5 W	63
FPGA	50	1142	83 mW	64
Photonics	388	1.3×10^7	150 W	38
Spintronics	57	10^5	16.64 mW	This work

Table S6. Summary of the energy consumption in the state-of-the-art implementation of AI tasks using CPU and GPU. RC: reservoir computing; LSTM-RNN: long short-term memory based recurrent neural network; CNN: convolutional neural network; FNN: feedforward neural network.

No.	Hardware	Tasks	Network	Energy/sample	Energy/task	Ref
1	CPU	speech recognition	RC	98.6 J	49.3 kJ	39
2	CPU	speech recognition	LSTM-RNN	0.223 mJ	>668 mJ	69
3	GPU	speech recognition	LSTM-RNN	16.2 μ J	>48.5 mJ	69
4	CPU	digit recognition	CNN	3.57 μ J	2.5 J	70
5	GPU	image classification	CNN	~250 mJ	300 kJ	72
6	GPU	node classification	RC	7.51 μ J	20.33 mJ	71
7	Spintronic memristor +CPU	digit recognition	RC	Device: 1.16 μ J CPU: 0.212 mJ Total: 0.213 mJ	Device: 23.1 mJ CPU: 4.25 J Total: 4.27 J	This work
8	CPU	digit recognition	RC	51.0 mJ	1.02 kJ	This work
9	CPU	digit recognition	FNN	4.07 mJ	285 J	This work

Movies S1-S3**Movie S1. Domain wall motion with a pulse width of 80 ns.****Movie S2. Domain wall motion with a pulse width of 140 ns.****Movie S3. Domain wall motion with a pulse width of 200 ns.**

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