ADVANCED ELECTRONIC MATERIALS

Supporting Information

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An Attention Mechanism-Based Adaptive Feedback Computing Component by Neuromorphic Ion Gated MoS_2 Transistors

*Chang Liu, Yanghao Wang, Teng Zhang, Rui Yuan, and Yuchao Yang**

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Material characterization and synapstic plasticity of MoS_2 transistor

Figure S1 depicts a detailed cross-section image of the electrode and the energy dispersive spectrometer (EDS) mapping of Ti, Au, Mo, S, and Si. This device has about 6-layers MoS_2. As shown in Figure S2a, The EPSC was measured by applying a fixed source–drain voltage of 100 mV alongside a series of voltage pulses of 100 ms duration and varying amplitudes (0.1, 0.5, 1.0, 2.0, and 3.0 V) to the gate electrode as an external action potential. A peak was reached by the EPSC at the end of the pulse, which increased with increasing voltage amplitude, and then it gradually decayed. In addition, the EPSC is also affected by the voltage pulse duration. As shown in Figure S2b, the EPSC increases as the duration time increases and then gradually decays. Synaptic transistors based on MoS_2 can exhibit both STP and LTP, with the transition from STP to LTP being triggered by applying a series of voltage pulses to the gate, as shown in Figure 1c, which is naturally analogous to biological synapses. The retention measurements, as shown in Figure S3, provided evidence of such a prolonged timescale of plasticity. Following the application of 100 gate pulses (2 V, 100 ms), it is possible to observe a prolonged potentiating state in MoS_2 synaptic transistors for >10000 s. The emergence of LTP can be explained by the intercalation of Li^+ ions into MoS_2. Furthermore, Figure S4 exhibits remarkable linearity and symmetry of the conductivity when responding to a continuous input of 100 enhancing (0.8 V, 200 ms) and suppressing (-0.4 V, 200 ms) gate pulses with an interval of 800 ms.

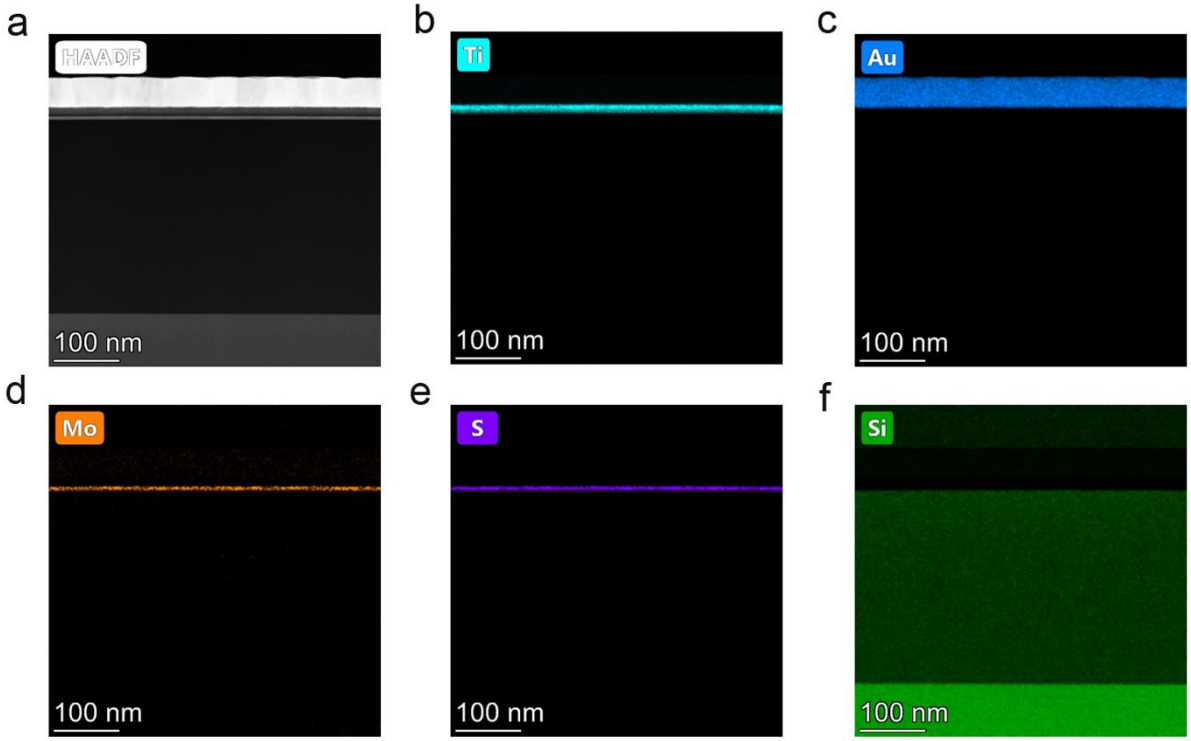

Figure S1. A detailed cross-section image of the electrode and the energy dispersive spectrometer (EDS) mapping of Ti, Au, Mo, S, and Si.

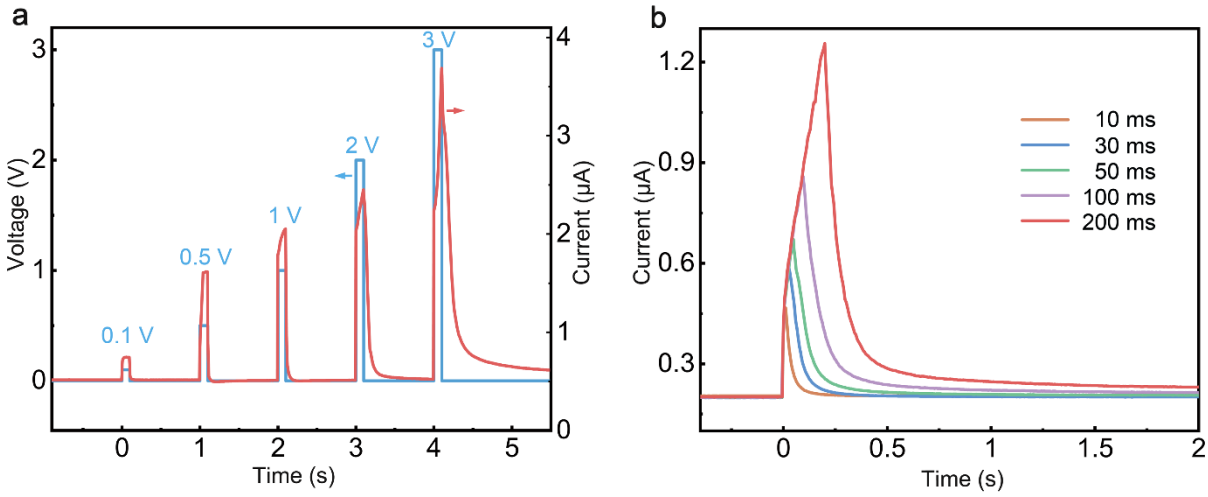

Figure S2. Short-term plasticity based on MoS_2 transistor. a) I_{ds} triggered by a series of gate voltage pulses with the same duration time (100 ms) and different amplitede (0.1, 0.5, 1.0, 2.0, and 3.0 V). b) I_{ds} triggered by gate voltages with same amplitude (V_g = 2.0 V) with different duration times (10, 30, 50, 100, and 200 ms).

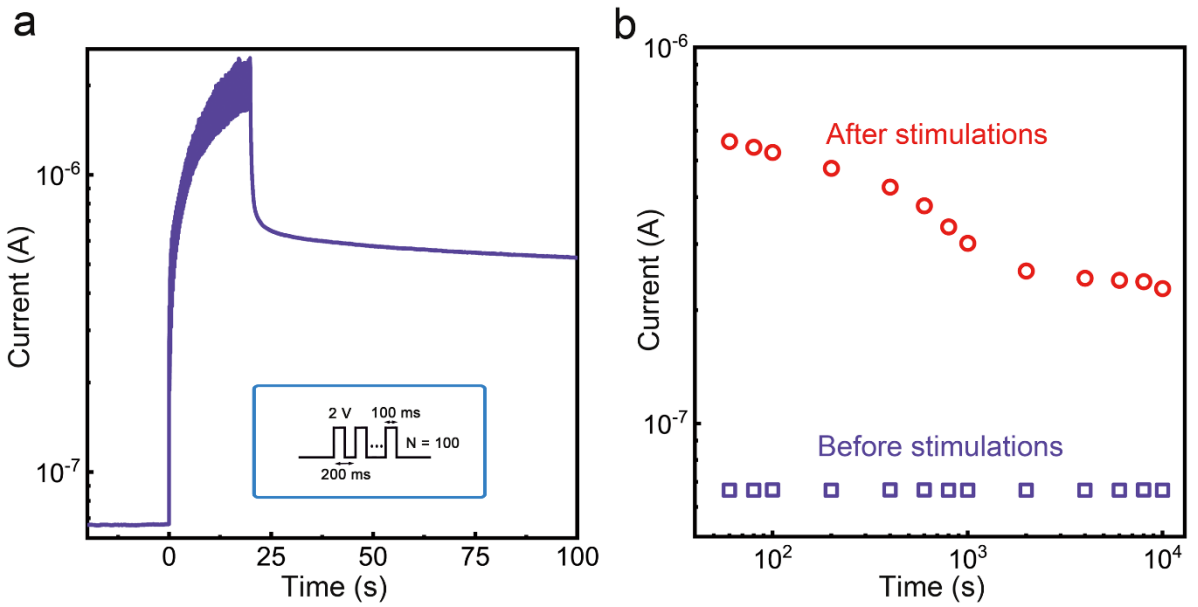

Figure S3. Long-term plasticity based on MoS_2 transistor. a) I_{ds} triggered by 100 gate pulses (2V, 100ms) with an interval of 100 ms. b) A remarkable long-term plasticity of synaptic transistors based on MoS_2 is demonstrated when gate pulse trains are applied.

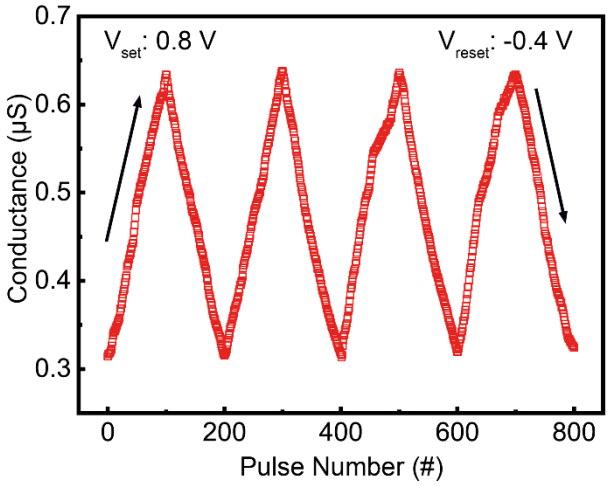

Figure S4. Analog incremental behavior realized by 100 potentiation (0.8 V, 200 ms) and depression (-0.4 V, 200 ms) gate pulses with an interval of 800 ms.

The magnitude of the gate current

As illustrated in Figure S5a and S5b, gate currents time-dependent for unbiased gate and biased gate at 2 V are measured, respectively. As can be seen, the current flowing through

the drain (I_d) and source (I_s) are approximately the same, so the gate current (I_g) can be ignored compared with I_d and I_s in both cases of V_g = 0 V (Figure S5a,c) and V_g = 2 V (Figure S5b,d), respectively. As shown in Figure S5a,c, when V_g = 0 V, Ig is less than ~pA level, but increases to less than ~nA with a gate voltage of 2 V due to a Li^+ ion migration and possible reactions (Figure S5b,d). In comparison with I_d and I_s of about 700 nA (Fig. S5b,d), the gate current is still negligible.

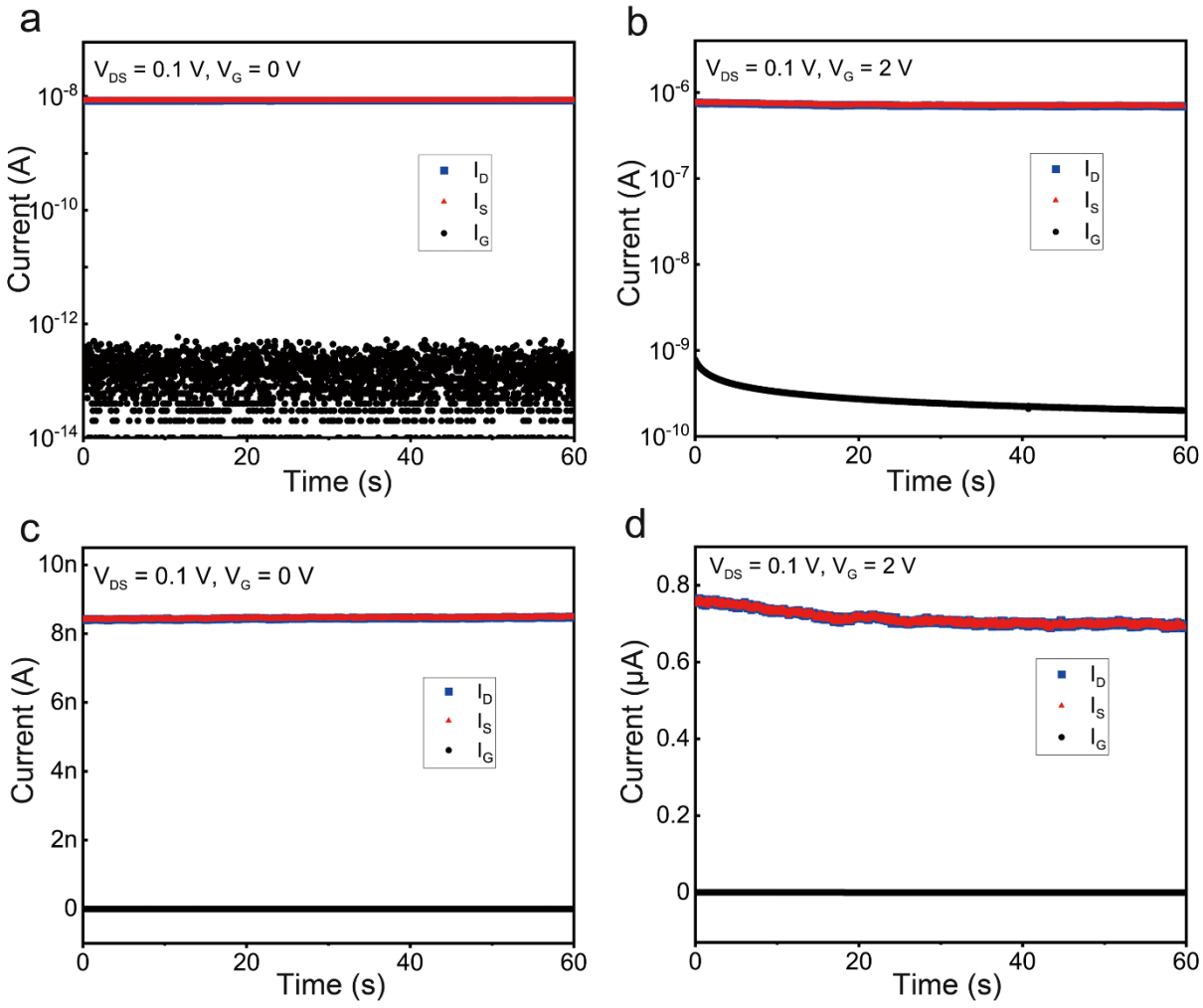

Figure S5. Source, drain, and gate current versus time, a) with the gate voltage unbiased (log scale), b) with the gate voltage biased at 2 V (log scale), c) with the gate voltage unbiased (linear scale), d) with gate voltage biased at 2 V (linear scale).

Energy consumption of MoS_2 transistor

We calculated the energy consumption of the spike in Figure S6. By scaling the amplitude and width of the pulses applied to the gate, the device exhibits ultralow energy consumption as low as ≈24 fJ per spike when a voltage pulse of 0.2 V is applied for 10 μs.

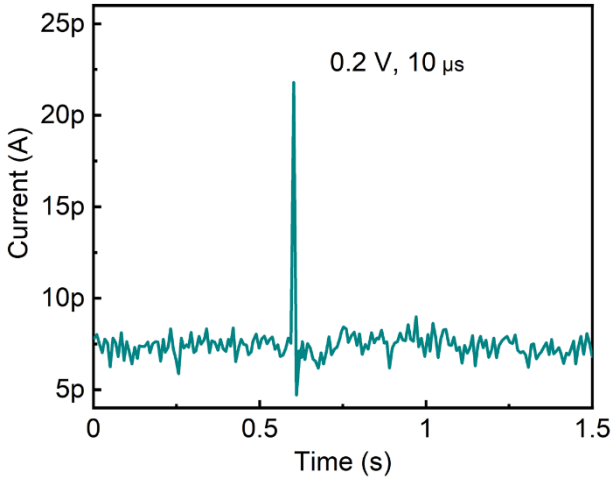

Figure S6. I_{ds} response when a voltage pulse of 0.2 V for 10 μs was applied to the gate.

Mechanism of the transition from short-term to long-term plasticity

The transition from STP to LTP is thought to be the result of a different physical or electrochemical process. In order to understand the mechanism of the transition, we performed systematic cross-sectional TEM observations on MoS_2 transistors that had either STP (Figure S7a,b) or LTP (Figure S7c,d) after applying pulse trains on the gate containing different numbers of pulses. When the MoS_2 channel is subjected to STP, the channel structure almost remains intact (Figure S7a,b); however, when MoS_2 is subjected to LTP, the channel structure changes distinctly (Figure S7c,d). The resulting MoS_2 structure is significantly different from the pristine state (**Figure 1**a) and the STP sample (Figure S7a,b). There is therefore a possibility that some of the Li+ arriving at the channel could have intercalated into MoS_2.

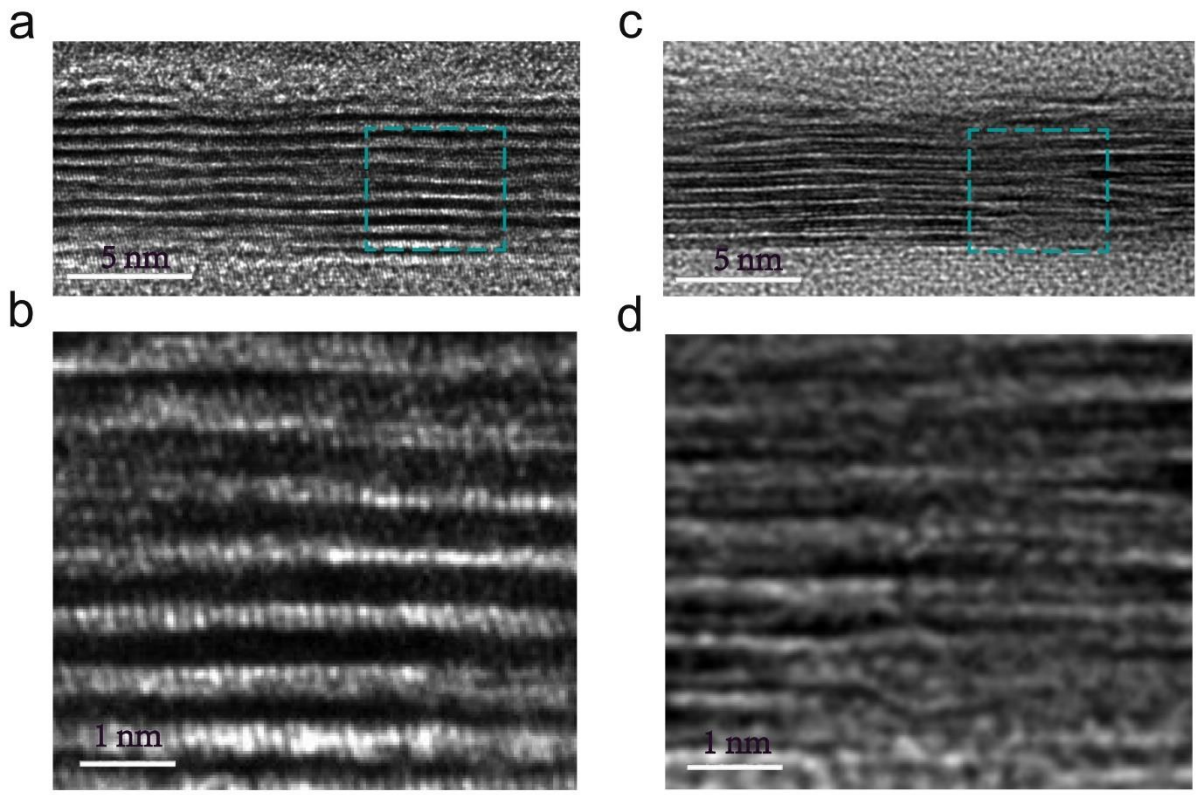

Figure S7. Analysis of microstructure reveals short-term to long-term plasticity transition. a) HRTEM imaging of MoS_2 channel in synaptic transistor showing STP with 50 gate pulses applied (2 V, 100 ms). the structure did not change significantly. b) Magnified HRTEM image of the rectangular area in panel (a). c) HRTEM imaging of MoS_2 channel in synaptic transistor showing LTP with 11000 gate pulses applied (2 V, 100 ms). Structure defects can be clearly identified as Li^+ is intercalated into the channels. d) Magnified HRTEM image of the rectangular area in panel (b).

Simulation details of attention computing component

The computing principle has been briefly introduced in Section 3.1, and the computing process is shown in Figure S8.

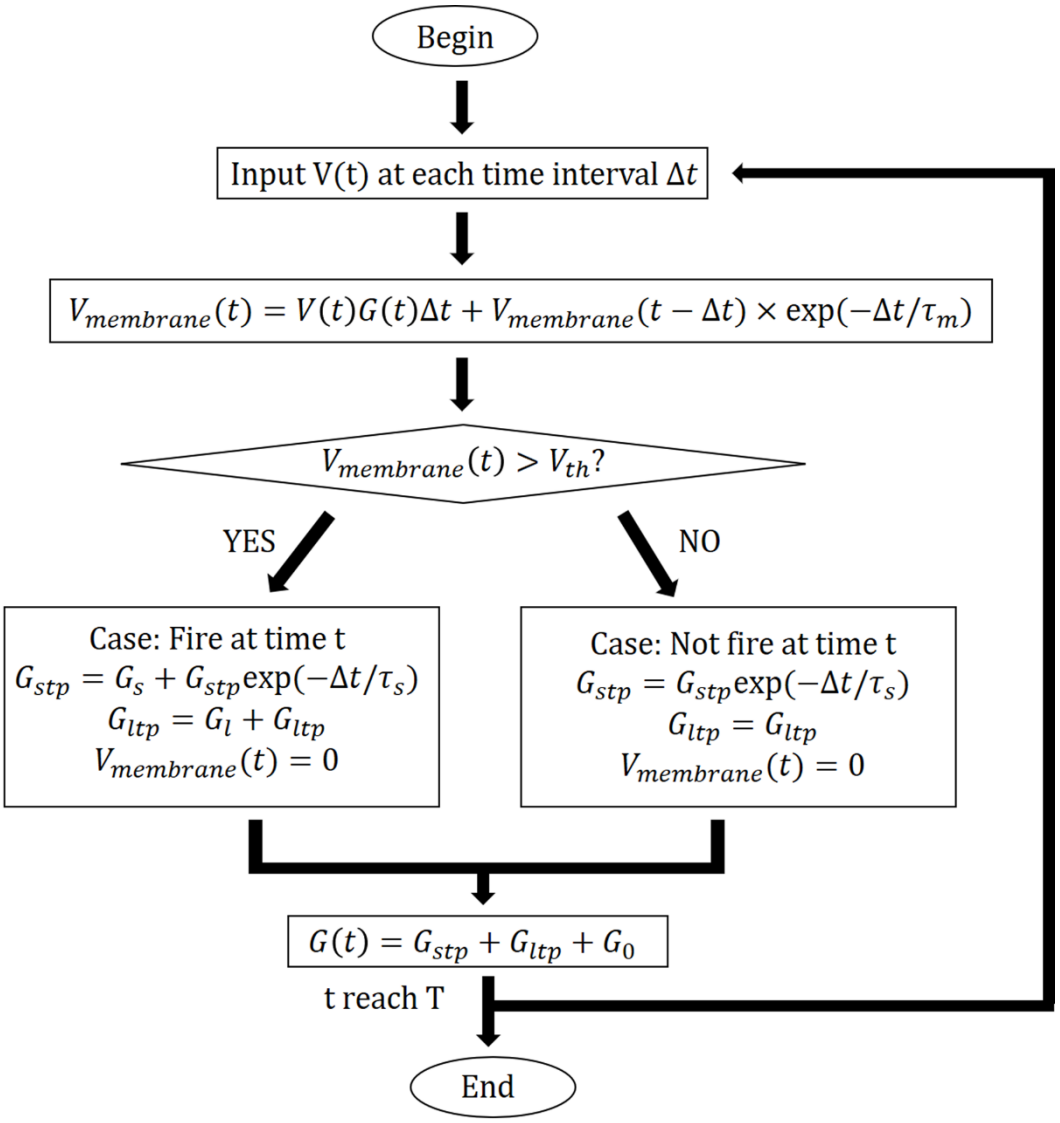

Figure S8. The chart of computing process about the attention component consisted of a synaptic transistor and a LIF neuron.

The parameter value in Figure 4 is G_0 = 0.25 μS, B = 0.0065 μS; A = 0.33e-6 μS; t_0 = 0.33 s; V_{th}=15e-5; τ_m = 10 s/τ_m = 0.5 s;

The corresponding four cases demonstrated in the experiment can also be verified by simulation, shown in Figure S9.

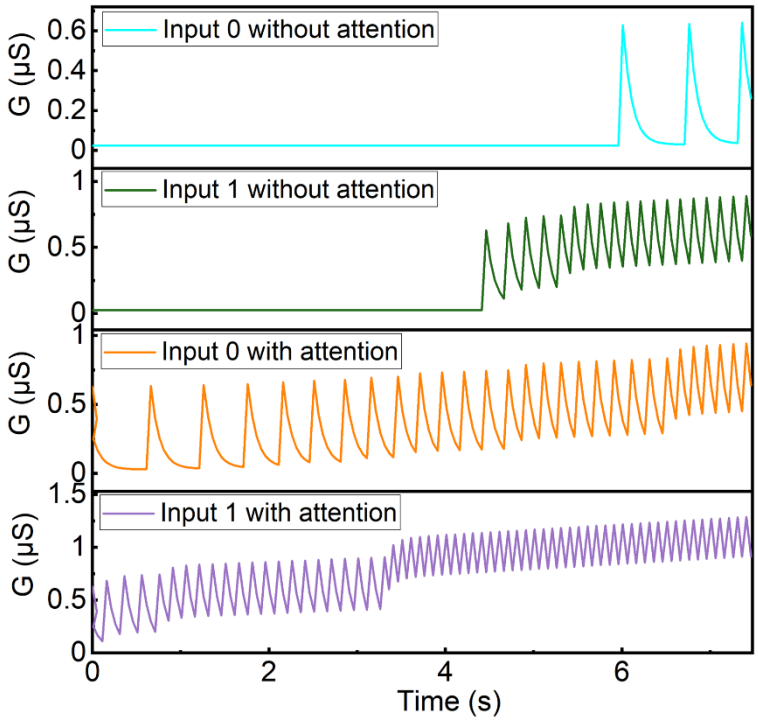

Figure S9. Conductance of synaptic transistor in four cases corresponding to input '1' or '0' with or without attention.