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Q.9 The Input devices can send information to the proces
- When the SIN status flag is set ✔
- When the data arrives regardless of the SIN flag
- Neither of the cases
- Either of the cases

Explanation: The input devices use buffers to store th ...essor.

Q.10 _____ bus structure is usually used to connect I/O
- Single bus ✔
- Multiple bus
- Star bus
- Rambus

Explanation: BUS is a bunch of wires which carry address, control signals and data. It is used to connect various components of the computer.

View Result

Analysis Of Test

Percentage: 100%

No. of Questions: 10	Answered Questions: 10
Unanswered Questions: 0	Marks: 10

See The Explanation

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Analysis Of Test

Percentage: 100%

No. of Questions: 10

Answered Questions: 10

Unanswered Questions: 0

Marks: 10

See The Explanation

Q.1 During the execution of the instructions, a copy of th

- Register
- RAM
- System heap
- Cache ✔

Explanation: None

Q.2 Two processors A and B have clock frequencies of 700 Mhz and 900 Mhz respectively. Suppose A can execute an instruction with an average of 3 steps and B can execute with an average of 5 steps. For the execution of the same instruction which processor is faster?

- A ✔
- B
- Both take the same time
- Insufficient information

Explanation: The performance of a system can be found out using the Basic performance formula.

Q.3 A processor performing fetch or decoding o

Superscaling

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Analysis Of Test

Percentage: 100%

No. of Questions: 10

Answered Questions: 10

Unanswered Questions: 0

Marks: 10

See The Explanation

Q.1 The instruction, Add #45,R1 does _____

- Adds the value of 45 to the address of R1 and stores 4
- Adds 45 to the value of R1 and stores it in R1 ✔
- Finds the memory location 45 and adds that content t
- None of the mentioned

Explanation: The instruction is using immediate addre

Q.2 In the case of, Zero-address instruction method the operands are stored in _____

- Registers
- Accumulators
- Push down stack ✔
- Cache

Explanation: In this case, the operands are implicitly loaded onto the ALU.

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- Accumulators
- Push down stack ✔
- Cache

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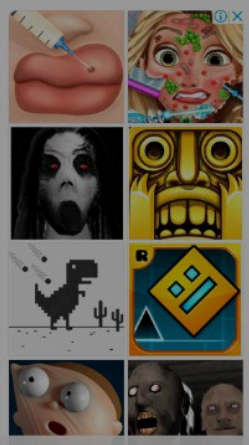
Q.3 Add #45, when this instruction is executed t

- The processor raises an error and requests
- The value stored in memory location 45 is rel



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Analysis Of Test

Percentage: 100%

No. of Questions: 10

Answered Questions: 10

Unanswered Questions: 0

Marks: 10

See The Explanation

Q.1 The main virtue for using single Bus structure is ____

- Fast data transfers
- Cost effective connectivity and speed
- Cost effective connectivity and ease of attaching peri
- None of the mentioned

Explanation: By using a single BUS structure we can m ost.

Q.2 _____ are used to overcome the difference in data transfer speeds of various devices.

- Speed enhancing circuitory
- Bridge circuits
- Multiple Buses
- Buffer registers ✔

Explanation: By using Buffer registers, the processor sends the data to the I/O device at the processor speed and the data gets stored in the buffer. After that the data gets sent to or from the buffer to the devices at the device speed.

Q.3 To extend the connectivity of the processor

PCI bus ✔