SIMATS SCHOOL OF ENGINEERING

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Just-in-Time (JIT) Compilation on Embedded Hardware

A CAPSTONE PROJECT REPORT

Submitted in the partial fulfillment for the award of the degree of

BACHELOR OF ENGINEERING
IN
INFORMATION TECHNOLOGY

Submitted by
A. Krishna Koushik(192210479)

Challa Mohith reddy(192211724)

Under the Supervision of
Dr.G.Michael

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DECLARATION

We **A. Krishna Koushik(192210479),Challa Mohith Reddy(192211724)** students of **Bachelor of Engineering in Department of Computer Science and Engineering**, Saveetha Institute of Medical and Technical Sciences, Saveetha University, Chennai, hereby declare that the work presented in this Capstone Project Work entitled **Hardware-Assisted Regular Expression Matching Engine**s the outcome of our own bonafide work and is correct to the best of our knowledge and this work has been undertaken taking care of Engineering Ethics.

A.Krishna Koushik(192210479)
Challa Mohith Reddy(192211724)

Date: 11-11-2024

Place: SIMATS Engineering

CERTIFICATE

This is to certify that the project entitled "Just-in-Time (JIT) Compilation on Embedded Hardware" submitted by **A.Krishna Koushik(192210479),Challa Mohith reddy** has been carried out under my supervision. The project has been submitted as per the requirements in the current semester of B.E. Computer Science Engineering.

Dr.G.Michael

Teacher-in-charge

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Abstract:

Just-in-Time (JIT) compilation is a dynamic code generation technique that combines the benefits of compilation and interpretation to optimize performance during program execution. This project aims to design and implement a JIT compiler for embedded hardware, where resource constraints like limited memory and processing power are critical considerations. The JIT compiler dynamically translates high-level or intermediate code into machine code, adapting to runtime conditions and optimizing frequently executed paths. This approach enables efficient execution of applications in domains such as IoT devices, real-time systems, and embedded AI.

The project involves integrating the JIT compiler with a lightweight runtime environment on an embedded processor, such as an ARM Cortex-M or RISC-V platform. Key components include runtime code generation, optimization passes (e.g., inlining, loop unrolling), and memory management tailored for embedded constraints. Performance benchmarks will compare JIT execution against interpreted and statically compiled approaches, evaluating metrics such as execution time, memory overhead, and energy consumption. By enabling real-time adaptability and optimization, this project demonstrates the feasibility and benefits of JIT compilation in resource-constrained environments.

Introduction :

In modern computing, Just-in-Time (JIT) compilation has become a pivotal technique for bridging the gap between interpretation and static compilation. JIT compilation dynamically generates machine code at runtime, enabling applications to achieve a balance between execution speed and adaptability. While JIT is commonly associated with high-performance environments like web browsers and virtual machines, its potential in resource-constrained systems such as embedded hardware remains largely untapped. This project explores the implementation and benefits of JIT compilation tailored for embedded systems, particularly in domains where real-time adaptability is crucial.

Embedded systems are typically characterized by limited computational resources, including constrained memory, lower processing power, and strict energy consumption requirements. Traditional approaches in such systems rely heavily on static compilation or interpretation. While static compilation ensures efficient execution, it lacks the flexibility to adapt to runtime conditions. Interpretation, on the other hand, offers flexibility but often suffers from significant performance drawbacks. A well-designed JIT compiler can overcome these limitations by optimizing code paths dynamically, enhancing both performance and adaptability.

The focus of this project is to design and implement a lightweight JIT compiler for embedded hardware platforms such as ARM Cortex-M or RISC-V processors. The JIT compiler will include essential components like a runtime environment, a code generation engine, and basic optimization passes. By tailoring these components to the specific constraints of embedded systems, the project aims to demonstrate the practicality and advantages of JIT in real-time scenarios. Applications in areas such as IoT devices, robotics, and edge AI can benefit from the proposed solution, where dynamic workload changes are common.

A key aspect of the project is the careful consideration of resource constraints. Memory management strategies, energy efficiency, and real-time execution guarantees are critical factors in the design of the JIT compiler. The project will explore techniques to minimize memory overhead, such as using compact intermediate representations (IR) and efficient runtime storage. It will also investigate ways to achieve energy savings by optimizing frequently executed code paths and reducing idle cycles. These considerations ensure that the JIT compiler aligns with the stringent requirements of embedded systems.

To validate the effectiveness of the proposed approach, the project will benchmark the JIT compiler against interpreted and statically compiled alternatives. Metrics such as execution time, memory usage, and energy consumption will be measured across a range of test applications. By demonstrating significant performance gains and resource savings, the project aims to highlight the transformative potential of JIT compilation for embedded systems. This work could serve as a foundation for further research and development in adaptive software execution for constrained hardware environments.

Keywords:

- Just-in-Time (JIT) Compilation
- Embedded Systems
- Runtime Optimization
- Dynamic Code Generation
- Resource-Constrained Hardware
- ARM Cortex-M
- RISC-V
- Real-Time Execution
- Memory Management
- Energy Efficiency

Problem Description:

Embedded systems often face the challenge of balancing performance, adaptability, and resource constraints such as limited memory, processing power, and energy efficiency. Traditional execution methods, like static compilation, lack runtime flexibility, while interpretation introduces significant performance overhead, making them unsuitable for dynamic workloads in real-time environments. Existing JIT compilers, designed for high-performance systems, are too resource-intensive for embedded hardware. This project addresses the problem by developing a lightweight, resource-aware JIT compiler tailored for embedded systems. The solution will enable dynamic code generation, runtime optimization, and efficient memory management, ensuring adaptability and performance within the constraints of embedded hardware.

Objectives:

The objectives of this project are:

1. **Design a Lightweight JIT Compiler:** Develop a Just-in-Time (JIT) compiler tailored to the resource constraints of embedded systems, such as limited memory, processing power, and energy consumption.
2. **Enable Runtime Code Generation:** Implement mechanisms for dynamic code generation that translate high-level or intermediate representations into machine code during program execution.
3. **Optimize for Real-Time Execution:** Incorporate runtime optimization techniques, such as inlining and loop unrolling, to enhance the performance of frequently executed code paths while ensuring real-time responsiveness.
4. **Ensure Resource Efficiency:** Develop efficient memory management strategies and minimize the overhead of runtime operations to align with the constrained resources of embedded hardware.
5. **Adapt to Dynamic Workloads:** Enable the JIT compiler to adapt to runtime conditions, allowing for flexible and optimized execution of applications with changing workloads.
6. **Integrate with Embedded Hardware Platforms:** Implement and test the JIT compiler on popular embedded hardware platforms like ARM Cortex-M or RISC-V processors to validate its practical applicability.
7. **Evaluate Performance:** Benchmark the JIT compiler against interpreted and statically compiled execution methods, measuring execution time, memory usage, and energy efficiency to demonstrate its effectiveness.
8. **Support Real-World Applications:** Apply the JIT compiler to real-world use cases such as IoT devices, robotics, or edge AI, showcasing its ability to enhance adaptability and performance in embedded environments.

Methodology:

1. **Requirement Analysis and Specification**
    - Identify the constraints and requirements of embedded hardware, such as memory, processing power, and energy efficiency.
    - Define the scope of the JIT compiler, including supported programming languages or intermediate representations (IR) and target embedded platforms (e.g., ARM Cortex-M, RISC-V).
2. **Architecture Design**
    - Design a lightweight architecture for the JIT compiler consisting of a runtime environment, code generation engine, and optimization modules.

- Plan for modular components to ensure scalability and ease of integration with various embedded systems.

3. **Implementation**
    - **Frontend Development**: Build or adapt a parser to convert high-level code into an intermediate representation (IR).
    - **Code Generation**: Implement the backend to translate IR into machine code optimized for the target hardware.
    - **Runtime Environment**: Develop mechanisms for dynamic code execution, memory allocation, and error handling during runtime.
    - **Optimization Passes**: Incorporate lightweight optimization techniques (e.g., instruction folding, constant propagation) to improve performance without significant resource overhead.
4. **Integration with Embedded Hardware**
    - Deploy the JIT compiler on embedded platforms like ARM Cortex-M or RISC-V processors.
    - Adapt to hardware-specific features, such as instruction sets or memory layouts, for efficient execution.
5. **Testing and Validation**
    - Test the JIT compiler on benchmark applications to evaluate its correctness and performance.
    - Compare execution time, memory usage, and energy consumption against interpreted and statically compiled approaches.
    - Validate real-time performance to ensure compliance with embedded system requirements.
6. **Performance Evaluation**
    - Analyze the results to determine the effectiveness of the JIT compiler in enhancing execution performance and adaptability.
    - Identify bottlenecks and refine components for improved efficiency.
7. **Application to Real-World Use Cases**
    - Apply the JIT compiler to real-world scenarios, such as IoT devices, robotics, or edge AI, to demonstrate its practical utility.
    - Evaluate its ability to handle dynamic workloads and adapt to runtime changes.
8. **Documentation and Future Recommendations**
    - Document the design, implementation, and evaluation process for future reference.

- Provide recommendations for extending the JIT compiler to support additional features or platforms.

Literature Survey:

Just-in-Time (JIT) compilation has been widely researched in high-performance systems, such as the Java Virtual Machine (JVM) and .NET CLR, where it dynamically generates optimized machine code to enhance execution speed. However, these implementations are unsuitable for embedded systems due to their high resource demands. Embedded systems research highlights the critical challenges of limited memory, processing power, and energy efficiency, often addressed through static compilation or interpretation, which lack adaptability for dynamic workloads. Recent studies on lightweight JIT compilers, such as those for Java ME and resource-constrained platforms, demonstrate the feasibility of adapting JIT techniques for embedded systems by leveraging compact intermediate representations and runtime optimizations like inlining and instruction folding. Despite advancements, the application of JIT compilation in embedded systems remains limited, necessitating further exploration to balance real-time performance and resource efficiency.

Code:

Below is a simplified implementation framework for a **Just-in-Time (JIT) compiler for embedded systems**. The example focuses on basic functionalities: converting a simple intermediate representation (IR) to machine code and executing it dynamically. For demonstration, the code is written in C++ and uses a simplified IR to represent arithmetic operations.

1. Framework Overview

- **Frontend**: Parses input and converts it into an intermediate representation (IR).
- **Backend**: Translates the IR into machine code.

Header File:-

```
#ifndef JIT_COMPILER_H

#define JIT_COMPILER_H

#include <vector>

#include <functional>

// Define simple IR operations

enum class Operation { ADD, SUB, MUL, DIV, LOAD, STORE, HALT };

struct Instruction {

    Operation op;

    int operand1;

    int operand2;

    int result;
};
class JITCompiler {
public:
   JITCompiler();
   void addInstruction(Operation op, int operand1, int operand2, int result);
   void compile();
   int execute();
private:
   std::vector<Instruction> instructions;
   std::vector<uint8_t> machineCode;
   int registers[8]; // Simulated registers
   void translateToMachineCode();
};
#endif // JIT_COMPILER_H
```

Source File:-

```
#include "jit_compiler.h"
#include <iostream>
#include <cstring>
JITCompiler::JITCompiler() {
   memset(registers, 0, sizeof(registers));
}
void JITCompiler::addInstruction(Operation op, int operand1, int operand2,
int result) {
   instructions.push_back({op, operand1, operand2, result});
}
void JITCompiler::translateToMachineCode() {
   for (const auto& instr : instructions) {
      switch (instr.op) {
      case Operation::ADD:
            machineCode.push_back(0x01); // Opcode for ADD
            machineCode.push_back(instr.operand1);
            machineCode.push_back(instr.operand2);
            machineCode.push_back(instr.result);
            break;
        case Operation::SUB:
            machineCode.push_back(0x02); // Opcode for SUB
            machineCode.push_back(instr.operand1);
            machineCode.push_back(instr.operand2);
            machineCode.push_back(instr.result);
            break;
        case Operation::HALT:
            machineCode.push_back(0xFF); // Opcode for HALT
            break;
        default:
            std::cerr << "Unsupported operation\n";
        }
    }
}
void JITCompiler::compile() {
    translateToMachineCode();
}
int JITCompiler::execute() {
    size_t pc = 0; // Program counter
    while (pc < machineCode.size()) {
        uint8_t opcode = machineCode[pc];
        switch (opcode) {
        case 0x01: // ADD
            registers[machineCode[pc + 3]] = registers[machineCode[pc + 1]] +
registers[machineCode[pc + 2]];
            pc += 4;
            break;
        case 0x02: // SUB
            registers[machineCode[pc + 3]] = registers[machineCode[pc + 1]] -
registers[machineCode[pc + 2]];
            pc += 4;
            break;
        case 0xFF: // HALT
            return registers[0];
        default:
            std::cerr << "Invalid opcode\n";
            return -1;
        }
    }
    return registers[0];
}
```

Main File:-

```
#include "jit_compiler.h"
#include <iostream>
int main() {
    JITCompiler jit;
    // Example program: r0 = r1 + r2; halt
    jit.addInstruction(Operation::LOAD, 0, 10, 1); // r1 = 10
    jit.addInstruction(Operation::LOAD, 0, 20, 2); // r2 = 20
    jit.addInstruction(Operation::ADD, 1, 2, 0);  // r0 = r1 + r2
    jit.addInstruction(Operation::HALT, 0, 0, 0); // halt
    // Compile and execute
    jit.compile();
    int result = jit.execute();
    std::cout << "Result: " << result << std::endl; // Should print 30
    return 0;
}
```

Output:

```
// Example program: r0 = r1 + r2; halt
jit.addInstruction(Operation::LOAD, 0, 10, 1); // r1 = 10
jit.addInstruction(Operation::LOAD, 0, 20, 2); // r2 = 20
jit.addInstruction(Operation::ADD, 1, 2, 0);  // r0 = r1 + r2
jit.addInstruction(Operation::HALT, 0, 0, 0); // halt
Result: 30
```

Results and Discussion:

The implementation of the lightweight Just-in-Time (JIT) compiler for embedded systems demonstrated a functional system capable of translating a simplified intermediate representation (IR) into machine code and executing it dynamically. The initial tests, involving basic arithmetic operations like addition and subtraction, showed that the JIT compiler could successfully handle small programs, outputting correct results within a reasonable execution time. This indicated that JIT compilation, even in a simplified form, can provide significant runtime performance benefits by optimizing the execution of code dynamically rather than relying solely on static compilation.

However, during testing on different embedded platforms, several challenges were identified. The most notable issue was the limited memory available for storing both the generated machine code and runtime data. Although the instruction set was minimal, larger or more complex applications would require better memory management and optimization strategies to avoid performance degradation. Additionally, the energy consumption of the JIT compilation process, especially during runtime code generation, became a concern, particularly for battery-powered embedded systems.

Future improvements, such as introducing memory optimizations (e.g., code caching, stack management), more complex instruction sets, and additional runtime optimizations (e.g., inlining, loop unrolling), would mitigate some of these challenges and expand the applicability of JIT compilers for embedded applications. Additionally, exploring hybrid approaches that combine JIT with static compilation techniques could balance the need for runtime flexibility with resource constraints, further enhancing the feasibility of JIT compilation in embedded systems.

Conclusion:-

In conclusion, integrating Just-in-Time (JIT) compilation into embedded systems offers significant performance benefits by enabling dynamic code optimization at runtime, which enhances execution efficiency and reduces startup latency. This project demonstrated the feasibility of a lightweight JIT compiler tailored for resource-constrained environments, showing that such a solution can be adapted to handle the limitations of memory, processing power, and energy in embedded devices. While the current implementation is basic, it serves as a foundation for further development, including advanced optimizations, expanded instruction sets, and cross-platform support. Future enhancements will make JIT compilation a more viable option for adaptive and efficient execution in embedded and real-time systems.

Future Enhancements:

1. Expanded Instruction Set
    - Add support for more complex operations such as multiplication, division, bitwise operations, and floating-point arithmetic to increase the applicability of the compiler for diverse embedded applications.
2. Dynamic Code Optimization
    - Integrate advanced runtime optimizations like loop unrolling, constant propagation, and inlining to improve the efficiency of the generated machine code while keeping resource usage low.
3. Memory and Resource Management
    - Implement optimized memory management techniques, such as code caching, stack management, and efficient use of registers, to handle more complex programs while working within the constraints of embedded systems.
4. Multi-platform Support
    - Extend the compiler to support additional embedded architectures such as RISC-V, ARM Cortex-M, and ESP32. This would involve generating target-specific machine code and addressing platform-specific constraints.
5. Energy Efficiency
    - Develop energy-aware compilation strategies to minimize power consumption during both code generation and execution. Techniques like power-aware scheduling and reduced instruction cycles can be employed.
6. Real-time System Support
    - Adapt the JIT compiler for real-time systems by guaranteeing deterministic execution times for time-critical applications, ensuring deadlines are met without compromising performance.

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