# HV7360/HV7361

## High-Speed ±100V 2.5A Two-or-Three-Level Ultrasound Pulsers

## Features

- HVCMOS® Technology for High Performance
- High Density Integration AC-coupled Pulser
- 0V to ±100V Output Voltage
- ±2.5A Source and Sink Minimum Pulse Current
- Up to 35 MHz Operating Frequency
- 2 ns Matched Delay Times
- 2.5V, 3.3V or 5V CMOS Logic Interface
- Built-in Two-terminal Low-noise Interface for HV7361
- Low Power Consumption and No Floating Power Supply Rails or Decoupling Capacitors

## Applications

- Medical Ultrasound Imaging
- Piezoelectric Transducer Drivers
- Ultrasound Industrial NDT
- Pulse Waveform Generator

## General Description

HV7360/HV7361 are high-voltage and high-speed pulse generators with built-in fast return-to-zero damping Field-Effect Transistors (FETs). An added feature to HV7361 is an integrated two-terminal low-noise T/R switch. These integrated circuits are designed not only for portable medical ultrasound image devices but also for NDT and test equipment applications.

Both HV7360/HV7361 are composed of controller logic interface circuits, level translators and AC-coupled Metal Oxide Semiconductor Field-Effect Transistor (MOSFET) gate drivers. They also have high-voltage and high-current P-channel and N-channel MOSFETs as output stages.

The peak output currents of each channel are guaranteed to be over ±2.5A with up to ±100V of pulse swing. The AC coupling topology for the gate drivers not only saves two floating voltage supplies but also makes the PCB layout easier.

## Package Type



**22-lead CABGA**
(Top View)
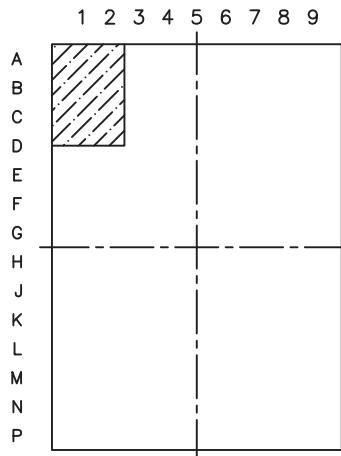
# HV7360/HV7361

## HV7360 Typical Application Circuit



**+/-100V 2.5A Three-level RTZ Transmit Pulsers**
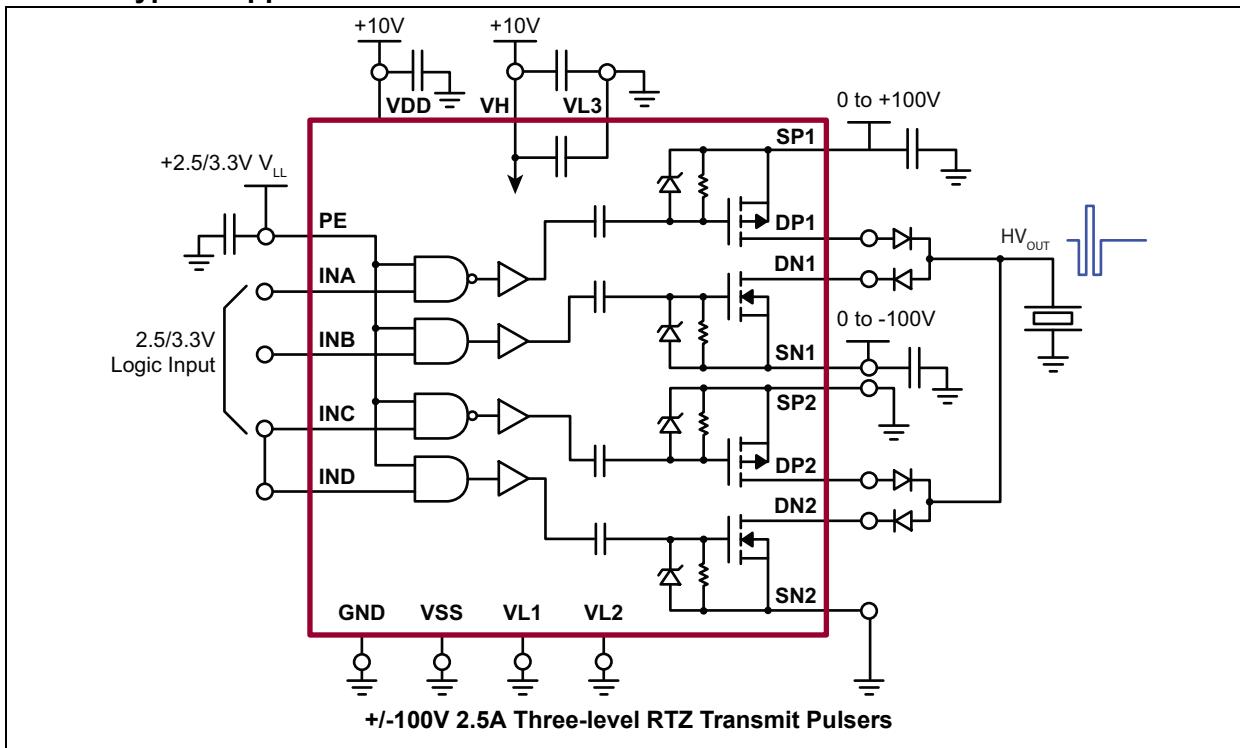
## HV7361 Typical Application Circuit



**+/-100V 2.5A Three-level RTZ Transmit Pulsers with T/R Switch**
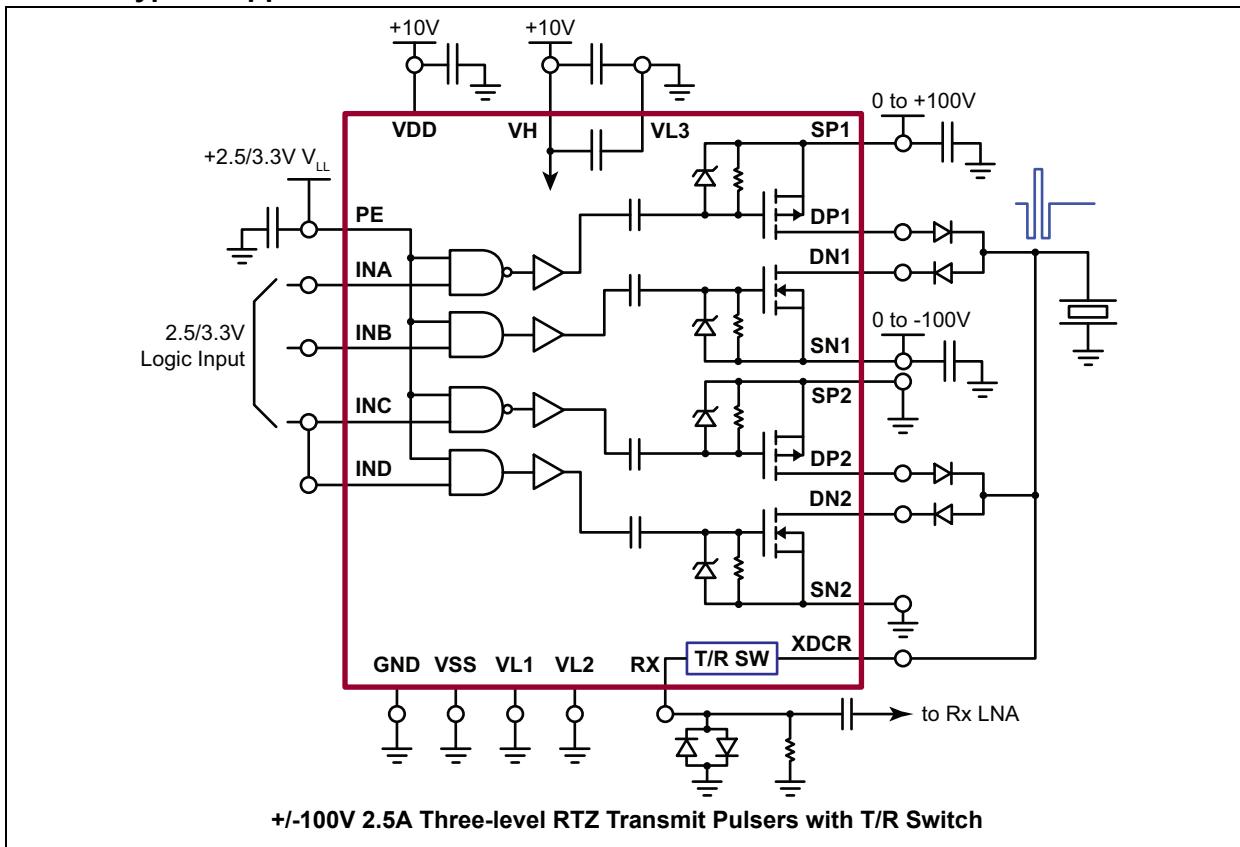
## 1.0    ELECTRICAL CHARACTERISTICS

### Absolute Maximum Ratings †

Chip Power Supply Voltage ($V_{DD}$-$V_{SS}$) ........................................................................................................ −0.5 to +12.5V
$V_H$ Output High Supply Voltage ..................................................................................... $V_L$−0.5 to $V_{DD}$ +0.5V
$V_L$ Output Low Supply Voltage.................................................................................... $V_{SS}$−0.5V to $V_H$ +0.5V
$V_{SS}$ Low Side Supply Voltage ............................................................................................................... −6 to +0.5V
Differential High Voltage ($V_{SP1}$-$V_{SN1}$), ($V_{SP2}$-$V_{SN2}$)................................................................................ +220V
$V_{SP1,2}$ Positive High Voltage ...............................................................................................................−0.5 to +110V
$V_{SN1,2}$ Negative High Voltage ...............................................................................................................+0.5 to −110V
All Logic Input Voltages.....................................................................................$V_{SS}$−0.5V to GND +5.5V
Rx to XDCR Differential Drop........................................................................................................... ±140V
Coupling Capacitor Breakdown Voltage.....................................................................................................±110V
Maximum Junction Temperature .................................................................................................................125°C
Operating Temperature ..................................................................................................................−20 to +85°C

> **† Notice:** Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at those or any other conditions above those indicated in the operational sections of this specification is not intended. Exposure to maximum rating conditions for extended periods may affect device reliability.

## OPERATING SUPPLY VOLTAGES AND CURRENT

**Electrical Specifications:** GND = 0V, $V_H$ = $V_{DD}$ = +10V, $V_L$ = $V_{SS}$ = 0V, $V_{PE}$ = 3.3V, $V_{PP}$ = +100V, $V_{NN}$ = −100V, $T_A$ = 25°C unless otherwise specified.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Logic Supply Voltage Range | $V_{LL}$ | 2.25 | — | 3.63 | V | |
| Supply Voltage | $V_{DD}$-$V_{SS}$ | 4.75 | — | 11.5 | V | 4 ≤ $V_{DD}$ ≤ 11.5V |
| Low Side Supply Voltage | $V_{SS}$ | −5.5 | — | 0 | V | |
| Gate Drive High Side Voltage | $V_H$ | $V_{SS}$+4 | — | $V_{DD}$ | V | $V_H$-$V_L$ ≥ 4V |
| Gate Drive Low Side Voltage | $V_L$ | $V_{SS}$ | — | $V_{DD}$-4 | V | |
| Output Positive High Voltage | $V_{SP1,2}$ | 0 | — | 100 | V | |
| Output Negative High Voltage | $V_{SN1,2}$ | −100 | — | 0 | V | |
| $V_{DD}$ Quiescent Current | $I_{DDQ}$ | — | 50 | — | µA | No input transitions, PE = 0 |
| $V_H$ Quiescent Current | $I_{HQ}$ | — | 2 | — | µA | |
| $V_{DD}$ Quiescent Current | $I_{DDQ}$ | — | 1 | — | mA | No input transitions, PE = 1 |
| $V_H$ Quiescent Current | $I_{HQ}$ | — | 2 | — | µA | |
| $V_{DD}$ Average Current | $I_{DD}$ | — | 4 | — | mA | One channel On at 5 MHz, No load |
| $V_H$ Average Current | $I_H$ | — | 10 | — | mA | |
| Input Logic Voltage High | $V_{IH}$ | $V_{PE}$-0.3 | — | $V_{PE}$ | V | For logic inputs INA, INB, INC and IND |
| Input Logic Voltage Low | $V_{IL}$ | 0 | — | 0.3 | V | |
| Input Logic Current High | $I_{IH}$ | — | — | 1 | µA | |
| Input Logic Current Low | $I_{IL}$ | — | — | 1 | µA | |
| PE Input Logic Voltage High | $V_{PEH}$ | 1.7 | 3.3 | 5.25 | V | For logic input PE |
| PE Input Logic Voltage Low | $V_{PEL}$ | 0 | — | 0.3 | V | |
| PE Input Impedance to GND | $R_{INPE}$ | 100 | — | — | kΩ | |

## AC ELECTRICAL CHARACTERISTICS

**Electrical Specifications**: GND = 0V, $V_H$ = $V_{DD}$ = +10V, $V_L$ = $V_{SS}$ = 0V, $V_{PE}$ = 3.3V, $V_{PP}$ = +100V, $V_{NN}$ = −100V, $T_A$ = 25°C unless otherwise specified.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Input or PE Rise and Fall Time | $t_{irf}$ | — | — | 10 | ns | Logic input edge speed requirement |
| Input to Output Delay | $t_{d1-4}$ | — | 7.5 | — | ns | $R_{LOAD}$ = 1Ω |
| Output Rise and Fall Time | $t_{r/f1-2}$ | — | 9.5 | — | ns | $C_{LOAD}$ = 330 pF, $R_{LOAD}$ = 2.5 kΩ |
| Rise and Fall Time Matching | $\Delta t_{rf}$ | — | 2 | — | ns | Channel to channel |
| Propagation Matching | $\Delta t_{dC2C}$ | — | 1 | — | | |
| Propagation Delay Matching | $\Delta t_{dD2D}$ | — | ±2 | — | ns | Device to device delay match |
| PE On-time | $t_{PE-ON}$ | — | — | 5 | μs | $V_{PE}$ = 1.7 ~ 5.25V, $V_{DD}$ = 7.5 ~ 11.5V, −20 ~ 85°C |
| PE Off-time | $t_{PE-OFF}$ | — | — | 4 | | |
| Output to MOSFET Gate Cap | $C_{OG}$ | — | 10 | — | nF | 100V X7S |
| $V_H$ to $V_{L3}$ Decoupling Cap | $C_{VH}$ | — | 0.22 | — | μF | 16V X7R |

## ELECTRICAL CHARACTERISTICS

**Electrical Specifications**: GND = 0V, $V_H$ = $V_{DD}$ = +10V, $V_L$ = $V_{SS}$ = 0V, $V_{PE}$ = 3.3V, $V_{PP}$ = +100V, $V_{NN}$ = −100V, $T_A$ = 25°C unless otherwise specified.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **PULSER AND DAMPING P-CHANNEL MOSFET** | | | | | | |
| **DC PARAMETERS** | | | | | | |
| Drain-to-source Breakdown Voltage | $BV_{DSS}$ | −200 | — | — | V | $V_{GS}$ = 0V, $I_D$ = −2 mA |
| Gate Threshold Voltage | $V_{GS(th)}$ | −1 | — | −2.4 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = −1 mA |
| Change in $V_{GS(th)}$ with Temperature | $\Delta V_{GS(th)}$ | — | — | 4.5 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = −1 mA |
| Gate-to-source Shunt Resistor | $R_{GS}$ | 10 | — | 50 | kΩ | $I_{GS}$ = 100 μA, if applied |
| Gate-to-source Zener Voltage | $V_{ZGS}$ | 13.2 | — | 25 | V | $I_{GS}$ = −2 mA, if applied |
| Zero-gate Voltage Drain Current | $I_{DSS}$ | — | — | −10 | μA | $V_{DS}$ = Maximum rating, $V_{GS}$ = 0V |
| | | — | — | −1 | mA | $V_{DS}$ = 0.8 maximum rating, $V_{GS}$ = 0V, $T_A$ = 125°C |
| ON-state Drain Current | $I_{D(ON)}$ | −1.2 | — | — | A | $V_{GS}$ = −5V, $V_{DS}$ = −25V |
| | | −2.3 | −2.5 | — | | $V_{GS}$ = −10V, $V_{DS}$ = −50V |
| Static Drain-to-source ON-state Resistance | $R_{DS(ON)}$ | — | — | 8.5 | Ω | $V_{GS}$ = −5V, $I_D$ = −150 mA |
| | | — | — | 7 | | $V_{GS}$ = −10V, $I_D$ = −1A |
| Change in $R_{DS(ON)}$ with Temperature | $\Delta R_{DS(ON)}$ | — | — | 1 | %/°C | $V_{GS}$ = −10V, $I_D$ = −1 mA |
| **AC PARAMETERS** | | | | | | |
| Forward Transconductance | $G_{FS}$ | 400 | — | — | mmho | $V_{DS}$ = −25V, $I_D$ = −500 mA |
| Input Capacitance | $C_{ISS}$ | — | 75 | — | pF | $V_{GS}$ = 0V, $V_{DS}$ = −25V, f = 1 MHz |
| Common Source Output Capacitance | $C_{OSS}$ | — | 21 | — | | |
| Reverse Transfer Capacitance | $C_{RSS}$ | — | 6.5 | — | | |
| **DIODE PARAMETERS** | | | | | | |
| Diode Forward Voltage Drop | $V_{SBD}$ | — | — | 1.8 | V | $V_{GS}$ = 0V, $I_{SD}$ = 500 mA |
| Reverse Recovery Time of Body Diode | $t_{rrBD}$ | — | 300 | — | ns | |
| **PULSER AND DAMPING N-CHANNEL MOSFET** | | | | | | |
| **DC PARAMETERS** | | | | | | |
| Drain-to-source Breakdown Voltage | $BV_{DSS}$ | 200 | — | — | V | $V_{GS}$ = 0V, $I_D$ = 2 mA |
| Gate Threshold Voltage | $V_{GS(th)}$ | 1 | — | 2.4 | V | $V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA |

## ELECTRICAL CHARACTERISTICS (CONTINUED)

**Electrical Specifications**: GND = 0V, $V_H$ = $V_{DD}$ = +10V, $V_L$ = $V_{SS}$ = 0V, $V_{PE}$ = 3.3V, $V_{PP}$ = +100V, $V_{NN}$ = −100V, $T_A$ = 25°C unless otherwise specified.

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Change in $V_{GS(th)}$ with Temperature | $\Delta V_{GS(th)}$ | — | — | −4.5 | mV/°C | $V_{GS}$ = $V_{DS}$, $I_D$ = 1 mA |
| Gate-to-source Shunt Resistor | $R_{GS}$ | 10 | — | 50 | kΩ | $I_{GS}$ = 100 µA |
| Gate-to-source Zener Voltage | $V_{ZGS}$ | 13.2 | — | 25 | V | $I_{GS}$ = 2 mA |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | — | — | 10 | µA | $V_{DS}$ = Maximum rating, $V_{GS}$ = 0V |
| | | — | — | 1 | mA | $V_{DS}$ = 0.8 maximum rating, $V_{GS}$ = 0V, $T_A$ = 125°C |
| ON-state Drain Current | $I_{D(ON)}$ | 1.3 | — | — | A | $V_{GS}$ = 5V, $V_{DS}$ = 25V |
| | | 2.3 | 2.5 | — | | $V_{GS}$ = 10V, $V_{DS}$ = 50V |
| Static Drain-to-source ON-state Resistance | $R_{DS(ON)}$ | — | — | 6.5 | Ω | $V_{GS}$ = 5V, $I_D$ = 150 mA |
| | | — | — | 6 | | $V_{GS}$ = 10V, $I_D$ = 1A |
| Change in $R_{DS(ON)}$ with Temperature | $\Delta R_{DS(ON)}$ | — | — | 1 | %/°C | $V_{GS}$ = 10V, $I_D$ = 1A |
| **AC PARAMETERS** | | | | | | |
| Forward Transconductance | $G_{FS}$ | 400 | — | — | mmho | $V_{DS}$ = 25V, $I_D$ = 500 mA |
| Input Capacitance | $C_{ISS}$ | — | 56 | — | | $V_{GS}$ = 0V, $V_{DS}$ = 25V, f = 1 MHz |
| Common Source Output Capacitance | $C_{OSS}$ | — | 13 | — | pF | |
| Reverse Transfer Capacitance | $C_{RSS}$ | — | 2 | — | | |
| **DIODE PARAMETERS** | | | | | | |
| Diode Forward Voltage Drop | $V_{SBD}$ | — | — | 1.8 | V | $V_{GS}$ = 0V, $I_{SD}$ = 500 mA |
| Reverse Recovery Time of Body Diode | $t_{rrBD}$ | — | 300 | — | ns | |

## HV7631 T/R SWITCH CHARACTERISTICS

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| Breakdown Voltage from XDCR to Rx | $B_{VA-B}$ | ±130 | — | — | V | $I_{A-B}$ = ±1 mA |
| Switch-on Resistance from XDCR to Rx | $R_{SW}$ | — | 15 | — | Ω | $I_{A-B}$ = ±5 mA |
| $V_{A-B}$ Trip Point to Turn Off | $V_{TRIP}$ | — | ±1 | ±2 | V | |
| Switch Turn-off Voltage | $V_{OFF}$ | — | ±2 | — | V | $I_{A-B}$ = ±1 mA |
| Switch-off Current | $I_{A-B(OFF)}$ | — | ±200 | ±300 | µA | $V_{A-B}$ = ±130V |
| Peak Switching Current | $I_{PEAK}$ | — | ±60 | — | mA | |
| Turn-off Time | $T_{OFF}$ | — | — | 20 | ns | |
| Turn-on Time | $T_{ON}$ | — | — | 20 | ns | |
| Switch-on Capacitance from A to B or B to A | $C_{SW(ON)}$ | — | 21 | — | pF | SW = On |
| Switch-off Capacitance from A to B or B to A | $C_{SW(OFF)}$ | — | 15 | — | pF | $V_{SW}$ = 25V |
| Small Signal Bandwidth | BW | — | 100 | — | MHz | $R_{LOAD}$ = 50Ω |

## TEMPERATURE SPECIFICATIONS

| Parameters | Sym. | Min. | Typ. | Max. | Units | Conditions |
|---|---|---|---|---|---|---|
| **Electrical Characteristics:** Unless otherwise noted, for all specifications $T_A = T_J = +25°C$. | | | | | | |
| **TEMPERATURE RANGES** | | | | | | |
| Maximum Junction Temperature | $T_{J(MAX)}$ | — | 125 | — | °C | |
| Operating Temperature | $T_A$ | −20 | — | +85 | °C | |
| **PACKAGE THERMAL RESISTANCE** | | | | | | |
| 22-Lead CABGA | $\theta_{JA}$ | — | 106 | — | °C/W | |

## POWER-UP AND POWER-DOWN SEQUENCE (Note 1)

| Power-Up | | Power-Down | |
|---|---|---|---|
| Step | Description | Step | Description |
| 1 | $V_{LL}$ | 1 | PE inactive |
| 2 | $V_{DD}$, $V_H$, $V_{SS}$ and $V_L$ with signal logic low | 2 | $V_{PP}$ and $V_{NN}$ off |
| 3 | $V_{PP}$ and $V_{NN}$ | 3 | $V_{DD}$, $V_H$, $V_{SS}$ and $V_L$ off |
| 4 | PE active | 4 | $V_{LL}$ off |

**Note 1:** Powering up or down in any arbitrary sequence will not cause any damage to the device. The power-up sequence and power-down sequence are only recommended to minimize possible inrush current.

## LOGIC CONTROL TABLE

| PE | Input Pulse | | | | Output MOSFETs | | | |
|---|---|---|---|---|---|---|---|---|
| | INA | INB | INC | IND | SP1 to DP1 | DN1 to SN1 | SP2 to DP2 | DN2 to SN2 |
| 1 | 1 | X | X | X | ON | X | X | X |
| | X | 1 | X | X | X | ON | X | X |
| | X | X | 1 | X | X | X | ON | X |
| | X | X | X | 1 | X | X | X | ON |
| | 0 | X | X | X | OFF | X | X | X |
| | X | 0 | X | X | X | OFF | X | X |
| | X | X | 0 | X | X | X | OFF | X |
| | X | X | X | 0 | X | X | X | OFF |
| 0 | X | X | X | X | OFF | OFF | OFF | OFF |

## 2.0   PAD DESCRIPTION

Table 2-1 details the description of pads in HV7360/HV7361.

**TABLE 2-1:   PAD FUNCTION TABLE**

| Pad Location | HV7360 Symbol | HV7361 Symbol | Description |
|---|---|---|---|
| A1 | GND | GND | Driver and level translator circuit ground return (0V) |
| A2 | IND | IND | Damping N-FET control signal logic input, controlling N-FET2 |
| A3 | INC | INC | Damping P-FET control signal logic input, controlling P-FET2 |
| A4 | $V_{SS}$ | $V_{SS}$ | Negative voltage power supply (0V) |
| A6 | $V_{DD}$ | $V_{DD}$ | Positive voltage supply (+10V), should connect to an external decoupling cap to $V_{SS}$ (0V) |
| A7 | INB | INB | Pulsing N-FET control signal logic input, controlling N-FET1 |
| A8 | INA | INA | Pulsing P-FET control signal logic input, controlling P-FET1 |
| A9 | PE | PE | Drive power enable Hi = On, Low = Off, logic '1' voltage reference input (+2.5V to +3.3V) |
| B2 | $V_{L2}$ | $V_{L2}$ | Gate-drive negative voltage power supply (0V) |
| B8 | $V_{L1}$ | $V_{L1}$ | Gate-drive negative voltage power supply (0V) |
| F4 | $V_H$ | $V_H$ | Gate-drive positive voltage power supply (+10V) |
| F7 | $V_{L3}$ | $V_{L3}$ | $V_H$ to $V_L$ decoupling cap. The trace connecting $V_{L1}$, $V_{L2}$, and $V_{L3}$ (0V) to ground plane should be as short as possible. |
| G4 | NC | — | No connection for HV7360 |
| | — | RX | T/R switch output for HV7361 |
| P1 | SP2 | SP2 | Source of P-FET2, positive high voltage power supply (0 to +100V) or GND |
| P2 | DP2 | DP2 | Drain of P-FET2, transmit pulser output |
| P3 | DN2 | DN2 | Drain of N-FET2, transmit pulser output |
| P4 | SN2 | SN2 | Source of N-FET2, negative high voltage power supply (0 to –100V) or GND |
| P5 | NC | — | No connection for HV7360 |
| | — | XDCR | T/R switch input for HV7361 |
| P6 | SP1 | SP1 | Source of P-FET1, positive high voltage power supply (0 to +100V) |
| P7 | DP1 | DP1 | Drain of P-FET1, transmit pulser output |
| P8 | DN1 | DN1 | Drain of N-FET1, transmit pulser output |
| P9 | SN1 | SN1 | Source of N-FET1, negative high voltage power supply (0 to –100V) |

# HV7360/HV7361

## 3.0    FUNCTIONAL DESCRIPTION
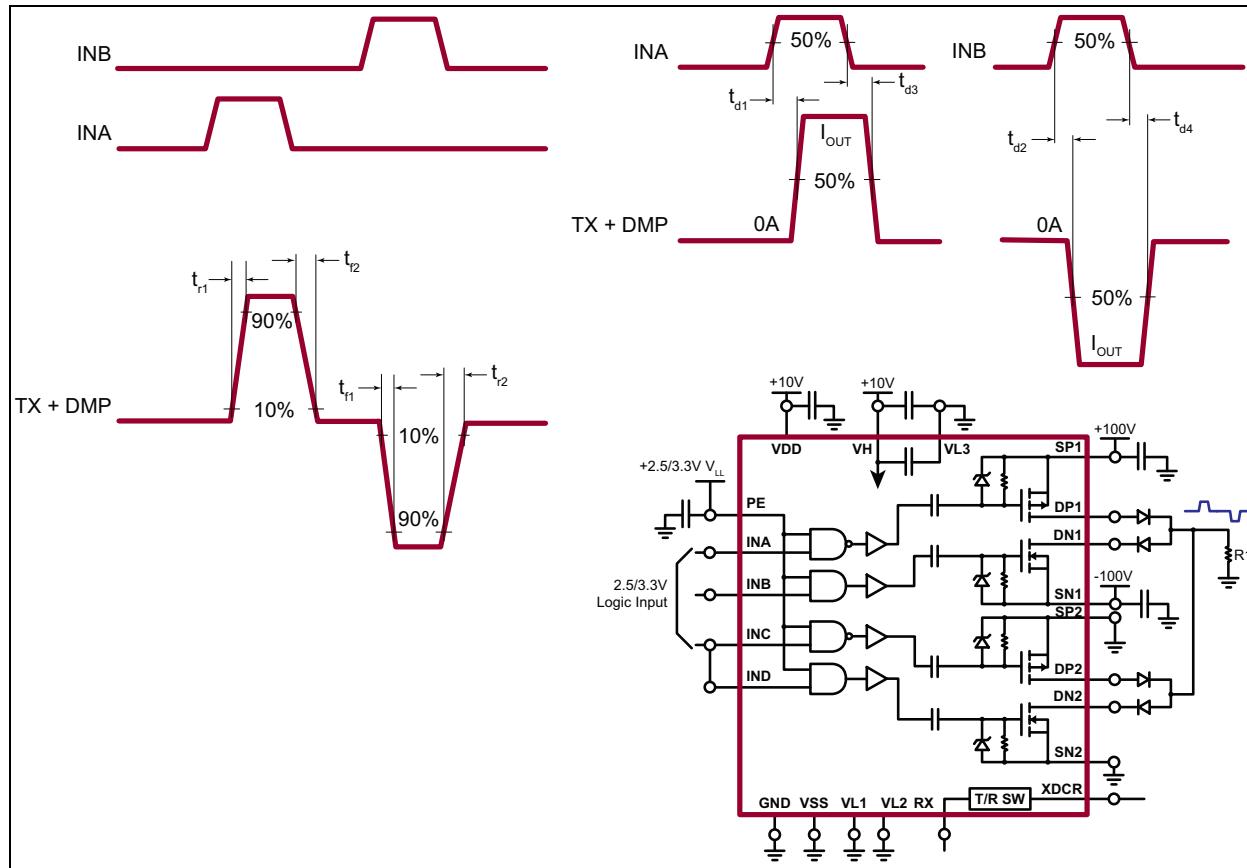


**FIGURE 3-1:**    *Pulser Timing Test for HV7360/HV7361.*
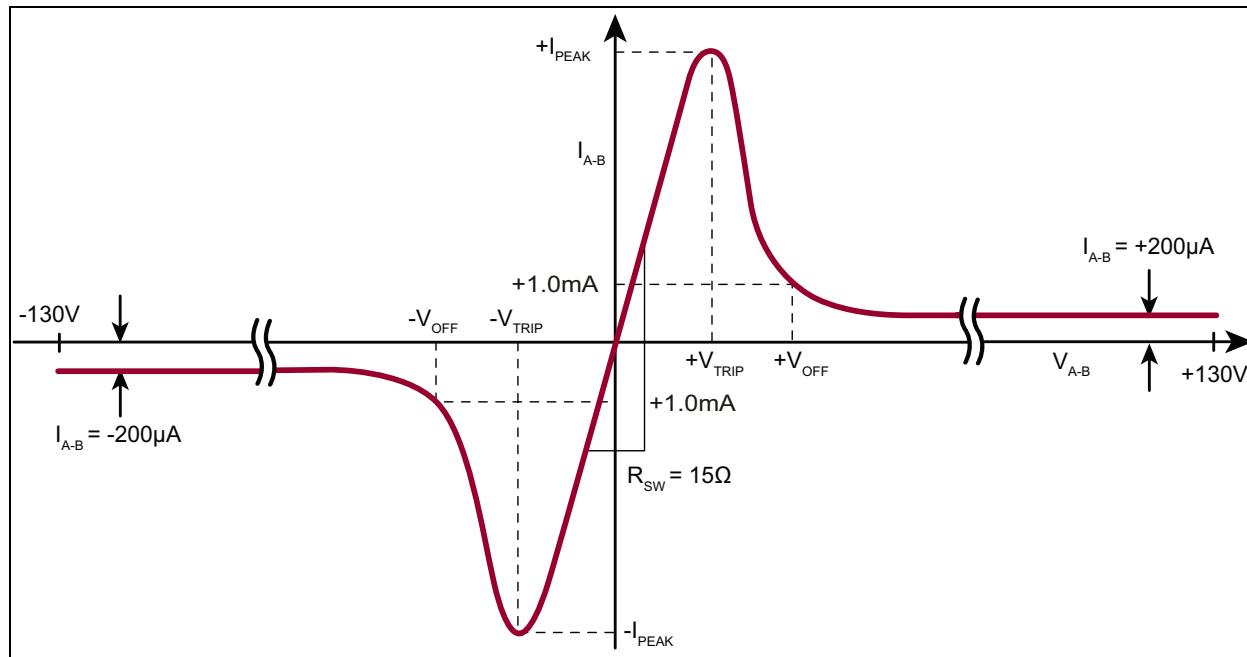


**FIGURE 3-2:**    *T/R Switch I-V curve for HV7361.*
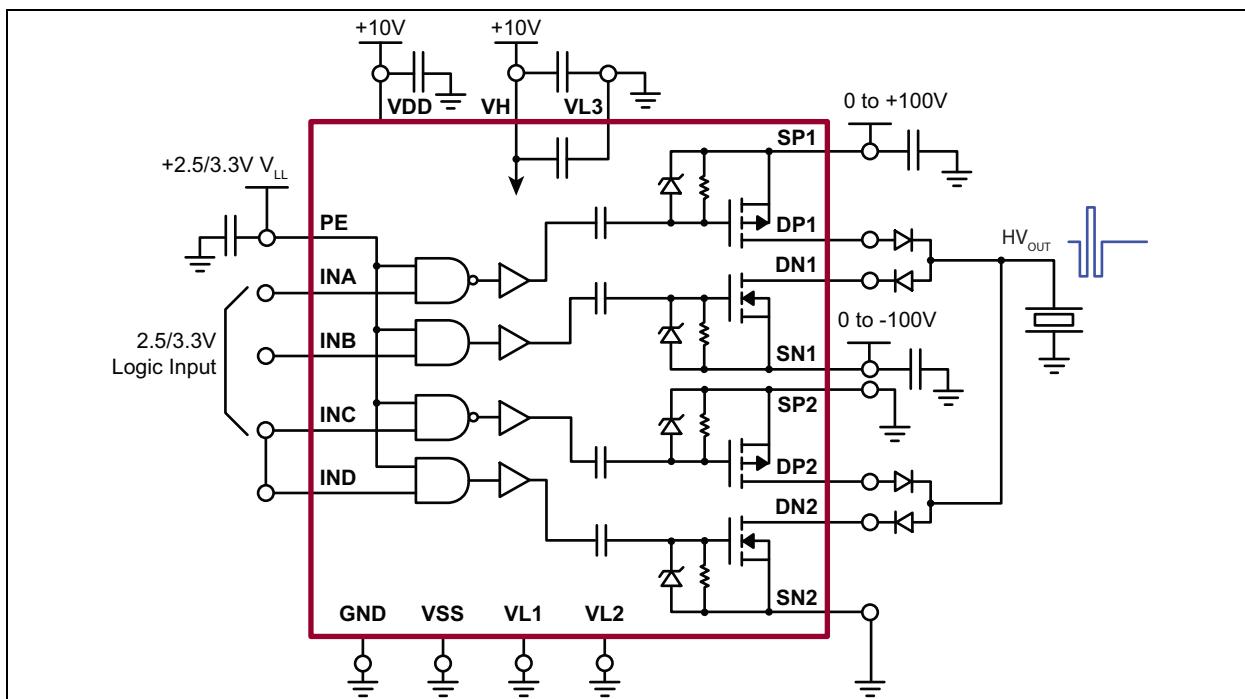
**FIGURE 3-3:** *Typical Bipolar One-channel Three-level Ultrasound Transmitter Application Circuit for HV7360.*
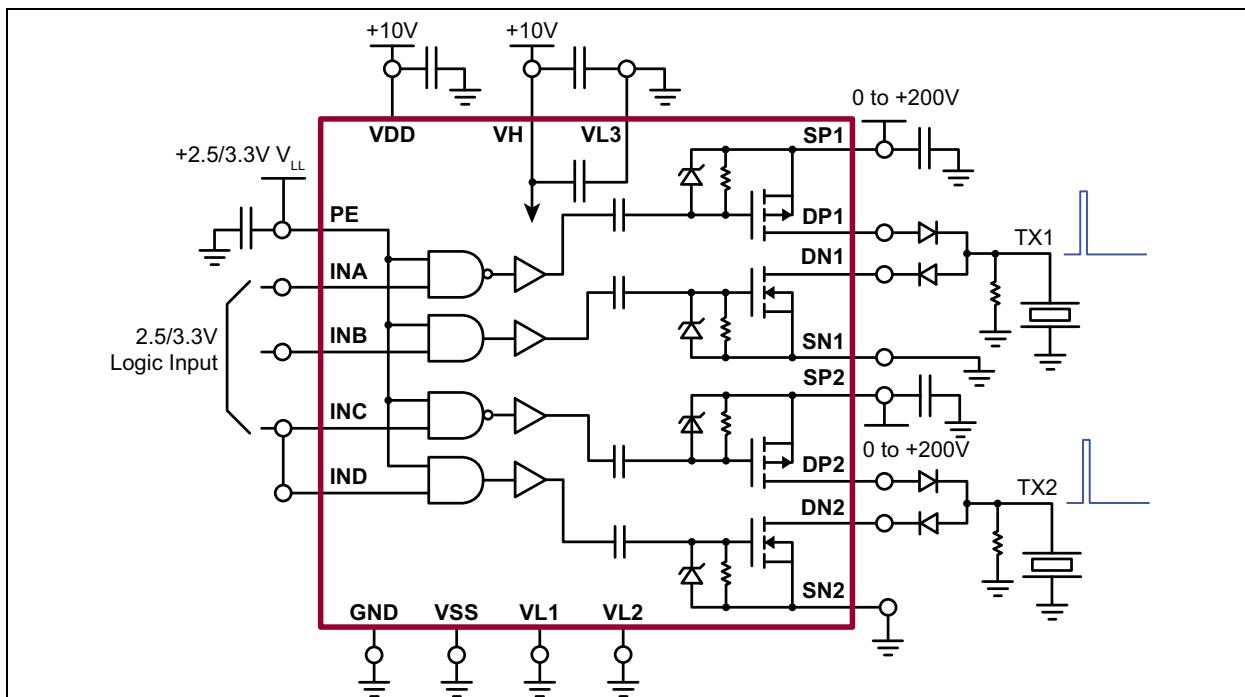


**FIGURE 3-4:** *Typical Unipolar Two-channel Two-level Ultrasound Transmitter Application Circuit for HV7361.*

## 4.0    PACKAGING INFORMATION

### 4.1    Package Marking Information

XXXXXX
XX (e3)
YYWWNNN

HV7360
GA (e3)
1624111

XXXXXX
XX (e3)
YYWWNNN

HV7361
GA (e3)
1618555
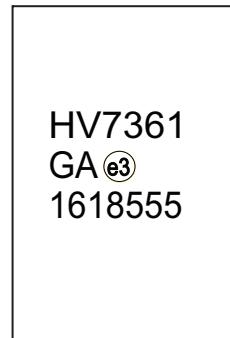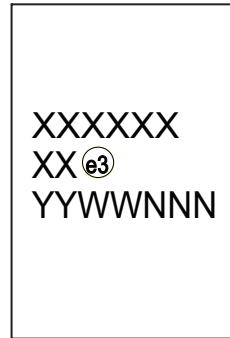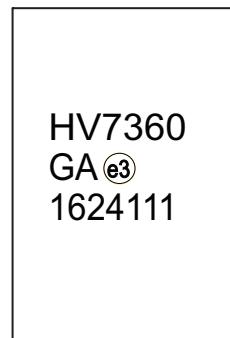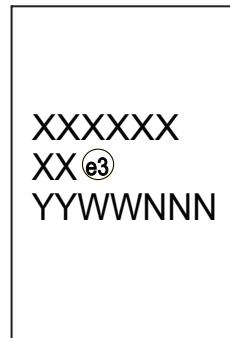
| Legend: | XX...X | Product Code or Customer-specific information |
|---|---|---|
| | Y | Year code (last digit of calendar year) |
| | YY | Year code (last 2 digits of calendar year) |
| | WW | Week code (week of January 1 is week '01') |
| | NNN | Alphanumeric traceability code |
| | (e3) | Pb-free JEDEC® designator for Matte Tin (Sn) |
| | * | This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package. |

**Note**:    In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for product code or customer-specific information. Package may or not include the corporate logo.

## 22-Ball Chip Array Ball Grid Array (JY) - 5x7 mm Body [CABGA]

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

TOP VIEW

SIDE VIEW

BOTTOM VIEW
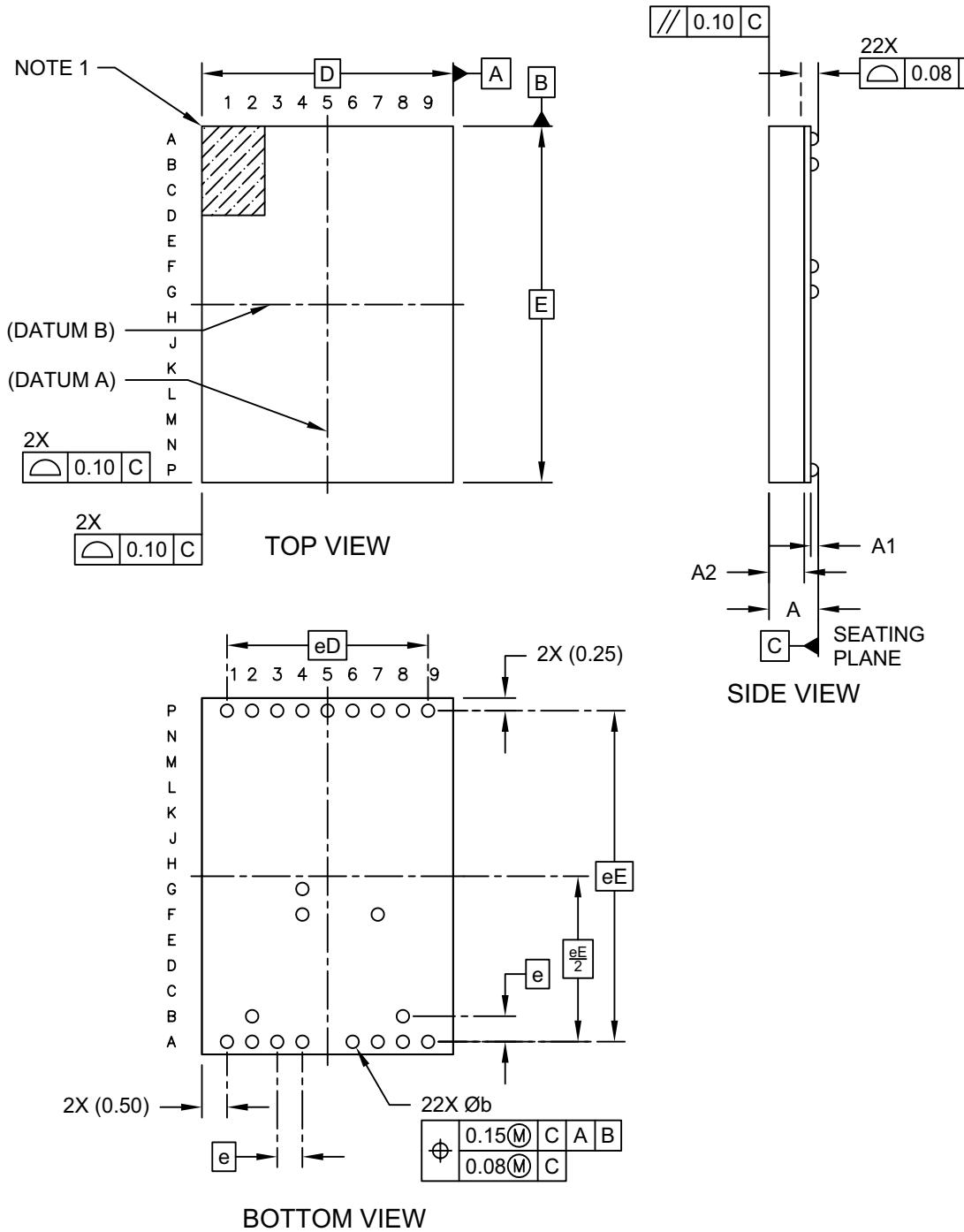
Microchip Technology Drawing  C04-414A Sheet 1 of 2

## 22-Ball Chip Array Ball Grid Array (JY) - 5x7 mm Body [CABGA]
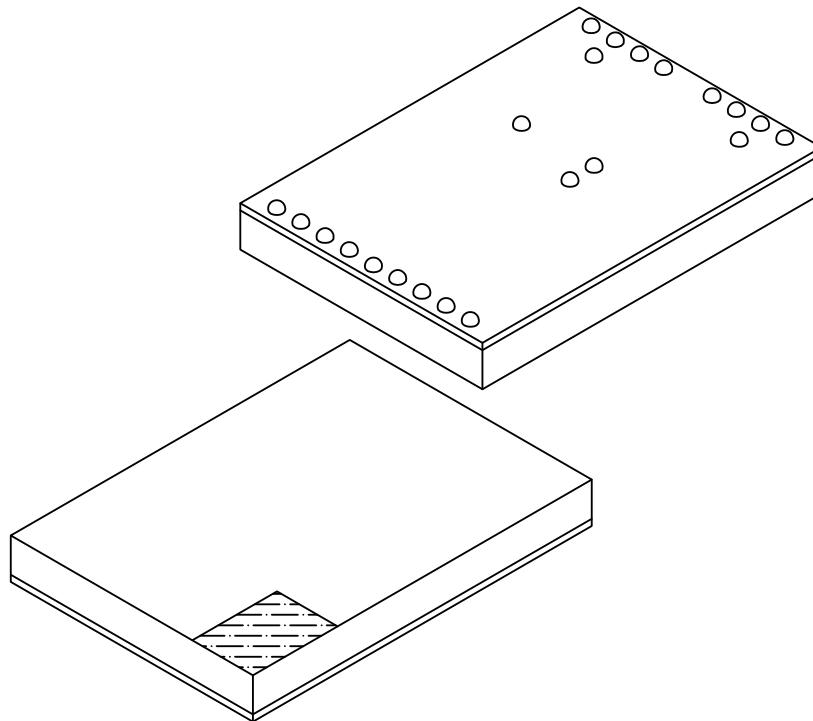
| Note: | For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging |
|---|---|



| | Units | MILLIMETERS | | |
|---|---|---|---|---|
| Dimension Limits | | MIN | NOM | MAX |
| Number of Terminals | - | | 22 | |
| Pitch | e | | 0.50 BSC | |
| Overall Height | A | 0.91 | 0.98 | 1.05 |
| Ball Height | A1 | 0.12 | 0.15 | - |
| Package Thickness | A2 | 0.66 | 0.70 | 0.74 |
| Overall Length | D | | 5.00 BSC | |
| Overall Terminal Pitch | eD | | 4.00 BSC | |
| Overall Width | E | | 7.00 BSC | |
| Overall Terminal Pitch | eE | | 6.50 BSC | |
| Ball Diameter | b | 0.20 | 0.25 | 0.30 |

Notes:
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing  C04-414A Sheet 2 of 2

## 22-Ball Chip Array Ball Grid Array (JY) - 5x7 mm Body [CABGA]

> **Note:** For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging
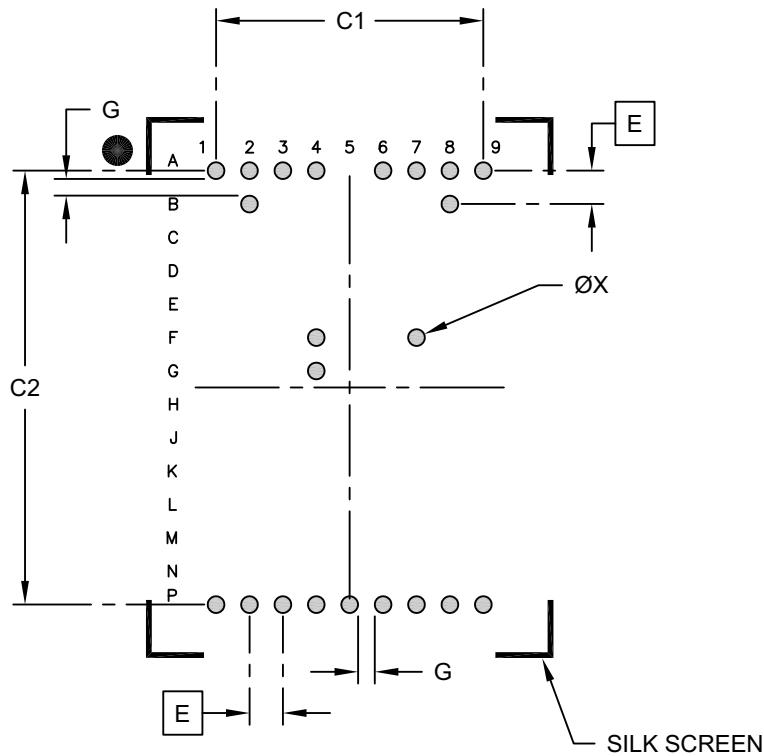


RECOMMENDED LAND PATTERN

| | Units | | MILLIMETERS | | |
|---|---|---|---|---|---|
| | Dimension Limits | | MIN | NOM | MAX |
| Contact Pitch | | E | | 0.50 BSC | |
| Contact Pad Spacing | | C1 | | 4.00 | |
| Contact Pad Spacing | | C2 | | 6.50 | |
| Contact Pad Diameter (X22) | | X | | 0.25 | |
| Contact Pad to Contact Pad | | G | 0.20 | | |

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-2414A

**NOTES:**

## APPENDIX A:   REVISION HISTORY

### Revision A (June 2016)

- Converted Supertex Doc# DSFP-HV7360 and Supertex Doc# DSFP-HV7361 to Microchip DS20005570A.
- Meged HV7360 and HV7361 into one document.
- Replaced the 22-lead LFGA "LA" package with 22-lead CABGA "GA" package.
- Made minor text changes throughout the document.

## PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, contact your local Microchip representative or sales office.

| PART NO. | XX | - | X | - | X |
|---|---|---|---|---|---|
| Device | Package Options | | Environmental | | Media Type |

| | | | |
|---|---|---|---|
| Device: | HV7360 | = | High-voltage High-speed Pulse Generator with Built-in Fast RTZ Damping FETs |
| | HV7361 | = | High-voltage High-speed Pulse Generator with Built-in Fast RTZ Damping FETs and an Integrated Two-terminal Low-noise T/R Switch |
| Packages: | GA | = | 22-lead CABGA |
| Environmental: | G | = | Lead (Pb)-free/RoHS-compliant Package |
| Media Type: | (blank) | = | 364/Tray for GA Package |

**Examples:**

a) HV7360GA-G:  High-voltage High-speed Pulse Generator with Built-in Fast RTZ Damping FET, 22-lead CABGA Package, 364/Tray

b) HV7361GA-G:  High-voltage High-speed Pulse Generator with Built-in Fast RTZ Damping FET and an Integrated Two-terminal Low-noise T/R Switch, 22-lead CABGA Package, 364/Tray

**Note the following details of the code protection feature on Microchip devices:**

• Microchip products meet the specification contained in their particular Microchip Data Sheet.

• Microchip believes that its family of products is one of the most secure families of its kind on the market today, when used in the intended manner and under normal conditions.

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