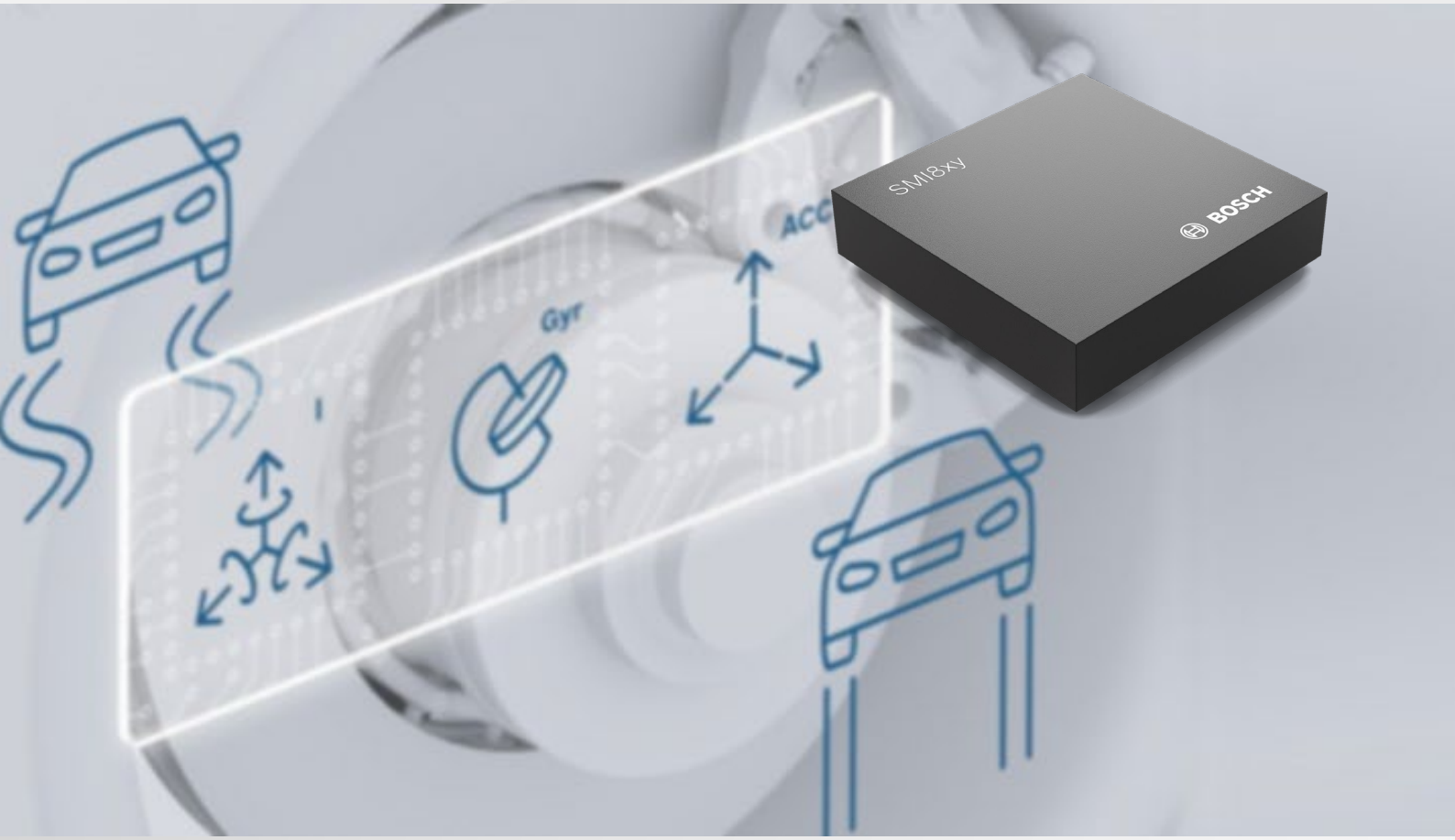
Technical Customer Documentation
SMI800, SMI810, SMI860 & SMG810

Combined angular rate and acceleration sensor for Vehicle Dynamic Control

Document revision	2.2
Release date	02/27/2020
Document number	1 279 940 250
Document Author	AE/PAS1.2-Barra

This document is valid for the following Bosch part numbers:

SMI800:	0 273 142 141
SMI810:	0 273 142 140
SMG810:	0 273 142 167
SMI860 6g:	0 273 142 142
SMI860 8g:	0 273 142 226



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Department	AE/PAS	AE/ESI	AE/PRM-S	RtP1/QMM	AE/SCS
Date	02/27/2020	02/27/2020	02/27/2020	02/28/2020	02/27/2020
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1 Product identification

The SMI8 sensor family consists of the sensor types SMI800, SMI810, SMI860 and SMG810. These sensors are combined angular rate and acceleration sensors with a measurement range of +/-300°/s and up to 8g.

1.1 Main functions and properties

The SMI8 sensor family consists of 4 different sensor modules for various applications. The sensor modules offer combined gyroscope and acceleration sensors with 1, 3 or 5 degrees of freedom (measurement axis).

- SMI800 Yaw rate (Ω_z) and 2 axis acceleration (a_x, a_y)
- SMI810 Roll rate (Ω_x) and 2 axis acceleration (a_y, a_z)
- SMG810 Roll rate (Ω_x)
- SMI860 Yaw rate (Ω_z), Roll rate (Ω_x) and 3 axis acceleration (a_x, a_y, a_z)

Sensor	SMI800	SMI810	SMG810	SMI860
Gyroscope measurement axis	z	x	x	x / z
Gyroscope measurement range	300 °/s			
Accelerometer measurement Axis	x / y	y / z	-	x / y / z
Accelerometer measurement range (LF channels)	6 g / 6 g 8g on request	6 g / 6 g 8g on request	-	6 g / 6 g / 6 g 8g on request
Acceleration Measurement Range (HF channels)	35 g / 35 g	35 g / 25 g	-	35 g / 35 g / 25 g
Operating Temperature Range	-40...125 °C			
Communication Interfaces	SPI 32bit, inframe & outofframe protocol (compliant to SafeSPI rev 1.0)			
Data width	16 bit			
Output filters	LF channel: selectable low pass filters: 11Hz, 20Hz, 75Hz HF channel (accelerometer only): lowpass 200Hz			
Functional safety	On board safety controller, sensors suitable for application with safety targets up to ASIL D			

The SMI8xx inertial sensor family provides acceleration and angular rate signals via a digital interface (SPI). The sensors consist of two Micro Electro Mechanical System (MEMS) elements (SMG810 only one MEMS element) and a sensor readout ASIC. The ASIC contains analogue front ends and a digital structure for signal processing and communication interface. The sensor modules are available in a surface mountable BGA (ball grid array) housing.

1.2 Intended use

The SMI8 inertial sensor family is intended for use in earthbound, noncommercial vehicles and designed for applications in the trunk, in the passenger or in the engine compartment.
Provided that SMI8 is used within the conditions (environment, application, installation, loads) as described in this Technical Customer Documentation (TCD) and agreed upon corresponding documents, Bosch ensures that the product complies with the agreed properties. Agreements beyond this require the written approval by Bosch. The product is considered fit for the intended use when the product successfully has passed the tests in accordance with the TCD and agreed upon documents.
It is the responsibility of the customer to ensure the proper application of the product in the overall system/vehicle.
Bosch does not assume any responsibility for changes to the environment of the product that deviate from the TCD or other agreed upon documents as well as all applications not released by Bosch.

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2 General product description

The SMI8 inertial sensor family provides acceleration and angular rate signals via a digital interface (SPI). The sensors consist of two Micro Electro Mechanical System (MEMS) elements (SMG810 only one MEMS element) and a sensor readout ASIC. The ASIC contains analogue front ends and a digital structure for signal processing and communication interface. The sensor modules are available in a surface mountable BGA (ball grid array) housing.
The SMI8 inertial sensor family represents a number of sensors capable of measuring all 6 degrees of freedom (yaw/pitch/roll rate and acceleration in x/y/z direction) in various combinations. The gyroscope channels are able to measure angular rates up to 300 °/s.
The acceleration sensor channels are able to measure low-g accelerations (up to ~6 g/8 g) with high resolution and middle-g accelerations (up to ~35 g) with reduced resolution.

This table gives an overview about the sensor modules:

Sensor	SMI800	SMI810	SMG810	SMI860
Rate Measurement Axis	z	x	x	x / z
Rate Measurement Range (LF)	300 °/s	300 °/s	300 °/s	300 °/s
Acceleration Measurement Axis	x / y	y / z	-	x / y / z
Acceleration Measurement Range (LF) *	6 g / 6 g	6 g / 6 g	-	6 g / 6 g / 6 g
Acceleration Measurement Range (HF)	35 g / 35 g	35 g / 25 g	-	35 g / 35 g / 25 g
Operating Temperature Range	-40...125 °C	-40...125 °C	-40...125 °C	-40...125 °C
Communication Interfaces	SPI	SPI	SPI	SPI

* Measurement range up to 8 g available on request

2.1 Sensor Evaluation

2.1.1 Block diagram

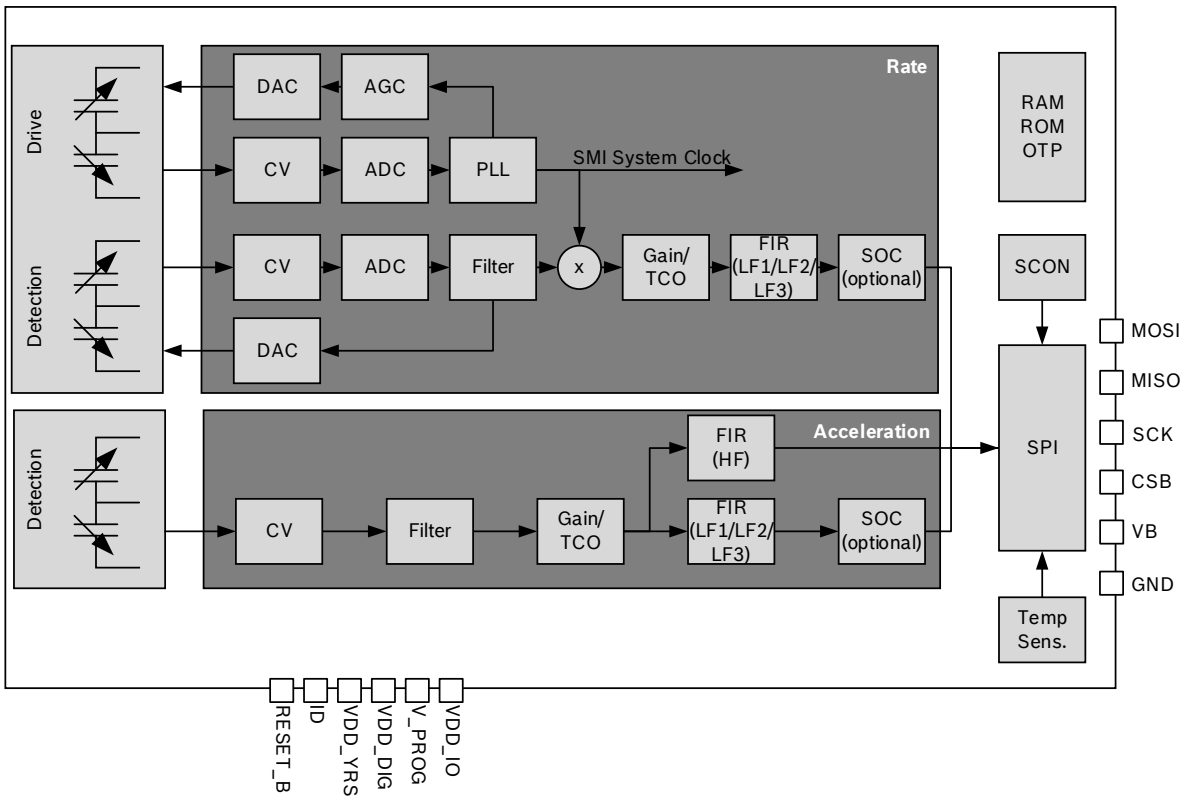

Figure 1 Block Diagram SMI8

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2.1.2 Angular rate Sensing Element

The angular rate-sensing element is based on the Coriolis Vibratory Gyroscope principle. As a silicon surface micro-machined comb structure is oscillated at its resonance frequency, an angular rate creates a Coriolis force perpendicular to the oscillation direction and the rotation axis. The resulting change in capacitance of the comb structure is measured and converted into a digital signal.
The signal path consists of two closed loop paths, the drive and the detection path. The drive path controls the oscillation of the angular rate sensing element and is also the base for the ASIC clock frequency. The detection path operates in a closed loop mode, where the signal generated by an applied angular rate is fed back to the detection frame of the sensor element. As a result, the detection frame is not deflected in the direction of the Coriolis force generated by the angular rate, but kept in a “zero” position. The signal is finally low pass filtered.
The micro machined structures on the surface of the measuring element are protected and hermetically sealed with a micro machined silicon cap.

2.1.3 Acceleration Sensing Element

The acceleration sensing element uses a silicon surface micro-machined comb structure (lateral sensing axis) or a non-symmetric rocker structure (vertical sensing axis) as capacitive accelerometers. Each structure forms a differential capacitor, consisting of a free-movable seismic mass suspended from silicon spring bars and fixed counter-electrodes. An acceleration along the sensing axis deflects the seismic mass, resulting in a capacitance change which is evaluated by the sensor readout ASIC. The micro machined structures on the surface of the sensor chip are protected and hermetically sealed by a micro machined silicon cap.

2.1.4 Evaluation ASIC

The evaluation ASIC provides the frontends for the sensor signal channels as well as the processing and filtering of the sensor signal, a safety controller for monitoring of the correct sensor function, the power supply for the sensor and its functional blocks and the communication interfaces to the system electronic control unit (ECU). The SMI8 sensor types SMI800, SMI810, SMG810 have the same ASIC named “XI800”. The SMI860 has another ASIC named “XI860”.

2.1.5 Filtering

The angular rate and accelerometer output signals of SMI8 are filtered by the digital signal processing unit of the evaluation ASIC. Three FIR low-pass filter are available that differ in terms of cut-off frequencies. The user can select between LF1 (~80Hz), LF2 (~20Hz) or LF3 (~10Hz). These FIR filters are realized by different sets of filter coefficients. Additionally, the acceleration channels have a high frequency (HF) channel with a higher corner frequency.

2.2 Safety Concept

To check the physical functionality at start-up the ASIC performs internal tests, LBIST and BITE. During operation, a safety controller (SCON) monitors important functional blocks, e.g. operating ranges of amplifiers, correct functionality of signal paths, phase-locked loop locked status, etc. A malfunction of the device is indicated by setting the corresponding error flags. The error flags lead to a status flag of the relevant output signal. The status of the output signal is accessible via the digital interface. A more detailed explanation is given in chapter 8.

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2.3 Configuration of sensor module

The sensor module is available in two ‘mode’ of configuration:

A. **Hard configuration:** The parts are configured by Bosch according to the customer specific requirements. The settings cannot be changed by the customer in application. Each configuration requires a specific part number to distinguish between the parts. Hard configured parts perform the power on routine automatically and will clear the channel status "CS" bit after successful completion of all internal test routines.

B. **Soft configuration:** Configurable by the customer application. The sensor module configuration must be programmed at each power on cycle using the SPI protocol. After powering on, the sensor goes into configuration mode and waits for being configured. The configuration of the sensor can be changed with respect to the following parameters:
   - Safety ID (SID)
   - Filter type (LF1, LF2, LF3) and filter flush time
   - Sign inversion and offset compensation mode
   - Error counter limits
   - Supply voltage monitor upper limit
   - Self-tests enabling
   - Self-tests configuration

   The soft configuration at start-up of the sensor module is secured by an EOC (end of configuration) command. After this command is received, the sensor will complete its startup routine and will perform the self-test. The sensor reports a failure by setting the channel status bit "CS", as long as the EOC has not been sent. Please note, even if no configuration is used, the EOC command must be sent to the sensor in order to complete the start-up routine.

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2.4 Orientation of sensing axes

Within this specification, the x-, y-, and z- axes form a Cartesian, right-handed coordinate system. The z-axis is perpendicular to the mounting plane. The gyroscope axes $\Omega_x, \Omega_y, \Omega_z$ are the rotations around the coordinate axes. Sensor functions and functional parameters of the sensor refer to the coordinate system of the sensor:

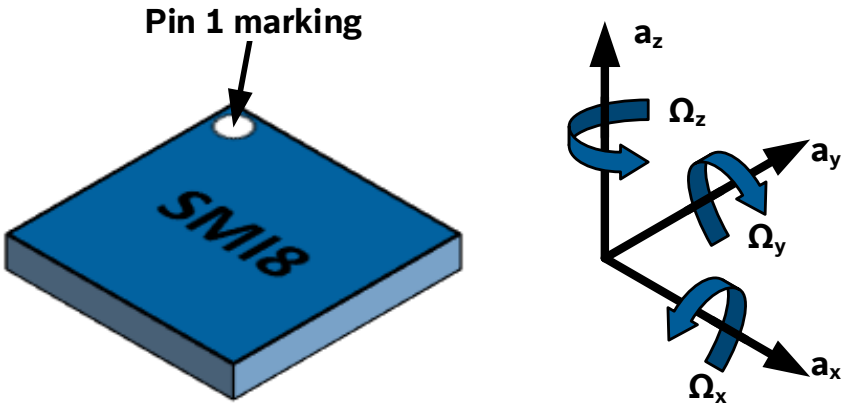


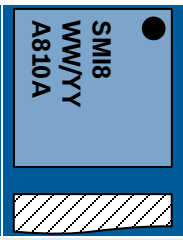
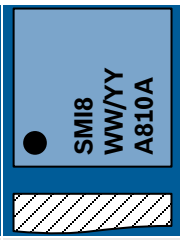
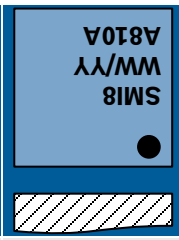
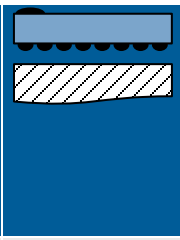
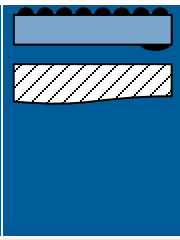
Figure 2 axis orientation

The arrows in Figure 2 indicate the positive sensing directions. The sensing directions can be inverted by soft configuration. When put in the gravitational field, the arrow of the gravitational force will point in the opposite direction than the arrow of acceleration when the module is accelerated, e.g. in a car. This is due to the inertial being active on the MEMS, which contains spring mass elements. The following table shows the sensor output when the sensor is put in the gravitational field.

Assignment of sensing directions

Signal name	SMI800	SMI810	SMG810	SMI860
ACC1	a_y	a_y		a_y
ACC2	a_x	a_z		a_x
ACC3				a_z
YRS1	Ωz	Ωx	Ωx	Ωx
YRS2				Ωz

Table assumes no sign inversion:

sensor orientation relative to gravitational field						
Output Signal ACC1	SMI800: + 1g SMI810: + 1g SMI860: + 1g	SMI800: 0g SMI810: 0g SMI860: 0g	SMI800: 0g SMI810: 0g SMI860: 0g	SMI800: - 1g SMI810: - 1g SMI860: - 1g	SMI800: 0g SMI810: 0g SMI860: 0g	SMI800: 0g SMI810: 0g SMI860: 0g
Output Signal ACC2	SMI800: 0g SMI810: 0g SMI860: 0g	SMI800: - 1g SMI810: 0g SMI860: - 1g	SMI800: + 1g SMI810: 0g SMI860: + 1g	SMI800: 0g SMI810: 0g SMI860: 0g	SMI800: 0g SMI810: + 1g SMI860: 0g	SMI800: 0g SMI810: - 1g SMI860: 0g
Output Signal ACC3	SMI860: 0g	SMI860: 0g	SMI860: 0g	SMI860: 0g	SMI860: +1g	SMI860: -1g

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3 Hardware interface and packaging

3.1 Package parameters

Parameter / Condition	Min	Typ	Max	Unit
Physical dimensions of sensor module (length * width * height)		7 x 7 x 2		mm^3
Weight		0.2		g
Thermal resistance		35		K/W

See offer drawing (separate document, see section 3.3) for details on package and marking.
The package is a ball grid array (BGA) package with 64 balls on the bottom side.
The sensor module meets the requirements of the EC restriction of hazardous substances (RoHS) directive 2011/65/EU - ROHS-2. The sensor module is recyclable according to the norm WEEE - 2012/19/EU.

3.2 Transport package

The sensor modules are delivered on tape and reel. The tape complies with either IEC 60286-3 or EIA-481. The transport package conforms to the ESD requirements in EIA 541, Packaging Material Standards for ESD sensitive Items. This is package material / production auxiliaries. Bosch reserves the right to use alternative package material.

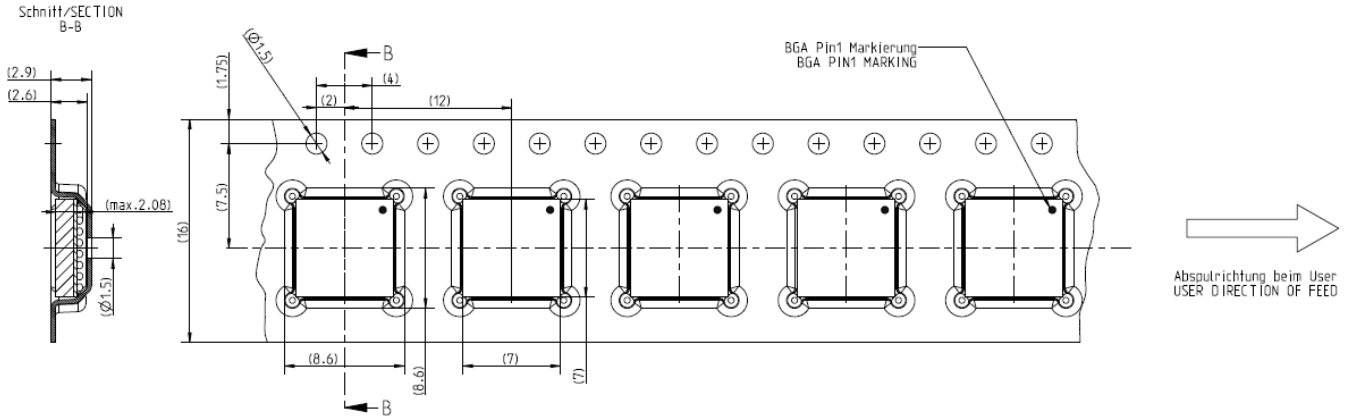

Figure 3 Orientation of BGA in tape

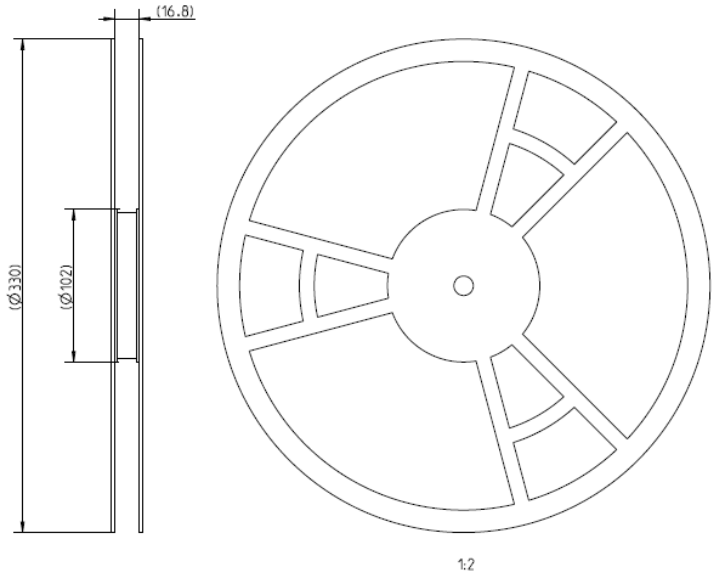

Figure 4 Reel dimensions

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3.3 Labeling of the product

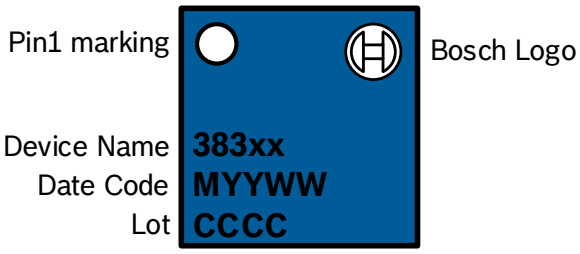

Figure 5 SMI8 Sensor Marking

For series production parts, the device name is given by a 5 digit number. The following Bosch offer drawing documents (separate documents) contain details on package and marking:

Sensortype	**device name**	**offer drawing document**
SMI860	38331	0274a01223
SMI800	38332	0274a01224
SMI810	38333	0274a01225
SMG810	38341	0274a01250

Date code: M: manufacturer, YY: year, MM: month
Lot: manufacturer lot number

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3.4 Pinning

3.4.1 Package pins

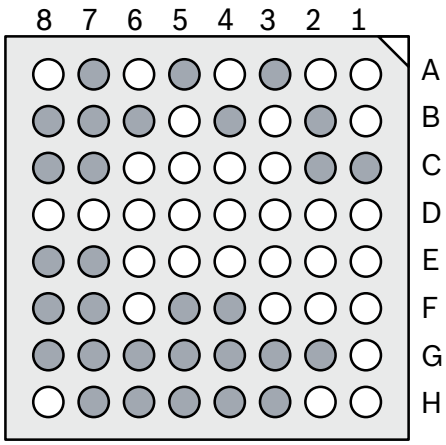

Figure 6 Pinning from the bottom view of the package

3.4.2 Application circuit

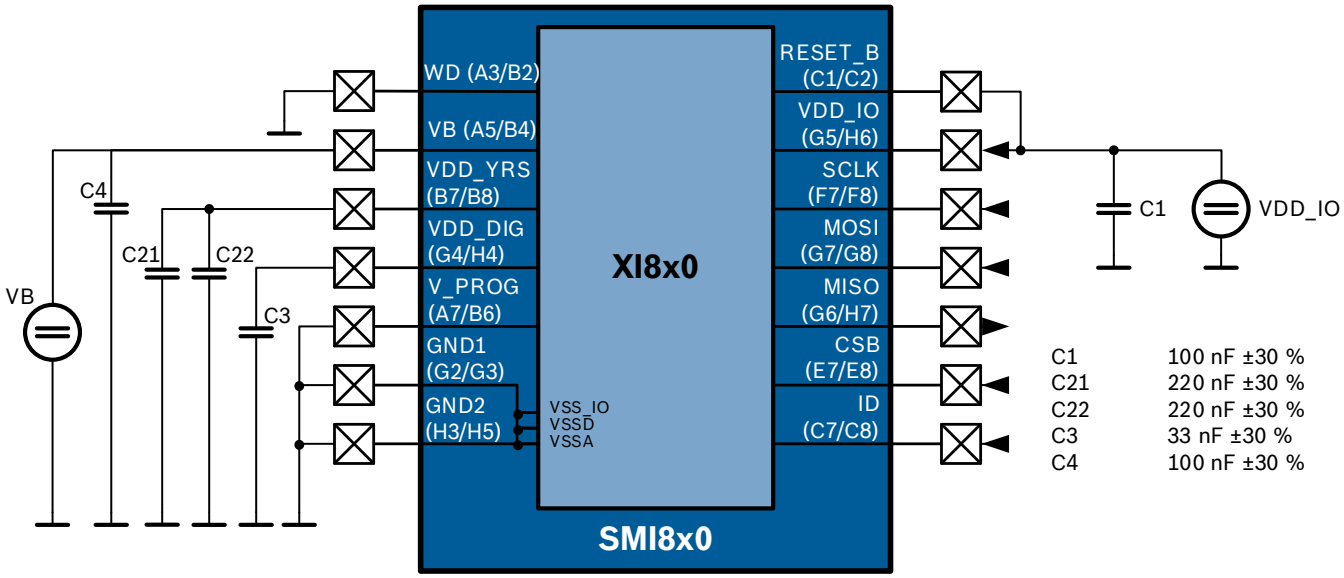

Figure 7 Application circuit for SPI application of SMI800, SMI810, SMG810, SMI860

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Pin name	Package Pin	Connected to	Supply Domain	Direction	Internal pull up/down	Remarks
ID	C7, C8	3,3V / GND	VDD_IO	in	up	ID Pin: Defines sensor bus address bit 3
V_PROG	A7, B6	GND	-	-	-	Only used during Bosch production
VDD_DIG	G4, H4	33nF to GND	-	-	-	
VDD_YRS	B7, B8	2x 220nF to GND	-	-	-	
VDD_IO	G5, H6	3,3V, 100nF to GND	-	-	-	
VB	A5, B4	100nF to GND	-	-	-	
CS_B	E7, E8	CS_B	VDD_IO	in	up	
SCLK	F7, F8	SCLK	VDD_IO	in	down	
MISO	G6, H7	MISO	VDD_IO	out	-	
MOSI	G7, G8	MOSI	VDD_IO	in	down	
RESET_B	C1, C2	RESET_B	VDD_IO	in	down	Optionally connected to VDD_IO
GND/WD	A3, B2	GND/WD	VDD_IO	out		Watchdog only for SMI860
GND1	G2, G3	GND	-	-	-	GND1/2 internally connected.
GND2	H3, H5	GND	-	-	-	GND1/2 internally connected.
Anti Twist	F4,F5	Anti Twist	-	-	-	Anti Twisting internally connected
n.c.	C3	D3	-	-	-	
n.c.	D1	E1, F1	-	-	-	
n.c	D4	D5, E5	-	-	-	
n.c	E2	F2	-	-	-	
n.c	E3	F3	-	-	-	
n.c	G1	H2	-	-	-	

* All pins not listed are not connected
* Connections of all balls on PCB are necessary and double pinning has to be used for electrical functional pins.

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3.4.3 Electrical pins specification

Parameter / Condition	Min	Typ	Max	Unit
Supply Pins (VB, VDD_IO)				
VB	3.13	-	11	V
VDD_IO	3.13	-	3.6	V
Input pins (RESET_B, MOSI; CSB, SCLK,ID)				
Input low voltage	0	-	0.3*VDD_IO	V
Input high voltage	0.7*VDD_IO	-	VDD_IO	V
Input high current CSB, SCK, ID and MOSI @ VDD_IO	-10	-	10	uA
Input high current RESET_B @ VDD_IO	20	-	65	uA
Input low current CSB, SCK, ID and MOSI @ 0V	20	-	65	uA
Input low current RESET_B @ 0V	-10	-	10	uA
Input capacitance INPUT PINS	1	-	6	pF
Reset detection time	-	-	110	µs
Output pins (MISO, GND/WD)				
Output high voltage @ IOH = +2mA	0.8*VDD_IO	-	VDD_IO	V
Output low voltage @ IOL = -2mA	0	-	0.2*VDD_IO	V
Output tristate current @ CSB = low	-10	-	10	uA
Capacitive load at OUTPUT PIN (Tristate mode)	-	-	6	pF
VDD_YRS, VDD_DIG				
Electrical specification for VDD_YRS	2.75	-	2.95	V
Electrical specification for VDD_DIG	1.35	-	1.65	V

CSB and ID have an internal pull-up resistor to VDD_IO. SCLK, MOSI and RESET_B have an internal pull-down resistor to GND.

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3.5 Soldering

The sensor modules are designed for a Pb-free solder process. Sensor modules are suitable for double sided soldering. The moisture sensitivity level is MSL 3 according to IPC/JEDEC J-STD-020D.
The sensor is qualified for mounting the device on a PCB using a lead-free reflow-soldering profile with a peak-temperature of up to 260°C. Below in Figure 3 reflow soldering profile shows the worst case temperature profile, which was used for qualification. When soldering the sensor, the manufacturing temperature profile must stay below the peak temperature and may not exceed the specified limits (e. g. ramp up, ramp down, dwell times) of this qualification reflow profile. The sensor has been qualified with 3 repetitions of this soldering profile, i. e. a maximum application of three soldering cycles is allowed.

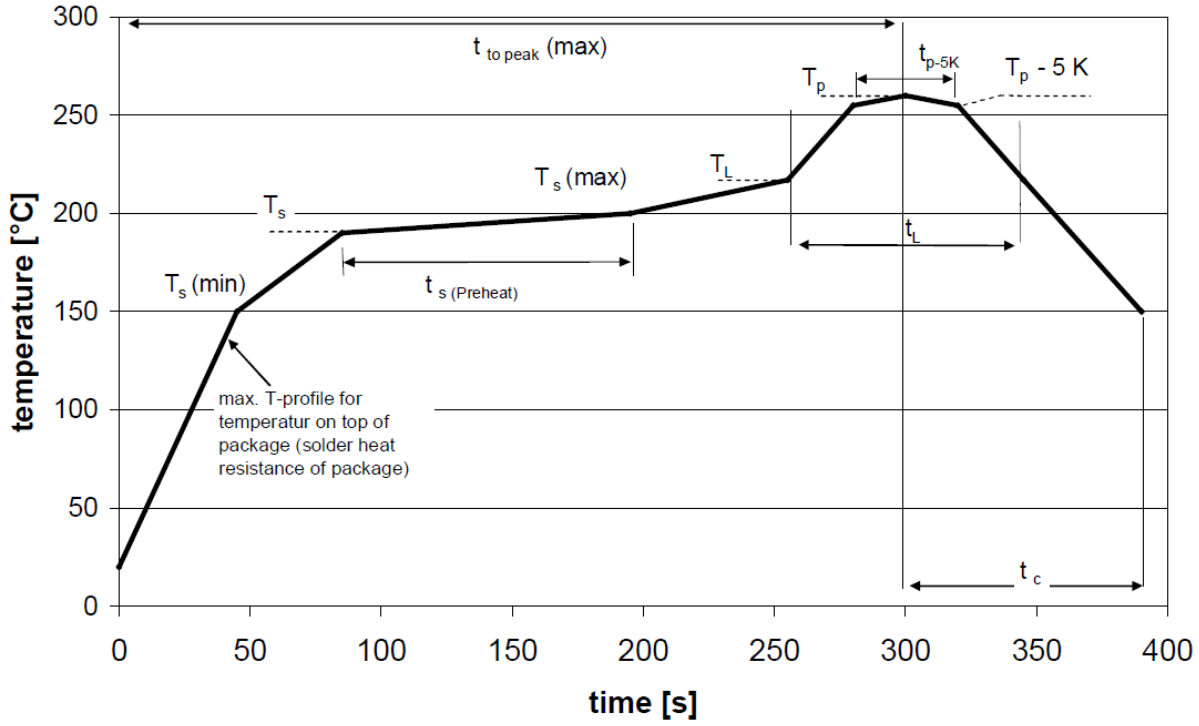

Figure 8 Lead-free reflow-soldering profile

Reflow soldering profile	
Preheating	
Ramp-up rate to 150°C	Max. 3 K/s
T_s (min)	Max. 150 °C
T_s (max)	Max. 200 °C
T_s (preheat)	Max. 110 s
Time between T_s (max) and T_L	Max. 85 s
Peak	
T_L	Max. 217 °C
t_L (time above T_L)	Max. 90 s
T_p (peak temperature)	Max. 260 °C
t_p-5k (time within 5 °C of actual peak temperature)	Max. 40s
Ramp-up rate from 200 °C to T_p	Max. 3 K/s
$t_{to\ peak}$	Max. 300 s
Cooling	
Max ramp-down rate from peak temperature	Max. 4 K/s
t_c (Max. cooling time T_p to T_s (min))	Max. 90 s

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3.5.1 Rework

For failure analysis, the SMI8 can be removed from the PCB and replaced by a spare one. Rework in series production has not been verified and is not allowed. For the removal of SMI8 (failure analysis) special rework equipment is recommended, which controls the temperature profile. Before a new SMI8 could be soldered on the PCB, the solder residuals have to be removed. Potential failure parts have to be removed very carefully, because the removal process itself can cause defects and failures. A local dry bake according to the packages moisture sensitivity level has to be applied at the SMI8 position before removal. Mechanical removal from the PCB is not recommended.

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3.6 Recommendations for PCB Layout

The following recommendations only represent one possible solution for the layout of the PCB based on Bosch experience and evaluation results. The PCB layout and its qualification lie in the responsibility of the customer and therefore other suitable solutions can be implemented. The SMI8 in principle is suitable for conformal coating. MEMS sensors, however, are sensitive to mechanical stress.
Please note that any measure on application level that influences the mechanical connection between the sensor and the PCB such as for example dip or spray or partial coating might potentially affect the sensor performance (e.g. shift of the package resonance frequencies) and board level reliability and therefore have to be chosen with care by and in responsibility of the PCB designer or manufacturer.

- Pads for balls are NSMD (non solder mask defined). NSMD is preferred against SMD due to better BLR (Board-level reliability)
- The solder pad on PCB should have the same design and dimensions on PCB as on the BGA side. In case of asymmetric pads a similar area, i.e. in particular an NSMD layout should be used.
- Pad size diameter B=400 µm, copper layer thickness 18-35µm, Opening solder mask A=500 µm

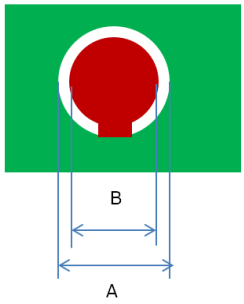

Figure 9 Pad design

- The solder paste is applied by screen-printing with a Solder-Stencil. Stencil thickness for solder is minimum 125 µm. Area of solder paste / pad minimum 0,145 mm²
- Pad configurations other than symmetric must be evaluated by customer
- No open vias in Pad at PCB-side allowed
- Underfill is possible, it must be evaluated by customer
- Permanent strain on the PCB is limited to 800 µm/m. If a strain level of 800 µm/m is exceeded, SMI8 specification values, as defined in this document, cannot be guaranteed. Temporary strain (few seconds) during production at room temperature up to 1100µm/m is allowed.
- As an indication for the applied strain level, the quadrature output of the sensor can be used. It can be read out by using the “QUAD1/2_FINE_DAC” registers described in chapter 6.4.1.3 and 6.4.2.3. It is recommended to allow a maximum limit of ±16000 LSB in the ECU end of line test.
- Because cleaning of the soldered BGA is difficult, a “no-clean” solder paste is preferred. All recommendations of paste manufacturer have to be followed. Cleaning with ultrasonic is not allowed.

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- Overlapping of BGA and leadless SMD package (e.g. QFN or SOT) at the opposite side of PCB are not allowed since BLR is reduced severely (see Figure 5).

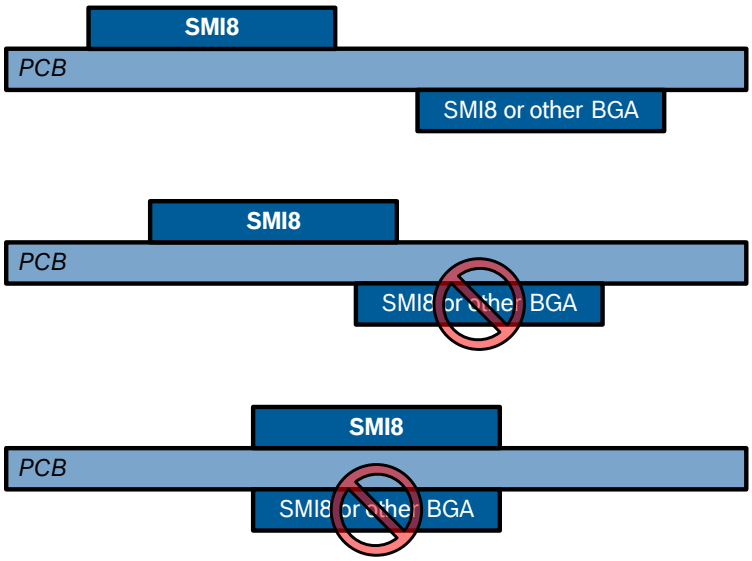

Figure 10 PCB guidelines SMI8 or other leadless SMD package

- The placement of small components like capacitors or resistors or SO8 on the opposite site of the PCB is possible.
- Connections of all balls on PCB are necessary
- Double pinning has to be used for electrical functional pins.

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4 Environment Specification

4.1 Maximum ratings

Values within the specified maximum conditions will not damage the sensor. No specification value is guaranteed at or above these maximum conditions. Any values beyond these maximum conditions may seriously damage the device. The sensor must be discarded if these limits are exceeded. A proper ESD environment during handling and processing of the sensor has to be in place. Please pay special attention to the safety and warning notes in section 10.1.

Parameter / Condition	Min	Typ	Max	Unit
Non-destructive supply voltage range VB	-	-	19.5	V
Non-destructive voltage range 3.3V PINs (MISO, MOSI, SCLK, CS, ID, Reset_B)	-0.3	-	3.6	V
Non-destructive voltage range VDD_IO	-0.3	-	3.6	V
Temperature gradient without damage of component	-	-	20	K/min
Mechanical shock acceleration without damage to the sensor module t < 0.5 ms, in x-, y-, z- direction	-	-	3 000	g
Drop test to concrete surface, drop height (Passive, 3 axis, 6 directions. Pass criteria: Sensor works within the full specification or occurred damage is indicated by the sensor electrically, mechanically or visibly) Production directive: Damaged parts must not be used			1.2	m
Min./max. temperature passive without damage for short time <10h over life-time.	-55		160	°C
Min./max. temperature active without damage of component	-40		140	°C
Electrostatic Discharge, HBM, for all pins 100pF/1.5K Ohm	2	-	-	kV

4.2 Operating conditions

All characteristics of SMI8xy sensors are valid for soldered parts on PCB, at any time during lifetime and specified under all operating conditions if not noted otherwise.

Parameter / Condition	Min	Typ	Max	Unit
Operating temperature range	-40	-	125	°C
Operating temperature gradient	+/- 6	-	-	K/min

4.3 Lifetime conditions

With respect to the use and usage conditions described in this TCD, the life of the SMI8 is designed for maximum lifetime figures given in the tables below (whichever of the figures occurs first). The commercial warranty and liability is governed separately by the delivery conditions.

Parameter / Condition	Min	Typ	Max	Unit
The Sensor is designed for a life expectancy of (operating)	-	-	16 000	hours
The Sensor is designed for a life expectancy (non- operating)	-	-	159200	hours
The Sensor is designed for switch off/on cycles	-	-	300 000	
Lifetime (including operating and non-operating time)			20	a

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The sensor module is designed and qualified for the following mission profile. In case a different mission profile shall be applied, it needs to be verified whether this profile is still covered by the qualification.

Duration [h]	at [°C]
160	125
800	100
3 840	80
5 440	60
3 840	25
1 600	-25
320	-40
Total: 16 000h / 20a	

4.4 Storage conditions

Valid for sensor module before and after assembly on PCB

Parameter / Condition	Min	Typ	Max	Unit
Storage Temperature min./max. temperature while storing without damage of component	-55		140	°C

The sensor module is designed and qualified for the following storage profile. In case a different mission profile shall be applied, it needs to be verified whether this profile is still covered by the qualification.

Storage of SMI, soldered to PCB:

Duration [h]	at [°C]
50	70 ... 30
130800	30 ... 10
500	10 ... -40
50	-40 ... - 55
Total: 131 400h/15a	

Storage of SMI, unsoldered:

Duration [h]	at [°C]
24	140 ... 70
50	70 ... 40
8660	40 ... 10
50	10 ... -40
Total: 8 784h/1a	

4.5 Sensitivity to mechanical stress

Parameter / Condition	Min	Typ	Max	Unit
Maximum acceleration during milling process without mechanical damage or change in performance after relaxing the mechanical stress. f: 0-23kHz	-	-	300	g
Maximum acceleration during milling process without mechanical damage or change in performance after relaxing the mechanical stress. f > 27kHz	-	-	20	g

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5 Parameter specification

5.1 Power supply

Parameter / Condition	Min	Typ	Max	Unit
Supply voltage range 1 VB (3.3V application)*	3.13	3.3	3.6	V
Supply voltage range 2 VB (5.0V application)*	4.5	5	5.5	V
Supply voltage range 3 VB (6.5V application)*	6.15	-	11	V
Supply voltage VDD_IO	3.13	3.3	3.6	V
Supply voltage transients at power on and off at VB, VDD_IO	-	-	0.2	V/ns
Supply current during normal operation (VB and VDD_IO) (sensor modules SMI800, SMI810, SMG810)	-	-	18	mA
Supply current during normal operation(VB and VDD_IO) (sensor module SMI860)	-	-	28	mA
VB monitor tolerance (using hard configuration)	-0.15	-	0.15	V
VB monitor tolerance (using soft configuration)	-0.5	-	0.5	V

* Voltages outside the ranges 1,2 and 3 are not characterized

The supply voltage VB is monitored.
The lower limit of VB monitor is fixed at 3.13V and the upper detection limit for VB can be modified by soft-configuration and/or hard configuration. (See 7.1.1.7)

5.2 Technical data

5.2.1 Gyroscope

The specifications given in this chapter are valid for the angular rate sensing axis Ωx, Ωz independent from the specific sensor module.

All specification cover the sensor module itself when using the standard circuitry.

All specification parameters regarding offset are valid at any time during lifetime, but only the total offset error includes the lifetime drift (i.e. drift between new and aged parts, e.g. resulting from qualification).

The influence of additional error sources like PSRR, EMC and vibration are not included. The behavior of the sensor under such conditions is described in separate reports are available on request.

The data in this section applies for the valid operation conditions.

All following figures include voltage, temperature and lifetime effects if not noted otherwise.

Sensor data are only valid if no failure flags indicate any malfunction. All values except the noise itself exclude noise effects.

Parameter / Condition	axis	Min	Typ	Max	Unit
Digital output range	XZ	-32768		+32767	LSB
Measurement range LF Highest/lowest input angular rate which can be measured by sensor (The spec is not guaranteed beyond this range)	XZ	-300	-	+ 300	°/s
Total offset error (without slow offset compensation)	X Z	-2 -3	- -	2 3	°/s °/s
Total offset error (with slow offset compensation) Mean value over 1s with a sample rate of 1kHz	XZ	-0.1	-	0.1	°/s
Residual rate offset after fast offset compensation	XZ	-0.2	-	0.2	°/s

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Parameter / Condition	axis	Min	Typ	Max	Unit
Regulations speed of rate signal slow offset compensation	XZ	-	-	0.05	°/s/s
Offset power-on span Maximum signal error relative to initial value @0°/s stimulus. Including power on drift effects only valid 0-20 s after power on	XZ	-0.5	-	0.5	°/s
Offset operational span over temperature and Power On Maximum signal span (|max-min| offset value) @0 °/s stimulus. Including temperature, power on effects.	X Z	-	-	1 2	°/s °/s
Offset short-term gradient @ max. +/- 6.0 K/min temperature ramp defined by linear fit over 1 minute intervals during temperature ramp valid >20s after power on	XZ	-0.2	-	0.2	°/s/min
Offset long-term gradient @ max +/- 6.0 K/min temperature ramp defined by linear fit over the whole temperature ramp valid >20 s after power on	XZ	-0.1	-	0.1	°/s/min
Offset temperature gradient @Temperature ramp up to +/-6 K/min valid >20 s after power on	XZ	-0.1	-	0.1	°/s/K
Offset drift over time at constant temperature (24h) Drift of output value after 24h under exactly same conditions (temperature = RT, rate stimulus = 0°/s, etc.), without power on drift	XZ	-0.2	-	0.2	°/s
Sensitivity	XZ	-	100	-	LSB/ °/s
Sensitivity error variation to nominal (measured value) (full measurement range)	XZ	-2.9	-	2.9	%
Nonlinearity up to 150 °/s least square fit [-150°/s ... 150°/s]	XZ	-0.5	-	0.5	°/s
Nonlinearity up to 300 °/s least square fit [-300°/s ... 300°/s]	XZ	-1.0	-	1.0	°/s
Micro linearity up to 150 °/s step width: 2.5°/s	XZ	-4	-	4	%
Micro linearity from 150°/s up to 300 °/s step width: 5°/s	XZ	-10	-	10	%
Resolution (physically) Smallest step of the output when raising the input Mean value over >5s with a sample rate of 1kHz per step	XZ	-	-	0.05	°/s
Hysteresis maximum difference between two output signal values at a certain input after changing the input and reapplying it at constant temperature. Valid over full temperature range and full measurement range. (step size 2.5°/s @range <10°/s, averaging time 1s)	XZ	-	-	0.25	°/s
Noise (LF1: 80 Hz filtered data) RMS = standard deviation, ( ) peak to peak Evaluation over a time interval of 1s.	XZ	-	-	0.1 (0.66)	$°/s_{rms}$ $°/s_{pp}$
Noise (LF2: 20 Hz filtered data) RMS = standard deviation, ( ) peak to peak Evaluation over a time interval of 1s.	XZ	-	-	0.06 (0.4)	$°/s_{rms}$ $°/s_{pp}$
Noise (LF3: 10 Hz filtered data) RMS = standard deviation, ( ) peak to peak Evaluation over a time interval of 1s.	XZ	-	-	0.04 (0.27)	$°/s_{rms}$ $°/s_{pp}$

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Parameter / Condition	axis	Min	Typ	Max	Unit
Cross axis sensitivity (w.r.t rotations of sensing element around x, y = tilt) Includes the misalignment of the MEMS element to the housing	Z	-1.74	-	1.74	%
Cross axis sensitivity (w.r.t rotations of sensing element around z = rotation) Includes the misalignment of the MEMS element to the housing.	X	-2.3	-	2.3	%
Overload: recovery time after overload (>1000 °/s) Mechanical shock according to ISO/CD 16750-3 “4.2.2 Mechanical shock test for components on rigid points on the body and on the frame”: 500 m/s² for a 6 ms half-sinusoidal pulse or equivalent shock. @LF1 Hz filter, w/o SOC	XZ	-	-	50	ms
Overload: recovery time after overload (>1000 °/s) (without filter delay)	XZ	-	-	10	ms
Deviation of angular rate signal due to mechanical shock (ISO-16750 50g 6ms shock)	XZ	-		2	°/s
Deviation of angular rate signal due to mechanical shock (JIS-0041 100g 6ms shock)	XZ	-	-	6	°/s
Internal headroom (DC angular rate)	XZ	1000[1]	-	-	°/s
Sensitivity to acceleration impacts for stimulus in either x, y or z direction for the given frequency range 0Hz-20kHz	XZ	-	-	0.2	°/s/g
Sensitivity to acceleration impacts for broadband noise stimulus in either x, y or z direction for the given frequency range 100Hz-5kHz	XZ	-	-	0.45	°/s/g rms
Gyroscope resonance frequency	XZ	22.5	25	27.5	kHz

[1] For configuration option „Error Bouncing Disabled“ the CS can temporarily be triggered earlier (due to noise effects)

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5.2.2 Low-g Sensor

The specifications given in this chapter are valid for the acceleration sensing axes a_x, a_y, a_z independent from the specific sensor module.
All specification cover the sensor module itself when using the standard circuitry.

All specification values are valid in all mounting directions regarding earth gravity.

All specification parameters regarding offset are valid at any time during lifetime, but only the total offset error includes the lifetime drift (i.e. drift between new and aged parts, e.g. resulting from qualification).

The influence of additional error sources like PSRR, EMC and vibration are not included. The behavior of the sensor under such conditions is described in separate reports that can be discussed on request.

The data in this section applies for the valid operation conditions.
All following figures include voltage, temperature and lifetime effects if not noted otherwise.
Sensor data are only valid if no failure flags indicate any malfunction. All values except the noise itself exclude noise effects.

Parameter / Condition	axis	Min	Typ	Max	Unit
Digital output range	XYZ	-32768	-	+32767	LSB
Measurement range LF highest/lowest acceleration which can be measured by sensor (The spec is not guaranteed beyond this range)	XYZ	-6	-	+6	g
Measurement range LF extended (calibration variant available on request) highest/lowest acceleration which can be measured by sensor (The spec is not guaranteed beyond this range)	XYZ	-8	-	+8	g
Total offset error (without slow offset compensation) Mean value over 1s with a sample rate of 1kHz	XY Z	-50 -55	- -	50 55	mg mg
Total offset error (with slow offset compensation)	XYZ	-10	-	10	mg
Residual acceleration offset after fast offset compensation	XYZ	-10	-	10	mg
Regulations speed of acceleration signal slow offset compensation (Measurement range 6g)	XYZ	-	-	1	mg/s
Regulation speed of acceleration signal slow offset compensation (extended measurement range 8g)	XYZ	-	-	1.4	mg/s
Offset power-on span Maximum signal error relative to initial value @0g stimulus Including power on drift effects only, constant temperature valid 0-20 s after power on	XY Z	-5 -10	- -	5 10	mg mg
Offset operational span over temperature and power on Maximum signal span (|max-min| offset value) @0g stimulus. Including temperature, power on effects.	XY Z	- -	- -	20 30	mg mg
Offset short-term gradient @ max +/- 6.0 K/min temperature ramp defined by linear fit over 1 minute intervals during temperature ramp valid >20 s after power on	XYZ	-5	-	5	mg/min
Offset temperature gradient @ max. +/- 6.0 K/min temperature ramp valid >20 s after power on	XYZ	-5	-	5	mg/K
Offset drift over time at constant temperature (24h) Drift of output value after 24h under exactly same conditions (temperature = RT, acceleration = 0g, etc.), without power on drift	XYZ	-10	-	10	mg
Sensitivity (6g range)	XYZ	-	5000	-	LSB/g
Sensitivity (8g range) calibration Variant	XYZ	-	3750	-	LSB/g
Sensitivity error variation to nominal (measured value) (full measurement range)	XYZ	-2.9	-	2.9	%

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Parameter / Condition	axis	Min	Typ	Max	Unit
Nonlinearity up to 2g least square fit [-2g ... 2g]	XYZ	-15	-	15	mg
Nonlinearity up to 8g (calibration Variant) least square fit [-8g ... 8g]	XYZ	-30	-	30	mg
Micro linearity up to 8g step width 100mg	XYZ	-5	-	5	%
Resolution (physically) Smallest step of the output when raising the input Mean value over >5s with a sample rate of 1kHz per step	XYZ	-	-	1	mg
Hysteresis maximum difference between two output signal values at a certain input after changing the input and reapplying it at constant temperature. Valid over full temperature range and full measurement range.	XYZ	-5	-	5	mg
Noise (LF1: 80Hz filtered data) RMS = standard deviation, ( ) peak to peak Evaluation over a time interval of 1s.	XY Z	-	-	4 (27) 6 (40)	$mg_{rms}(mg_{pp})$ $mg_{rms}(mg_{pp})$
Noise (LF2: 20Hz filtered data) RMS = standard deviation, ( ) peak to peak Evaluation over a time interval of 1s.	XY Z	-	-	2 (14) 3 (20)	$mg_{rms}(mg_{pp})$ $mg_{rms}(mg_{pp})$
Noise (LF3: 10Hz filtered data) RMS = standard deviation, ( ) peak to peak Evaluation over a time interval of 1s.	XY Z	-	-	1.5 (10) 2.2 (15)	$mg_{rms}(mg_{pp})$ $mg_{rms}(mg_{pp})$
Cross axis sensitivity a_z (w.r.t rotations of sensing element around x, y = tilt) Includes the misalignment of the mechanical element to the housing	Z	-1.74	-	1.74	%
Cross axis sensitivity a_x, a_y (w.r.t rotations of sensing element around z = rotation) Includes the misalignment of the mechanical element to the housing.	XY	-2.3	-	2.3	%
Overload: recovery time after shock Mechanical shock according to ISO/CD 16750-3 “4.2.2 Mechanical shock test for components on rigid points on the body and on the frame”: 500 m/s² for a 6 ms half-sinusoidal pulse. @80Hz filter, w/o SOC	XYZ	-	-	50	ms
Overload: recovery time on over range Additional delay to the time shift of the transfer characteristics of the output signal (= without filter flush time) to return to 95 % of the final value of the output signal after over range.	XYZ	-	-	10	ms
Internal headroom (static clipping) (static condition at 0 Hz)	XY Z	+/- 35 +/- 25	-	-	g

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5.2.3 Mid-g Sensor (HF Channel)

The specifications given in this chapter are valid for the acceleration sensing axes ax, ay, az unless stated otherwise. Independent from the specific sensor module.

All specification cover the sensor module itself when using the standard circuitry.
All specification cover the sensor module itself and its standard circuitry, unless stated otherwise.
All specification values are valid in all mounting directions regarding earth gravity.
All specification parameters regarding offset are valid at any time during lifetime, but only the total offset error includes the lifetime drift (i.e. drift between new and aged parts, e.g. resulting from qualification).

The influence of additional error sources like PSRR, EMC and vibration are not included. The behavior of the sensor under such conditions is described in separate reports that can be discussed on request.

The data in this section applies for the valid operation conditions.

All following figures include voltage, temperature and lifetime effects if not noted otherwise.

Sensor data are only valid if no failure flags indicate any malfunction. All values except the noise itself exclude noise effects.

Parameter / Condition	axis	Min	Typ	Max	Unit
Digital output range	XYZ	-	±18250	-	LSB
Measurement range HF channel (symmetric around zero) highest/lowest acceleration which can be measured by sensor. Z-channel range is part individual.	XY Z	±35 ±25	- -	±35 ±35	g g
Total offset error	XY Z	-50 -55	- -	50 55	mg mg
Offset short term drift span over temperature and power on. Maximum signal span (|max-min| offset value) @0g stimulus. Including temperature, power on effects.	XYZ	-	-	100	mg
Sensitivity calibration Variant (LF 6g range)	XYZ	-	500	-	LSB/g
Sensitivity calibration Variant (LF 8g range)	XYZ	-	375	-	LSB/g
Sensitivity error measurement range [-8g;+8g]	XYZ	-2.9	-	2.9	%
Sensitivity error full measurement range	XYZ	-5	-	5	%
Nonlinearity full measurement range	XYZ	-700	-	700	mg
Resolution (physically) Smallest step of the output when raising the input	XYZ	-	-	2	mg
Noise HF RMS = standard deviation, ( ) peak to peak Evaluation over a time interval of 1s.	XYZ	-	-	20 (132)	mg_{rms} mg_{pp}
Cross axis sensitivity a_z (w.r.t rotations of sensing element around x, y = tilt) Includes the misalignment of the mechanical element to the housing	Z	-1.74	-	1.74	%
Cross axis sensitivity a_x, a_y (w.r.t rotations of sensing element around z = rotation) Includes the misalignment of the mechanical element to the housing.	XY	-2.3	-	2.3	%

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5.2.4 Temperature Sensor

The parameter specification is valid only for the on-chip temperature of the ASIC. All parameters are referenced to on chip condition.

The temperature offset and a deviant dynamic behavior caused by the sensor package, PCB or/and ECU environment must be considered in addition.

Parameter / Condition	Min	Typ	Max	Unit
Measurement range	-40	-	150	°C
Temperature signal internal bit width (see SPI definition for output bit width)	-	16	-	LSB
Sensitivity	-	200	-	LSB/K
Sensitivity error	-6	-	6	%
Nonlinearity (full measurement range)	-2	-	2	K
Offset over all	-4	-	4	K
Temperature offset at 0 LSB	-	50	-	°C
Noise	-	-	0.1 (0.66)	K_{rms} K_{pp}
Corner frequency (-3dB)	70	-	90	Hz
Update rate at output	-	1024	-	Hz

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5.3 Signal filtering and digital signal processing

The SMI8 offers 3 different LF filter characteristics described in chapter 5.3.2. Only one of these selections is active in the LF channel at the same time. The LF filter setting applies to all LF output signal channels. The HF output channels have a fixed filter setting.

5.3.1 Signal update rate

Parameter / Condition	Min	Typ	Max	Unit
New signal value available, rate and acceleration output after LF-filter	1875	2083	2292	Hz
New signal value available, acceleration output after HF-filter	7500	8332	9167	Hz

5.3.2 Frequency response

The following filter specification is valid for the complete sensor including mechanical, analogue and digital filter elements. Specifications for the filters are valid without offset cancelation.

Parameter definition:

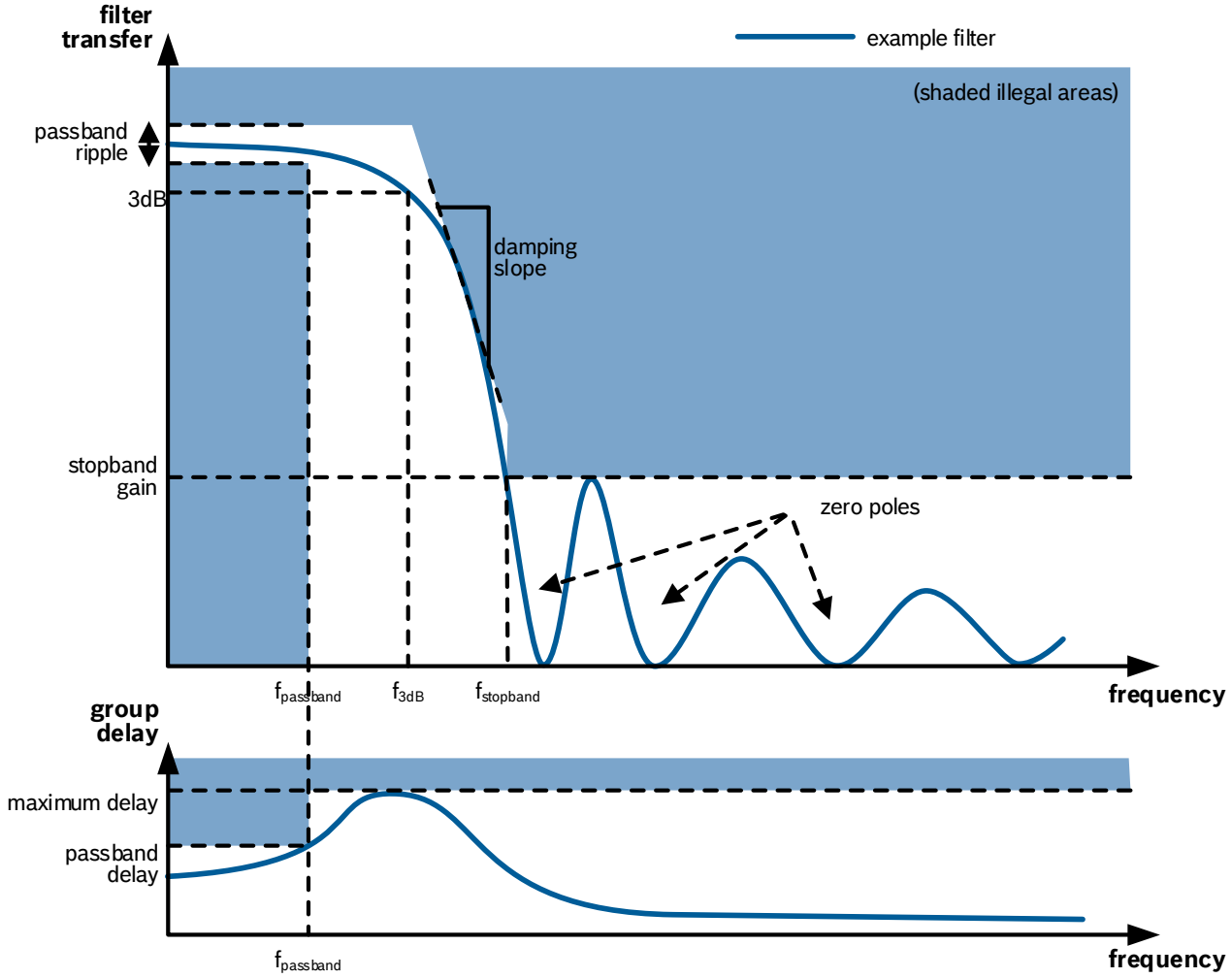

Figure 11 Signal filtering definition

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5.3.2.1 Filter specification LF1 (80Hz)

Parameter / Condition	Min	Typ	Max	Unit
$f_{passband}$ (Damping <0.2dB)	-	20	-	Hz
$f_{stoppband}$ (Damping -40dB)	-	170	-	Hz
Corner frequency (-3dB) Rate	67.5	75	82.5	Hz
Corner frequency (-3dB) ACC (x/y)	66.6	75	81.4	Hz
Corner frequency (-3dB) ACC (z)	57	70	79	Hz
Passband group delay	6	-	10	ms
Filter flush time (default and recommended)		25		ms
Phase delay Difference Any channel versus another	-2	-	2	ms
3dB difference of acc. x/y channel vs. acc. x/y channel or angular rate channel	-4	-	4	Hz
3dB difference of acc. z channel vs. acc. x/y channel or angular rate channel	-10	-	4	Hz

5.3.2.2 Filter specification LF2 (20Hz)

Parameter / Condition	Min	Typ	Max	Unit
$f_{passband}$ (Damping <0.2dB)	-	5	-	Hz
$f_{stoppband}$ (Damping -40dB)	-	50	-	Hz
Corner frequency (-3dB)	15.3	17.3	19	Hz
Passband group delay	24		31	ms
Filter flush time (default and recommended)		60		ms

5.3.2.3 Filter specification LF3 (10Hz)

Parameter / Condition	Min	Typ	Max	Unit
$f_{passband}$ (Damping <0.2dB)	-	2.5	-	Hz
$f_{stoppband}$ (Damping -50dB)	-	25	-	Hz
Corner frequency (-3dB)	9.8	10.8	11.8	Hz
Passband group delay	51		65	ms
Filter flush time (default and recommended)	-	160	-	ms

5.3.2.4 Filter specification HF

Parameter / Condition	Min	Typ	Max	Unit
Corner frequency (-3dB) x,y axis	210	266	330	Hz
Passband group delay x,y axis	1		2	ms
Corner frequency (-3dB) z axis	110	170	240	Hz
Passband group delay z axis	1		3	ms
Filter flush time (default and recommended)	-	10	-	ms

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5.4 Start-up Timing

Parameter / Condition	Min	Typ	Max	Unit
SPI communication fully functional (waiting time after power on / reset / soft reset)	-	-	50	ms
Waiting time after power on / reset /soft reset until writing end of configuration (EOC) bit	50	-	-	ms
Soft configuration phase (defined by SPI Master) dependent on the amount of configuration services triggered. Depends on SPI clock rate and sequential transfer delay time. Typical value assuming 2 full configuration services (16 SPI commands @4MHz) with sequential transfer delay of 1ms.	-	17	-	ms
Start-up time after EOC (end of configuration) Includes the timing for sensor start-up and 1 successful initial self-test (BITE+ACC Sum-C test). Sensor is fully functional, and flags cleared. Using LF1 filter setting with the corresponding flush time	-	-	150	ms
Power on start-up time Time interval from power supply reaching the specified supply voltage range to an output within the specified accuracy. The sensor is fully functional, initial self-tests with 1 BITE and 1 ACC Sum-C test is complete and flags cleared. This parameter does not include waiting time for configuration commands to be sent by the system. Using LF1 filter setting with the corresponding flush time.	-	-	200	ms
Self-test time (for one BITE) Note: in the case of the ACC BITE repetitions, a break of varied duration with the following sequence is implemented: 5ms, 10ms, 15ms, 10ms, 5ms, 10ms,... (see 7.1.3.2 and 7.1.1.8)	-	60	65	ms
ACC-Sum-C Sum Self-test time (for one BITE)	-	-	30	ms

Earlier SPI communication than "SPI communication fully functional" is allowed but the sensor's response might be invalid or no communication at all.

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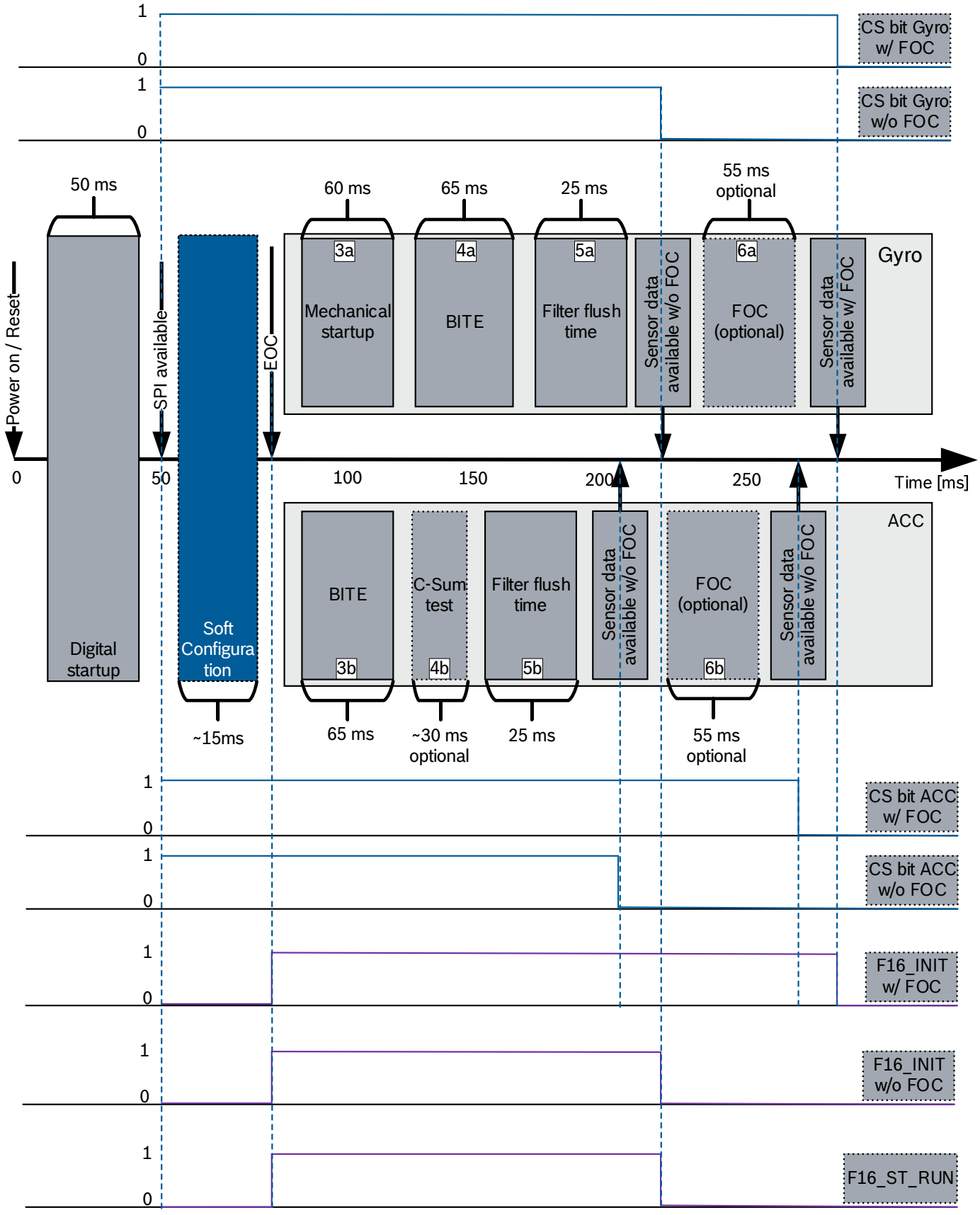

Figure 12 Start-up Timing diagram: typical timing for LF1 filter, 1 BITE and offset cancellation

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Gyroscope start-up timing table for LF1 with 1 BITE and fast offset compensation with typical timing

Step	Description	Time [ms]
1	Digital start, after this is the SPI is available	50
2	Sensor module soft configuration (see 7.1.1)	17
3a	Mechanical startup of gyroscope.	60
4a	Self-test for gyroscope (BITE)	65
5a	Filter flush waiting time	25
Sensor data available without FOC		**217**
6a	Fast offset compensation	55
Sensor data available		**272**

Accelerometer start-up timing table for LF1 with 1 BITE and fast offset compensation with typical timing

Step	Description	Time [ms]
1	Digital start, after this is the SPI is available	50
2	Sensor module soft configuration (see 7.1.1)	17
3b	Self-test for acceleration (BITE)	65
4b	ACC-Sum-C Sum test	30
5b	Filter flush waiting time	25
Sensor data available without FOC		**187**
6b	Fast offset compensation	55
Sensor data available		**242**

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6 Software interface description

6.1 SPI System Description

The Serial Clock (SCK) input represents the master's clock signal. This clock determines the speed of data transfer and the data transmission is done synchronous to this clock. Chip Select (CSB) activates the SPI interface. As long as CSB is high, the sensor will not accept the clock signal or data input. The sensor output (MISO) is in high impedance. Whenever CSB is in a low physical state, data can be transferred between the microcontroller and sensor module. Commands are transmitted through the Sensor Input (MOSI) pin to the sensor and the sensor returns its response through the Sensor Output (MISO) pin. Sensors can be logically addressed and only sensors which are asked will respond. Each module may contain several sensor channels. Several modules may be connected on one chip select line.

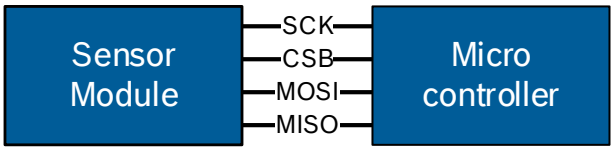

Figure 13 SPI Interface

If two modules on the same bus receive different bus addresses (e.g. due to errors) it may lead to two modules which drive the bus. This will lead to a CRC error.

The sensor modules have individual bus addresses. This allows to connect up to 4 modules to the same CSB line. In case that two sensors are addressed simultaneously (e.g. due to errors) it may lead to two sensors trying to drive the bus. This will lead to a CRC error.

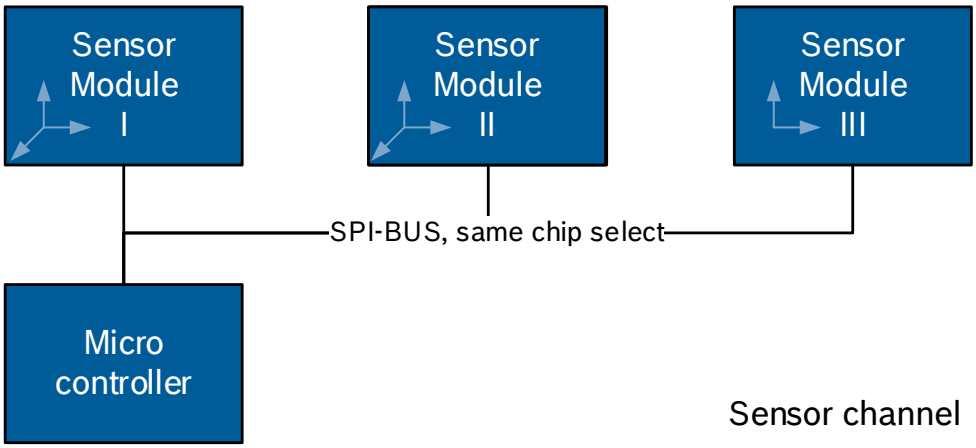

Figure 14 Sensor configuration and difference between sensor modules and sensor channel

6.2 Timing for SPI slave

SPI clock phase and polarity are sensor individually configurable.

SPI Timing: Master-point of view

(SMI is slave)

Parameter / Condition	Min	Typ	Max	Unit
A- MISO data valid time (CSB)	-	-	40	ns
B- MISO data valid time (SCK)	-	-	40	ns
C- MISO data hold time MISO data is stable until the next SCK shift edge	half clock period + switch time		-	ns
D- MISO rise/fall time	-		15	ns
E- MISO data disable lag time	-		50	ns

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The parameters mentioned in the table are valid for minimum VDD_IO voltage, capacitive load of 100 pF (SCK) and the minimum MEMS resonance frequency (PLL).

Parameters may be better for specified operating conditions, i.e.voltages, drive frequency and capacitive loads (as far as covered by operating condition specification).

Parameter A, B do not include the rise/fall time of CSB and SCK.

Requirements to master from slave-point of view (SMI is slave, parameters to be guaranteed by external SPI master):

SPI Timing: Slave-point of view

(SMI is slave, parameters to be guaranteed by external SPI master)

Parameter / Condition	Min	Typ	Max	Unit
4- SCK disable lead time	10	-	-	ns
5 - SCK enable lead time (CPHA = 0)	40	-	-	ns
5 - SCK enable lead time (CPHA = 1)	10	-	-	ns
6 - SCK enable lag time	20	-	-	ns
7 - SCK disable lag time	10	-	-	ns
9 - Sequential transfer delay SMI8-32OUT	750	-	-	ns
9 - Sequential transfer delay SMI8-32OUT after writing CONF_IREG0 register	500	-	-	µs
9 - Sequential transfer delay SMI8-32IN	200	-	-	ns
9 - Sequential transfer delay SMI8-32IN after writing CONF_IREG0 register	500	-	-	µs
10 - MOSI rise / fall time	-	-	-	ns
11 - MOSI data setup time	10	-	-	ns
12 - MOSI data hold time	20	-	-	ns

The table assumes 10 MHz mode, max load.

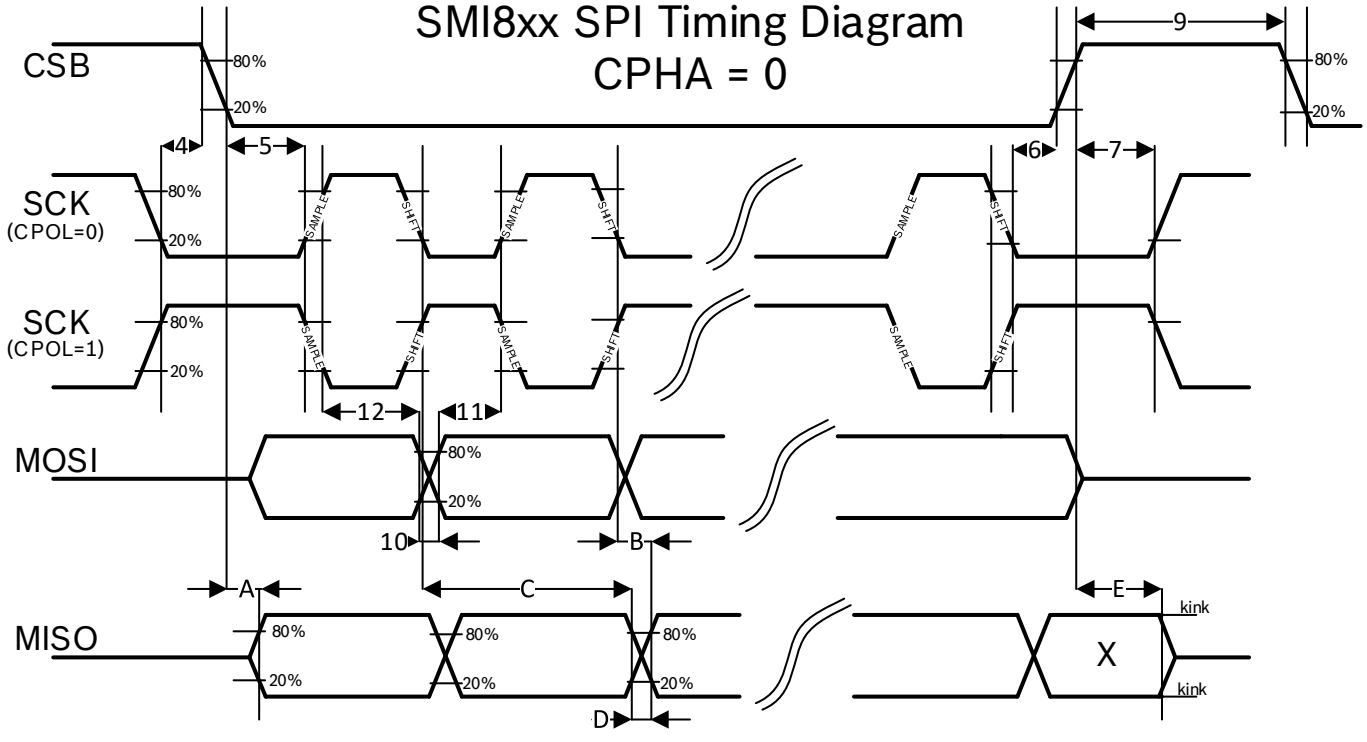

Figure 15 Timing diagram of information on 1st edge of SCK

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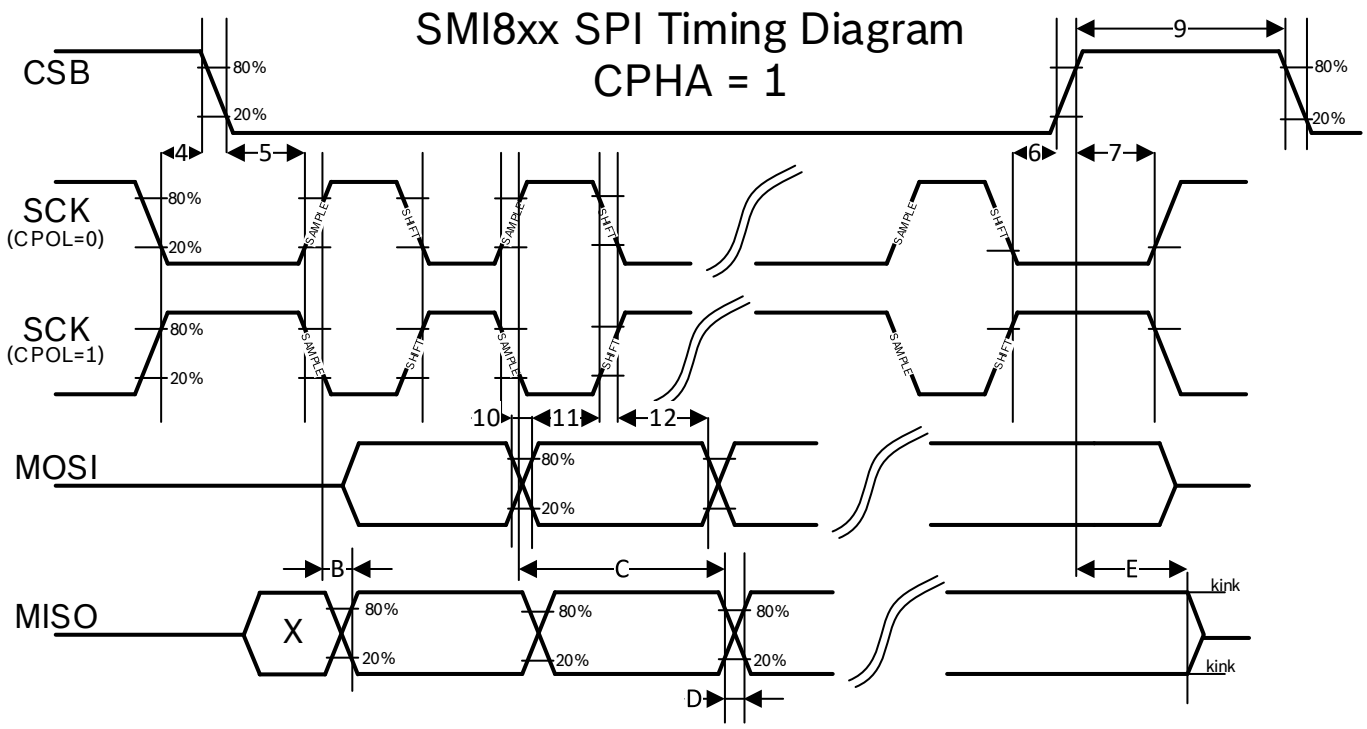

Figure 16 Timing diagram-sampling of information on 2nd edge of SCK

6.3 Data link layer

6.3.1 SPI slave activation

The SPI slave interface is locked after power on until the interface has been configured by the internal bootloader. While the interface is locked all requests are ignored and no response will be generated (MISO will stay at high impedance).

6.3.2 Polarity, phase and protocol selection / command calibration

The initial polarity, phase and type for the SPI protocol (SMI8-32IN or SMI8-32OUT) is programmed at Bosch plant.

6.3.3 Data capturing

The protocol features data capturing on different channels and modules. This means that sensor measurement data and channel status of all channels (LF and HF) on one chip select line can be captured (stored sensor internally) at one point in time and read out at a later point in time. For the cluster flags channel, the data capturing is not supported. A capturing of cluster flag channel results in wrong CRC in the SPI MISO frame (inframe) or CE bit (out of frame).

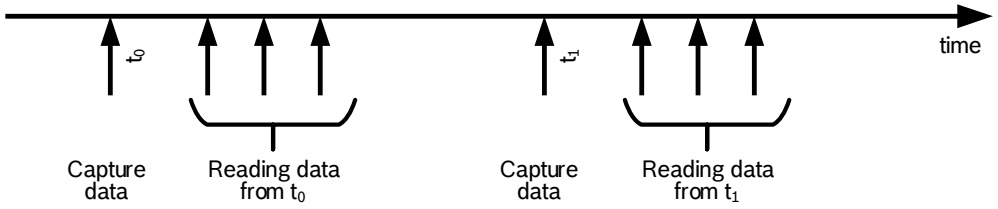

Figure 17 Data capturing

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6.3.4 Sensor addressing

The sensor can be used on a SPI bus with several sensors on one chip select line. Different sensors can be addressed logically. Each sensor module has a specific bus address to communicate with. Each channel of a sensor module (e.g. rate, acceleration, and for acceleration channels LF and HF output) has also its own bus address. For example, a 3DOF sensor has 1 module-address, 1 broadcast address and 5 channel addresses. If measurement data of a sensor is requested, one of the channel addresses is used.

The busaddress (BADR) is the beginning of each MOSI SPI communication frame described in chapter 6.4 it covers the bits 31 to 27 of the 32-bit SPI protocols.

BADR(3): Used to address sensors that are connected to the same CSB line. The sensor address bit 3 can be set by applying a voltage level to the ID pin. via the potential applied to the ID pin. The ID pin logic level will be sampled once at the end of the boot loading. (Low potential = 0, high potential = 1).

BADR(4): Denotes the module type (SMI810/SMI800) and is provided during boot loading from the OTP (written during module calibration at Bosch plant). Please note that for a 5DoF sensor, BADR (4) is part of the sensor channel address and cannot be programmed.

Broadcast Address: Using the broadcast address BADR(2:0)= 000b the upper bits of the bus address BADR(4:3) are ignored and a module always reacts regardless of its actual module address as if a module command had been sent. This address can be used in a single sensor configuration or during manufacturing when the module address is not known.

Module Address: Using the module address BADR (2:0) = 001b the upper bits of the bus address BADR(4:3) are evaluated and only the module configured with the corresponding settings will recognize the module command. Other sensors possibly connected on the same chip select line will not react.

Unused addresses are detected by wrong CRC in MISO.

Valid addresses for SMI860 are:

BADR(4)	BADR(3)	BADR(2)	BADR(1)	BADR(0)	Meaning
0	ID pin	0	0	0	Module Broadcast
0	ID pin	0	0	1	Module Address
0	ID pin	0	1	0	YRS1_LF(ωx)
0	ID pin	0	1	1	Cluster Flags
0	ID pin	1	0	0	ACC1_LF(y)
0	ID pin	1	0	1	ACC1_HF(y)
0	ID pin	1	1	0	ACC2_LF(x)
0	ID pin	1	1	1	ACC2_HF(x)
1	ID pin	0	1	0	YRS2_LF(ωz)
1	ID pin	1	1	0	ACC3_LF(z)
1	ID pin	1	1	1	ACC3_HF(z)

BADR(4): 0: SMI800, 1: SMI810, SMG810

Valid addresses for SMI800 are:

BADR(4)	BADR(3)	BADR(2)	BADR(1)	BADR(0)	Meaning
0	ID pin	0	0	0	Module Broadcast
0	ID pin	0	0	1	Module Address
0	ID pin	0	1	0	YRS1-LF(ωz)
0	ID pin	0	1	1	Cluster Flags
0	ID pin	1	0	0	ACC1_LF(y)
0	ID pin	1	0	1	ACC1_HF(y)
0	ID pin	1	1	0	ACC2_LF(x)
0	ID pin	1	1	1	ACC2_HF(x)

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Valid addresses for SMI810 are:

BADR(4)	BADR(3)	BADR(2)	BADR(1)	BADR(0)	Meaning
1	ID pin	0	0	0	Module Broadcast
1	ID pin	0	0	1	Module Address
1	ID pin	0	1	0	YRS1-LF(ωx)
1	ID pin	0	1	1	Cluster Flags
1	ID pin	1	0	0	ACC1_LF(y)
1	ID pin	1	0	1	ACC1_HF(y)
1	ID pin	1	1	0	ACC2_LF(z)
1	ID pin	1	1	1	ACC2_HF(z)

Valid addresses for SMG810 are:

BADR(4)	BADR(3)	BADR(2)	BADR(1)	BADR(0)	Meaning
1	ID pin	0	0	0	Module Broadcast
1	ID pin	0	0	1	Module Address
1	ID pin	0	1	0	YRS1-LF(ωx)
1	ID pin	0	1	1	Cluster Flags

Assignment of sensing directions to SPI addresses and error counters:

	Error Counter	SMI800	SMI810	SMG810	SMI860
ACC1_HF	EC0	Y	Y		Y
ACC1_LF	EC1	Y	Y		Y
ACC2_HF	EC2	X	Z		X
ACC2_LF	EC3	X	Z		X
ACC3_HF	EC6				Z
ACC3_LF	EC7				Z
YRS1_LF	EC5	Z	X	X	X
YRS2_LF	EC4				Z

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6.4 SPI protocols

The sensor module provides two types of SPI protocols: in- frame and out of frame. Both have request and reply messages with 32 bit length. The in-frame protocol interleaves request and reply in one frame. The second protocol separates request and reply in two consecutive frames.

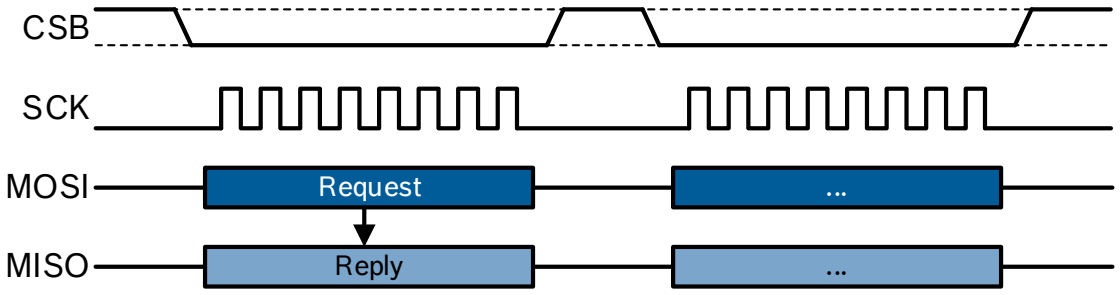

Figure 18 In-frame communication. Request and reply in one frame.

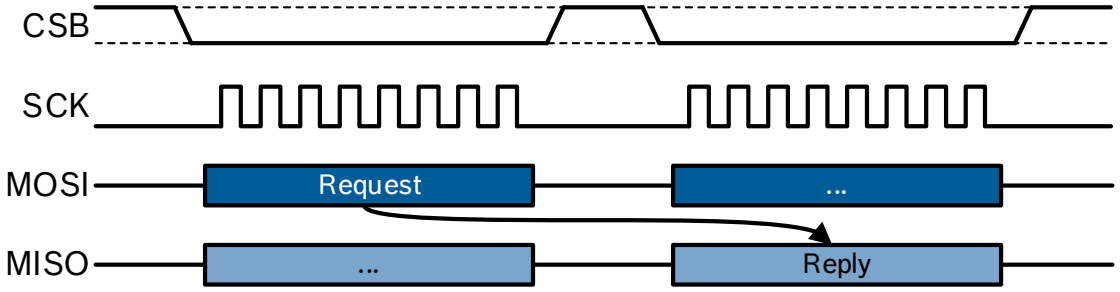

Figure 19 Out-of -frame communication. Reply is given in the frame after the request.

6.4.1 SPI dialect SMI8-32OUT

The frame is an 'out- of- frame' protocol with 32 clock cycles. Out- of- frame means that the logical response to a request is given in the next frame. All internal registers can be accessed using an offset-address concept. The dialect SMI8-32OUT conforms to Safe SPI requirements.

6.4.1.1 Sensor data commands

If the bus-address is not a sensor module address (XX000b or XX001b) the sensor interprets the command as sensor channel command. The addressed channel will respond to the command. Capture bits are interpreted from all modules on a chip select line.

MOSI frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
BADR (4..0)					CAP			*	*	*	*	*	*	*	*	*	*	*	*	*	*	CRCA		
1/0					1/0			0	*													1/0		

Field	Description
BADR (4..0)	Bus Address
	5 bit combined sensor and channel address XX001b: valid module-address, one module will react XX000b: broadcast-address : all modules will react If BADR(4..0) is a broadcast address the command will be interpreted as module command
CAP (2..0)	Capture mode

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Field	Description
	Bits to define if captured or current data should be read and if data should be captured: 011b: read current data and channel-status (do not alter captured data) 010b: read captured data and channel status (do not capture or alter captured data) 101b: sensor channels of any module on the bus must capture data and channel status of all channels. The channel which is addressed with BADR feedbacks captured data of selected channel as response to capture command. else: reserved (illegal command)
CRCA	3bit CRC
	Polynom: x^3+x+1, target value 000b. CRCA over bits 31 to 3, start value: 101b (SPI32 out-of-frame)

MISO frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
SD	SID (4..0)					*	CE	OC	*	*	INIT	Data (15..0)									CS	CRCA		
1	1/0					*	1/0	1/0	*	*	1/0	1/0									1/0	1/0		

Field	Description
SID (4..0)	Safety ID
	Channel ID for a specific channel (rate, acceleration A, acceleration B, HF and LF output channel). While BADR is fixed, SID is programmable.
SD	Sensor Data (Frame Select)
	Selects Sensor channel data or module data frame. 0: module data 1: sensor data
INIT	Initialization Status
	0: Self-Test inactive 1: Self-Test active: Initialization after reset OR ASIC internal tests (e.g. LBIST) OR mechanical self-test
CE	Command Error
	0: no error 1: error occurred in last frame
OC	Offset Controller Status for specific channel
	0: Offset Controller deactivated 1: Offset controller activated
DATA (15..0)	Data
	Two’s complement sensor data of selected channel
CS	Channel Status
	0: channel sensor data fully valid 1: channel sensor data not valid (sensor error, initialization, or self-test) if captured data is read, then the CS-bit is the captured CS OR the actual CS Please note: CS and CE Bit are not correlated, i.e. customer needs to evaluate both bits on system level independently Not used for “cluster flags” command (always 0)
CRCA	3bit CRC
	Polynom: x^3+x+1, target value 000b. CRCA over bits 31 to 3, start value: 101b (SPI32 out-of-frame)

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Examples of out of frame sensor data commands

The following table shows the SPI commands in hex format that can be sent out (on MOSI line) by the master in order to read data from the sensor.

Command	SMI800 ID0	SMI800 ID1	SMI810 ID0	SMI810 ID1	SMG810 ID0	SMG810 ID1	SMI860 ID0	SMI860 ID1
YRS1	13000007 ωZ	53000003 ωZ	93000004 ωX	D3000000 ωX	93000004 ωX	D3000000 ωX	13000007 ωX	53000003 ωX
YRS2	-	-	-	-	-	-	93000004 ωZ	D3000000 ωZ
ACC1 LF	23000004 aY	63000000 aY	A3000007 aY	E3000003 aY	-	-	23000004 aY	63000000 aY
ACC1 HF	2B000001 aY	6B000005 aY	AB000002 aY	EB000006 aY	-	-	2B000001 aY	6B000005 aY
ACC2 LF	33000005 aX	73000001 aX	B3000006 aZ	F3000002 aZ	-	-	33000005 aX	73000001 aX
ACC2 HF	3B000000 aX	7B000004 aX	BB000003 aZ	FB000007 aZ	-	-	3B000000 aX	7B000004 aX
ACC3 LF	-	-	-	-	-	-	B3000006 aZ	F3000002 aZ
ACC3 HF	-	-	-	-	-	-	BB000003 aZ	FB000007 aZ
Cluster flags	1B000002	5B000006	9B000001	DB000005	9B000001	DB000005	1B000002	5B000006
Trigger capture & Read YRS1	15000006 ωZ	55000002 ωZ	95000005 ωX	D5000001 ωX	95000005 ωX	D5000001 ωX	15000006 ωX	55000002 ωX
captured YRS1	12000004 ωZ	52000000 ωZ	92000007 ωX	D2000003 ωX	92000007 ωX	D2000003 ωX	12000004 ωX	52000000 ωX
captured YRS2	-	-	-	-	-	-	92000007 ωZ	D2000003 ωZ
captured ACC1 LF	22000007 aY	62000003 aY	A2000004 aY	E2000000 aY	-	-	22000007 aY	62000003 aY
captured ACC1 HF	2A000002 aY	6A000006 aY	AA000001 aY	EA000005 aY	-	-	2A000002 aY	6A000006 aY
captured ACC2 LF	32000006 aX	72000002 aX	B2000005 aZ	F2000001 aZ	-	-	32000006 aX	72000002 aX
captured ACC2 HF	3A000003 aX	7A000007 aX	BA000000 aZ	FA000004 aZ	-	-	3A000003 aX	7A000007 aX
captured ACC3 LF	-	-	-	-	-	-	B2000005 aZ	F2000001 aZ
captured ACC3 HF	-	-	-	-	-	-	BA000000 aZ	FA000004 aZ

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6.4.1.2 Module Commands

MOSI frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
BADR (4..0)					W	A (6..0)							W-Data (15..0)									CRCA		
1/0					1/0	1/0							1/0									1/0		

Field	Description
BADR (4..0)	Bus Address
	5 bit combined sensor and channel address XX001b: valid module-address, one module will react XX000b: broadcast-address : all modules will react If BADR(4..0) is a broadcast address the command will be interpreted as module command
W	Write access
	W=1: write W-DATA (bits 3 to 18) to sensor register A(6:0) W=0: read data from address A(6:0). Bits 3-18 are ignored. Writing to a read only register gives a CE in the response frame.
A (6..0)	Address
	Address of data to be read or to be written A(6..0)
W-DATA (15..0)	Write Data
	Data to be written to the sensor if W=1
CRCA	3bit CRC
	Polynom: x^3+x+1, target value 000b. CRCA over bits 31 to 3, start value: 101b (SPI32 out-of-frame)

MISO frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
SD	MID (2..0)			CE	*	A (6..0)							R-Data (15..0)									CRCA		
0	1/0			1/0	*	1/0							1/0									1/0		

Field	Description
MID (2..0)	Module ID
	identifies, which module responded MID(2:1) = BADR(4:3) MID(0) = BADR(0) 1: reaction on individual module command 0: reaction on broadcast command (broadcast commands are often used during final measurement in order to simplify the communication)
CE	Command Error
	0: no error 1: error occurred in last frame
SD	Sensor Data (Frame Select)
	Selects sensor channel data or module data frame. 0: module data 1: sensor data
A (6..0)	Address
	Address of data to be read or to be written A(6..0) = PG(2..0) + ADR(3..0)
R_DATA (15..0)	Read Data
	Data read from sensor: Answers to module command 'WRITE' contain the written data in the 'R-DATA'-field
CRCA	3bit CRC
	Polynom: x^3+x+1, target value 000b. CRCA over bits 31 to 3, start value: 101b (SPI32 out-of-frame)

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Examples of out of frame module commands

The following table shows the SPI commands in hex format that can be sent out (on MOSI line) by the master in order to read register data from the sensor.

Command	SMI800 ID0	SMI800 ID1	SMI810 ID0	SMI810 ID1	SMG810 ID0	SMG810 ID1	SMI860 ID0	SMI860 ID1
Write EOC bit	0C50000D	4C500009	8C50000E	CC50000A	8C50000E	CC50000A	0C50000D	4C500009
Read SPI counter	08580006	48580002	88580005	C8580001	88580005	C8580001	08580006	48580002
Read Reset detection flag	08700000	48700004	88700003	C8700007	88700003	C8700007	08700000	48700004
Read State of Offset Controller	08900007	48900003	88900004	C8900000	88900004	C8900000	08900007	48900003
Write 0xB26C to reset sensor	0CD59361	4CD59365	8CD59362	CCD59366	8CD59362	CCD59366	0CD59361	4CD59365
Read temperature signal	09000005	49000001	89000006	C9000002	89000006	C9000002	09000005	49000001
Read error flag bank 0	09080002	49080006	89080001	C9080005	89080001	C9080005	09080002	49080006
Read error flag bank 1	09100000	49100004	89100003	C9100007	89100003	C9100007	09100000	49100004
Read error flag bank 2	09180007	49180003	89180004	C9180000	89180004	C9180000	09180007	49180003
Read error flag bank 3	09200004	49200000	89200007	C9200003	89200007	C9200003	09200004	49200000
Read error flag bank 4	09280003	49280007	89280000	C9280004	89280000	C9280004	09280003	49280007
Read error flag bank 5	09300001	49300005	89300002	C9300006	89300002	C9300006	09300001	49300005
Read error flag bank 6	09380006	49380002	89380005	C9380001	89380005	C9380001	09380006	49380002
Read error flag bank 7	09400007	49400003	89400004	C9400000	89400004	C9400000	09400007	49400003
Read error flag bank 8	09480000	49480004	89480003	C9480007	89480003	C9480007	09480000	49480004
Read error flag bank 9	09500002	49500006	89500001	C9500005	89500001	C9500005	09500002	49500006
Read err_cnt_comb_0	09580005	49580001	89580006	C9580002	89580006	C9580002	09580005	49580001
Read err_cnt_comb_1	09600006	49600002	89600005	C9600001	89600005	C9600001	09600006	49600002
Read err_cnt_comb_2	09680001	49680005	89680002	C9680006	89680002	C9680006	09680001	49680005
Read err_cnt_comb_3	09700003	49700007	89700000	C9700004	89700000	C9700004	09700003	49700007
Read error_group_out	09780004	49780000	89780007	C9780003	89780007	C9780003	09780004	49780000
Read ASIC_SERIAL_NR_0	0A000000	4A000004	8A000003	CA000007	8A000003	CA000007	0A000000	4A000004
Read ASIC_SERIAL_NR_1	0A080007	4A080003	8A080004	CA080000	8A080004	CA080000	0A080007	4A080003
Read ASIC_SERIAL_NR_2	0A100005	4A100001	8A100006	CA100002	8A100006	CA100002	0A100005	4A100001
Read ASIC_NAME	0A180002	4A180006	8A180001	CA180005	8A180001	CA180005	0A180002	4A180006
Read SMI_SERIAL_NR_0	0A280006	4A280002	8A280005	CA280001	8A280005	CA280001	0A280006	4A280002
Read SMI_SERIAL_NR_1	0A300004	4A300000	8A300007	CA300003	8A300007	CA300003	0A300004	4A300000
Read SMI_SERIAL_NR_2	0A380003	4A380007	8A380000	CA380004	8A380000	CA380004	0A380003	4A380007
Read CUSTOMER_SERIAL_NR	0A400002	4A400006	8A400001	CA400005	8A400001	CA400005	0A400002	4A400006

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6.4.1.3 Register addressing

The SMI8-32OUT protocol allows direct addressing of registers. For that the module command SPI frame is used:

MOSI frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
BADR (4..0)					W	A (6..0)							W-Data (15..0)									CRCA		
1/0					1/0	1/0							1/0									1/0		

The A field contains the register address to access.

The following table describes the accessible registers. Please note:

Not used. Stands for ‘not allowed’. A write attempt to a 'not allowed' register will be ignored and the CE (Command error) bit is set in the response. Write access to n.a. register must be avoided.

- means ‘content not defined’.

SPI32OUT address(A)	Signal	Access	Function
0x00	CONF_IREG0	r/w	SMI8xy micro controller service routines. Used to trigger self test or soft configuration.
0x01	CONF_IREG1	r/w	SMI8xy micro controller service routines. Used to trigger self test or soft configuration.
0x02	CONF_IREG2	r/w	SMI8xy micro controller service routines. Used to trigger self test or soft configuration.
0x03	CONF_IREG3	r/w	SMI8xy micro controller service routines. Used to trigger self test or soft configuration.
0x04	CONF_OREG0	r-only	SMI8xy micro controller service routines.
0x05	CONF_OREG1	r-only	SMI8xy micro controller service routines.
0x06	CONF_OREG2	r-only	SMI8xy micro controller service routines.
0x07	CONF_OREG3	r-only	SMI8xy micro controller service routines.
0x08	not used	-	-
0x09	not used	-	-
0x0A	EOC	r/w	Writing "1" to EOC indicates End of Configuration at startup
0x0B	SPI Counter	r-only	Free running counter on PLL frequency / 4
0x0C	not used	-	-
0x0D	not used	-	-
0x0E	Reset Detection Flag	r-only	"1" at startup and clear-on-read property, read-only
0x0F	not used	-	-
0x10	QUAD2_FINE_DAC	r-only	SMI860 only. Quadrature controller output. Signed 16 bit number, two’s complement
0x11	not used	-	-
0x12	Status of Offset Controller	r-only	Max. 6x2 Bits for SMI860
0x13	not used	-	-
0x14	not used	-	-
0x15	QUAD1_FINE_DAC	r-only	Quadrature controller output. Signed 16 bit number, two’s complement
0x16	not used	-	-
0x17	not used	-	-
0x18	not used	-	-
0x19	not used	-	-
0x1A	MAIN_SOFT_RESET	r/w	Same password (0xB26C) as in SMI7 for downwards compatibility
0x1B	not used	-	-
0x1C	not used	-	-

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SPI32OUT address(A)	Signal	Access	Function
0x1D	not used	-	-
0x1E	not used	-	-
0x1F	not used	-	-
0x20	TEMP1	r-only	Temperature Sensor 1 (Signed 16 Bit value)
0x21	error_flag_16_bank0	r-only	see flag list
0x22	error_flag_16_bank1	r-only	see flag list
0x23	error_flag_16_bank2	r-only	see flag list
0x24	error_flag_16_bank3	r-only	see flag list
0x25	error_flag_16_bank4	r-only	see flag list
0x26	error_flag_16_bank5	r-only	see flag list
0x27	error_flag_16_bank6	r-only	see flag list
0x28	error_flag_16_bank7	r-only	see flag list
0x29	error_flag_16_bank8	r-only	see flag list
0x2A	error_flag_16_bank9	r-only	see flag list
0x2B	err_cnt_comb_0	r-only	Bit[15..8] =Acc1 LF Bit[7..0] =Acc1 HF
0x2C	err_cnt_comb_1	r-only	Bit[15..8] =Acc2 LF Bit[7..0] =Acc2 HF
0x2D	err_cnt_comb_2	r-only	Bit[15..8] =Rate1 LF Bit[7..0] =Rate2 LF (SMI860 only)
0x2E	err_cnt_comb_3	r-only	Bit[15..8] =Acc3 LF (SMI860 only) Bit[7..0] =Acc3 HF (SMI860 only)
0x2F	error_group_out	r-only	16 Bit Cluster Flags
0x40	ASIC_SERIAL_NR_0	r-only	Unsigned 16 bit number *
0x41	ASIC_SERIAL_NR_1	r-only	Unsigned 16 bit number*
0x42	ASIC_SERIAL_NR_2	r-only	Unsigned 16 bit number*
0x43	ASIC_NAME	r-only	Unsigned 16 bit number
0x44	not used	-	-
0x45	SMI_SERIAL_NR_0	r-only	Unsigned 16 bit number *
0x46	SMI_SERIAL_NR_1	r-only	Unsigned 16 bit number *
0x47	SMI_SERIAL_NR_2	r-only	Unsigned 16 bit number *
0x48	Configuration number	r-only	Unsigned 16 bit number *
0x49	not used	-	-
0x4A	SIDs	r-only	Bit[14..10] =Clusterflag Bit[9..5] =Acc2-HF Bit[4..0] =Acc1-HF
0x4B	SIDs	r-only	Bit[14..10] =Rate1-LF Bit[9..5] =Acc2-LF Bit[4..0] =Acc1-LF
0x4C	SIDs	r-only	Bit[14..10] =Rate2-LF Bit[9..5] =Acc3-HF Bit[4..0] =Acc3-LF
0x4D	not used	-	-
0x4E	not used	-	-
0x4F	not used	-	-
0x50	LAST_BITE_ACC1_POS	r-only	Result of last BITE Signed 16 bit value
0x51	LAST_BITE_ACC1_NEG	r-only	Result of last BITE Signed 16 bit value
0x52	LAST_BITE_ACC2_POS	r-only	Result of last BITE Signed 16 bit value
0x53	LAST_BITE_ACC2_NEG	r-only	Result of last BITE Signed 16 bit value

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SPI32OUT address(A)	Signal	Access	Function
0x54	LAST_BITE_ACC3_POS	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x55	LAST_BITE_ACC3_NEG	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x56	LAST_BITE_QUAD1_POS	r-only	Result of last BITE Signed 16 bit value
0x57	LAST_BITE_QUAD1_NEG	r-only	Result of last BITE Signed 16 bit value
0x58	LAST_BITE_RATE1_POS	r-only	Result of last BITE Signed 16 bit value
0x59	LAST_BITE_RATE1_NEG	r-only	Result of last BITE Signed 16 bit value
0x5A	LAST_BITE_QUAD2_POS	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x5B	LAST_BITE_QUAD2_NEG	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x5C	LAST_BITE_RATE2_POS	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x5D	LAST_BITE_RATE2_NEG	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x5E	not used	-	-
0x5F	not used	-	-
0x60	not used	-	-
0x61	not used	-	-
0x62	not used	-	-
0x63	not used	-	-
0x64	LAST_BITE_ACC1_DEVIATION	r-only	BITE evaluation signal Signed 16 bit value
0x65	LAST_BITE_ACC2_DEVIATION	r-only	BITE evaluation signal Signed 16 bit value
0x66	LAST_BITE_QUAD1_DEVIATION	r-only	BITE evaluation signal Signed 16 bit value
0x67	LAST_BITE_RATE1_DEVIATION	r-only	BITE evaluation signal Signed 16 bit value
0x68	LAST_BITE_ACC3_DEVIATION	r-only	BITE evaluation signal Signed 16 bit value (SMI860 only)
0x69	LAST_BITE_QUAD2_DEVIATION	r-only	BITE evaluation signal Signed 16 bit value (SMI860 only)
0x6A	LAST_BITE_RATE2_DEVIATION	r-only	BITE evaluation signal Signed 16 bit value (SMI860 only)
0x6B	not used	-	-
0x6C	not used	-	-
0x6D	BITE repetition counter RATE	r-only	Bit(11..8) =- Bit(7..4) =Rate2 Bit(3..0) =Rate1
0x6E	BITE repetition counter ACC	r-only	Bit(11..8) =Acc3 Bit(7..4) =Acc2 Bit(3..0) =Acc1
0x6F	not used		

* BIT definition in chapter 7.2 traceability

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6.4.1.4 Error Handling SMI8-32OUT

Error	Reaction
CRCA MOSI is incorrect	high impedance of MISO (next frame)
CPOL error	high impedance of MISO (next frame)
CPHA error	MISO answer 0x0, detected by wrong CRC in MISO
SCK cycles not equal to 32	high impedance of MISO (next frame)
CAP Wrong (CAP is not equal to: 011b, 010b,101b)	CE bit set
BADR wrong (The addressed sensor is not connected to this chip select line OR sensor channel address is not valid)	high impedance of MISO (next frame)
PG wrong (not possible, all pages do exist)	n.a.
A wrong (not possible, all addresses do exist)	n.a.
Write command to a read only register	CE bit set
Read/Write command to an unused register	CE bit set
Time error (internal-bus-access not finished between 2 SPI-frames)	CE bit set
Bus error - write (internal Bus error. Write access on the internal bus failed, parity error on internal bus)	CE bit set
Bus error - read (internal Bus error. Read access on the internal bus failed, parity error on internal bus)	CE bit set
Error counter value above LIMIT	CS bit set

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6.4.2 SPI dialect SMI8-32IN

The frame is an 'in-frame' protocol with 32 clock cycles. In-frame means that the logical response to a request is in the same frame. All internal registers can be accessed using an offset-address concept.

6.4.2.1 Sensor data commands

If the bus-address is not a sensor module address (XX000b or XX001b), the sensor interprets the command as sensor channel command. The addressed channel will respond to the command. Capture bits are interpreted from all modules on a chip select line.

MOSI frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
BADR (4..0)					CAP (2..0)			*	*	*	*	*	*	*	*	*	...	*	*	CRC*			*	*
1/0					1/0			*	0	0	0	0	0	*						1/0			*	

Field	Description
BADR (4..0)	Bus Address
	5 bit combined sensor and channel address XX001b: valid module-address, one module will react XX000b: broadcast-address : all modules will react If BADR(4..0) is a broadcast address the command will be interpreted as module command
CAP (2..0)	Capture mode
	Bits to define if captured or current data should be read and if data should be captured: 011b: read current data and channel-status (do not alter captured data) 010b: read captured data and channel status (do not capture or alter captured data) 101b: sensor channels of any module on the bus must capture data and channel status of all channels. The channel which is addressed with BADR feedbacks captured data of selected channel as response to capture command. else: reserved (illegal command)
CRC	3bit CRC
	Polynom: x^3+x+1, target value 000b. CRC over bits 31 to 5, start value: 111b (SPI32 in-frame)

MISO frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
TRI (4..0)					OE	SD	SID (4..0)					Data (15..0)									CS	CRC/TF		
X					1/0	1	1/0					1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0		

Field	Description
TRI (4..0)	Tristate
	Sensor output is tri-state (high impedance, high resistance)
OE	Of frame-Error
	(Please note: OE will be transmitted in next frame, only visible in next frame) 1: Last write bus access on internal bus not successful or sclk-cycles not equal 32 0: indicates status 'o.k.' Note: If the next frame after a write command is sensor data command the information of the write status will be lost. It will only be visible in an immediately following non-sensor command.
SD	Sensor Data (Frame Select)
	Select Sensor channel data or module data frame. 0: module data 1: sensor data
SID (4..0)	Safety ID
	Channel ID for a specific channel (rate, acceleration A, acceleration B, HF and LF output channel). While BADR is fixed, SID is programmable.
DATA (15..0)	Data
	Two's complement sensor data of selected channel
CS	Channel Status

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Field	Description
	0: channel sensor data fully valid 1: channel sensor data not valid (sensor error, initialization, or self-test) if captured data is read, then the CS-bit is the captured CS OR the actual CS Please note: CS and OE Bit are not correlated, i.e. customer needs to evaluate both bits on system level independently Not used for “cluster flags” command (always 0)
CRC/TF	CRC/Transfer Failure Flag (in frame only)
	Polynom: x^3+x+1, target value 000b. CRC/TF over bits 26 to 3, start value: 111b (SPI32 in-frame) If CRC of request (MOSI) was wrong or command is unknown or a read access on the APB bus failed a transfer failure will be signaled by destroying the CRC of the response (MISO): the last bit of the calculated CRC will be inverted.

Examples of inframe sensor data commands

The following table shows the SPI commands in hex format that can be sent out (on MOSI line) by the master in order to read data from the sensor.

Command	SMI800 ID0	SMI800 ID1	SMI810 ID0	SMI810 ID1	SMG810 ID0	SMG810 ID1	SMI860 ID0	SMI860 ID1
YRS1	13000000 ωZ	53000004 ωZ	93000008 ωX	D300000C ωX	93000008 ωX	D300000C ωX	13000000 ωX	53000004 ωX
YRS2	-	-	-	-	-	-	93000008 ωZ	D300000C ωZ
ACC1 LF	23000008 aY	6300000C aY	A3000000 aY	E3000004 aY	-	-	23000008 aY	6300000C aY
ACC1 HF	2B000010 aY	6B000014 aY	AB000018 aY	EB00001C aY	-	-	2B000010 aY	6B000014 aY
ACC2 LF	33000014 aX	73000010 aX	B300001C aZ	F3000018 aZ	-	-	33000014 aX	73000010 aX
ACC2 HF	3B00000C aX	7B000008 aX	BB000004 aZ	FB000000 aZ	-	-	3B00000C aX	7B000008 aX
ACC3 LF	-	-	-	-	-	-	B300001C aZ	F3000018 aZ
ACC3 HF	-	-	-	-	-	-	BB000004 aZ	FB000000 aZ
Cluster flags	1B000018	5B00001C	9B000010	DB000014	9B000010	DB000014	1B000018	5B00001C
Trigger capture & Read YRS1	1500001C ωZ	55000018 ωZ	95000014 ωX	D5000010 ωX	95000014 ωX	D5000010 ωX	1500001C ωX	55000018 ωX
captured YRS1	12000008 ωZ	5200000C ωZ	92000000 ωX	D2000004 ωX	92000000 ωX	D2000004 ωX	12000008 ωX	5200000C ωX
captured YRS2	-	-	-	-	-	-	92000000 ωZ	D2000004 ωZ
captured ACC1 LF	22000000 aY	62000004 aY	A2000008 aY	E200000C aY	-	-	22000000 aY	62000004 aY
captured ACC1 HF	2A000018 aY	6A00001C aY	AA000010 aY	EA000014 aY	-	-	2A000018 aY	6A00001C aY
captured ACC2 LF	3200001C aX	72000018 aX	B2000014 aZ	F2000010 aZ	-	-	3200001C aX	72000018 aX
captured ACC2 HF	3A000004 aX	7A000000 aX	BA00000C aZ	FA000008 aZ	-	-	3A000004 aX	7A000000 aX
Captured ACC3 LF	-	-	-	-	-	-	B2000014 aZ	F2000010 aZ
captured ACC3 HF	-	-	-	-	-	-	BA00000C aZ	FA000008 aZ

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6.4.2.2 Module Commands

MOSI frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
BADR (4..0)					ADR (3..0)				W	*	W-Data(15..0)									CRC			-	-
1/0					1/0				1/0	0	1/0									1/0			*	

Field	Description
BADR (4..0)	Bus Address
	5 bit combined sensor and channel address XX001b: valid module-address, one module will react XX000b: broadcast-address : all modules will react If BADR(4..0) is a broadcast address the command will be interpreted as module command
ADR (3..0):	Address
	Address of data to be read or to be written
W	Write access
	If: W=0 and bit 20=1: bits 5/6/7 of SPI word is being interpreted for Page Offset Address handling. Bits 8-16 must be set to 0. W=1: write W-DATA(bits 5 to 20) to sensor register ADR(3:0) W=0 and bit 20=0: read data from address ADR(3:0). Bits 5-19 are ignored. Writing to a read only register gives a transfer failure
W-DATA (15..0)	Write Data
	Data to be written to the sensor if W=1
CRC	3bit CRC
	Polynom: x^3+x+1, target value 000b. CRC over bits 31 to 5, start value: 111b (SPI32 in-frame)

MISO frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
TRI (4..0)					OE	SD	MID (2..0)			PG (2..0)			R-Data (15..0)										CRC/TF	
X					1/0	0	1/0			1/0			1/0										1/0	

Field	Description
TRI (4..0)	Tristate
	Sensor output is tri-state (high impedance, high resistance)
OE	Of frame-Error
	(Please note: OE will be transmitted in next frame, only visible in next frame) 1: Last write bus access on internal bus not successful or sclk-cycles not equal 32 0: indicates status 'o.k.' Note: If the next frame after a write command is sensor data command the information of the write status will be lost. It will only be visible in an immediately following non-sensor command.
SD	Sensor Data (Frame Select)
	Selects Sensor channel data or module data frame. 0: module data 1: sensor data
MID (2..0)	Module ID
	Identifies, which module responded MID(2..1) = BADR(4:3) MID(0) = BADR(0) 1: reaction on individual module command 0: reaction on broadcast command (broadcast commands are often used during final measurement in order to simplify the communication)
PG (2..0)	Page

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Field	Description
	Identifies page number (Offset) from which data is read or written to OFFS = 0x000 corresponds to Page0 OFFS = 0x001 corresponds to Page1 ... OFFS = 0x007 or higher corresponds to Page7
R_DATA (15..0)	Read Data
	Data read from sensor: Answers to module command 'WRITE' contain the value of the register before writing in the 'R-DATA'-field
CRC/TF	CRC/Transfer Failure Flag
	Polynom: x^3+x+1, target value 000b. CRC/TF over bits 26 to 3, start value: 111b (SPI32 in-frame) If CRC of request (MOSI) was wrong or command is unknown or a read access on the APB bus failed a transfer failure will be signaled by destroying the CRC of the response (MISO): the last bit of the calculated CRC will be inverted

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Examples of inframe module commands

The following table shows the SPI commands in hex format that can be sent out (on MOSI line) by the master in order to read register data from the sensor

Command	Valid on page	SMI800 ID0	SMI800 ID1	SMI810 ID0	SMI810 ID1	SMG810 ID0	SMG810 ID1	SMI860 ID0	SMI860 ID1
Change to page 0	All	08100004	48100000	8810000C	C8100008	8810000C	C8100008	08100004	48100000
Write EOC bit	0	0D400020	4D400024	8D400028	CD40002C	8D400028	CD40002C	0D400020	4D400024
Read SPI counter	0	0D80001C	4D800018	8D800014	CD800010	8D800014	CD800010	0D80001C	4D800018
Read Reset detection flag	0	0F000008	4F00000C	8F000000	CF000004	8F000000	CF000004	0F000008	4F00000C
Change to page 1	All	08100028	4810002C	88100020	C8100024	88100020	C8100024	08100028	4810002C
Read State of Offset Controller	1	09000014	49000010	8900001C	C9000018	8900001C	C9000018	09000014	49000010
Write 0xB26C to reset sensor	1	0D564D80	4D564D84	8D564D88	CD564D8C	8D564D88	CD564D8C	0D564D80	4D564D84
Change to page 2	All	0810005C	48100058	88100054	C8100050	88100054	C8100050	0810005C	48100058
Read temperature signal	2	0800001C	48000018	88000014	C8000010	88000014	C8000010	0800001C	48000018
Read error flag bank 0	2	08800018	4880001C	88800010	C8800014	88800010	C8800014	08800018	4880001C
Read error flag bank 1	2	09000014	49000010	8900001C	C9000018	8900001C	C9000018	09000014	49000010
Read error flag bank 2	2	09800010	49800014	89800018	C980001C	89800018	C980001C	09800010	49800014
Read error flag bank 3	2	0A00000C	4A000008	8A000004	CA000000	8A000004	CA000000	0A00000C	4A000008
Read error flag bank 4	2	0A800008	4A80000C	8A800000	CA800004	8A800000	CA800004	0A800008	4A80000C
Read error flag bank 5	2	0B000004	4B000000	8B00000C	CB000008	8B00000C	CB000008	0B000004	4B000000
Read error flag bank 6	2	0B800000	4B800004	8B800008	CB80000C	8B800008	CB80000C	0B800000	4B800004
Read error flag bank 7	2	0C000010	4C000014	8C000018	CC00001C	8C000018	CC00001C	0C000010	4C000014
Read error flag bank 8	2	0C800014	4C800010	8C80001C	CC800018	8C80001C	CC800018	0C800014	4C800010
Read error flag bank 9	2	0D000018	4D00001C	8D000010	CD000014	8D000010	CD000014	0D000018	4D00001C
Read err_cnt_comb_0	2	0D80001C	4D800018	8D800014	CD800010	8D800014	CD800010	0D80001C	4D800018
Read err_cnt_comb_1	2	0E000000	4E000004	8E000008	CE00000C	8E000008	CE00000C	0E000000	4E000004
Read err_cnt_comb_2	2	0E800004	4E800000	8E80000C	CE800008	8E80000C	CE800008	0E800004	4E800000
Read err_cnt_comb_3	2	0F000008	4F00000C	8F000000	CF000004	8F000000	CF000004	0F000008	4F00000C
Read error_group_out	2	0F80000C	4F800008	8F800004	CF800000	8F800004	CF800000	0F80000C	4F800008
Change to page 4	All	08100098	4810009C	88100090	C8100094	88100090	C8100094	08100098	4810009C
Read ASIC_SERIAL_NR_0	4	0800001C	48000018	88000014	C8000010	88000014	C8000010	0800001C	48000018
Read ASIC_SERIAL_NR_1	4	08800018	4880001C	88800010	C8800014	88800010	C8800014	08800018	4880001C
Read ASIC_SERIAL_NR_2	4	09000014	49000010	8900001C	C9000018	8900001C	C9000018	09000014	49000010
Read ASIC_NAME	4	09800010	49800014	89800018	C980001C	89800018	C980001C	09800010	49800014
Read SMI_SERIAL_NR_0	4	0A800008	4A80000C	8A800000	CA800004	8A800000	CA800004	0A800008	4A80000C
Read SMI_SERIAL_NR_1	4	0B000004	4B000000	8B00000C	CB000008	8B00000C	CB000008	0B000004	4B000000

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Command	Valid on page	SMI800 ID0	SMI800 ID1	SMI810 ID0	SMI810 ID1	SMG810 ID0	SMG810 ID1	SMI860 ID0	SMI860 ID1
Read SMI_SERIAL_NR_2	4	0B800000	4B800004	8B800008	CB80000C	8B800008	CB80000C	0B800000	4B800004
Read CUSTOMER_SERIAL_NR	4	0C000010	4C000014	8C000018	CC00001C	8C000018	CC00001C	0C000010	4C000014

6.4.2.3 Register addressing

The SMI8-32IN protocol uses a paging mechanism in order to access internal registers. Each page contains 16 registers. Each register has 16 bit data. For accessing the registers, the module command frame is used:

MOSI frameset

31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	...	6	5	4	3	2	1	0
BADR (4..0)					ADR (3..0)				W	*	W-Data(15..0)									CRC			-	-
1/0					1/0				1/0	0	1/0									1/0			*	

The address field (ADR) defines the register address to be used. To access a certain register, it must be ensured that the correct page was selected before accessing the registers.

To change the page set the bit 22 (W) to 0 and set the bit 20 to 1. The bits 5,6,7 of the MOSI frame contain the target page to change to.
When sending the “change to page” command, the MISO response from the senor will contain the data from the current page. Afterwards the target page will be selected

A new page will be valid from the subsequent frame to the switching command.

After sensor startup the default page is 0.

The following table describes the accessible registers. Please note:

Not used. stands for ‘not allowed’. A write attempt to a locked register cannot be indicated by the sensor. Write access to n.a. register must be avoided.

- means ‘content not defined’.

PG Page

ADR Address within page

Page 0

PG	ADR	Signal	Access	Function
0x0	0x0	CONF_IREG0	r/w	SMI8xy micro controller service routines. Used to trigger self test or soft configuration.
0x0	0x1	CONF_IREG1	r/w	SMI8xy micro controller service routines. Used to trigger self test or soft configuration.
0x0	0x2	CONF_IREG2	r/w	SMI8xy micro controller service routines. Used to trigger self test or soft configuration.
0x0	0x3	CONF_IREG3	r/w	SMI8xy micro controller service routines. Used to trigger self test or soft configuration.
0x0	0x4	CONF_OREG0	r-only	SMI8xy micro controller service routines.
0x0	0x5	CONF_OREG1	r-only	SMI8xy micro controller service routines.
0x0	0x6	CONF_OREG2	r-only	SMI8xy micro controller service routines.
0x0	0x7	CONF_OREG3	r-only	SMI8xy micro controller service routines.
0x0	0x8	not used	-	-
0x0	0x9	not used	-	-
0x0	0xA	EOC	r/w	Writing "1" to EOC indicates End of Configuration at startup
0x0	0xB	SPI Counter	r-only	Free running counter on PLL frequency / 4

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PG	ADR	Signal	Access	Function
0x0	0xC	not used	-	-
0x0	0xD	not used	-	-
0x0	0xE	Reset Detection Flag	r-only	"1" at startup and clear-on-read property, read-only
0x0	0xF	not used	-	-

Page 1

PG	ADR	Signal	Access	Function
0x1	0x0	QUAD2_FINE_DAC	-	SMI860 only. Quadrature controller output. Signed 16 bit number, two's complement
0x1	0x1	not used	-	-
0x1	0x2	Status of Offset Controller	r-only	Max. 6x2 Bits for SMI860
0x1	0x3	not used	-	-
0x1	0x4	not used	-	-
0x1	0x5	QUAD1_FINE_DAC	r-only	SMI860 only. Quadrature controller output. Signed 16 bit number, two's complement
0x1	0x6	not used	-	-
0x1	0x7	not used	-	-
0x1	0x8	not used	-	-
0x1	0x9	not used	-	-
0x1	0xA	MAIN_SOFT_RESET	r/w	Same password (0xB26C) as in SMI7 for downwards compatibility
0x1	0xB	not used	-	-
0x1	0xC	not used	-	-
0x1	0xD	not used	-	-
0x1	0xE	not used	-	-
0x1	0xF	not used	-	-

Page 2

PG	ADR	Signal	Access	Function
0x2	0x0	TEMP1	r-only	Temperature Sensor 1 (Signed 16 Bit value)
0x2	0x1	error_flag_16_bank0	r-only	see flag list
0x2	0x2	error_flag_16_bank1	r-only	see flag list
0x2	0x3	error_flag_16_bank2	r-only	see flag list
0x2	0x4	error_flag_16_bank3	r-only	see flag list
0x2	0x5	error_flag_16_bank4	r-only	see flag list
0x2	0x6	error_flag_16_bank5	r-only	see flag list
0x2	0x7	error_flag_16_bank6	r-only	see flag list
0x2	0x8	error_flag_16_bank7	r-only	see flag list
0x2	0x9	error_flag_16_bank8	r-only	see flag list
0x2	0xA	error_flag_16_bank9	r-only	see flag list
0x2	0xB	err_cnt_comb_0	r-only	Bit[15..8] =Acc1 LF Bit[7..0] =Acc1 HF
0x2	0xC	err_cnt_comb_1	r-only	Bit[15..8] =Acc2 LF Bit[7..0] =Acc2 HF
0x2	0xD	err_cnt_comb_2	r-only	Bit[15..8] =Rate1 LF Bit[7..0] =Rate2 LF (SMI860 only)
0x2	0xE	err_cnt_comb_3	r-only	Bit[15..8] =Acc3 LF (SMI860 only) Bit[7..0] =Acc3 HF (SMI860 only)
0x2	0xF	error_group_out	r-only	16 Bit Cluster Flags

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Page 3

Not used.

Page 4

PG	ADR	Signal	Access	Function
0x4	0x0	ASIC_SERIAL_NR_0	r-only	Unsigned 16 bit number (LSB)*
0x4	0x1	ASIC_SERIAL_NR_1	r-only	Unsigned 16 bit number (LSB)*
0x4	0x2	ASIC_SERIAL_NR_2	r-only	Unsigned 16 bit number (LSB)*
0x4	0x3	ASIC_NAME	r-only	Unsigned 16 bit number (LSB)
0x4	0x4	not used	-	-
0x4	0x5	SMI_SERIAL_NR_0	r-only	Unsigned 16 bit number (LSB)*
0x4	0x6	SMI_SERIAL_NR_1	r-only	Unsigned 16 bit number (LSB)*
0x4	0x7	SMI_SERIAL_NR_2	r-only	Unsigned 16 bit number (LSB)*
0x4	0x8	Configuration number	r-only	Unsigned 16 bit number (LSB)*
0x4	0x9	not used	-	-
0x4	0xA	SIDs	r-only	Bit[14..10] =Clusterflag Bit[9..5] =Acc2-HF Bit[4..0] =Acc1-HF
0x4	0xB	SIDs	r-only	Bit[14..10] =Rate1-LF Bit[9..5] =Acc2-LF Bit[4..0] =Acc1-LF
0x4	0xC	SIDs	r-only	Bit[14..10] =Rate2-LF Bit[9..5] =Acc3-HF Bit[4..0] =Acc3-LF
0x4	0xD	not used	-	-
0x4	0xE	not used	-	-
0x4	0xF	not used	-	-

* BIT definition in chapter 7.2 traceability

Page 5

PG	ADR	Signal	Access	Function
0x5	0x0	LAST_BITE_ACC1_POS	r-only	Result of last BITE Signed 16 bit value
0x5	0x1	LAST_BITE_ACC1_NEG	r-only	Result of last BITE Signed 16 bit value
0x5	0x2	LAST_BITE_ACC2_POS	r-only	Result of last BITE Signed 16 bit value
0x5	0x3	LAST_BITE_ACC2_NEG	r-only	Result of last BITE Signed 16 bit value
0x5	0x4	LAST_BITE_ACC3_POS	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x5	0x5	LAST_BITE_ACC3_NEG	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x5	0x6	LAST_BITE_QUAD1_POS	r-only	Result of last BITE Signed 16 bit value
0x5	0x7	LAST_BITE_QUAD1_NEG	r-only	Result of last BITE Signed 16 bit value
0x5	0x8	LAST_BITE_RATE1_POS	r-only	Result of last BITE Signed 16 bit value
0x5	0x9	LAST_BITE_RATE1_NEG	r-only	Result of last BITE Signed 16 bit value
0x5	0xA	LAST_BITE_QUAD2_POS	r-only	Result of last BITE SMI860 only Signed 16 bit value

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PG	ADR	Signal	Access	Function
0x5	0xB	LAST_BITE_QUAD2_NEG	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x5	0xC	LAST_BITE_RATE2_POS	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x5	0xD	LAST_BITE_RATE2_NEG	r-only	Result of last BITE SMI860 only Signed 16 bit value
0x5	0xE	not used	-	-
0x5	0xF	not used	-	-

Page 6

PG	ADR	Signal	Access	Function
0x6	0x0	not used	-	-
0x6	0x1	not used	-	-
0x6	0x2	not used	-	-
0x6	0x3	not used	-	-
0x6	0x4	LAST_BITE_ACC1_DEVIATION	r-only	BITE evaluation signal
0x6	0x5	LAST_BITE_ACC2_DEVIATION	r-only	BITE evaluation signal
0x6	0x6	LAST_BITE_QUAD1_DEVIATION	r-only	BITE evaluation signal
0x6	0x7	LAST_BITE_RATE1_DEVIATION	r-only	BITE evaluation signal
0x6	0x8	LAST_BITE_ACC3_DEVIATION	r-only	BITE evaluation signal (SMI860 only)
0x6	0x9	LAST_BITE_QUAD2_DEVIATION	r-only	BITE evaluation signal, written by FW (SMI860 only)
0x6	0xA	LAST_BITE_RATE2_DEVIATION	r-only	BITE evaluation signal, written by FW (SMI860 only)
0x6	0xB	not used	-	-
0x6	0xC	not used	-	-
0x6	0xD	BITE repetition counter RATE	r-only	Bit(11..8) =- Bit(7..4) =Rate2 Bit(3..0) =Rate1
0x6	0xE	BITE repetition counter ACC	r-only	Bit(11..8) =Acc3 Bit(7..4) =Acc2 Bit(3..0) =Acc1
0x6	0xF	not used		

* BIT definition in chapter 7.2 traceability

6.4.2.4 Error Handling SMI8-32IN

Error	Reaction
CRC MOSI is incorrect	TF Bit set, i.e. last bit of CRC inverted (within same frame)
CPOL error	high impedance of MISO (next frame)
CPHA error	wrong CRC in MISO
SCK cycles not equal to 32	OE error (in next frame)
CAP Wrong (CAP is not equal to: 011b, 010b,101b)	TF Bit set i.e. last bit of CRC inverted (within same frame)
BADR wrong (The addressed sensor is not connected to this chip select line OR sensor channel address is not valid)	high impedance of MISO (next frame)
PG wrong (not possible, all pages do exist)	n.a.
ADR wrong (not possible, all addresses do exist)	n.a.
Write command to a read only register	OE bit set (in the next frame)
Read/Write command to an unused register	Wrong CRC
Time error (internal-bus-access not finished between 2 SPI-frames)	not applicable for in frame communication (note: this is also true for page change, since page is returned in answer)

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Error	Reaction
Bus error - write (internal Bus error. Write access on the internal bus failed, parity error on internal bus)	OE bit set (in the next frame)
Bus error - read (internal Bus error. Read access on the internal bus failed, parity error on internal bus)	TF Bit set, i.e. last bit of CRC inverted (within same frame)
Error counter value above LIMIT	CS bit set

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7 Application Details

7.1 Service functions

Service functions can be clustered into following two main functions and can executed using the CONF_IREGx and CONF_OREGx registers (page 0x0):

Routine A Soft configuration of the sensor module
Routine B Controlling the BITE, Fast Offset compensation, ACC-Sum-C Sum and Watchdog routine

The functionality 'Soft configuration' is available as soon as the SPI interface is available. Soft configuration is locked after the end of configuration (EOC) is set to 1, i.e. EOC=1 is written to register address (A: 0x0A). After EOC, various functions like BITE, Fast Offset compensation, ACC-Sum-C and Watchdog service function are still available.

In input registers CONF_IREG1 - CONF_IREG3 the parameters of the configuration service which are to be executed are defined. Once these parameters are defined/ written in the respective registers, the execution of configuration service is done by finally writing in CONF_IREG0. The structure of the input registers depends on the configuration service, which is to be called.

Please note that in the SMI8-32IN protocol, the correct page must be selected before addressing the register (PG and ADR). SMI8-32OUT offers direct access to the full register address (A).

Application Note:

- A minimum delay of 500µs after a write access to CONF_IREG0 is required. Otherwise, due to an interrupt, which will be triggered immediately after writing into CONF_IREG0, the internal µC of the sensor might be overloaded. This may result in the error flag *uc_watchdog_err*.
- When using soft configuration it is important to write all CONF_IREG1 - CONF_IREG3 registers before executing the configuration service as these registers might still contain previous data and hence lead to an unintended programming of registers.

General structure of the input registers CONF_IREGx (16-bit data field of MOSI frame):

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved							SERVICE_ID					0x3		0x0	0x0
CONF_IREG1	0x0	0x1	0x01	*depends*															
CONF_IREG2	0x0	0x2	0x02	*depends*															
CONF_IREG3	0x0	0x3	0x03	*depends*															

Field	Value	Description
SERVICE_ID	0x4	FOC trigger
	0x5	ACC Sum-C trigger
	0xC	Soft configuration
	0xD	Manual BITE trigger
	0xE	Watchdog for external SPI Master

Status of execution of configuration service is available in CONF_OREG0. It is also important to verify the programming of configuration service. This can be done reading out CONF_OREG1-CON_OREG3, which should contain the same data and format as programed in CONG_IREG1-CONF_IREG3.

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General structure of CONF_OREGx (16-bit read data field of MISO frame):

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0
CONF_OREG1	0x0	0x5	0x05	*depends*															
CONF_OREG2	0x0	0x6	0x06	*depends*															
CONF_OREG3	0x0	0x7	0x07	*depends*															

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0x4	FOC trigger
	0x5	ACC Sum-C trigger
	0xC	Soft configuration
	0xD	Manual BITE trigger
	0xE	Watchdog for external SPI Master
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07 to 0x1E	Service Specific failure
	0x1F	Hard Fault

The soft configuration routine contains the following steps:

When using SMI8-32IN, select page **PG 0x0**

Step 1: Write data to CONFIG_**IREG1-3**

Step 2: Start configuration with CONFIG_**IREG0**

Step 3: Read CONFIG_**OREG0** and verify status
Read data written to sensor module in CONFIG_**OREG1-3**

Repeat steps 1-3 for additional parameters (Par ID).

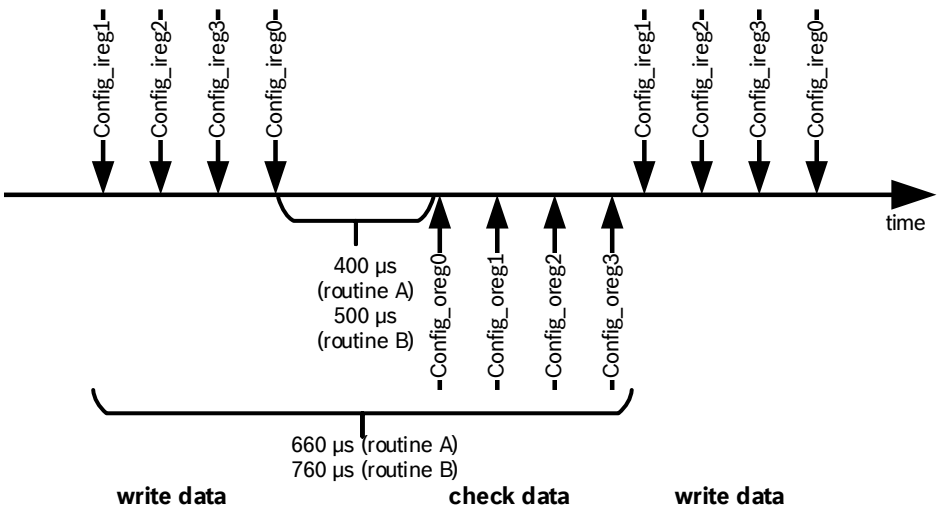

Figure 20 Configuration timing diagram

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Parameter / Condition	Min	Typ	Max	Unit
Time between writing and reading back service **routine A** (Soft configuration of the sensor module)	400	-	-	µs
Time between writing and reading back service **routine B** (controlling the BITE,FOC, ACC-Sum-C Sum and Watchdog routine)	500		-	µs
Typical time for soft configuration during start up Assuming 14 SPI commands @ 1kHz SPI frame rate. Time for soft configuration calculated between start of programming until data are written to ASIC registers.			15	ms

7.1.1 Sensor Module Soft Configuration

The soft configuration is only available if the sensor is configured by Bosch to Mode “B” described in chapter 2.3. The soft configuration is possible only after a power on/reset. Once the soft configuration is completed by writing the “end of configuration” bit, it is no longer possible to configure the sensor until the next reset or power off/on. Soft configuration of the sensor is used to select the following sensor parameters (Par ID 0 - 9) at each startup of the sensor:

CONFIG_IREG1 is always required and contains the Par ID to select the parameter to be configured.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*Depends on Par.ID*												Par. ID			

Par ID	Parameter
0x0	Configuration of Safety IDs (SID)
0x1	Extended configuration of Safety IDs (SID)
0x2	Selection of LF filter and configuration of BITE flush time
0x3	Sign inversion and offset compensation mode individually for each channel
0x4	Configuration of error counters
0x5	Extended configuration of error counters
0x6	Configuration of VB monitor upper limit
0x8	Maximum number of BITE counts
0x9	Configuration of ACC-Sum-C test

7.1.1.1 Configuration of SID (Par ID 0x0)

Step 1: define the SID per channel by CONF_IREG1-3

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*res.*	SID ACC1 LF					SID YR1 LF					*res.*	Par. ID = 0x0			
CONF_IREG2	0x0	0x2	0x02	*res.*	SID ACC2 HF					SID ACC1 HF					SID ACC2 LF				
CONF_IREG3	0x0	0x3	0x03	*res.*	*reserved*					SID YR2 LF*					SID Cluster Flags				

Fields of CONF_IREG1-3

Field	Description
SID ACC1 LF	See SPI description Out of Frame 6.4.1.1 In frame 6.4.2.1
SID YR1 LF	See SPI description Out of Frame 6.4.1.1 In frame 6.4.2.1
PAR_ID	Parameter ID, 0x0
SID ACC2 HF	See SPI description Out of Frame 6.4.1.1 In frame 6.4.2.1
SID ACC1 HF	See SPI description Out of Frame 6.4.1.1 In frame 6.4.2.1
SID ACC2 LF	See SPI description Out of Frame 6.4.1.1 In frame 6.4.2.1
SID YR2 LF (available in SMI860 only)	See SPI description Out of Frame 6.4.1.1 In frame 6.4.2.1
SID Cluster Flags	See SPI description Out of Frame 6.4.1.1 In frame 6.4.2.1
reserved	Write 0x0

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Step 2: Trigger configuration service

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved							0xC					0x3		0x0	0x0

Step 3: Check correct configuration by reading and verifying the contents of CONF_OREG0-3.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	*res.*	SID ACC1 LF						SID YR1 LF				*res.*	Par. ID = 0x0			
CONF_OREG2	0x0	0x6	0x06	*res.*	SID ACC2 HF						SID ACC1 HF				SID ACC2 LF				
CONF_OREG3	0x0	0x7	0x07	*res.*	*reserved*						SID YR2 LF*				SID Cluster Flags				

CONF_**OREG1** - CONF_**OREG3** contains the data, which has been read back from the sensor module after writing in CONF_**IREG1** - CONF_**IREG3** registers.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xC	Soft configuration
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07	Invalid parameter ID
	0x08	Service is not allowed after EOC
	0x1F	Hard Fault

7.1.1.2 Extended configuration of SID for SMI860 only (Par ID 0x1)

Step 1: define the SID per channel

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*res.*	SID ACC3 HF*						SID ACC3 LF*				*res.*	Par. ID = 0x1*			
CONF_IREG2	0x0	0x2	0x02	*reserved*															
CONF_IREG3	0x0	0x3	0x03	*reserved*															

Fields of CONF_IREG1-3

Field	Description
SID ACC3 HF (available in SMI860 only)	See SPI description
SID ACC3 LF (available in SMI860 only)	See SPI description
PAR_ID	Parameter ID, 0x1
reserved	Write 0x0

Step 2: Trigger configuration service

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved							0xC					0x3		0x0	0x0

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Step 3: Check correct configuration by reading and verifying the contents of CONF_OREG0-3

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	*res.*	SID ACC3 HF*					SID ACC3 LF*					*res.*	Par. ID = 0x1*			
CONF_OREG2	0x0	0x6	0x06	*reserved*															
CONF_OREG3	0x0	0x7	0x07	*reserved*															

CONF_**OREG1** - CONF_**OREG3** contains the data, which has been read back from the sensor module after writing in CONF_**IREG1** - CONF_**IREG3** registers.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xC	Soft configuration
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07	Invalid parameter ID
	0x08	Service is not allowed after EOC
	0x1F	Hard Fault

7.1.1.3 Configure filter type and filter flush time (Par ID 0x2)

Step 1: Select LF Filter type by CONF_IREG1-3.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*reserved*										LF filt.		Par. ID = 0x2			
CONF_IREG2	0x0	0x2	0x02	Flushtime for LF channels in ms*								Err. Cnt. Hold time for LF channels in ms*							
CONF_IREG3	0x0	0x3	0x03	*reserved*															

*the minimum value for the filter flush time and the hold time is 1ms. For the cases Err. Cnt Hold time = 0 or Flushtime = 0, the default value is used. It is recommended to use the default values or higher values for the filter flush time. For setting the flushtime and hold time, please consider the specific flush time of the selected LF filter in chapter 5.3.2.

Fields of CONF_IREG1-3

Field	Description
LF filt.	LF filter type
Flushtime for LF channels in ms	Flushtime for LF channels in ms
Err. Cnt. Hold time for LF channels in ms	Error Counter Hold time for LF channels in ms
reserved	Write 0x0

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Filter settings

LF filter type	Description
00b	Low pass filter Typ1 (80Hz)
01b	Low pass filter Typ2 (20Hz)
10b	Low pass filter Typ3 (10Hz)
11b	Not used

In any case, also in case of input value = 0 (default Value), the **read back** values for LF flush times and Error Counter hold times can be read out with CONF_OREG2.

Step 2: Trigger configuration service

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved							0xC					0x3		0x0	0x0

Step 3: Check correct configuration by reading and verifying the contents of CONF_OREG0-3

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	*reserved*										LF filt.		Par. ID = 0x2			
CONF_OREG2	0x0	0x6	0x06	Flushtime for LF channels in ms*								Err. Cnt. Hold time for LF channels in ms*							
CONF_OREG3	0x0	0x7	0x07	*reserved*															

CONF_**OREG1** - CONF_**OREG3** contains the data, which has been read back from the sensor module after writing in CONF_**IREG1** - CONF_**IREG3** registers.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xC	Soft configuration
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07	Invalid parameter ID
	0x08	Service is not allowed after EOC
	0x09	Discrepancy between written and read values
	0x1F	Hard Fault

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7.1.1.4 Configuration of sign inversion and offset compensation (Par ID 0x3)

Step 1: Select channels for offset compensation by CONF_IREG1-3.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	R1 OC		R1 Inv.	A3 OC*		A3 Inv.*	A2 OC		A2 Inv.	A1 OC		A1 Inv.	Par ID = 0x3			
CONF_IREG2	0x0	0x2	0x02	*reserved*									*R2 OC**		*R2** Inv.	*reserved*			
CONF_IREG3	0x0	0x3	0x03	*reserved*															

* available in SMI860 only

Fields of CONF_IREG1-3

Field	Description
R1 OC	Rate 1 offset compensation
R1 Inv.	Rate 1 Sign inversion
A3 OC*	ACC 3 offset compensation
A3 Inv.*	ACC 3 Sign inversion
A2 OC	ACC 2 offset compensation
A2 Inv.	ACC 2 Sign inversion
A1 OC	ACC 1 offset compensation
A1 Inv.	ACC 1 Sign inversion
R2 OC*	Rate 2 offset compensation
R2 Inv.*	Rate 2 Sign inversion
reserved	Write 0x0

* available in SMI860 only

Offset compensation values **OC Selection**	Description
00b	deactivated
01b	deactivated
10b	FOC/SOC (fast offset/slow offset compensation) activated
11b	FOC/single pole high pass filter (HPF) activated

Offset compensation setting is only effective if the BITE was passed before. In case of a BITE fail, no offset compensation is active.

Step 2: Trigger configuration service

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved							0xC					0x3		0x0	0x0

Step 3: Check correct configuration by reading and verifying the contents of CONF_OREG0-3

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	R1 OC		R1 Inv.	A3 OC*		A3 Inv.*	A2 OC		A2 Inv.	A1 OC		A1 Inv.	Par ID = 0x3			
CONF_OREG2	0x0	0x6	0x06	*reserved*									*R2 OC**		*R2** Inv.	*reserved*			
CONF_OREG3	0x0	0x7	0x07	*reserved*															

CONF_**OREG1** - CONF_**OREG3** contains the data, which has been read back from the sensor module after writing in CONF_**IREG1** - CONF_**IREG3** registers.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

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Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xC	Soft configuration
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
ERROR_CODE	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07	Invalid parameter ID
	0x08	Service is not allowed after EOC
	0x1F	Hard Fault

7.1.1.5 Configuration of error counter limits (Par ID 0x4)

Step 1: Define error counter limits by CONF_IREG1-3.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	Err. Cnt Limit YR1 LF								*reserved*				Par. ID = 0x4			
CONF_IREG2	0x0	0x2	0x02	Err. Cnt. Limit ACC1 HF								Err. Cnt. Limit ACC1 LF							
CONF_IREG3	0x0	0x3	0x03	Err. Cnt. Limit ACC2 HF								Err. Cnt. Limit ACC2 LF							

Unit of error counter Limit: 2LSB =1 ms

Fields of CONF_IREG1-3 (further counters in Par ID 0x5)

Field	Description
Err. Cnt Limit YR1 LF	Error counter for Rate 1 low pass filter
Err. Cnt. Limit ACC1 LF	Error counter for ACC1 low pass filter
Err. Cnt. Limit ACC1 HF	Error counter for ACC1 high pass filter
Err. Cnt. Limit ACC2 LF	Error counter for ACC2 low pass filter
Err. Cnt. Limit ACC2 HF	Error counter for ACC2 high pass filter
PAR_ID	Parameter ID, 0x4
reserved	Write 0x0

Step 2: Trigger configuration service

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved								0xC				0x3		0x0	0x0

Step 3: Check correct configuration by reading and verifying the contents of CONF_OREG0-3

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	Err. Cnt Limit YR1 LF								*reserved*				Par. ID = 0x4			
CONF_OREG2	0x0	0x6	0x06	Err. Cnt. Limit ACC1 HF								Err. Cnt. Limit ACC1 LF							
CONF_OREG3	0x0	0x7	0x07	Err. Cnt. Limit ACC2 HF								Err. Cnt. Limit ACC2 LF							

CONF_**OREG1** - CONF_**OREG3** contains the data, which has been read back from the sensor module after writing in CONF_**IREG1** - CONF_**IREG3** registers.

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	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xC	Soft configuration
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
ERROR_CODE	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07	Invalid parameter ID
	0x08	Service is not allowed after EOC
	0x1F	Hard Fault

7.1.1.6 Extended Configuration of error counter limits (Par ID 0x5)

Step 1: Define error counter limits by CONF_IREG1-3.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	Err. Cnt Limit YR2 LF*								*reserved*				Par. ID = 0x5*			
CONF_IREG2	0x0	0x2	0x02	Err. Cnt. Limit ACC3 HF*								Err. Cnt. Limit ACC3 LF*							
CONF_IREG3	0x0	0x3	0x03	*reserved*								*reserved*							

* available in SMI860 only

Fields of CONF_IREG1-3

Field	Description
Err. Cnt Limit YR2 LF*	Error counter for Rate 2 low frequency filter
Err. Cnt. Limit ACC3 LF*	Error counter for ACC3 low frequency filter
Err. Cnt. Limit ACC3 HF*	Error counter for ACC3 high frequency filter
PAR_ID	Parameter ID, 0x5
reserved	Write 0x0

* available in SMI860 only

Step 2: Trigger configuration service

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved								0xC				0x3		0x0	0x0

Step 3: Check correct configuration by reading and verifying the contents of CONF_OREG0-3

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	Err. Cnt Limit YR2 LF*								*reserved*				Par. ID = 0x5*			
CONF_OREG2	0x0	0x6	0x06	Err. Cnt. Limit ACC3 HF*								Err. Cnt. Limit ACC3 LF*							
CONF_OREG3	0x0	0x7	0x07	*reserved*								*reserved*							

CONF_**OREG1** - CONF_**OREG3** contains the data, which has been read back from the sensor module after writing in CONF_**IREG1** - CONF_**IREG3** registers.

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	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xC	Soft configuration
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07	Invalid parameter ID
	0x08	Service is not allowed after EOC
	0x1F	Hard Fault

7.1.1.7 Configuration of VB monitor (Par ID 0x6)

VB monitor offers the possibility to set the upper limit of VB threshold.

Step 1: Define VB monitor upper limit by CONF_IREG1-3.

The calibration value for the VB upper limit is calculated with the formula:

VB_upper_limit_LSB = -3725 LSB + VB_upper_limit_Volt * 154.28 LSB/V

Default value of -1874 LSB corresponds to 12V.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*reserved*												Par. ID = 0x6			
CONF_IREG2	0x0	0x2	0x02	Upper limit for VB monitor															
CONF_IREG3	0x0	0x3	0x03	*reserved*															

Fields of CONF_IREG1-3

Field	Description
Upper limit for VB monitor	Upper limit for VB monitor
PAR_ID	Parameter ID, 0x6
reserved	Write 0x0

Step 2: Trigger configuration service

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved							0xC					0x3		0x0	0x0

Step 3: Check correct configuration by reading and verifying the contents of CONF_OREG0-3

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	*reserved*												Par. ID = 0x6			
CONF_OREG2	0x0	0x6	0x06	Upper limit for VB monitor															
CONF_OREG3	0x0	0x7	0x07	*reserved*															

CONF_**OREG1** - CONF_**OREG3** contains the data, which has been read back from the sensor module after writing in CONF_**IREG1** - CONF_**IREG3** registers.

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	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xC	Soft configuration
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07	Invalid parameter ID
	0x08	Service is not allowed after EOC
	0x1F	Hard Fault

7.1.1.8 Configuration of BITE counts (Par ID 0x8)

The maximum valid value for BITE Count is 1...15. In case of an invalid value for the BITE count is set, the service does not change the value and returns the respective error code.

Step 1: Define max number of BITE counts.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*reserved*								Max BITE Count				Par. ID = 0x8			
CONF_IREG2	0x0	0x2	0x02	*reserved*															
CONF_IREG3	0x0	0x3	0x03	*reserved*															

Fields of CONF_IREG1-3

Field	Description
Max BITE Count	Maximum BITE counts. If this parameter is set to 0, no BITE is executed. As a result, the BITE is not passed which leads to a permanent error flag.
PAR_ID	Parameter ID, 0x8
reserved	Write 0x0

Step 2: Trigger configuration service

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved							0xC					0x3		0x0	0x0

Step 3: Check correct configuration by reading and verifying the contents of CONF_OREG0-3

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	*reserved*								Max BITE Count				Par. ID = 0x8			
CONF_OREG2	0x0	0x6	0x06	*reserved*															
CONF_OREG3	0x0	0x7	0x07	*reserved*															

CONF_**OREG1** - CONF_**OREG3** contains the data, which has been read back from the sensor module registers after writing in CONF_**IREG1** - CONF_**IREG3** registers.

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	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xC	Soft configuration
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
ERROR_CODE	0x6	OTP programming failure
	0x07	Invalid parameter ID
	0x08	Service is not allowed after EOC
	0x0A	Incorrect value for max BITE count
	0x1F	Hard Fault

7.1.1.9 Configure ACC-Sum-C test (Par ID 0x9)

The maximum value for SumC Count is 1...15. In case of an invalid value for the SumC count is set, the service does not change the value and returns the respective error code.

Default configuration: SumC count is 3

Step 1: Define max number of SumC counts by CONF_IREG1-3.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*reserved*				Max. SumC Count				*reserved*			SC	Par. ID = 0x9			
CONF_IREG2	0x0	0x2	0x02	*reserved*															
CONF_IREG3	0x0	0x3	0x03	*reserved*															

Fields of CONF_IREG1-3 **Field**	**Description**
Max SumC Count	Maximum SumC counts 1..15.
SC	1: Automatic Sum-C test sequence before ACC-Startup-BITE enabled. 0: Automatic Sum-C test sequence before ACC-Startup-BITE disabled.
PAR_ID	Parameter ID, 0x8
reserved	Write 0x0

Step 2: Trigger configuration service

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	reserved							0xC					0x3		0x0	0x0

Step 3: Check correct configuration by reading and verifying the contents of CONF_OREG0-3

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	*reserved*				Max. SumC Count				*reserved*			SC	Par. ID = 0x9			
CONF_OREG2	0x0	0x6	0x06	*reserved*															
CONF_OREG3	0x0	0x7	0x07	*reserved*															

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CONF_**OREG1** - CONF_**OREG3** contains the data, which has been read back from the sensor module registers after writing in CONF_**IREG1** - CONF_**IREG3** registers.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xC	Soft configuration
STATUS	0x0	Service done
	0x1	Service terminated with errors
STATUS	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07	Invalid parameter ID
	0x08	Service is not allowed after EOC
	0x0B	Incorrect value for max Sum C count
	0x1F	Hard Fault

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7.1.2 Offset compensation

The sensor module provides a fast (initial) and slow (continuous) offset compensation (FOC, SOC). The offset compensation can be enabled or disabled for each channel individually. The offset compensation is available for rate and accelerations LF channels only (i.e. not for the HF acceleration channels).

If offset compensation is used in an application, initial raw offsets of rate and acceleration channels are cancelled during start-up by the fast offset compensation (FOC). After each reset of the sensor, the initial offset may be present.

The slow offset compensation (SOC) or the single pole high pass filter (HPF) will start automatically after the fast offset compensation (FOC), when the power on sequence is completed. In addition, the fast offset compensation (FOC) can be triggered manually.

FOC duration is nominally 50 ms for each trigger. In order to verify that the offset compensation has canceled an existing offset during start-up, the signals must be evaluated after finishing the FOC. It must be taken into account in the application that an external stimuli can be responsible for the offset.

The offset compensation has to be repeated in case an offset is still present after the FOC (e.g. due to external stimulus during power on).

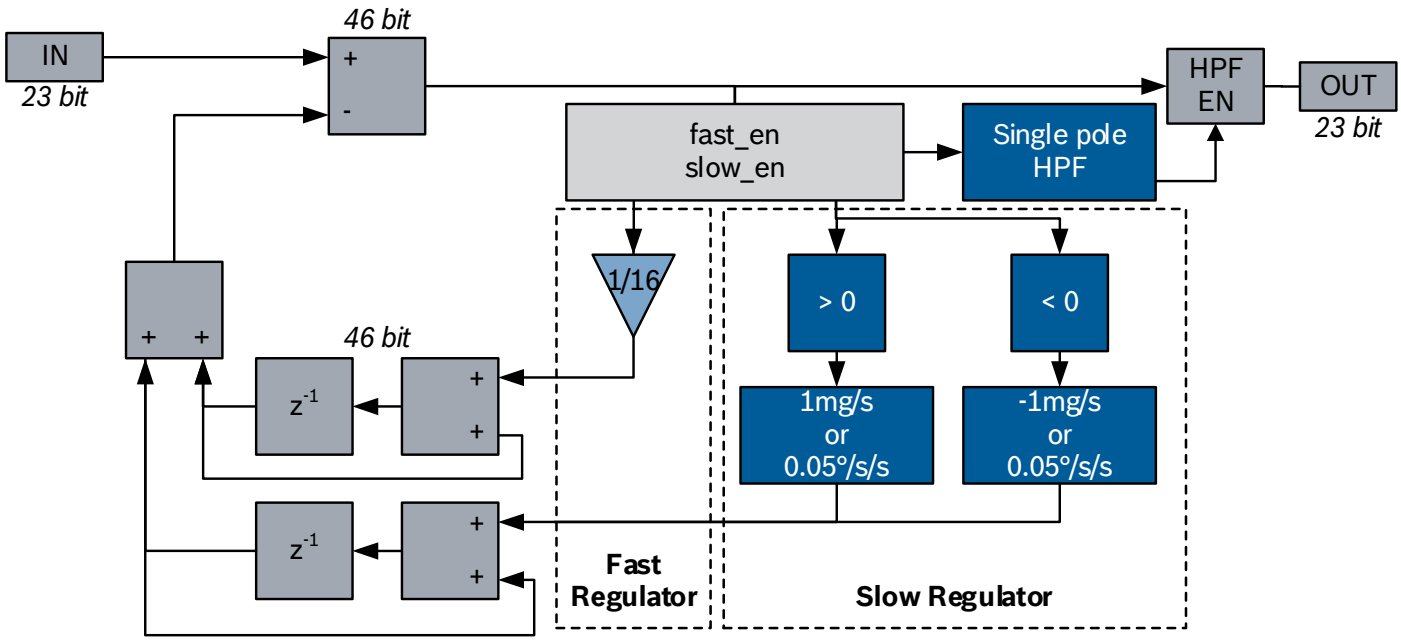

Figure 21 Offset regulator block diagram

Parameter / Condition	Min	Typ	Max	Unit
Regulations speed of rate signal slow offset compensation	-	-	0.050	°/s/s
Residual rate offset after fast offset compensation	-	-	0.2	°/s
Regulations speed of acceleration signal slow offset compensation (6g)	-	-	1	mg/s
Regulations speed of acceleration signal slow offset compensation (extended measurement range 8g)	-	-	1.4	mg/s
Residual acceleration offset after fast offset compensation	-	-	10	mg
Fast offset compensation time	-	-	55	ms

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As an additional option, single pole high pass filter (HPF) is available Its transfer function is

$$\frac{z-1}{z-\left(1-\frac{1}{2^n}\right)}$$

with N=16 and 2 kHz sampling rate.

The digital output signal after offset compensation is implemented with symmetric rounding:

-2.51 → -3 +2.51 → +3

-2.50 → -3 +2.50 → +3

-2.49 → -2 +2.49 → +2

7.1.2.1 Triggering offset compensation

Offset compensation is applied by soft configuring the respective channel. After power on, the sensor module will start the fast and subsequent slow offset compensation routine automatically.

After EOC, offset compensation can be repeated by performing the following steps:

Step 1: Select channel for manual triggering of offset compensation by CONF_IREG1.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*reserved*											R2*	*R1*	*A3**	A2	A1

* available in SMI860 only

Fields of CONF_IREG1

Field	Values	Description
A1	0x0	Don´t trigger ACC1 FOC
	0x1	Trigger ACC1 FOC
A2	0x0	Don´t trigger ACC2 FOC
	0x1	Trigger ACC2 FOC
A3*	0x0	Don´t trigger ACC3 FOC
	0x1	Trigger ACC3 FOC
R1	0x0	Don´t trigger Rate 1 FOC
	0x1	Trigger Rate 1 FOC
R2*	0x0	Don´t trigger Rate 2 FOC
	0x1	Trigger Rate 2 FOC

* available in SMI860 only

Step 2: Start service for FOC

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	*reserved*							0x4					0x3		0	0

Step 3: Read and verify FOC status

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	*reserved*											R2*	*R1*	*A3**	A2	A1

* available in SMI860 only

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Fields of CONF_OREG1

Field	Values	Description
A1	0x0	ACC1 FOC is not triggered
	0x1	ACC1 FOC is triggered
A2	0x0	ACC2 FOC is not triggered
	0x1	ACC2 FOC is triggered
A3*	0x0	ACC3 FOC is not triggered
	0x1	ACC3 FOC is triggered
R1	0x0	Rate 1 FOC is not triggered
	0x1	Rate 1 FOC is triggered
R2*	0x0	Rate 2 FOC is not triggered
	0x1	Rate 2 FOC is triggered

Step 4: Read and verify FOC error codes

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Error of FOC execution are reported in CONF_OREG0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0x4	FOC trigger
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x07	Invalid channel status (channel status !=0)
	0x08	Deactivated offset regulator
	0x1F	Hard Fault

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7.1.3 BITE (Built In Self-Test)

7.1.3.1 Triggering BITE & Reading BITE status

The BITE is always executed during a power on cycle. If necessary, it can be repeated at any time during operation. A manual BITE is triggered by the following steps:

Step 1: Select channel for manual BITE by CONF_IREG1.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*reserved*						BITE_TYPE		*reserved*		ACC_BITE		*reserved*		YRS_BITE	

Fields of CONF_IREG1

Field	Values	Description
BITE_TYPE	0x0	Request BITE status without change
	0x1	Trigger a dynamic BITE sequence
	0x2 to 0x3	Request BITE status without change
ACC_BITE	0x0 to 0x2	no action
	0x3	Start dynamic ACC BITE
YRS_BITE	0x0 to 0x2	no action
	0x3	Start dynamic YRS BITE

Step 2: Start service for BITE

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	*reserved*								0xD				0x3		0	0

Step 3: Read and verify BITE status

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	*reserved*						BITE_TYPE		*reserved*		ACC_BITE		*reserved*		YRS_BITE	

Fields of CONF_OREG1

Field	Values	Description
BITE_TYPE	0x0	All BITEs are off
	0x1	Dynamic BITE sequence is running
ACC_BITE	0x0 to 0x2	Dynamic ACC BITE is off
	0x3	Dynamic ACC BITE is on
YRS_BITE	0x0 to 0x2	Dynamic YRS BITE is off
	0x3	Dynamic YRS BITE is on

Step 4: Read and verify BITE error codes

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS			SERVICE_ID				0x3		0x0	0x0

Error of BITE execution are reported in CONF_OREG0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xD	Manual BITE trigger
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure

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Field	Value	Description
ERROR_CODE	0x07	Attempt to start a dynamic BITE with wrong parameters
	0x08	Triggering dynamic BITE is not allowed while init ready is not set
	0x09	Triggering dynamic BITE is not allowed while FOC is running
	0x0B	Triggering dynamic BITE is not allowed while ACC Sum-C is running
	0x0A	All BITE trigger requests are rejected while a dynamic BITE is running
	0x1F	Hard Fault

Step 5: Check result of the last BITE:

By running the BITE, the cluster flag F16_ST_RUN and F16_INIT will be triggered, indicating that that the BITE is running.

If a BITE sequence fails, the channel status bit (CS) of the affected channel is set to “1". The BITE deviation values of all channels are available in the registers listed on page (PG) 5 and 6.

At every BITE execution 16bit BITE evaluation signals which are SPI32 accessible are updated. The signals contains the minimum difference of the last BITE signal difference (POS-NEG) of channel XXX to its respective temperature-dependent test limits:

LAST_BITE_XXX_DEVIATION (XXX=RATE1, RATE2, QUAD1, QUAD2, ACC1, ACC2, ACC3).

In the self-test for the rate channel, the regulator value of the quadrature is measured and evaluated.

Interpretation hints:
BITE evaluation signal < 0 means: BITE passed
BITE evaluation signal > 0 means: BITE failed.

Large positive BITE evaluation signals >2^15-1=32767 are possible in theory but not likely for properly configured sensors. Since the output registers have signed 16 bit, large evaluation signals would result in an overflow and cannot be displayed properly. The internal evaluation of BITE flags will be correct in any case, since internal calculations use a larger bit width.

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7.1.3.2 BITE Specification

The following BITE limits are stored sensor internally to evaluate each BITE against the new part limits.

Parameter / Condition	Min	Typ	Max	Unit
BITE repeatability of acceleration signal path without external stimulus	-5	-	5	%
BITE limit of acceleration signal path	-10		10	%
BITE repeatability of rate signal path without external stimulus	-5	-	5	%
BITE limit ofoff rate signal path	-5		5	%
Self-test time (for one BITE)	-	60	65	ms
BITE amplitude of acceleration signals	4.2	-	-	g
BITE amplitude of angular rate (quadrature channel) signal	150			°/s

ACC BITE and RATE BITE are independent: If BITE in one channel fails, only ACC OR RATE BITE are repeated.
If BITE in one ACC channel fails, BITE in all ACC channels is repeated but only the one that failed is re-evaluated.
In SMI860, if BITE in one RATE channel fails, both RATE BITEs will be repeated but only the one that failed is re-evaluated.
INIT-Bit and CS Bits in ACC and RATE SPI MISO frames are set independently.

Note: in the case of the ACC BITE repetitions, a break of varied duration with the following sequence is implemented: 5ms, 10ms, 15ms, 10ms, 5ms, 10ms,... As illustrated in the following graph, the break sequence repeats after a 5 BITE cycle. In case of the gyroscope BITE repetitions, there is no break implemented between the repetitions.

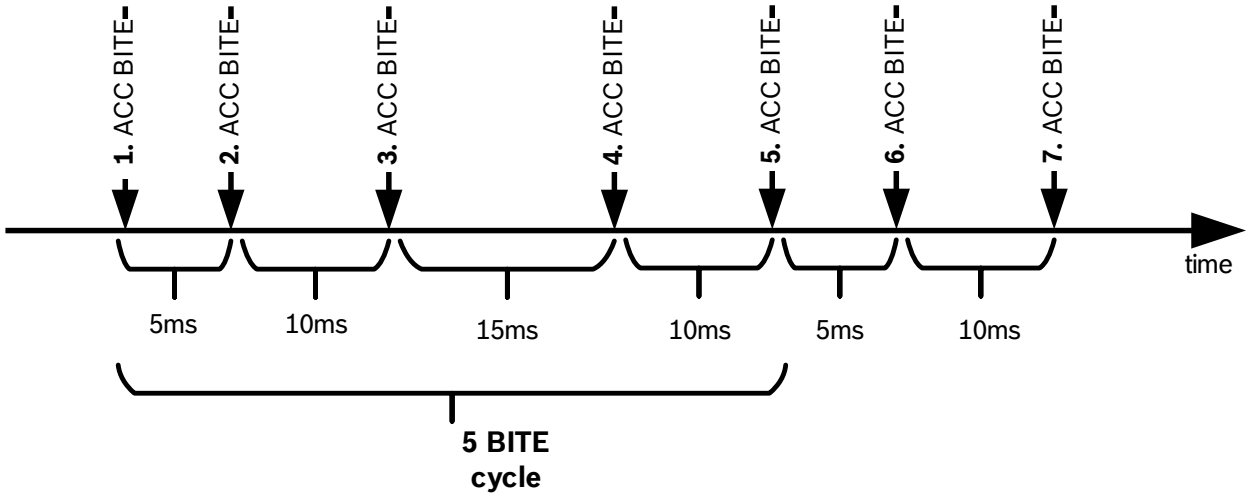

Figure 22 ACC BITE repetitions diagram

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7.1.4 ACC-Sum-C test

7.1.4.1 Triggering ACC-Sum-C test & Reading ACC-Sum-C test status

The principle of the ACC-Sum-C test is as follows: the difference and the sum of both capacitances are determined and are compared to part individual stored trimming values. The following parameters are evaluated with this test:

- Change in ACC parasitic capacitance (i.e. broken MEMS fingers / particles are detectable)
- Leakage between ACC bonds and bond pads (i.e. contamination is detectable)

The ACC-Sum-C test has to be enabled through configuration to execute during a power on cycle. If necessary, it can be repeated at any time during operation.

The repeating of the ACC-Sum-C test is not allowed in case that any offset compensation method is used. In case of a running offset compensation, the ACC-Sum-C test might fail when it is repeated.

The duration of the ACC-Sum-C test is defined as the test duration + the filter flush time. Please refer to chapter 5.4. The manual ACC-Sum-C test is triggered by the following steps:

Step 1:Start service of ACC Sum-C Test

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	*reserved*							0x5					0x3		0	0

Step 2: Read ACC-Sum-C test error codes from CONF_OREG0

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Error of ACC-Sum-C Sum execution are reported in CONF_OREG0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0x5	ACC Sum-C trigger
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
ERROR_CODE	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0x7	Service can not be called before init rdy is set
	0x8	ACC Sum-C test cannot be started because Sum C test is alredy running
	0x9	ACC Sum-C test cannot be started because BITE is running
	0xA	ACC Sum-C test cannot be started because FOC is running
	0x1F	Hard Fault

Step 3: Check and verify the result of the ACC-Sum-C test

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7.1.5 Watchdog for external SPI Master

The watchdog service is only available in SMI860.
The watchdog service allows to control the microcontroller of the external SPI master. The SPI data is used to verify the functionality of the microcontroller. It's a simple question and answer game where the sensor's ASIC is giving the question to the microcontroller and the microcontroller is supposed to give correct response within a defined time frame. This will check the internal logic of the microcontroller for correct functionality.

If an answer from the microcontroller does not match the expected value, or if the answer was given too late, the sensor will pull its watchdog pin to logical high level.
A table of request and response pairs is stored within the sensor's memory:

Request	Response
0x00B3	0xA272
0xE1CC	0x57FD
0x1069	0xBFCB
0x79A4	0x3212
0xA1C5	0x03E7
0x20A6	0x4AB5
0x8AB4	0xE7C3
0xC361	0xA144
0x4D4A	0x9939
0xAC61	0xB2F6
0xE614	0x2658
0xE35A	0x5E48
0xC9B3	0x02DE
0x1683	0x1483
0x2016	0xFF66
0xF1BB	0xF4A8

The request is issued by the sensor using the output register CONF_OREG1. After reading out this register the SPI master (microcontroller) needs to write the corresponding response according to the table into the input register CONF_IREG1. After writing that register, the master must trigger the watchdog check by writing into the control register CONF_IREG0. After that the sensor checks if the master's response matches the expected value.

Definition of configuration register:

register	Description
CONF_IREG1	The SPI Master has to write its response into here
CONF_IREG2	Start watchdog functionality by SPI Master
CONF_IREG3	Set max response time for the SPI master

register	Description
CONF_OREG1	Request of the sensor (to be read out by the master)
CONF_OREG0	Status

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How to use watchdog:

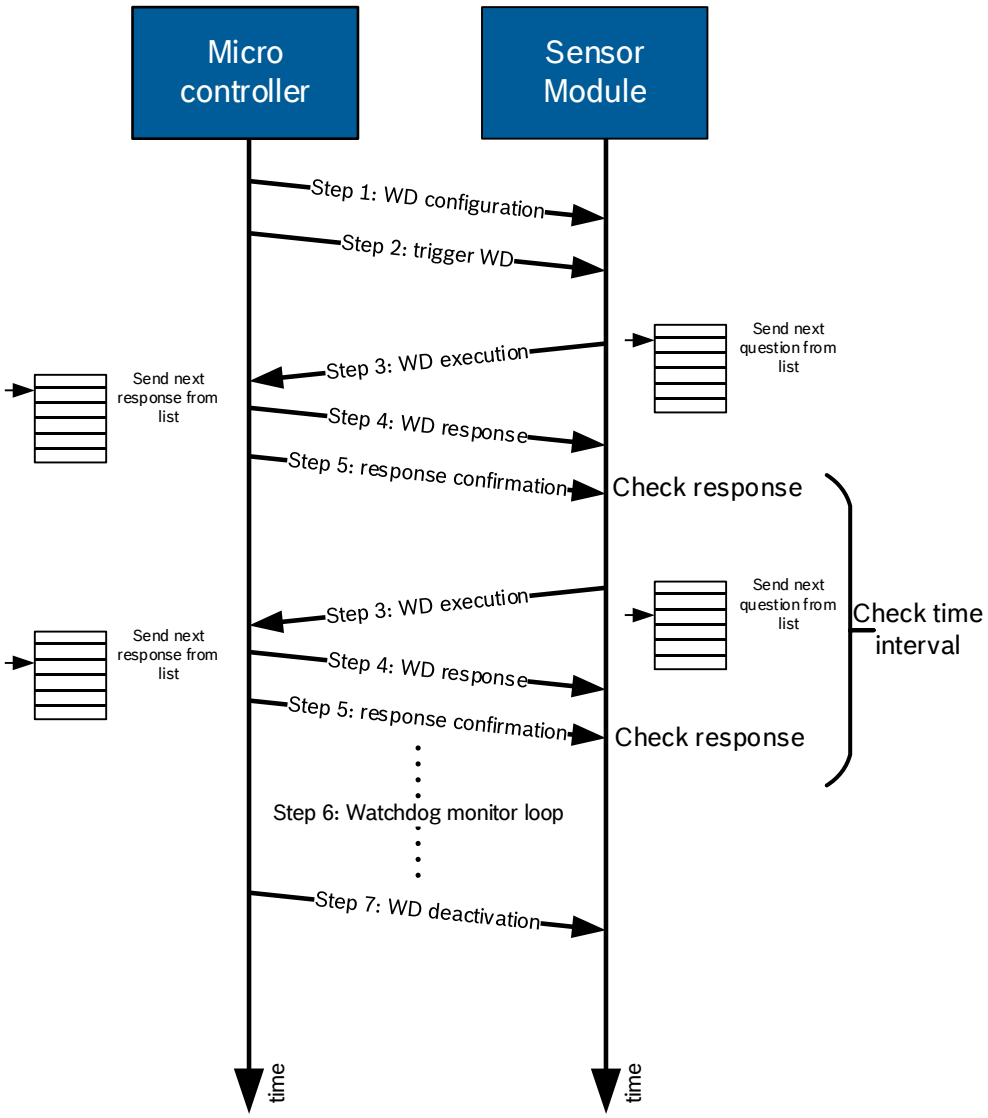

Figure 23 Watchdog monitor handling diagram

Step 1: Watchdog monitor configuration:

The first call of the Watchdog service is used for activation and configuration of the watchdog.

The master has to configure the following registers to start watchdog functionality:

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*0*															
CONF_IREG2	0x0	0x2	0x02	0xAAAA															
CONF_IREG3	0x0	0x3	0x03	Maximum response time from SPI master [ms]															

Step 2: Trigger watchdog service

The watchdog process starts right after triggering by writing into CONF_IREG0:

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x1	0x01		*reserved*						0xF					0x3		0	0

After activation the 1st request is issued in CONF_OREG1. The internal time-out counter starts running. The watchdog cannot be activated if it has already failed before in the same reset cycle of the sensor. The

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watchdog can only be activated after the end of configuration sequence.

Step 3: Watchdog Monitor execution

After triggering the watchdog service (step 2), the master needs to read out the sensor's requests (CONF_OREG1).

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG1	0x0	0x5	0x05	request															
CONF_OREG2	0x0	0x6	0x06	reserved															
CONF_OREG3	0x0	0x7	0x07	reserved															
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0	0

With the watchdog activated the SPI master must call the service cyclically with the correct RESPONSE according to the last issued REQUEST. If the watchdog has not failed within the same reset cycle it is possible to restart the watchdog during execution by calling the service with a new activation parameter set. If RESPONSE is wrong or the SPI master doesn't respond within the specified time-out the watchdog has failed, i.e. the output current sink is deactivated and the watchdog cannot be reactivated in the same reset cycle.

Step 4: SPI master response during watchdog operation

After reading CONF_OREG1 the master has to check for the correct response by using the table above. The corresponding response must then be written into the CONF_IREG_1 register.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	response															
CONF_IREG2	0x0	0x2	0x02	reserved															
CONF_IREG3	0x0	0x3	0x03	reserved															

Step 5: SPI master response confirmation

After writing the correct response into CONF_IREG1 the master needs to confirm the answering cycle by writing into the control register CONF_IREG0.

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	*reserved*							0xF					0x3		0	0

The confirmation of the SPI master response must be done within the defined maximum response time that was set in Step 1.

Step 6: Watchdog monitor loop

As long as the watchdog process is not stopped by the master, the steps 3,4 and 5 will be repeated. The sensor awaits the correct responses within the defined time interval.

Step 7: Watchdog monitor deactivation

The watchdog service can be stopped by the SPI master by writing a specific content into the input registers CONF_IREG1-3 anytime:

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG1	0x0	0x1	0x01	*0*															
CONF_IREG2	0x0	0x2	0x02	0x5555															
CONF_IREG3	0x0	0x3	0x03	reserved															

The deactivation of the watchdog service needs to be confirmed by writing into the control register CONF_IREG0:

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_IREG0	0x0	0x0	0x00	*reserved*							0xF					0x3		0	0

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Status of watchdog service

The current status of the watchdog service can be read out using the CONF_OREG0 register:

	PG	ADR	A	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CONF_OREG0	0x0	0x4	0x04	ERROR_CODE					STATUS		SERVICE_ID					0x3		0x0	0x0

Fields of CONF_OREG0:

Field	Value	Description
SERVICE_ID	0xE	Watchdog for external SPI Master
STATUS	0x0	Service done
	0x1	Service terminated with errors
	0x2	Service in progress
	0x3	Service requested
ERROR_CODE	0x0	No Error
	0x1	Service is not supported
	0x2	Service is protected
	0x3	Read access error
	0x4	Write access denied
	0x5	DSP parity failure
	0x6	OTP programming failure
	0xC	Service can not be called before end of configuration is set
	0xD	Invalid command no correct request
	0xE	wrong answer to the request
	0xF	response Time to long
	0x1F	Hard Fault

If the watchdog has not failed within the same reset cycle it is possible to restart the watchdog during execution by calling the service with a new activation parameter set (step 1).

If RESPONSE is wrong or the SPI master doesn't respond within the specified time-out the watchdog has failed, i.e. the sensor will pull its watchdog pin to logical high level and the watchdog cannot be reactivated in the same reset cycle.

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7.2 Traceability

The sensor module is traceable up to lot data and final test results. This is possible as each single sensor module has a unique serial number. This unique serial number is stored at final test and allows assignment of ASIC and sensor module test data.

The sensor module is traceable to lot data and wafer level test results of a single ASIC by a unique ASIC serial number.

PG	ADR	A	Signal	Function
0x4	0x0	0x40	ASIC_SERIAL_NO_0	ASIC serial BIT 0-15
0x4	0x1	0x41	ASIC_SERIAL_NO_1	ASIC serial BIT 16-31
0x4	0x2	0x42	ASIC_SERIAL_NO_2	ASIC serial BIT 32-47
0x4	0x5	0x45	SMI_SERIAL_NO_0	SMI Serial No.: Sample status, SMI type, Part no: [15..0] Series production lot no. cont.
0x4	0x6	0x46	SMI_SERIAL_NO_1	SMI Serial No.: Sample status, SMI type, Part no: [15..11] Last five digits of RRB part no. cont. [10..0] Series production lot no.
0x4	0x7	0x47	SMI_SERIAL_NO_2	SMI Serial No.: Sample status, SMI type, Part no: [15] 0: sample 1: series part [14..12] SMI type: SMI800 = 001 SMI810 = 010 SMI860 = 011 SMG810 = 100 [11..0] Last five digits of RRB part no.

A unique 16bit configuration number, which is customer specific and SMI8xx specific allows to identify the sensor type and configuration variant.

The configuration number is stored on PG 4 ADR: 0x8:

PG	ADR	A	Signal	Function
0x4	0x8	0x48	Configuration number	Sample status, SMI type, Configuration variant: [15..12] Sample Status 0001 = A0 0010 = C0 0011 = C1 0100 = C2 & production [11..9] Sensor type 001 = SMI800 010 = SMI810 011 = SMI860 100 = SMG810 [8..0] Configuration number (customer specific)

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7.3 Gyro resonance frequency

The sensor's resonance frequency can be determined by reading the register "SPI counter". The SPI counter value is a 16 bit unsigned value, incrementing with an update rate of PLL frequency / 4. The frequency is determined by reading the "SPI counter" value twice within a defined time interval:

Definitions:

c1 = counter value at start time (first read)
c2 = counter value at end time (second read)
T = Time interval between two reads
W = number of counter overflows during T
f_{CMG} = Drive frequency of angular rate sensor
df = Resolution of frequency measurement

Calculation Formula:

f_{CMG} = (c2-c1+W*65536) / T / 256

Frequency Resolution:

$df = 1/T^2*dt$

The resolution of frequency measurement df depends on the measurement period T. The nominal uncertainty in time measurement caused by the counter discretization is

$dt = 1/(f_{counter}) = 1/(256*25kHz) = 0.156\mu s$.

Example: to obtain a frequency resolution of df=1Hz the measurement time interval T must be at least

$T >= (1/1Hz*0.156\mu s)^{0.5} = \sim 0.4ms$

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7.4 Overload

Digital clipping of the signal output does not occur at values lower than the specified measurement range.
The output value of a sensor channel is in saturation, if input signal exceeds the measurement range.
As long as the input exceeds the measurement range but remains below the internal headroom, the output will stay in saturation. No failure flag (CS bit of SPI message) is set in this condition.
At input values higher than the internal headroom the output signal is marked invalid by the failure flag (CS bit of SPI message) indicating the violation of the internal headroom.
In case the internal headroom is violated, the gyroscope can show undefined output signals (flagged as invalid) with values lower than the measurement range.
SMI860 cross-axis interaction for gyro:
In case that one of the gyro channels of SMI860 is in overload condition, the other one is affected by this overload condition not more than specified in the cross-axis sensitivity specification.

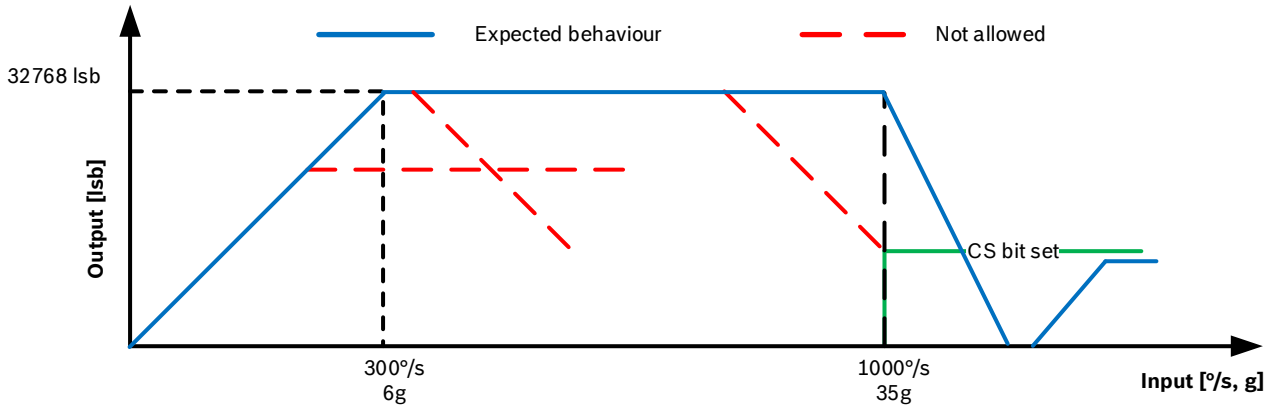

Figure 24 Definition of the sensor behavior with overload

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8 Safety Concept

The SMI8xy sensor is designed for use in safety relevant systems (passive and active safety) and is equipped with an internal Safety Controller (SCON), which is responsible for tagging every SPI message as valid or invalid. The SCON is a functional block within the sensor ASIC. The SCON autonomously performs a variety of checks and monitors and tags each inertial signal individually as valid or invalid according to the results.

Monitor functions can be continuous (with a constant repetition rate during operation) or performed during “power-on” (the test is only conducted at power on).

When a signal monitored by the SCON does not meet the programmed tolerances, monitoring flags are generated by the SCON itself. Flags are processed by the SCON in error counters. The purpose of the error counters is to act as a low pass filter in case of toggling error flags in order to increase the system availability. It reduces the probability of valid signals being marked invalid. The output of the channel specific error counters is a valid/invalid tag i.e. channel status bit called CS-Bit. CS-Bit is part of each SPI-module data communication frame (described in Chapter 6.4).

The error flags themselves fall into two groups: permanent and temporary. When a permanent error flag is set, the sensor signal will be immediately tagged as invalid until the next power-on cycle. These invalid tags cannot be removed by the sensor. In contrast, a temporary error flag is only set as long as the error source is present and can be cleared by read.

As each inertial signal has its own valid/ invalid status, it is possible for the rate signal to be used despite of an error in an acceleration channel and vice versa.

The safe state is the state a sensor may go to, if any safety criterion is violated. There are three possible states. If it is technically possible, criterion a) should be used:

- **A.** status flag set for corresponding channel
- **B.** wrong checksum for response
- **C.** no response

At start-up, as long as the supply voltage has not reached the specified supply voltage range, the sensor stays either in reset state, sets a failure flag or provides output values which are in specification.

8.1 Diagnostic Features

8.1.1 Monitors

In order to detect sensor failures, the read-out of the channel status bit (CS bit) and the control of the CRC check sum is strongly recommended (see chapter 6.4).

Details on sensor failures can be read-out via the following error flags. To read out the error flag registers use the module commands described in the chapters 6.4.1.2. or 6.4.2.2

There are two types of error flag registers. The “error flag banks” show all the failure monitors in the sensor located at different positions within the signal chain.
The second type is the so called “Cluster flag” register. In that register, the error flags are grouped into several categories, allowing the user to get a brief overview about the failure category that is happening.

The evaluation of the cluster flags is recommended to detect the failure category. For deeper understanding or analysis purposes, the error flag banks can be used.
The cluster flags as well as the error flag banks are latched until read, meaning that the corresponding failure bit stays active until it is read out by a SPI command. By reading, the flag is cleared in case that the failure is not present anymore.

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Recommendation: clear all failure flags once after start-up of the sensor.
In case of a sensor failure recognized by the CS bit, store at least the cluster flags once in order to determine the failure's root cause. Additional storing of the error flag banks further helps for failure analysis. After the failure condition is vanished (CS bit cleared to 0), read all error flag registers once in order to clear them all.

The following tables describes the error flags which are located in the "error_flag_16_bank" registers.

Error Flag Bank 0

BitPos	Flagname
0	lbist_err
1	not used
2	bg_err
3	vb_err
4	not used
5	vdd_yrs_err
6	vdd_acc_err
7	vddio_err
8	yrs_rate_v_cm
9	yrs1_rate_v_tn
10	yrs1_rate_v_com
11	yrs_rate_v_fb1_cm
12	yrs2_rate_v_tn
13	yrs2_rate_v_com
14	yrs_rate_v_fb2_box
15	not used

Error Flag Bank 1

BitPos	Flagname
0	acc1_v_cm
1	acc2_v_cm
2	acc3_v_cm
3	not used
4	not used
5	not used
6	pc_shld
7	pc_csub
8	dcm_err
9	not used
10	yrs_agc_irregular
11	yrs_drv_pi_tol
12	yrs_drv_adc_mean
13	yrs_drv_adc
14	yrs_pll_tol
15	yrs_pll_unlock

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Error Flag Bank 2

BitPos	Flagname
0	yrs1_rate_adc_mean
1	yrs1_rate_pt2_lim
2	yrs2_rate_adc_mean
3	yrs2_rate_pt2_lim
4	not used
5	yrs1_quad_i_tol
6	yrs2_quad_i_tol
7	not used
8	acc1_ds_lim
9	acc2_ds_lim
10	acc3_ds_lim
11	not used
12	not used
13	not used
14	yrs2_pe_flag_freq_1k_err
15	yrs1_pe_flag_freq_1k_err

Error Flag Bank 3

BitPos	Flagname
0	yrs1_pe_flag_rate_1k_err
1	yrs1_pe_flag_quad_1k_err
2	yrs2_pe_flag_rate_1k_err
3	yrs2_pe_flag_quad_1k_err
4	not used
5	acc1_pe_flag_1k_err
6	acc1_pe_flag_8k_err
7	acc2_pe_flag_1k_err
8	acc2_pe_flag_8k_err
9	acc3_pe_flag_1k_err
10	acc3_pe_flag_8k_err
11	not used
12	not used
13	not used
14	not used
15	not used

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Error Flag Bank 4

BitPos	Flagname
0	dsp1_ram_check_err
1	dsp1_crom_check_err
2	dsp1_prom_check_err
3	dsp1_pe_flag_ram
4	dsp1_pe_flag_crom
5	dsp1_pe_flag_prom
6	dsp1_debug_on
7	dsp2_ram_check_err
8	dsp2_crom_check_err
9	dsp2_prom_check_err
10	dsp2_pe_flag_ram
11	dsp2_pe_flag_crom
12	dsp2_pe_flag_prom
13	dsp2_debug_on
14	not used
15	not used

Error Flag Bank 5

BitPos	Flagname
0	dsp1_online_test
1	dsp2_online_test
2	dsp1_pe_flag_general
3	dsp1_pe_flag_dapa
4	dsp1_pe_flag_agpcstk
5	dsp1_pe_flag_io
6	dsp2_pe_flag_general
7	dsp2_pe_flag_dapa
8	dsp2_pe_flag_agpcstk
9	dsp2_pe_flag_io
10	not used
11	not used
12	not used
13	not used
14	not used
15	not used

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Error Flag Bank 6

BitPos	Flagname
0	yrs1_dsp_lf_adjust
1	yrs2_dsp_lf_adjust
2	acc1_dsp_hf_in
3	acc1_dsp_hf_in_l
4	acc1_dsp_lf_in
5	acc1_dsp_hf_adjust
6	acc1_dsp_lf_adjust
7	acc2_dsp_hf_in
8	acc2_dsp_hf_in_l
9	acc2_dsp_lf_in
10	acc2_dsp_hf_adjust
11	acc2_dsp_lf_adjust
12	acc3_dsp_hf_in
13	acc3_dsp_hf_in_l
14	acc3_dsp_lf_in
15	acc3_dsp_hf_adjust

Error Flag Bank 7

BitPos	Flagname
0	acc3_dsp_lf_adjust
1	not used
2	yrs1_foc_active (indication, no error)
3	yrs2_foc_active (indication, no error)
4	acc1_foc_active (indication, no error)
5	acc2_foc_active (indication, no error)
6	acc3_foc_active (indication, no error)
7	acc1_sum_c
8	acc2_sum_c
9	ctm1_range
10	ctm2_range
11	ctm1_dsp_adjust
12	ctm2_dsp_adjust
13	ctm_diff
14	acc3_sum_c
15	not used

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Error Flag Bank 8

BitPos	Flagname
0	yrs1_rate_seq_bite
1	yrs1_quad_seq_bite
2	yrs2_rate_seq_bite
3	yrs2_quad_seq_bite
4	acc1_seq_bite
5	acc2_seq_bite
6	acc3_seq_bite
7	not used
8	ahb_hang_up
9	uc_ram_online_err
10	uc_ram_startup_err
11	uc_rom_online_err
12	uc_rom_startup_err
13	otp_startup_ecc_bist
14	uc_watchdog_err
15	not used

Error Flag Bank 9

BitPos	Flagname
0	uc_stack_check
1	uc_unrecoverable_err
2	uc_registercheck_err
3	uc_tuple_readback_mismatch
4	uc_bootloader_crc_err
5	uc_program_flow
6	uc_dsp_parity_err
7	uc_invalid_tuple
8	uc_corrupt_bank
9	not used
10	uc_initial_flag_check
11	bootloading_not_complete
12	-
13	-
14	-
15	apb_slv

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Cluster Flags

The cluster flags group the individual error flags mentioned above into several categories. It gives a fast overview about the type of error that occurs. The cluster flags F16_ST_RUN and F16_INIT are not linked to other error flags. F16_INIT is set to “1” if at least one channel is in initialization. F16_RUN is set to “1” during active BITE sequence or ACC Sum-C test including flushtime.

BitPos	Cluster flag name
0	F16_ST_RUN
1	F16_INIT
2	F16_MECH_OVERLOAD_ACC1
3	F16_ST_FAILED
4	F16_MECH_OVERLOAD_RATE2
5	F16_TEMP
6	F16_SUPPLY
7	F16_EMC_PSRR
8	F16_MECH_OVERLOAD_RATE1
9	F16_DIGITAL
10	F16_FW
11	F16_MEMORY_DATA_AND_DSP
12	F16_MECH_OVERLOAD_ACC3
13	F16_MECH_OVERLOAD_ACC2
14	F16_UC_WD
15	F16_MEMORY

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8.1.2 Error counters

Error counters are implemented in order to allow debouncing of safety monitor flags and increase availability of sensor signals. Error counters are implemented for each sensor data channel:

YRS1_LF, YRS2_LF, ACC1_LF, ACC1_HF, ACC2_LF, ACC2_HF, ACC3_LF, ACC3_HF

Error counters report the validity of a single sensor channel by summarizing all safety monitor flags relevant for this specific channel.
All error counters are 8 bit counters containing values from 0 to 255. Each counter has 2 parameters: limit and hold. With a repetition rate of about 2 kHz the error counter is either incremented by 1 LSB if an error is present or decremented by 0.5 LSB if the error is not present. Consequently the error counter is decremented with an actual frequency of about 1 kHz.

In case a defined limit is reached, the error counter value is immediately set to limit + hold and the channel status bit (CS bit in SPI frame) is set to logical 1, meaning "channel sensor data not valid". Once this status is reached an additional error will not increase the value of the error counter any further.
This status will be held for the defined hold time, after the error condition is no longer present. The hold limits determines the filter flush time for the error counters.

If the failure condition is no more present the error counter starts to decrement. Once the limit is reached the SPI message is set to “valid”, i.e. CS bit is set to ‘0’.

The error counter flush time is the minimum time span needed to reach the limit value once the error is no more present (starting point from the limit + hold value). This time span ensures that no remaining signal, causing a CS bit to be set, is processed within the digital signal path of the sensor, once the SPI message is set to “valid” again.

The current error counter value can be read by SPI command. The limit and hold value are set by Bosch at the end of line measurement or soft configured by the user.

Fatal errors will set error counters permanently to the maximum value deactivating the decrementation. Such errors will only vanish after a restart of the sensor.

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Below figure shows an example of the schematic behavior of an arbitrary error counter in case of temporary safety monitor flags. The top graph shows the occurrence of the safety monitor flag at the entry of the error counter, while the middle graph shows the evolution of the error counter value over time as a result of the safety monitor flags. The maximum value of the error counter (limit + hold) is not increased further by safety monitor flag occurrences once maximum value is reached. The last graph shows the output of the error counter (CS bit will be set).

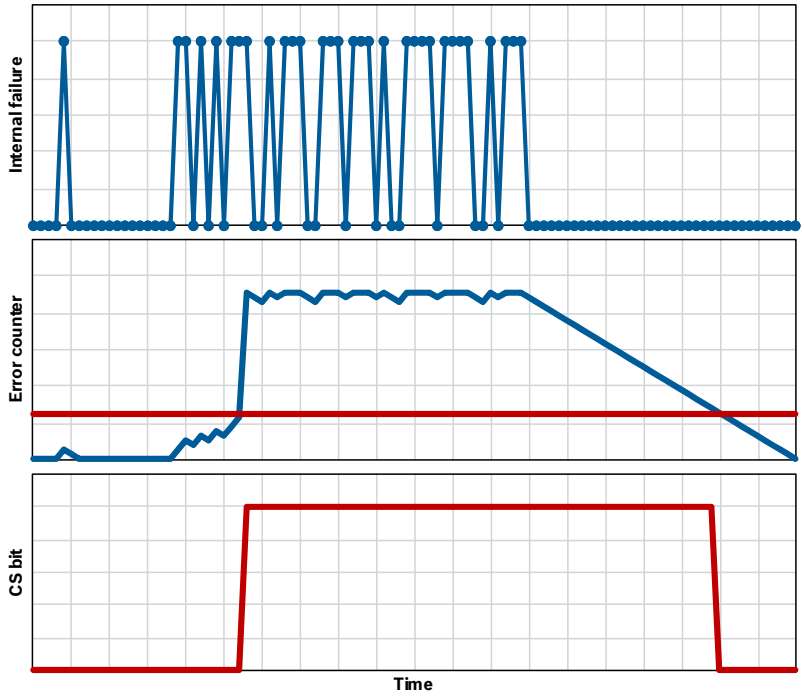

Figure 25 Relation between internal failure, error counter and external error

Error counter hold values are soft configurable. It is possible to turn off counters to achieve a direct feed through of the internal errors making it possible for the application to implement its own debouncing.

8.1.3 Cluster Flags

Cluster flags are available in order to provide a top-level summary of monitor flags in a meaningful and hierarchical order to give a better overview of the possible reasons for the defect.

8.1.4 BITE

The sensor module provides an electro-mechanical self-test (BITE) which is bidirectional, deflecting the sensing element in positive and negative measurement direction. The BITE tests verifies the functionality of the MEMS elements and ASIC signal path.
A BITE sequence consists of a positive, negative and zero stimulus. The sensor automatically evaluates the BITE sequence by comparing the current result to sensor specific BITE new part values (i.e. as measured in RB end of line testing). If a sequence is finished without a positive result, it will be repeated by default up to 2 times (i.e. in total 3 BITE counts). The maximum number of BITE counts can be soft configured. If the BITE fails in all BITE counts, the corresponding failure flags and "CS" bits are set (permanently and immediately).

After BITE is switched off, the sensor waits for the filters to be flushed and will not provide valid data earlier than the programmed filter flush time. This filter flush time can be set by soft configuration according to the selected LF filter type. The result of the self-test can be read out.

Please note: The sensor signal might be incorrect, if the flush time is set to value shorter than the default time for the filter type!

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The BITE routine is executed by either one of the following methods:

A. Automatically started sequence of positive and negative test during initialization, directly after power-up. See chapter 7.1.1.8 for details on configuring the BITE.

B. A test sequence triggered by SPI command at any time, after start-up.

8.1.5 Logic built in self-test (LBIST)

The logic built in self-test (LBIST) checks the ASIC functionality at each start-up of the sensor. The result of the self-test can be seen in the status bit. In case the self-test fails, the channel status bit "CS" of all output channels is set to 1 = "sensor data not valid"

8.1.6 ACC-Sum-C-test

The principle of the ACC-Sum-C test is as follows: the difference and the sum of both capacitances of an acceleration sensor are determined and are compared to part individual stored trimming values. The following parameters are evaluated with this test:

- Change in ACC parasitic capacitance (i.e. broken MEMS fingers / particles are detectable)
- Leakage between ACC bonds and bond pads (i.e. contamination is detectable)

8.1.7 SPI Communication

The sensor module checks the SPI communication for specific errors:

On physical level the polarity, a sufficient transfer delay time between two frames and a correct number of SPI clock pulses (32) is verified.

On logical level, the validity of the commands and the CRC checksums are evaluated.

See also chapter 6 for error handling of the SPI protocols.

The sensor cannot respond to signal transfer delay times (STD) shorter than defined. For example, in case a reset is triggered, the SMI8 will not accept/ recognize any SPI commands before a time span of 50ms has elapsed. If SPI communication is forced before the specified start-up timing, sensor module response might be invalid. The sequential transfer delay time may differ from the specification.

8.1.8 Voltage Checks

After start-up (and SPI is functional) the supply voltage is monitored. If the sensor is operated outside its specified voltage range due to over- or under voltage, it leads to an error condition (flag) and the sensor signal specification can no longer be guaranteed. The sensor module is fully functional until an over/ under -voltage-detection-flag is set. The upper detection limit for VB can be modified by soft-configuration (chapter 7.1.1.7).
If under voltage is detected, the sensor is reset until the voltage returns back to the operating range. The under voltage detection has a hysteresis to ensure, that the sensor cannot be trapped in a reset loop.

8.2 Safety Documentation

See the "SMI8xy Safety Element out of Context" for all relevant information on application of SMI8xy sensor modules in safety relevant applications.

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9 Functional and Lifetime Qualification Test plan

The sensor modules are tested to the following qualification plan in accordance to AEC-Q100.

Test item	Parameter	
Preconditioning, soldering simulation lead-free, class small devices	MSL3	
High temperature HTOL 125°C	1000	duration [h]
High temperature HTSL 150°C	1000	duration [h]
Temperature cycles TC -50°C/150°C; dwell time: 10 min; transition time: 10 sec	1000	cycles
Humidity THB 85°C/85%rH	1000	duration [h]
Humidity uHAST 130°C/ 85%rH	96	duration [h]
Drop test; +-x, +-y, +-z, 9 DUTs; 3 DUTs per axis, 2 Falls per DUT; Impact on concrete	120	height [cm]
ESD, MM (Machine model)	200	Voltage [V]
ESD, HBM (Human body model)	2000	Voltage [V]
ESD, CDM (Charge device model) all pins @ 500V; corner pins @ 750V	750	Voltage [V]
Latch up test		
Gate leakage test according to AEC-Q100-006		
Vibration Resistance condition A MIL-STD883 method 2005 +-20g->196,2m/s², 60Hz, xyz-axis, 3x 32h (96h in total), RT, no operation, sine-sweep fixed		
Vibration Resistance condition 1 JESD 22-B103 20-2000Hz,crossover frequency 80Hz, 1decade/min, log (2min/sweep) sweep direction upward 2min/ downward 2min, 20g->196,2m/s² xyz-axis, 3x 16min (48min in total), RT, no operation, sine-sweep sliding		
Impact test 20000m/s^2 (2000G), width: 1ms, x,y,z 3axis (3times each), RT, not operating		
Wire bond pull and shear test		
Solder ball shear test		

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10 Disclaimer

10.1 Safety and warning notes

In order to ensure proper functionality during operation, it is the responsibility of the customer to evaluate:
• The proper function of the sensor in the overall system (e.g. see section 5.2).
• The mechanical stability of each system design including the sensor (e.g. see section 3.6).
• The electrical stability, e. g. power supply and EMC, of each system design including the sensor (e.g. see section 5.1).

The sensor / semiconductor complies with all statutory regulations regarding restriction of hazardous substances and recyclability which are in the scope of IMDS, insofar as such restrictions of hazardous substances and recyclability are regarded, the target market of the sensor is worldwide.

If other or additional regulations are required for marketing the product or marketing is effected outside the named target markets, the customer requests compliance with the specific regulations of the target market from Bosch, or ensures these by itself. In the IMDS (International Material Data System), all materials present in the component are collected, maintained, analyzed and archived.

Repair and manual soldering of the sensor is not permitted.

Sensors with visible damages (housing, connectors, pins, etc.) and sensors which might have exceeded the absolute maximum ratings (e.g. see section 4.1) must not be mounted in the vehicle. These sensors must be scrapped.

Returned products are considered good if they fulfil the specifications / test data for 0-mileage and field listed in this specification.

Data security: The sensor only contains the explicitly stated characteristics for product, data and information security. It is the responsibility of the system integrator to verify and validate on system level, if the stated characteristics comply with and fulfil the requirements of the product.

10.2 ISO26262

Bosch points out that the ASIL-classified requirements (in the sense of ISO 26262), their implementation and the assumptions made for this purpose are documented in the document SEooC (safety element out of context).

It is the customer’s responsibility that these requirements, their implementation and the assumptions made for this purpose are valid for the application within the customer’s system.

The customer must ensure that the Bosch scope of delivery complies with the requirements for functional safety within the overall system.

10.3 Considerations regarding electrical and mechanical robustness

Due to the measurement principle, the sensor is sensitive to mechanical disturbances, such as shocks, vibrations or stress. Therefore, the printed circuit board (PCB) has to be designed in such a way, as to suppress any of these influences and ensure the proper functionality in each application. The following sections describe the different influences that might be relevant in the application.

The sensor elements have to be protected against extreme shock loads such as e.g. hammer blows on or next to the sensor elements, vibrations of a power wrench when fixing bolts, dropping of the sensor elements onto hard surfaces, etc. (e.g. see section 4.1). We recommend the avoidance of g-forces beyond the maximum rating during transport, handling and mounting of the sensors resulting in a defined and qualified installation process. As the sensor is sensitive to mechanical stress, any bending or torsion of the

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PCB close to the sensor, e.g during forcing in, has to be avoided (e.g. see section 3.6). The sensors must not be handled as bulk good.

As a consequence of the drive oscillation of the rate sensing element, the SMI8 may induce oscillation energy into the PCB. Therefore, if more than one SMI8 are mounted on the same PCB it is important, that any mechanical interference between the two sensors is suppressed by the design of the PCB itself and the mechanical connection between the sensors and the PCB. Failing to do this, the sensors can exhibit an increased noise level of the rate signal.

Due to the sensing principle, the SMI8 is sensitive to disturbances at its resonance frequencies (~23 kHz to ~27 kHz). Therefore, any resonances of the PCB in the critical frequency range must be avoided. In addition to that the mechanical connection of the sensor to the PCB should be designed in a way that the sensor package does not amplify any disturbances induced by the PCB at critical frequencies (~23 kHz to ~27 kHz; >45 kHz). If this is not done carefully, the sensor may show rate offset variations over temperature, which might result in an offset out of specification.

The SMI8 in principle is suitable for conformal coating. MEMS sensors, however, are sensitive to mechanical stress. Please note that any measure on application level that alters the mechanical connection between the sensor and the PCB such as for example dip or spray or partial coating might potentially affect the sensor performance (e.g. shift of the resonance frequencies) and board level reliability and therefore, have to be chosen with care by and in responsibility of the customer. It is the responsibility of the customer to ensure the proper application of the product in the vehicle.

10.4 Vibrational Sensitivity

Note that any measures to alter the mechanical connection between the sensor and the PCB are application specific and therefore have to be evaluated and qualified by the customer. Robert Bosch does not take any responsibility for the implementation of any of those options in the customer specific application.

In any case, the mechanical stability of each system design including the SMI800/810/860 and SMG810 must be evaluated by the customer in advance to guarantee proper functionality during operation.

10.5 Electrical Considerations

The sensors are sensitive to electrical disturbances. Any disturbances on the supply voltage must be avoided. Especially frequency contents in the power supply at the resonance frequency of the sensing element can be critical. A decent filter strategy must be applied if a stable power supply cannot be guaranteed (e.g. see section 5.1).

In any case, the electrical stability (power supply and EMC, e.g. see section 5.1) of each system design, including the SMI8, must be evaluated by the customer in advance to guarantee proper functionality during operation.

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11 Changes

Revision	Chapter	Change description	Responsible
2.0	7.2.4	ACC-Sum-C test: forbidden usage after offset cancellation	Barra (AE/PAS1.2)
	1	Re-worked according to new Bosch guideline	Barra (AE/PAS1.2)
	8.3	Configuration number: added C2 and production	Barra (AE/PAS1.2)
	10.2.4	Cross-axis overload for SMI860 added	Barra (AE/PAS1.2)
	3.1	Refer to offer drawing as a separate document	Barra (AE/PAS1.2)
	2.2.1	Added chapter: monitoring during operation	Barra (AE/PAS1.2)
	3.4	Pinning / Electrical pins specification – restructured	Barra (AE/PAS1.2)
	6	Renamed: Software interface description	Barra (AE/PAS1.2)
	7	Error flag description moved to chapter 8	Barra (AE/PAS1.2)
	8	Overload chapter moved to chapter 7: application details	Barra (AE/PAS1.2)
	8	Re-structured	Barra (AE/PAS1.2)
	2.2	Details about safety concept information moved to chapter 8	Barra (AE/PAS1.2)
	10	Disclaimer added	Barra (AE/PAS1.2)
	3.3	Labeling info updated	Barra (AE/PAS1.2)
	12	Updated	Barra (AE/PAS1.2)
	5.1	VB monitor tolerance narrowed	Barra (AE/PAS1.2)
	7.1.3	Added comment, that BITE triggers clusterflags	Barra (AE/PAS1.2)
	5.2.1	Spec for gyro resonance corrected	Barra (AE/PAS1.2)
	5.3.2	Added stop band gain at f>500Hz for ACC	Barra (AE/PAS1.2)
	3.5	Reflow soldering profile corrected	Barra (AE/PAS1.2)
	2.3	Soft configuration B: more general description for self tests	Barra (AE/PAS1.2)
	6.4.2.3	Page 4 adr register 0xD unused	Barra (AE/PAS1.2)
	6.4.1.3	Register 0x4D unused	Barra (AE/PAS1.2)
	8.1.1	Explanation of F16_ST_RUN and F16_INIT	Barra (AE/PAS1.2)
	3.2	Tape and reel specification updated	Barra (AE/PAS1.2)
	7.1	Clarification of MOSI/MISO frame for configuration registers	Barra (AE/PAS1.2)
	3.4.2	Figure of application circuit clarified	Barra (AE/PAS1.2)
	3.4.2	Capacitance tolerances added	Barra (AE/PAS1.2)
	5.2.3	Measurement range ACC HF Z-channel: max 35g	Barra (AE/PAS1.2)
	5.2.3	Nonlinearity HF 8g range reduced to 30mg	Barra (AE/PAS1.2)
	5.2.2	Nonlinearity LF 8g range reduced to 30mg	Barra (AE/PAS1.2)
	5.2.2	Nonlinearity LF 6g range removed. Covered by 8g range	Barra (AE/PAS1.2)
	5.2.2	Microlinearity extended to 8g range	Barra (AE/PAS1.2)
	3.6	Recommendation for PCB layout – structured, figure added	Barra (AE/PAS1.2)
	3.5.1	Rework chapter added	Barra (AE/PAS1.2)
	5.4	Start-up diagram updated, more details	Barra (AE/PAS1.2)
	10.2	Added reference to document “SEooC”	Barra (AE/PAS1.2)
	7.1.3.2	BITE description in more detail	Barra (AE/PAS1.2)
	2.4	Chapter removed. Voltage detection info merged with 8.1.8	Barra (AE/PAS1.2)
	8.1.8	Updated description due to move of chapter 2.4	Barra (AE/PAS1.2)
	7.4	Overload: more precise description of CS bit behavior	Barra (AE/PAS1.2)
	5.2.1, 5.2.2	Offset power on gradient removed because already covered by offset power on span and 20s interval	Barra (AE/PAS1.2)
	3.6	Added info about checking the strain level	Barra (AE/PAS1.2)
	6.4.1.3, 6.4.2.3	Added registers for QUAD1/2_FINE_DAC	Barra (AE/PAS1.2)
	9	Updated	Barra (AE/PAS1.2)
	5.2.3	Sensitivity error: valid for range +/-8g	Barra (AE/PAS1.2)
2.1	5.4	Added the waiting time for setting EOC bit	Barra (AE/PAS1.2)
	5.2.1	Internal headroom - Added remark for bypassed error counters	Barra (AE/PAS1.2)
	7.2	Corrected: …each single sensor module has a unique ~~SMI~~ serial number…..	Barra (AE/PAS1.2)

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Revision	Chapter	Change description	Responsible
	2.1.4	Added info about ASIC names	Barra (AE/PAS1.2)
2.2	1.2	Added sentence ".. as well as all applications not released by Bosch."	Barra (AE/PAS1.2)
	4.3	Added more precise definition of lifetime specification above and within first table	Barra (AE/PAS1.2)
	4.1	Additional sentence "A proper ESD environment during handling and processing of the sensor has to be in place." Reference to section 10.1 added.	Barra (AE/PAS1.2)
	5.2.3	More details on part individual measurement range HF channel added.	Barra (AE/PAS1.2)
	5.2.3	Digital output range corrected to ±18250	Barra (AE/PAS1.2)
	10.1	Added explanation of IMDS	Barra (AE/PAS1.2)
	10.1	Added references to the respective sections	Barra (AE/PAS1.2
	10.2	Added "valid for the application within the customer's system"	Barra (AE/PAS1.2)
	10.3	Added references to the respective sections	Barra (AE/PAS1.2)
	10.5	Added reference to the respective sections	Barra (AE/PAS1.2)
	Coversheet, 1	Bosch part numbers moved from chapter 1 to coversheet	Barra (AE/PAS1.2)
	3.1	Reference to section 3.3 added for details on Bosch offer drawing document numbers	Barra (AE/PAS1.2)
	3.3	Bosch offer drawing document numbers added	Barra (AE/PAS1.2)
	Coversheet	SMI860 8g part number added	Haller (AE/PAS1.2)

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12 Terms and Definitions

1g 9.81 m/s^2 (earth gravity acceleration)

AB Airbag (Standard airbag ECU with front, side, roll over crash detection)

ABplus Airbag ECU containing addition sensors for other application (ESP, damper control, automatic front steering). Sensor data is provided to other ECUs via the vehicle bus.

AGC **A**utomatic **G**ain **C**ontrol

DLL **D**ynamic **L**ink **L**ibrary

FIR **F**inite **I**mpulse **R**esponse

SafeSPI Serial Peripheral Interface for Automotive Safety. Open standard based on the de-facto Serial Peripheral Interface (SPI) industry standard (please refer to http://www.safespi.org/)

System within the context of this specification, a system is the system understood as a master responsible for gathering sensor data, evaluating those data for validity and controlling the state of the sensor by any of the available communication interface (e.g. final test equipment, ESC or AB ECU, etc.)

SMI **S**ensor **M**icromechanic **I**nertial

SMI8xx is the acronym used for any sensor of the SMI8 Generation with any of the specified sensing axes, interfaces, temperature ranges etc. (**S**ensor **M**icromechanic **I**nertial **8**th Generation)

RMS **R**oot **M**ean **S**quare
The RMS (Root Mean Square) value is calculated as follows:
First take the deviation to the mean value of each value, then calculate the square of these values, finally calculate the mean of these results and take the square root (standard deviation).

$$RMS = s_{(x)} = \sqrt{\frac{1}{N} \cdot \sum_{i=1}^{N} (x_i - \bar{x})^2}$$

if **i**n **f**rame SPI communication protocol

oof **o**ut **o**f **f**rame SPI communication protocol

os **o**ffset **s**table

SCON **S**afety **c**ontroller

SOC **S**low **o**ffset **c**ompensation

TCO **T**emperature **c**ompensation **o**ffset

RVS **R**equired limits for sensor **v**ibration **s**ensitivity

3 DOF 3 degrees of freedom

VDD_DIG power supply digital

VDD_YRS power supply angular rate analog

VB main power supply

VDD_IO power supply SPI communication

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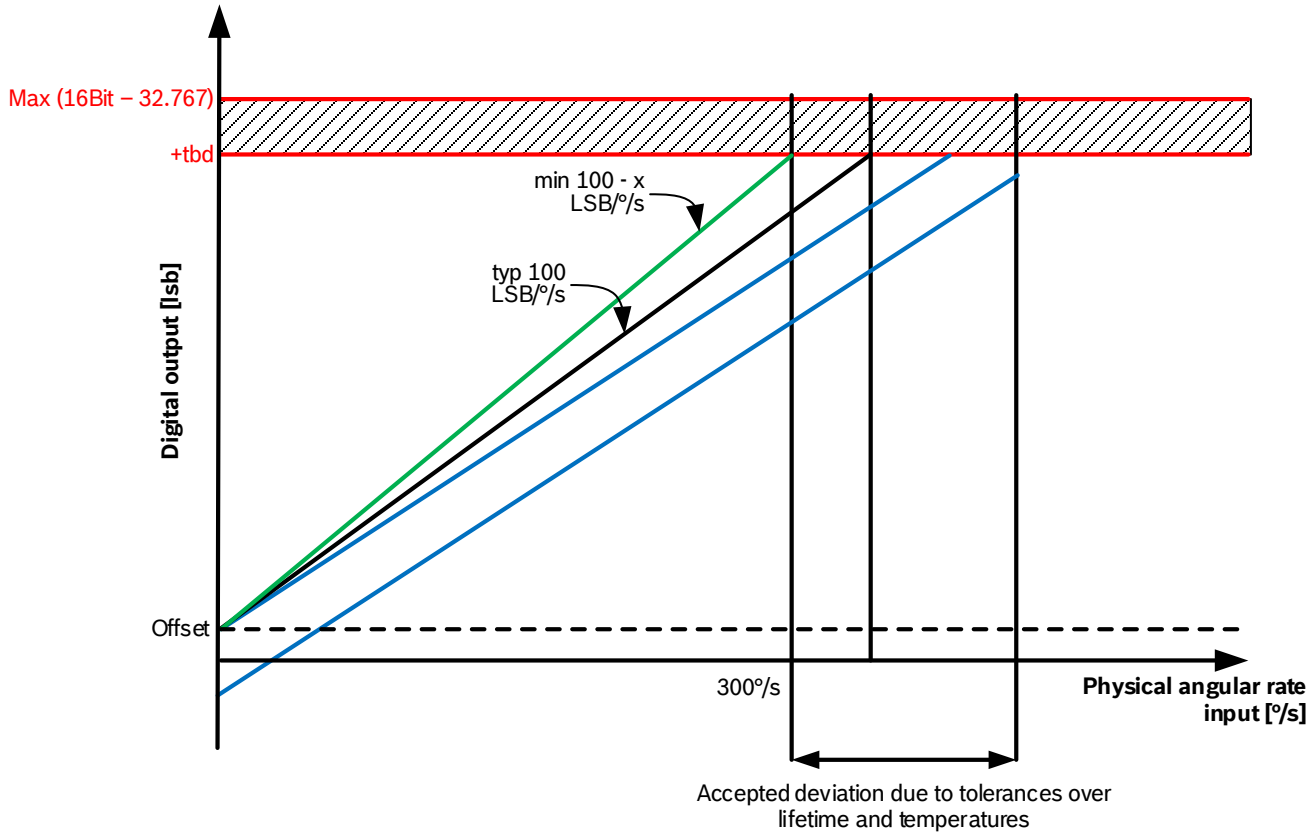

Figure 26 Measurement range definition

(Note: Definition for first quadrant shown. This definition also applies analogue to the third quadrant)

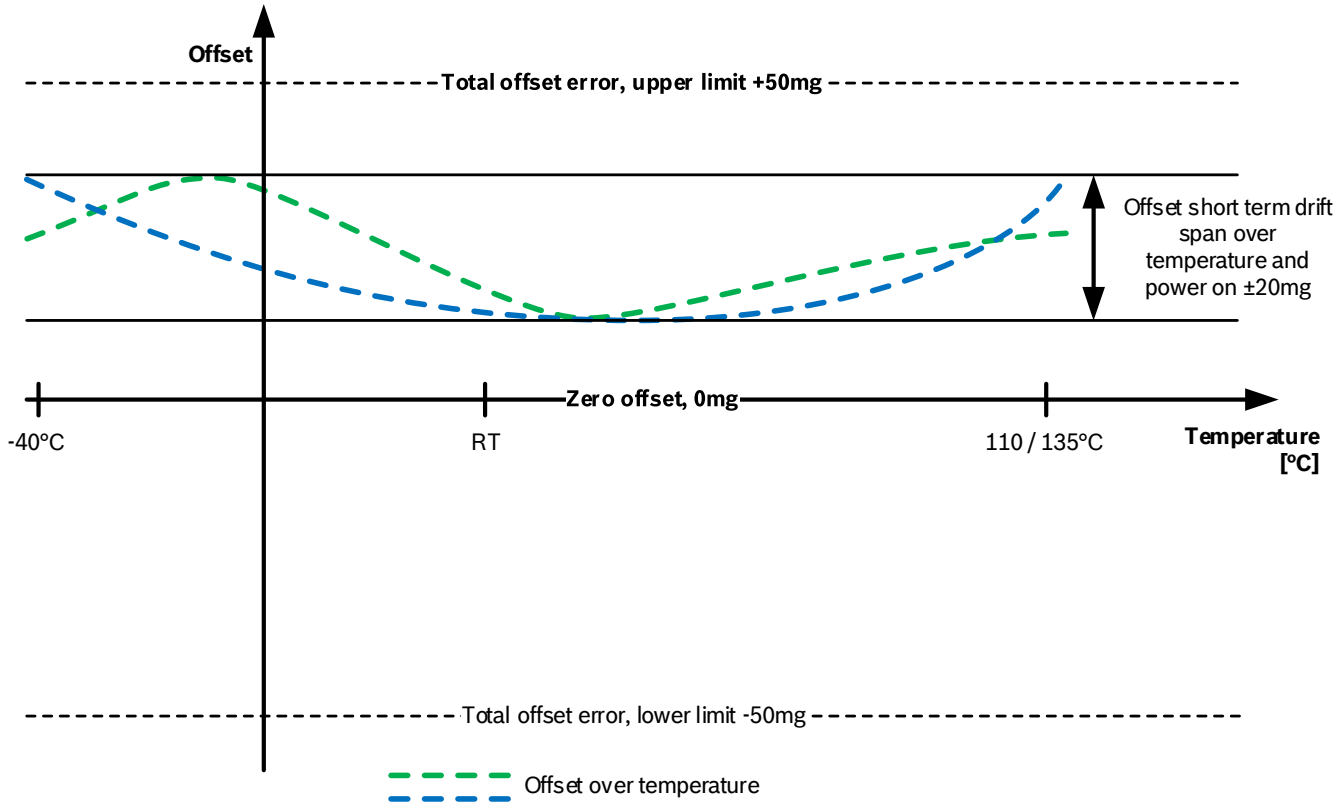

Figure 27 Definition of offset error

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13 Table of Figures

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