Digital
System
Design

Project

Mu0 processor

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Introduction

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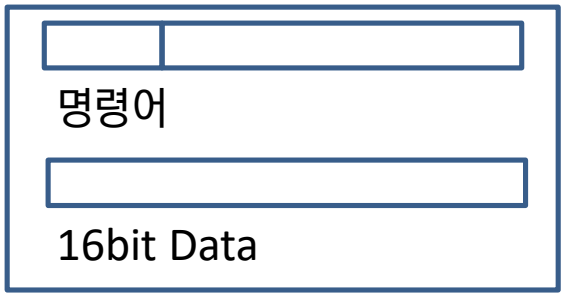
02 기존 Mu0 Processor

MU0의 기본 동작

기존 Mu0 Processor

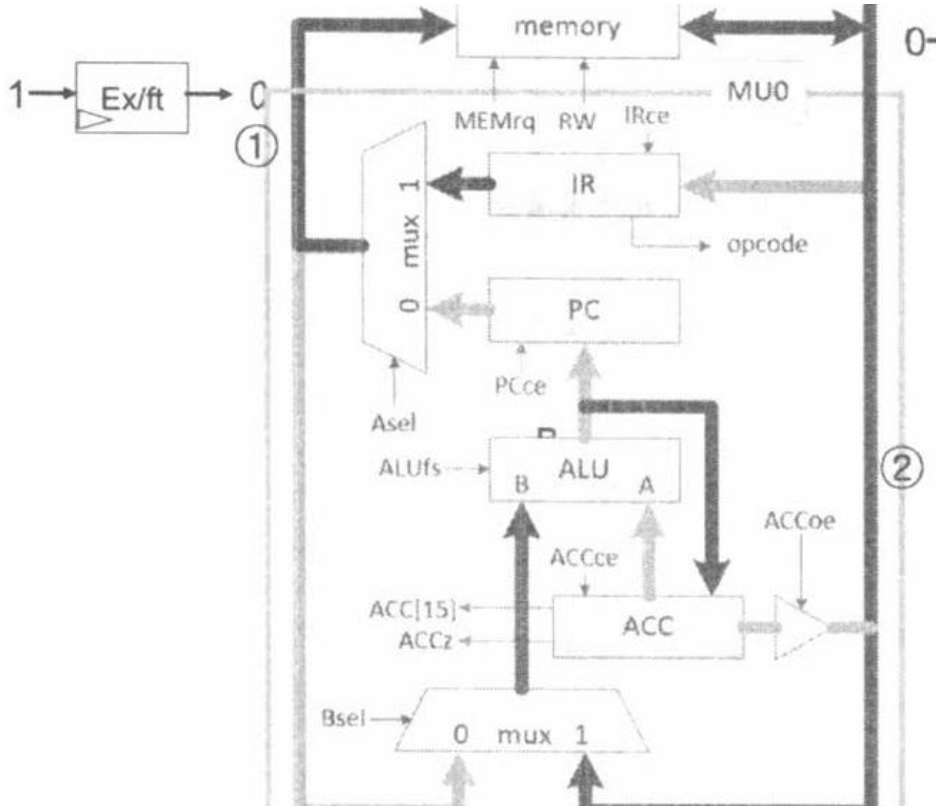
메모리



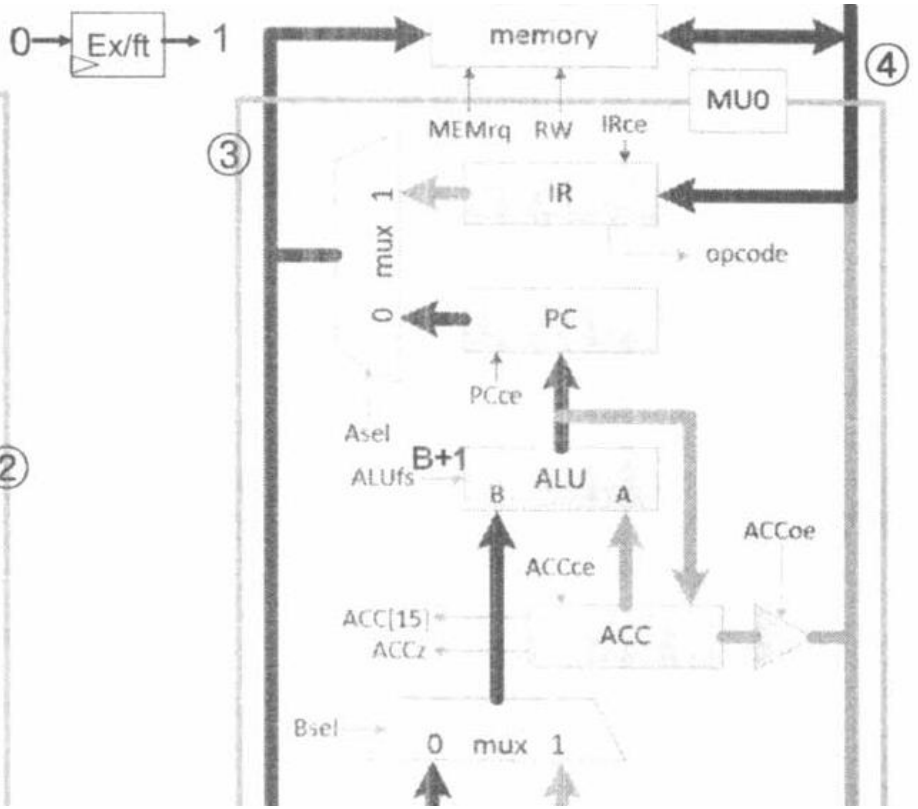
INOUT BUS

주소 BUS

DATA BUS



EX 실행

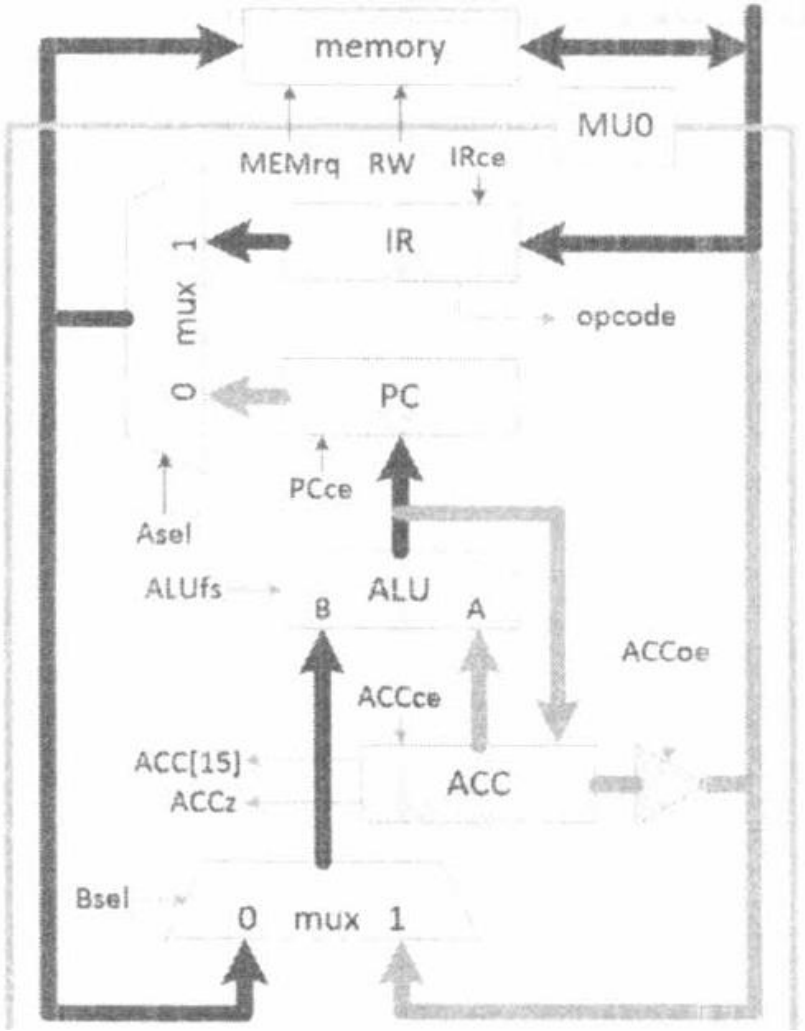


FT 다음 명령어 준비

기존 Mu0 Processor

- JMP(0100) data flow

EX 실행



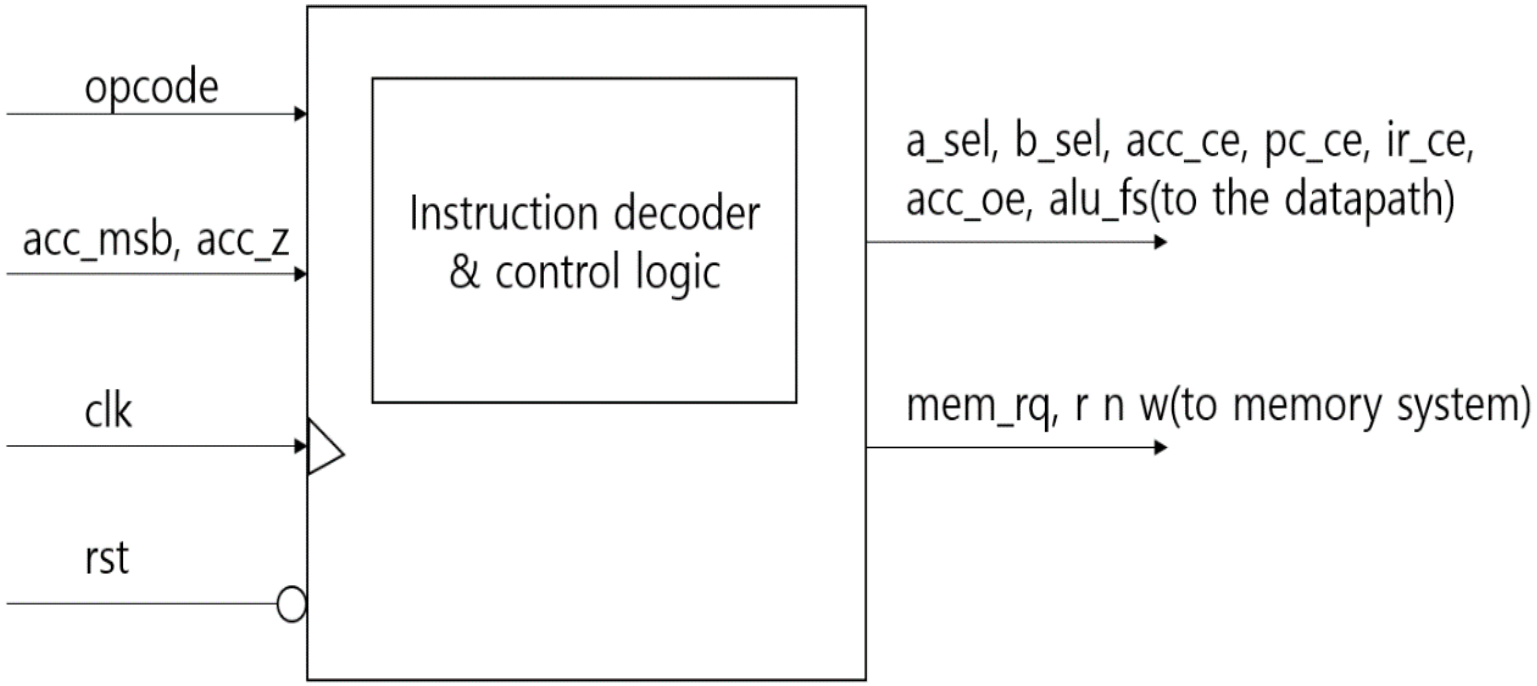
기존 Mu0 Processor

- Control logic

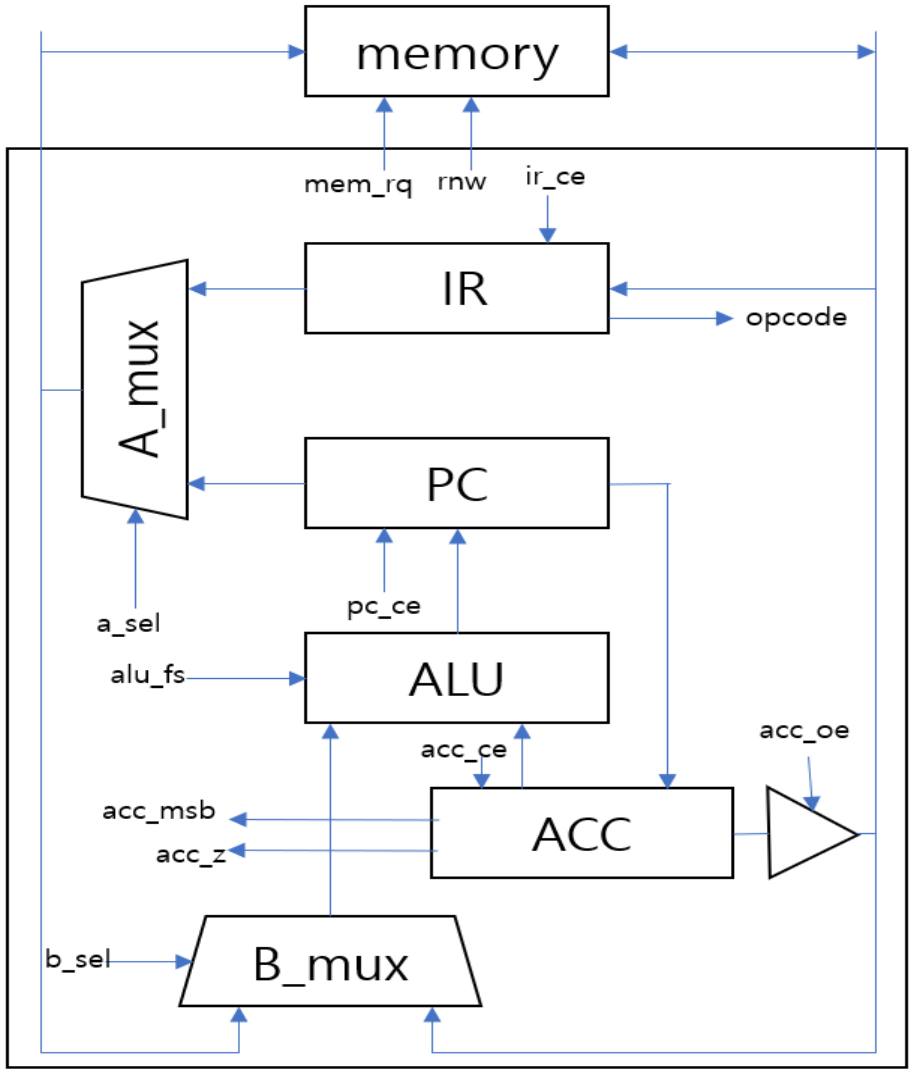
Inputs						Outputs									
	Opcode		Ex/ft	ACC15			Bsel		PCce	ACCoe		MEMrq	Ex/ft		
Instruction		Reset		ACCz		Asel		ACCce		IRce		ALUfs		RnW	
Reset	xxxx	1	x	x	x	0	0	1	1	1	0	=0	1	1	0
LDA S	0000	0	0	x	x	1	1	1	0	0	0	=B	1	1	1
	0000	0	1	x	x	0	0	0	1	1	0	B+1	1	1	0
STO S	0001	0	0	x	x	1	x	0	0	0	1	x	1	0	1
	0001	0	1	x	x	0	0	0	1	1	0	B+1	1	1	0
ADD S	0010	0	0	x	x	1	1	1	0	0	0	A+B	1	1	1
	0010	0	1	x	x	0	0	0	1	1	0	B+1	1	1	0
SUB S	0011	0	0	x	x	1	1	1	0	0	0	A-B	1	1	1
	0011	0	1	x	x	0	0	0	1	1	0	B+1	1	1	0
JMP S	0100	0	x	x	x	1	0	0	1	1	0	B+1	1	1	0
JGE S	0101	0	x	x	0	1	0	0	1	1	0	B+1	1	1	0
	0101	0	x	x	1	0	0	0	1	1	0	B+1	1	1	0
JNE S	0110	0	x	0	x	1	0	0	1	1	0	B+1	1	1	0
	0110	0	x	1	x	0	0	0	1	1	0	B+1	1	1	0
STOP	0111	0	x	x	x	1	x	0	0	0	0	x	0	1	0

block diagram - FSM

기존 Mu0 Processor

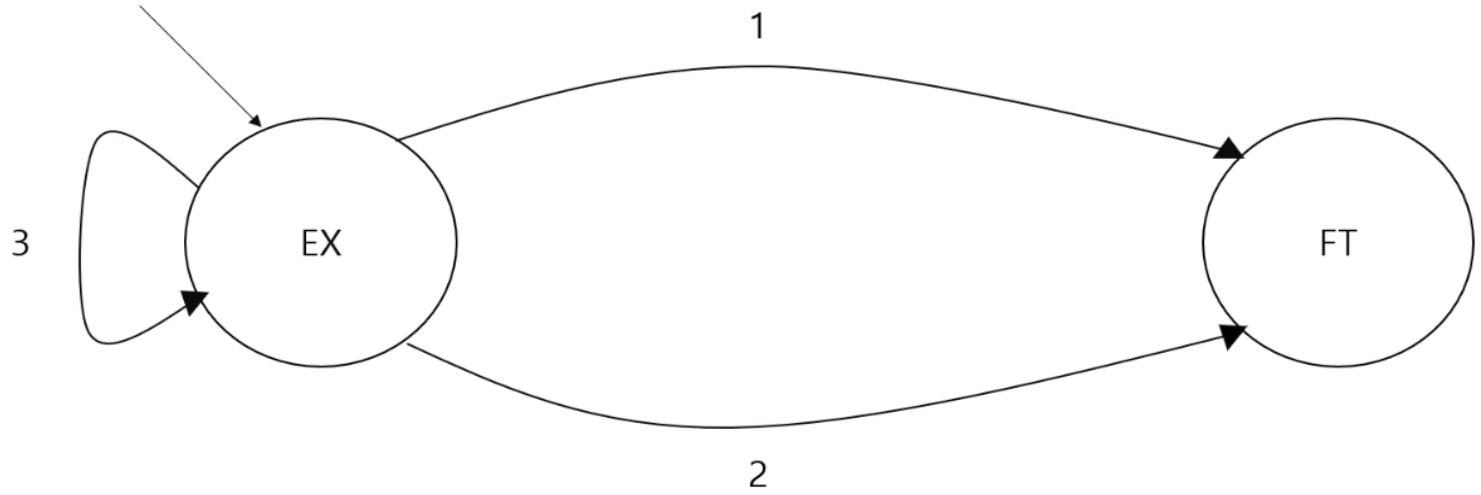


block diagram - Data Path 기존 Mu0 Processor



기존 Mu0 Processor

Input: opcode, acc_z, acc_msb
Output: a_sel, b_sel, acc_ce, pc_ce, ir_ce, acc_oe, alu_fs, mem_rq, rnw



기존 Mu0 Processor

1. EX->FT

input				Output									
opcode	acc_z	acc_msb	comp_sn	a_sel	b_sel	acc_ce	pc_ce	ir_ce	acc_oe	alu_fs		mem_rq	rnw
0000(LDA)	x	x	x	1	1	1	0	0	0	011	B	1	1
0001(STO)	x	x	x	1	x	0	0	0	1	x	x	1	0
0010(ADD)	x	x	x	1	1	1	0	0	0	001	A+B	1	1
0011(SUB)	x	x	x	1	1	1	0	0	0	010	A-B	1	1

2. FT->EX

input				Output									
opcode	acc_z	acc_msb	comp_sn	a_sel	b_sel	acc_ce	pc_ce	ir_ce	acc_oe	alu_fs		mem_rq	rnw
0000(LDA)	x	x	x	0	0	0	1	1	0	100	B+1	1	1
0001(STO)	x	x	x	0	0	0	1	1	0	100	B+1	1	1
0010(ADD)	x	x	x	0	0	0	1	1	0	100	B+1	1	1
0011(SUB)	x	x	x	0	0	0	1	1	0	100	B+1	1	1

3. EX->EX

input				Output									
opcode	acc_z	acc_msb	comp_sn	a_sel	b_sel	acc_ce	pc_Ce	ir_Ce	acc_oe	alu_fs		mem_rq	rnw
0100(JMP)	x	x	x	1	0	0	1	1	0	100	B+1	1	1
0101(JGE)	x	0	x	1	0	0	1	1	0	100	B+1	1	1
0101(JGE)	x	1	x	0	0	0	1	1	0	100	B+1	1	1
0110(JNE)	0	x	x	1	0	0	1	1	0	100	B+1	1	1
0110(JNE)	1	x	x	0	0	0	1	1	0	100	B+1	1	1
0111(STP)	x	x	x	1	x	0	0	0	0	x	x	0	1

기존 Mu0 Processor

IR과 PC등의 reg를 처음에 reset해주지 않으면 처음 명령어를 가지고 오지 않는다. 따라서 실행 시 초반에 무조건 reset을 시켜야 한다.

↓

처음 상태는 무조건 EX가 된다.

↓

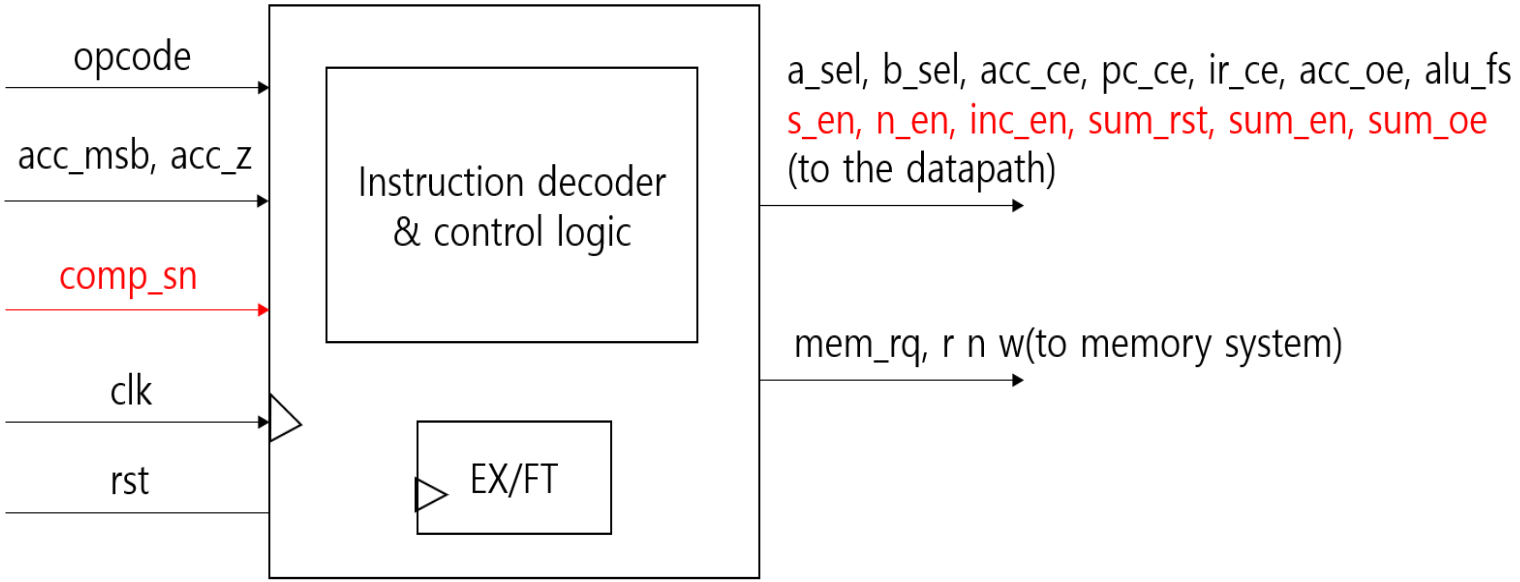
Ns상태를 EX/Ft 신호가 아니라 현재 state와 opcode로 결정하면 된다.
→ex/ft 신호 삭제

출력 값부분은 출력 개수 만큼의 always문으로 작성하지 않고
하나의 always문에 모든 출력 표시

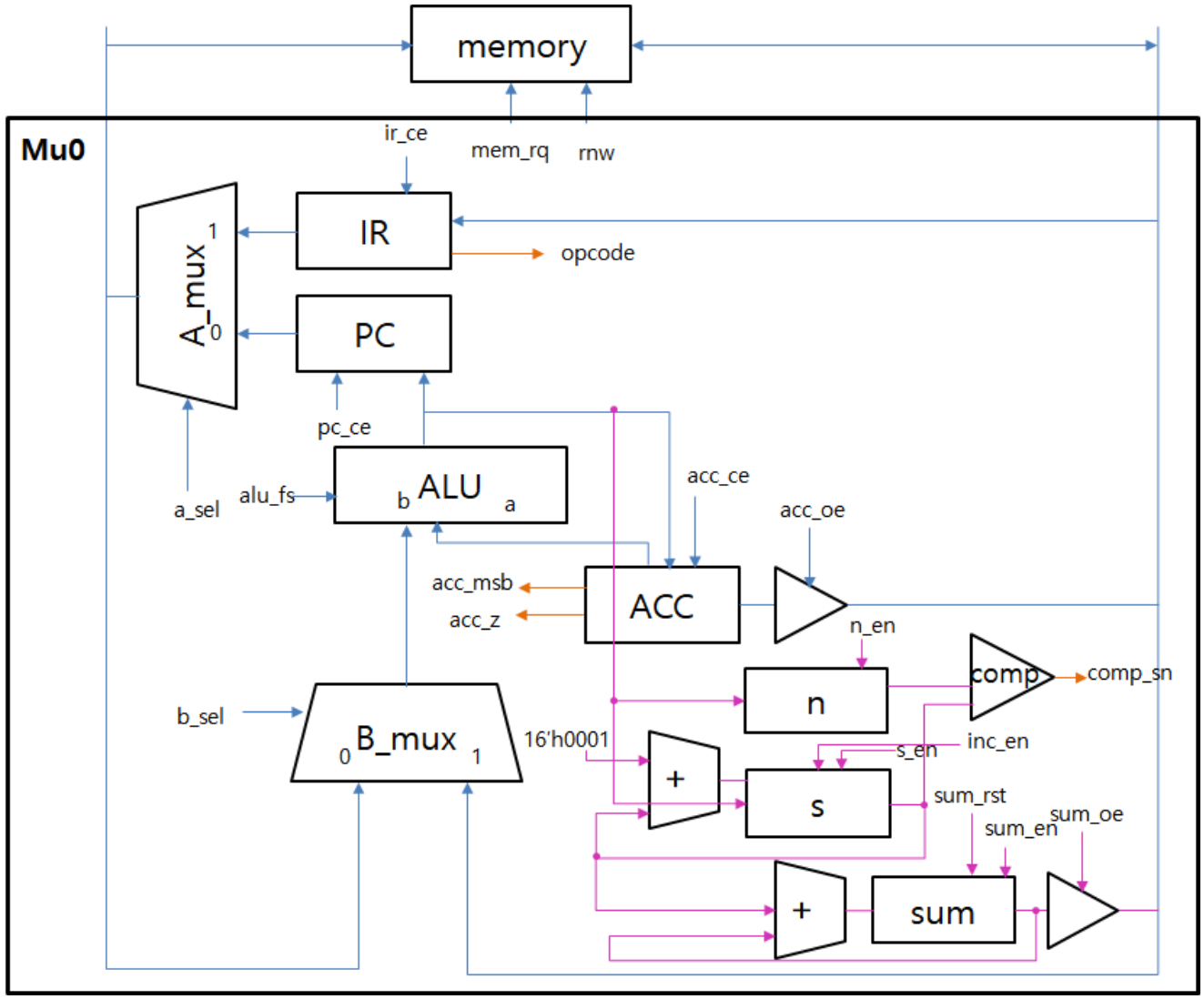
03 확장된 Mu0 Processor

block diagram - FSM

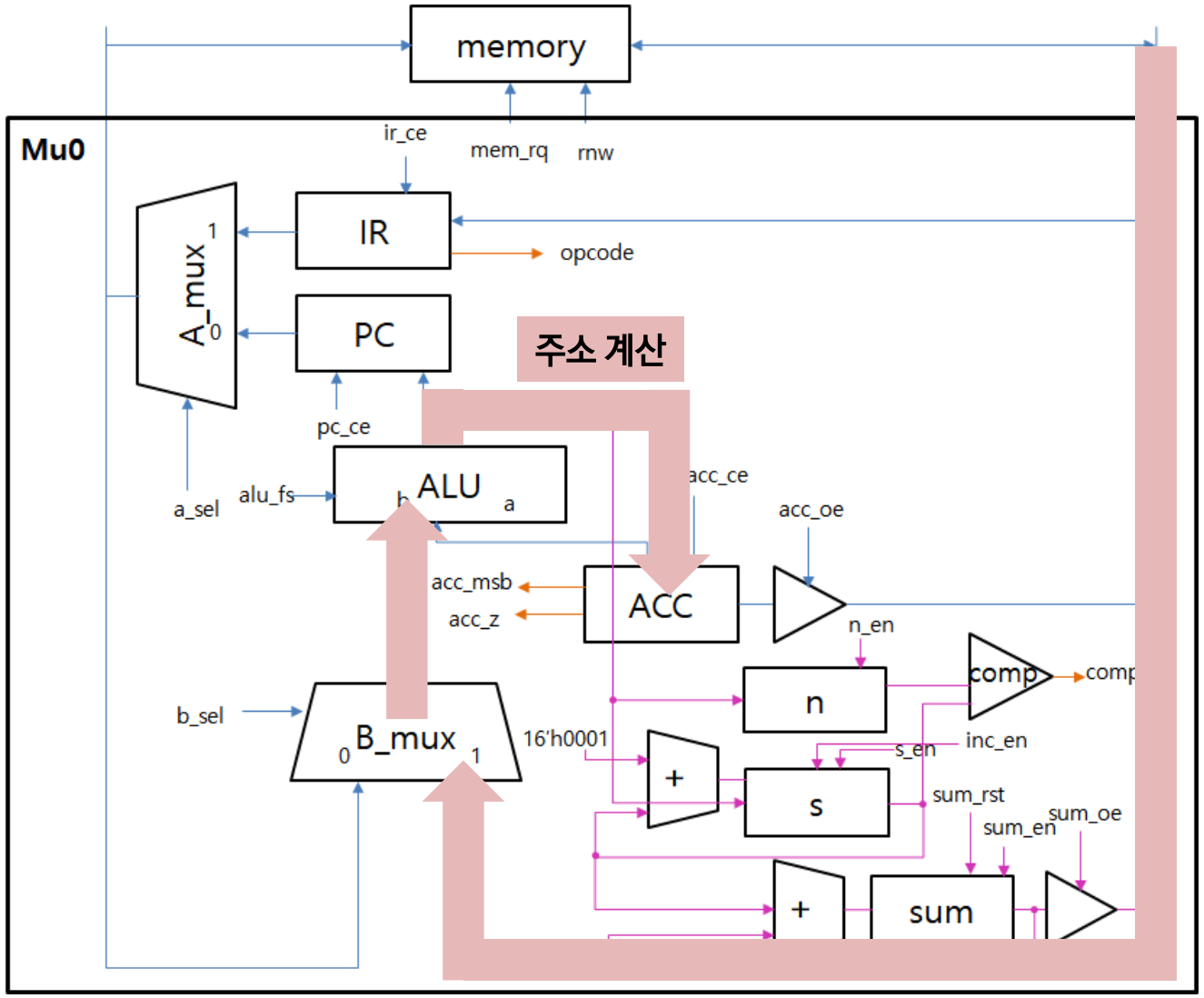
확장 Mu0 Processor



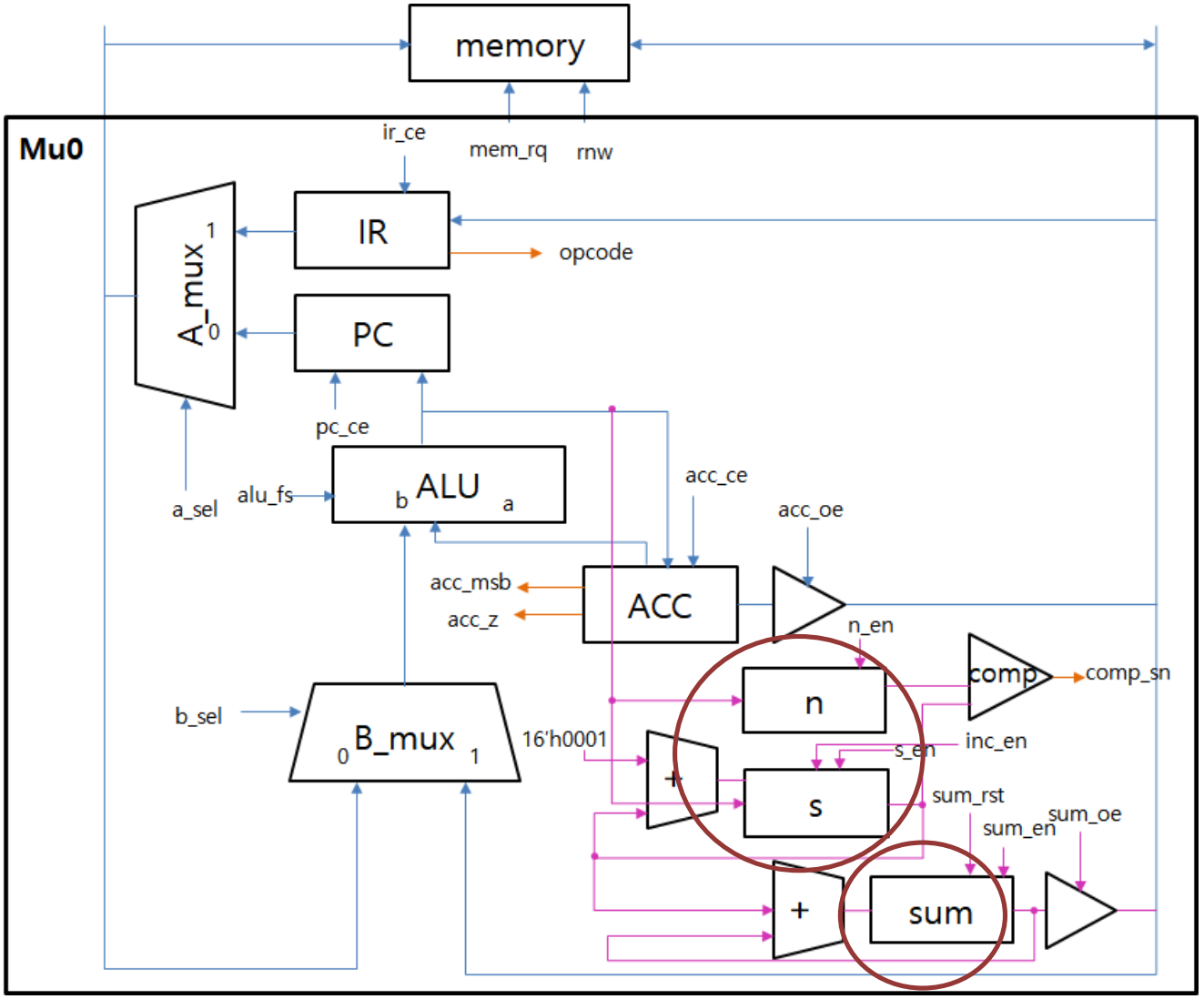
block diagram – Data Path 확장 Mu0 Processor



block diagram – Data Path 확장 Mu0 Processor

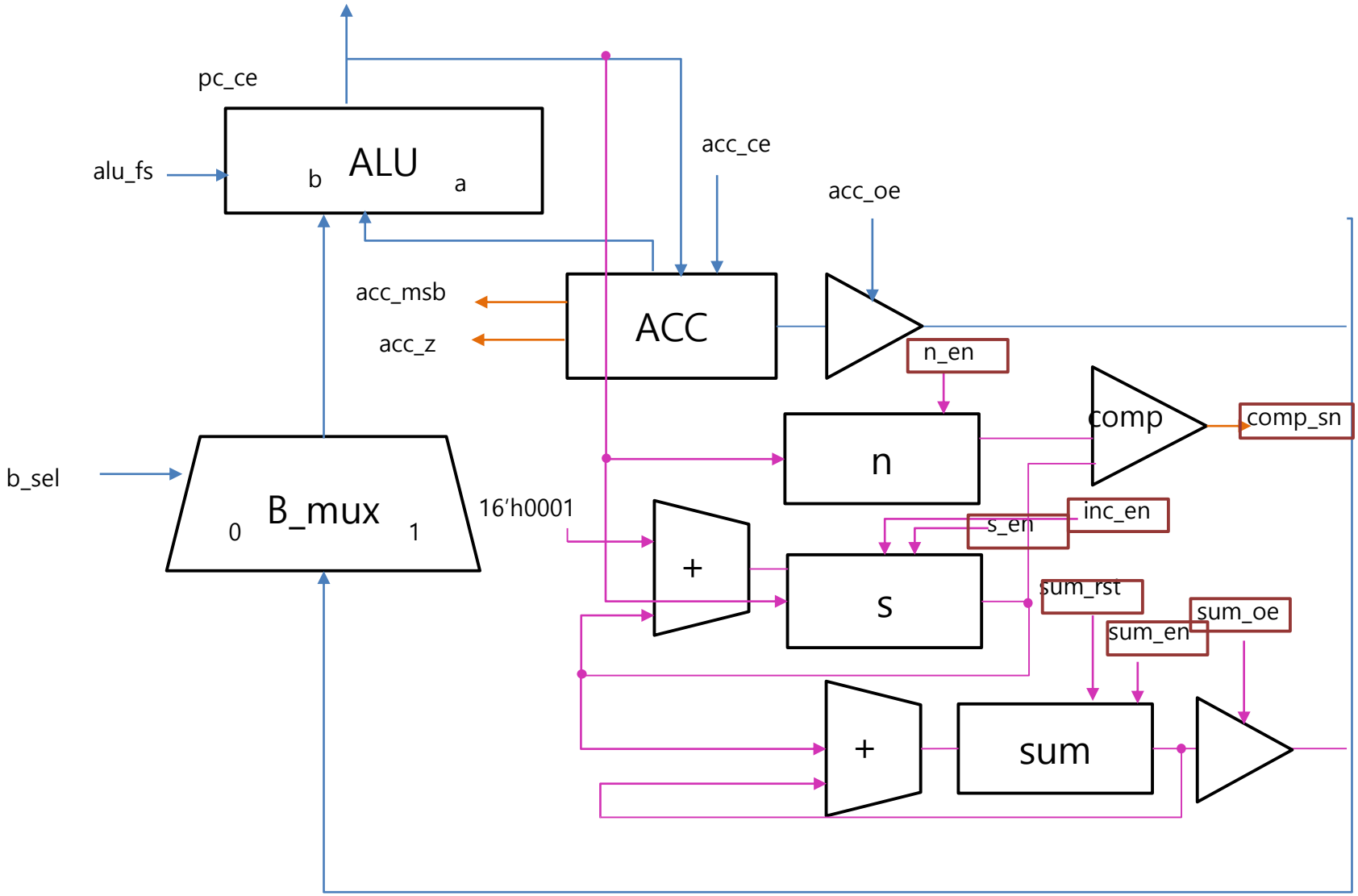


block diagram – Data Path 확장 Mu0 Processor



시그마 누적값

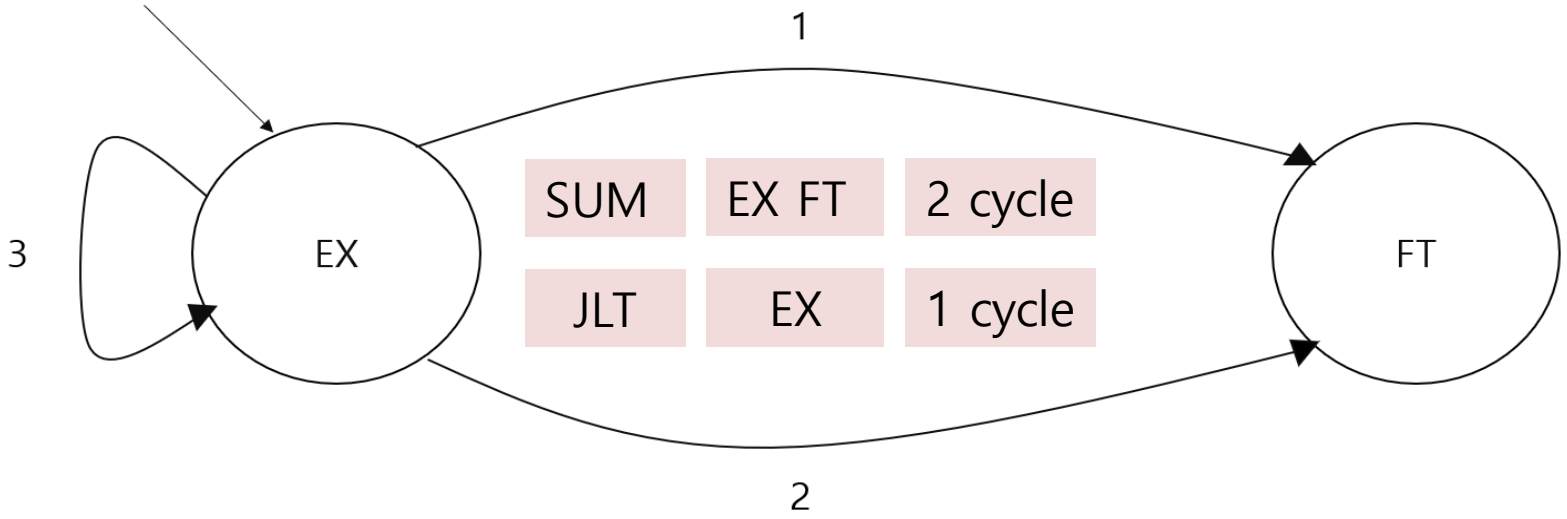
block diagram – Data Path 확장 Mu0 Processor



Instructions	opcode	Effect
LDSA S	1000	s:=mem[S], sum:=0
LDN S	1001	n:=mem[S]
SUM	1010	sum:=sum+s, s:=s+1 If s!=n pc:=S
JLT S	1011	If s!=n pc:=S
STS S	1100	mem[S]:=sum

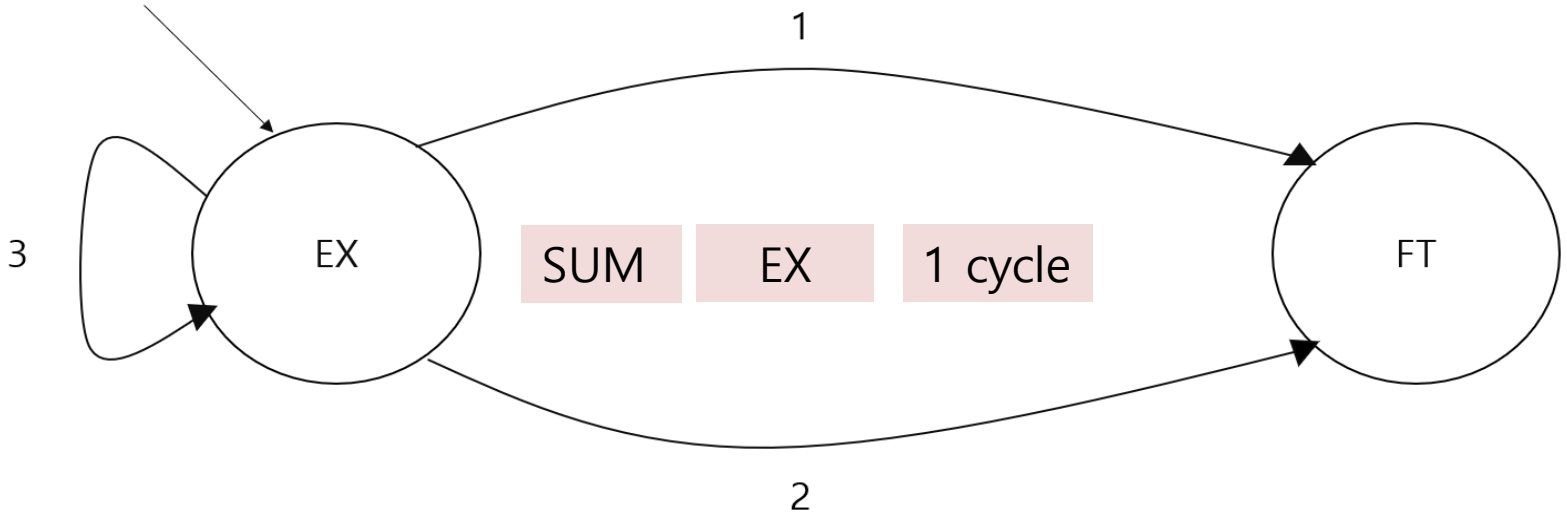
초반 설계 SUM+JLT 분리

Input: opcode, acc_z, acc_msb
Output: a_sel, b_sel, acc_ce, pc_ce, ir_ce, acc_oe, alu_fs, mem_rq, rnw
s_en, n_en, inc_en, sum_rst, sum_en, sum_oe



최종 설계 SUM+JLT 합쳐 SUM

Input: opcode, acc_z, acc_msb
Output: a_sel, b_sel, acc_ce, pc_ce, ir_ce, acc_oe, alu_fs, mem_rq, rnw
s_en, n_en, inc_en, sum_rst, sum_en, sum_oe



모든 명령어의 추가된 data path control signal

input				output					
opcode	acc_z	acc_ msb	comp_sn	s_en	n_en	inc_en	sum_rst	sum_en	sum_oe
0000(LDA)	x	x	x	0	0	0	0	0	0
0001(STO)	x	x	x	0	0	0	0	0	0
0010(ADD)	x	x	x	0	0	0	0	0	0
0011(SUB)	x	x	x	0	0	0	0	0	0
1000(LDSA)	x	x	x	1	0	0	1	0	0
1001(LDN)	x	x	x	0	1	0	0	0	0
1100(STS)	x	x	x	0	0	0	0	0	1

input				output					
opcode	acc_z	acc_ msb	comp_sn	s_en	n_en	inc_en	sum_rst	sum_en	sum_oe
0100(JMP)	x	x	x	0	0	0	0	0	0
0101(JGE)	x	0	x	0	0	0	0	0	0
0101(JGE)	x	1	x	0	0	0	0	0	0
0110(JNE)	0	x	x	0	0	0	0	0	0
0110(JNE)	1	x	x	0	0	0	0	0	0
0111(STOP)	x	x	x	0	0	0	0	0	0
1010(SUM)	x	x	1	0	0	0	0	0	0
1010(SUM)	x	x	0	0	0	1	0	1	0
1011(JLT)	x	x	1	0	0	0	0	0	0
1011(JLT)	x	x	0	0	0	0	0	0	0

추가된 명령어의 기존 data path control signal

input				Output									
opcode	acc_z	acc_msb	comp_sn	a_sel	b_sel	acc_ce	pc_Ce	ir_Ce	acc_oe	alu_fs		mem_rq	rnw
0100(JMP)	x	x	x	1	0	0	1	1	0	100	B+1	1	1
0101(JGE)	x	0	x	1	0	0	1	1	0	100	B+1	1	1
0101(JGE)	x	1	x	0	0	0	1	1	0	100	B+1	1	1
0110(JNE)	0	x	x	1	0	0	1	1	0	100	B+1	1	1
0110(JNE)	1	x	x	0	0	0	1	1	0	100	B+1	1	1
0111(STOP)	x	x	x	1	x	0	0	0	0	x	x	0	1
1010(SUM)	x	x	1	0	0	0	1	1	0	100	B+1	1	1
1010(SUM)	x	x	0	1	0	0	1	1	0	100	B+1	1	1
1011(JLT)	x	x	1	0	0	0	1	1	0	100	B+1	1	1
1011(JLT)	x	x	0	1	0	0	1	1	0	100	B+1	1	1

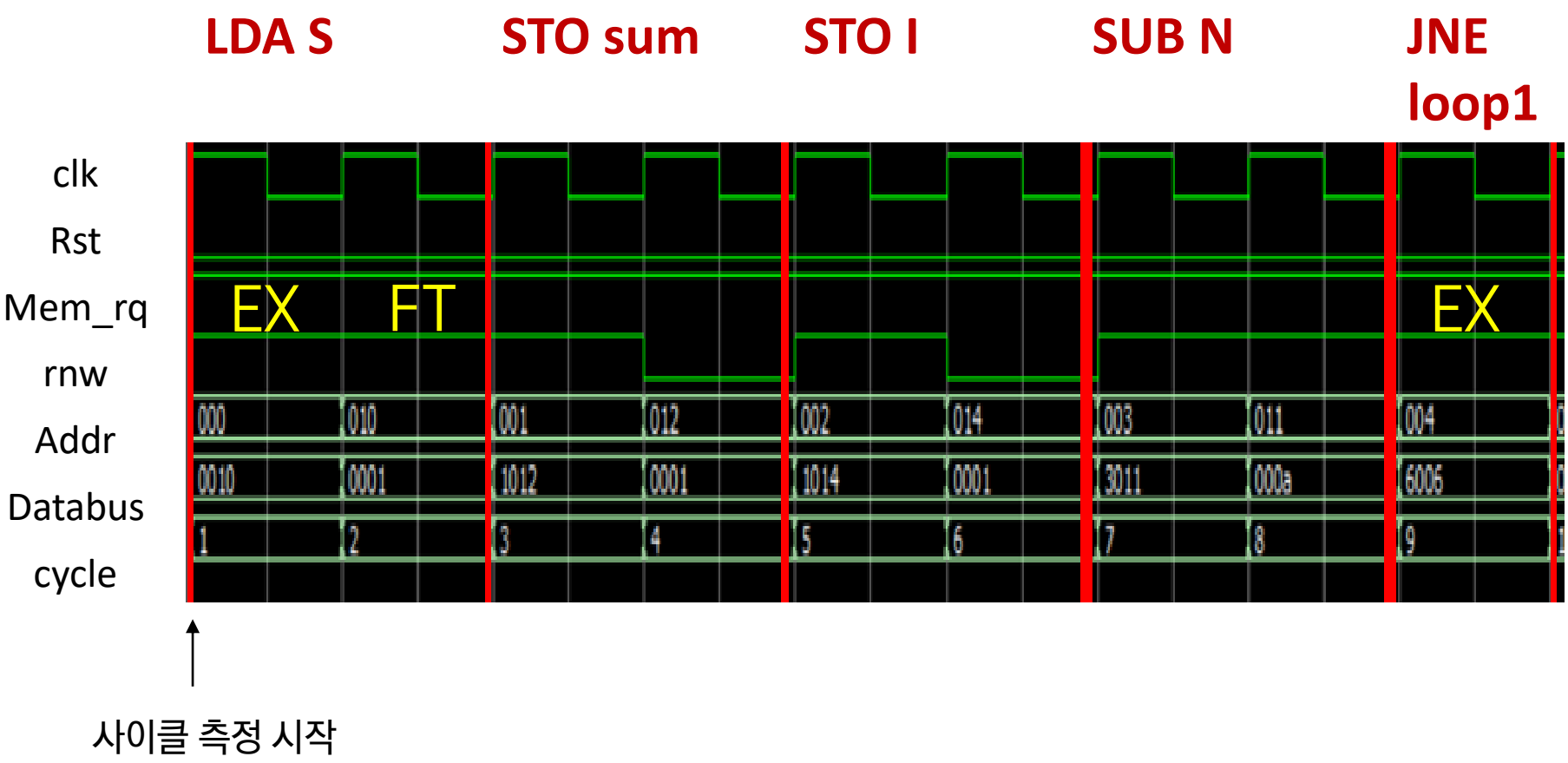
04 결과 분석

Simulation plan 기존 Mu0 Processor

memory			
주소		opcode	S
0	LDA S	0000	0000_0001_0000
1	STO sum	0001	0000_0001_0010
2	STO I	0001	0000_0001_0100
3	SUB N	0011	0000_0001_0001
4	JNE loop1	0110	0000_0000_0110
5	STP	0111	0000_0000_0000
6(loop1)	LDA I	0000	0000_0001_0100
7	ADD V1	0010	0000_0001_0011
8	STO I	0001	0000_0001_0100
9	ADD sum	0010	0000_0001_0010
10	STO sum	0001	0000_0001_0010
11	LDA I	0000	0000_0010_0100
12	SUB N	0011	0000_0001_0011
13	JNE loop1	0110	0000_0000_0110
14	STP	0111	0000_0000_0000

memory		
주소	mean	Data
16	S	1
17	N	10
18	Sum	
19	I	
20	VI	1
…		
31		

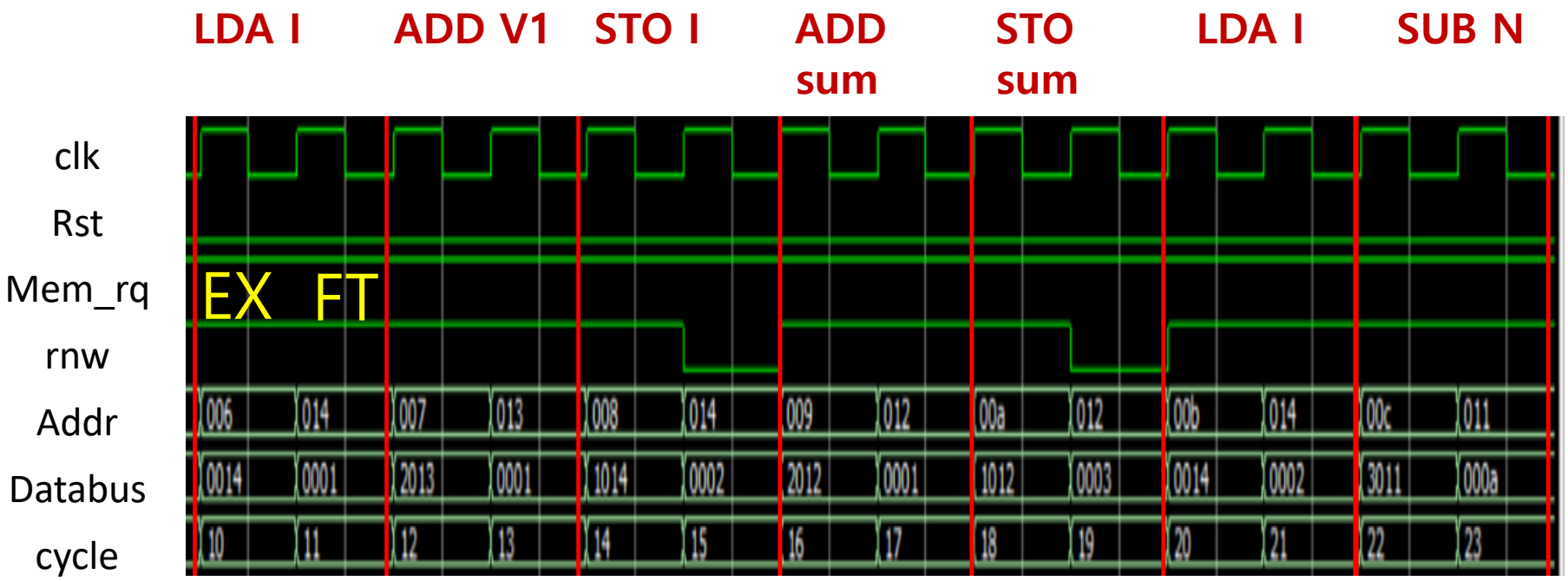
Simulation result 기존 Mu0 Processor



사이클 측정 시작

Simulation result 기존 Mu0 Processor

LOOP1 동작

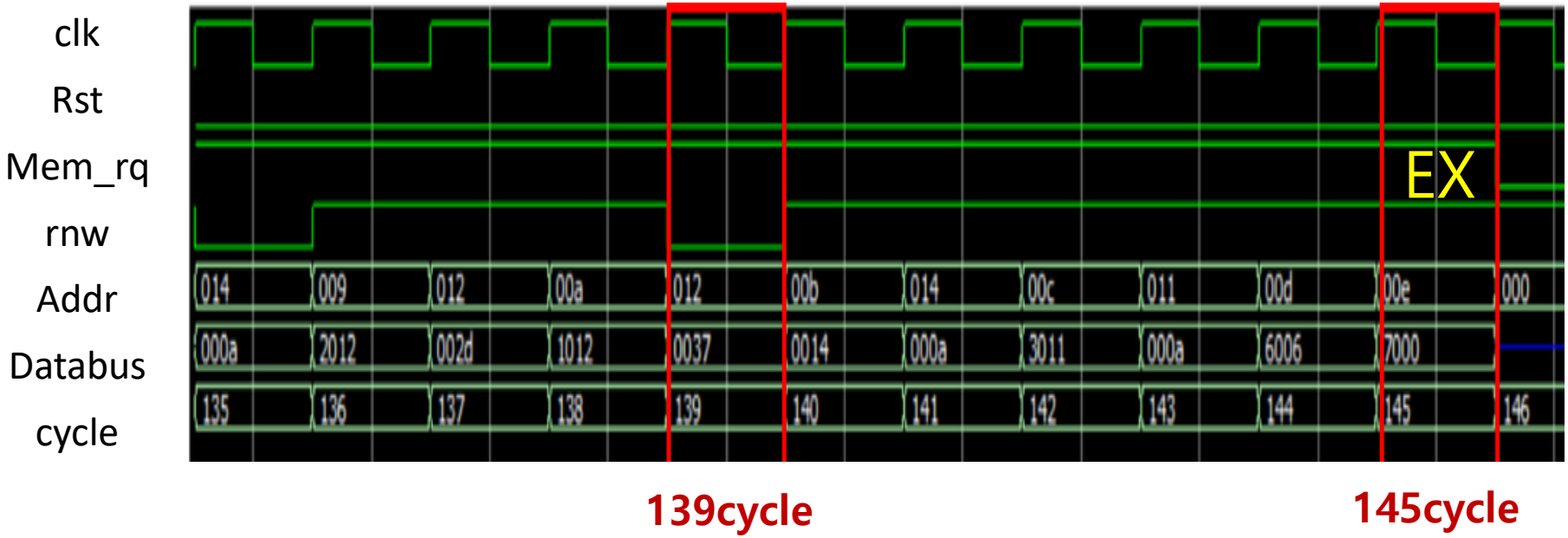


LOOP1 안의 명령어들은 총 9번 반복된다

Simulation result 기존 Mu0 Processor

1~10까지의 합 55가 처음 나오는 순간

STP



139cycle

145cycle

Assembly와 비교 기본 Mu0 Processor

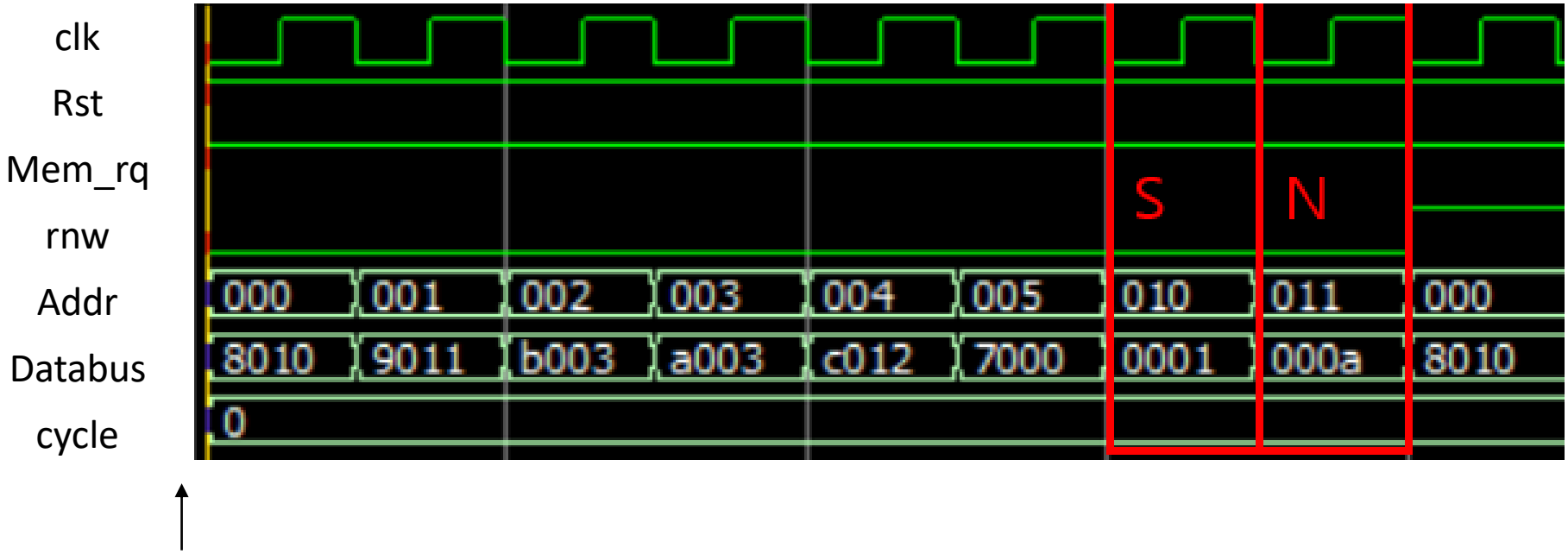
명령어	Cycle 수
LDA	2
STO	2
STO	2
SUB	2
JNE	1
STP	1
LDA	2 x 9 = 18
ADD	2 x 9 = 18
STO	2 x 9 = 18
ADD	2 x 9 = 18
STO	2 x 9 = 18
LDA	2 x 9 = 18
SUB	2 x 9 = 18
JNE	1 x 9 = 9
STP	1
합	**145**

Simulation plan 확장된 Mu0 Processor

memory			
주소		**opcode**	**S**
0	LDSA S	1000	0000_0001_0000
1	LDN N	1001	0000_0001_0001
2	JLT LOOP1	1011	0000_0000_0011
3(LOOP1)	SUM LOOP1	1010	0000_0000_0011
4	STS RESULT	1100	0000_0001_0010
5	STP	0111	0000_0000_0000

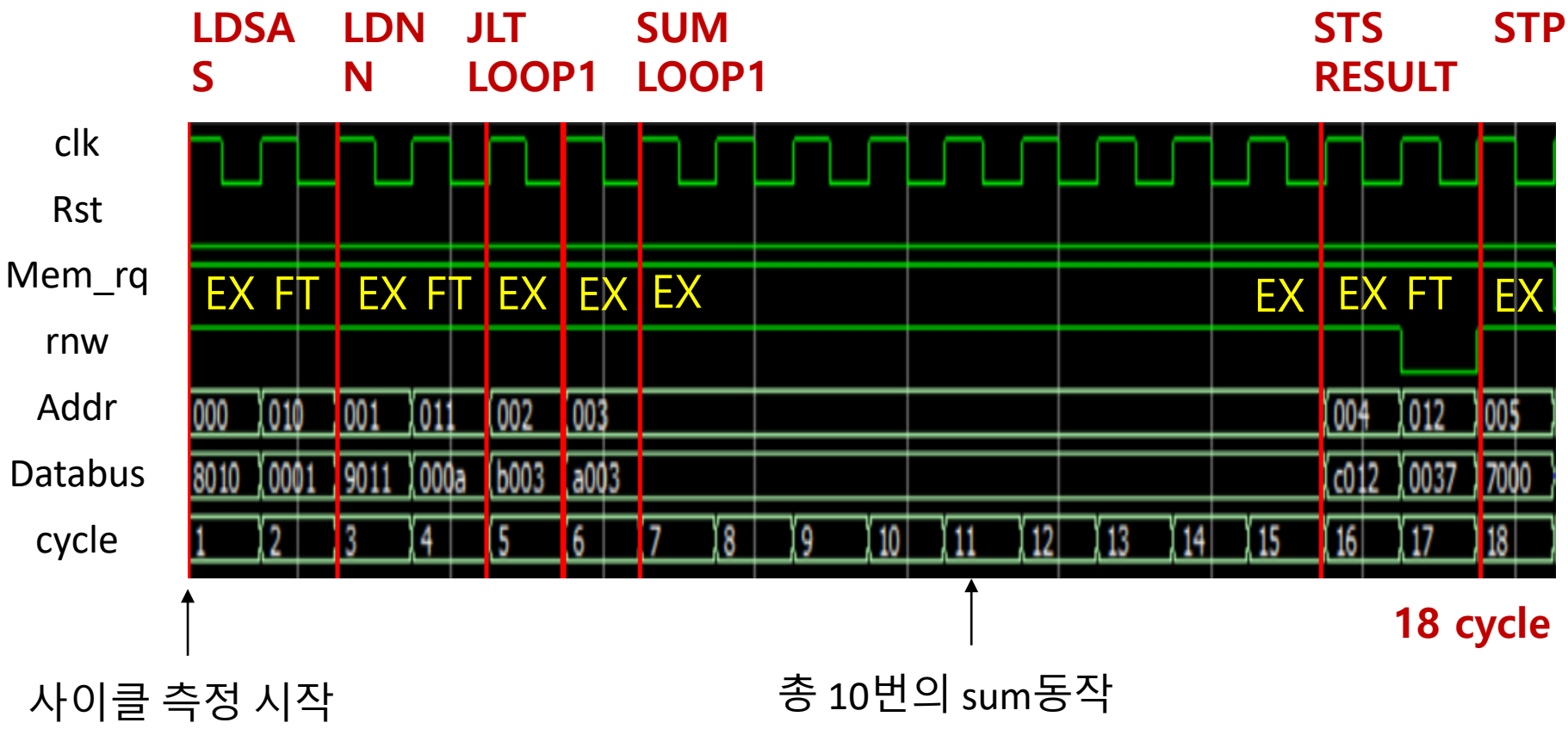
memory		
주소	**mean**	**Data**
16	S	1
17	N	10
18	RESULT	
19		
…		
31		

force-release



Reset 0일 때 동작 시작

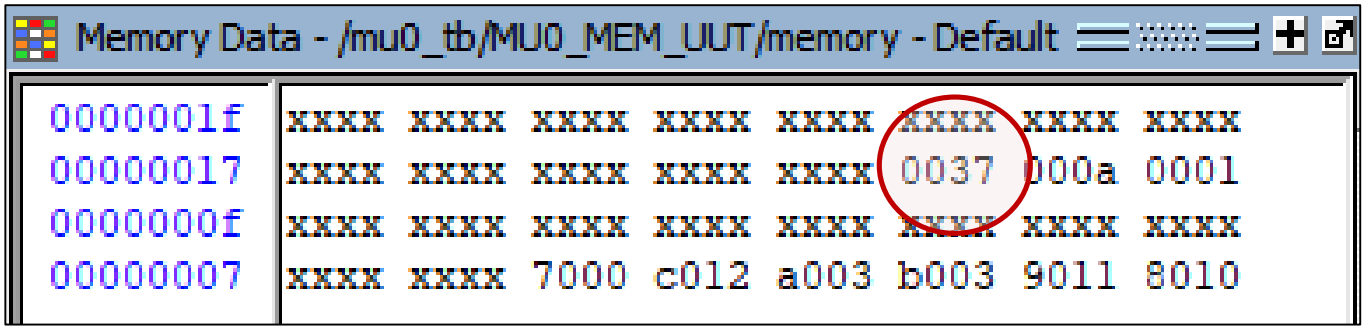
Simulation result 확장된 Mu0 Processor



Assembly와 비교 확장된 Mu0 Processor

명령어	Cycle 수
LDSA	2
LDN	2
JLT	1
SUM	1X10=10
STS	2
STP	1
합	**18**

메모리 결과



Hex 37 = Dec **55**

합성 결과-process 기존 Mu0 Processor

Flow Summary	
<<Filter>>	
Flow Status	Successful - Mon Dec 02 19:53:42 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	mu0_process
Top-level Entity Name	mu0_process
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	47
Total pins	32
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	0
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

```
286030 Timing-Driven Synthesis is running
144001 Generated suppressed messages file D:/quartus/d/mu0_process/output_files/mu0_process.map.smsg
 16010 Generating hard_block partition "hard_block:auto_generated_inst"
 21057 Implemented 161 device resources after synthesis - the final resource count might be different
       Quartus Prime Analysis & Synthesis was successful. 0 errors, 8 warnings
```

합성 결과-process 확장된 Mu0 Processor

Flow Summary

<<Filter>>

Flow Status	Successful - Mon Nov 25 11:26:42 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	mu0_process
Top-level Entity Name	mu0_process
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	95
Total pins	32
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	0
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Type	ID	Message
		***
		Running Quartus Prime Analysis & Synthesis
		Command: quartus_map --read_settings_files=on --write_settings_files=off mu0_process -c mu0_process
	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the global assignment
	20030	Parallel compilation is enabled and will use 2 of the 2 processors detected
	12021	Found 1 design units, including 1 entities, in source file /modelsim/mu0_project/mu0_process.v
	12127	Elaborating entity "mu0_process" for the top level hierarchy
	286030	Timing-Driven Synthesis is running
	144001	Generated suppressed messages file D:/quartus/mu0_process/output_files/mu0_process.map.smsg
	16010	Generating hard_block partition "hard_block:auto_generated_inst"
	21057	Implemented 254 device resources after synthesis - the final resource count might be different
		Quartus Prime Analysis & Synthesis was successful. 0 errors, 1 warning

합성 결과-memory

Flow Summary

<<Filter>>

Flow Status	Successful - Mon Nov 25 11:32:11 2019
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	mu0_memory
Top-level Entity Name	mu0_memory
Family	Cyclone V
Device	5CGXFC7C7F23C8
Timing Models	Final
Logic utilization (in ALMs)	N/A
Total registers	512
Total pins	32
Total virtual pins	0
Total block memory bits	0
Total DSP Blocks	0
Total HSSI RX PCSs	0
Total HSSI PMA RX Deserializers	0
Total HSSI TX PCSs	0
Total HSSI PMA TX Serializers	0
Total PLLs	0
Total DLLs	0

Type	ID	Message
		Running Quartus Prime Analysis & Synthesis
		Command: quartus_map --read_settings_files=on --write_settings_files=off mu0_memory -c mu0_memory
⚠	18236	Number of processors has not been specified which may cause overloading on shared machines. Set the gl
	20030	Parallel compilation is enabled and will use 2 of the 2 processors detected
	12021	Found 1 design units, including 1 entities, in source file /modelsim/mu0_project/mu0_memory.v
	12127	Elaborating entity "mu0_memory" for the top level hierarchy
	276014	Found 1 instances of uninferred RAM logic
	286030	Timing-Driven Synthesis is running
	144001	Generated suppressed messages file D:/quartus/mu0_memory/output_files/mu0_memory.map.smsg
	16010	Generating hard_block partition "hard_block:auto_generated_inst"
⚠	21074	Design contains 8 input pin(s) that do not drive logic
	21057	Implemented 737 device resources after synthesis - the final resource count might be different
		Quartus Prime Analysis & Synthesis was successful. 0 errors, 10 warnings

05 Conclusion

Conclusion

기존 MU0

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cycle

성능 8.05배 증가

명령어 추가
레지스터 추가
덧셈 기, 비교기를 추가

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cycle

Thank you