University of Pennsylvania
Department of Electrical and Systems Engineering
ESE319
Laboratory Experiment 2 - BJT Linear Amplifier

1. Introduction. This lab is designed to examine the characteristics of the single-stage bipolar junction transistor amplifier. Temperature and device parameter variation effects will be examined and biasing circuits that minimize these effects will be used in the experiment.

NOTICE: Parts 2 through 5 of this experiment are to be performed as a **PRE-LAB** assignment prior to the lab session. Items to be turned in are: the "pencil and paper" calculations used to come up with your circuit designs, the Multisim simulation schematics, and the frequency responses obtained for your design.

Also bring a copy of your design results to the lab. Choose one of the group's designs for implementation and submit this version of the design data with the group lab report.

2. Transistor models. For biasing and "low frequency" operation, we shall use the simple model:

$$i_C = I_S e^{\frac{v_{BE}}{V_T}}$$

and

$$i_B = \frac{1}{\beta} i_C$$

For the two transistors available in the lab, the *nominal* parameter values for these equations are:

	2N2222	2N3904
I_S (at 20 Degrees Celsius)	1.16E-14 A	7.62E-16 A
β (nominal value)	200	204

The saturation current, I_s, is strongly temperature dependent, doubling for about a 5 degree Celsius increase in temperature. For Celsius temperature measurements and for a reference temperature of 20 Degrees Celsius (room temperature), this current versus temperature expression becomes:

$$\frac{I_S}{I_{S(20)}} = 2^{\left(\frac{T_C - 20}{5}\right)}$$

and, for V_T, the expression is:

$$V_T = \frac{kT}{q}$$

where Boltzmann's constant is k=1.38E-23 Joules/°Kelvin, the electron charge is q=1.6E-19 coulomb and T is absolute temperature in degrees Kelvin. $V_T = 25.28mV$ approx. $25\ mV$ at room temperature (20 degrees Celsius or 293 degrees Kelvin).

3. Transistor sensitivity to V_{BE} value and to operating temperature. Complete the fill-in of the following tables for the 2N2222 and 2N3904 transistors.

HINT: You may find it helpful to use Scilab, Matlab or Excel to help you fill in the tables.

3.1 Calculate the dependence of I_C on V_{BE} at 20 degrees C:

	2N2222		2N3904	
I_C	V_{BE}	ΔV_{BE}	V_{BE}	ΔV_{BE}
1.00E-06				
1.00E-05				
1.00E-04			0.64717	
1.00E-03	0.63655		0.70538	
1.00E-02	0.69476	0.05821		
1.00E-01				
1.00E-00				

Please note that ΔV_{BE} is the change in V_{BE} that corresponds to the change in I_C, i.e. for the 2N2222 BJT the ΔV_{BE} entry in the table above is $\Delta V_{BE} = 0.05821\ V = 0.69476\ V - 0.63655\ V$.

3.2 Calculate the 2N2222 variation of I_C with temperature for **fixed** V_{BE} or variation in V_{BE} for **fixed** I_C:

	Temperature-sensitive parameters		**VBE = 0.63633 V**	**IC = 0.001 A**
TC	*VT*	*IS*	*IC*	*VBE*
0	0.02356			
20	0.02528	1.16000E-14	0.00100	0.63655
40		1.85600E-13	0.00319	
60				0.56419
80				
100				

4. Voltage source biasing.

4. 1 Design a transistor amplifier using the circuit shown in the Fig. 1 below. Determine values of the resistors, R_C, R_E, R_1, and R_2 to satisfy the following constraints with $V_{CC} = 10\ V$:

$V_{CG} = 5\ V;\ \ I_C = 1 mA;\ \ \frac{R_C}{R_E} = 5;\ \ I_1 = \frac{I_C}{10}$ Note: V_{CG} (= V_C) is the dc collector voltage with respect to ground.

Choose R_1, R_2 and R_E such that $R_B << (\beta+1)R_E$ and use $\beta = 200$ to estimate I_B. To complete your design, use Detkin Lab STANDARD size resistors closest in value to your calculated values of resistance. For R_E, use two standard equal-value resistors to form a resistance $R_E = R_{E1} + R_{E2}$ that is as close as possible to your calculated value of R_E.

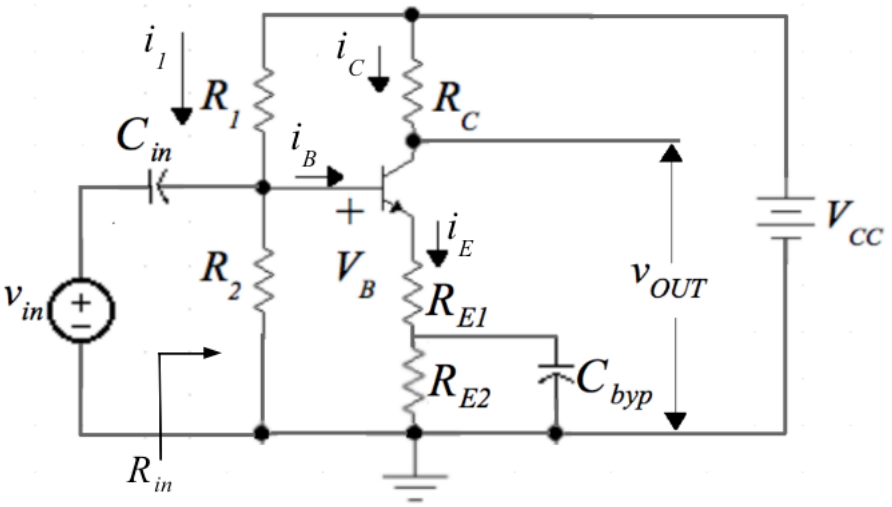

Fig. 1 Voltage Source Biasing

Choose the input coupling capacitor C_{in} = 3.3 μF so that its reactance at 10 Hz is about equal to the input impedance of the amplifier. ($X_{Cin} = R_{in} \approx R_B$ at 10 Hz). This will make the reactance negligible at about 100 Hz and above and the capacitor should act like an ac "short" at these frequencies. Simulate the resulting amplifier circuit in Multisim.

4.2 Bypass the resistor $R_{E2} = R_E/2$ on the grounded-side of the emitter with a capacitor $C_{byp} = 3.3\ \mu F$ so that its reactance $X_{Cbyp} \simeq R_E/2$ at 100 Hz and repeat the simulation in Multisim. What changes, if any, occur to the dc and ac components of the collector voltage v_{OUT}, to the dc collector current, to the gain, and to the bandwidth? What do you expect will happen to the gain if the total $R_E = R_{E1} + R_{E2}$ is "bypassed"?

5. Simulation. Do not forget to include the function generator output impedance and the scope probe input impedance in your *Multisim* model. (See the Lab 1 materials to obtain information on the scope probe characteristics.)

6. Construction. Use either of the above transistors to construct the circuit(s) designed in 4.1 and 4.2. In the implementation of the section 4.1 design, insert the transistor base and collector wires into adjacent Protoboard rows. Then measure and record v_C, v_B, and v_E to verify your design.

7. Operation.

7.1 Common emitter amplifier with emitter resistor feedback. Couple a function generator (through C_{in}) to the amplifier base input node and set the function generator output to deliver a 100Hz sine wave with a peak amplitude less than 0.5 volt. (Remember, this is an AMPLIFIER - DON'T OVERDRIVE IT) Using two 10x probes, connect scope probes to the function generator output and to the collector of the amplifier transistor. (Set the oscilloscope to read in ac mode.) Starting at 10 Hz., measure the magnitude voltage gain ((|Vout/Vin|) over the range of frequencies between the points where the gain drops to 0.707 times the value of the **1 kHz** gain. The high and low frequencies where the output voltage falls to 0.707 of this *mid-band* value are called the "3dB" points of the amplifier and define its *bandwidth*.

7.2 Common emitter amplifier with emitter resistor bypass. Repeat the experiment with ground-side $R_E/2$ resistor bypassed as prescribed in 4.2.

7.3 Shielding. Repeat the experimental runs above with the base and collector wires separated as shown in Fig. 2 below.

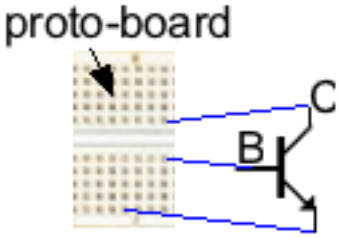

Fig. 2 Transistor connection for part 7.3

8. **Conclusions and Discussion.** Do your design gain and your experimental frequency response results agree with those from the simulations? If not, where do the results differ? Try to explain why they differ. What is ignored in the pencil and paper design? What is included in ***Multisim*** that is not present in the pencil and paper analysis? What is missing from the ***Multisim*** circuit simulation?

Kenneth R. Laker 27 Sep 2009 (revised 21 Sept. 2012)