iCEZUM Alhambra Clock 12Mhz **ADC FPGA** Serial iCE40HX1K ADS7924 Power **GND** Serial Pin Analog Pin Control € 6 - 17V FPGA GPIO (5V) Input pins: at least +/- 2mA Physical Pin driving strength required GND lcestudio name Output pins impedance: 95 **1_62 LED0** 4K (steady state) 96 <u>1</u>63 <u>LED1</u> 40R (Transitions) VIN 97 1_64 LED2 98 1<u>65 LED3</u> 99 1_66 LED4 FPGA Direct GPIO (3V3) 101 1_67 LED5 Absolute Max per pin 8mA Recommended 6 mA 102 **1_68 LED6** 104 **1_6**9 **LED7** <mark>GP0</mark> 2_24 | 37 38 2<u>25</u> GP1 GP2 2_26 39 41 2<u>2</u>7 GP3 10 3<u>4B</u> sw1 GP4 2_28 42 11 3_5A SW2 43 2<u>2</u>29 GP5 50 2_36 GP7 CLK CLE 87 1<u>56 DD5</u> SCL **RST** Reset 88 1<u>57 DD4</u> SDA POWER BUTTON **CLK** Clock AREF CLE Clock Enable GND 144 0<u>96 D13</u> • 143 **0_95 D12** RESET • 142 0<u>94</u> D11 11 = 10 3V3 • 141 0<u>9</u>3 <mark>D10</mark> 139 0<u>9</u>2 D9 GND 138 0<u>9</u>1 D8 GND 0 6 - 17V 💿 -112 **0_73 D7** • 113 0_74 D6 • DD0 1<u>52</u> 78 114 0<u>75</u> D5 • •

