AMBA Peripheral Bus Controller

Data Sheet

ARM®

ARM DDI 0044C

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Release Information

Issue	Date	Change
A	Dec 1995	Created
B	Jan 1996	Minor edits
C	Apr 1997	Minor edits

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Chapter 1
AMBA Peripheral Bus Controller

This module converts Advanced System Bus (ASB) signals to Advanced Peripheral Bus (APB) signals.

1.1 Overview

This module provides an interface between the Advanced System Bus (ASB) and the Advanced Peripheral Bus (APB).

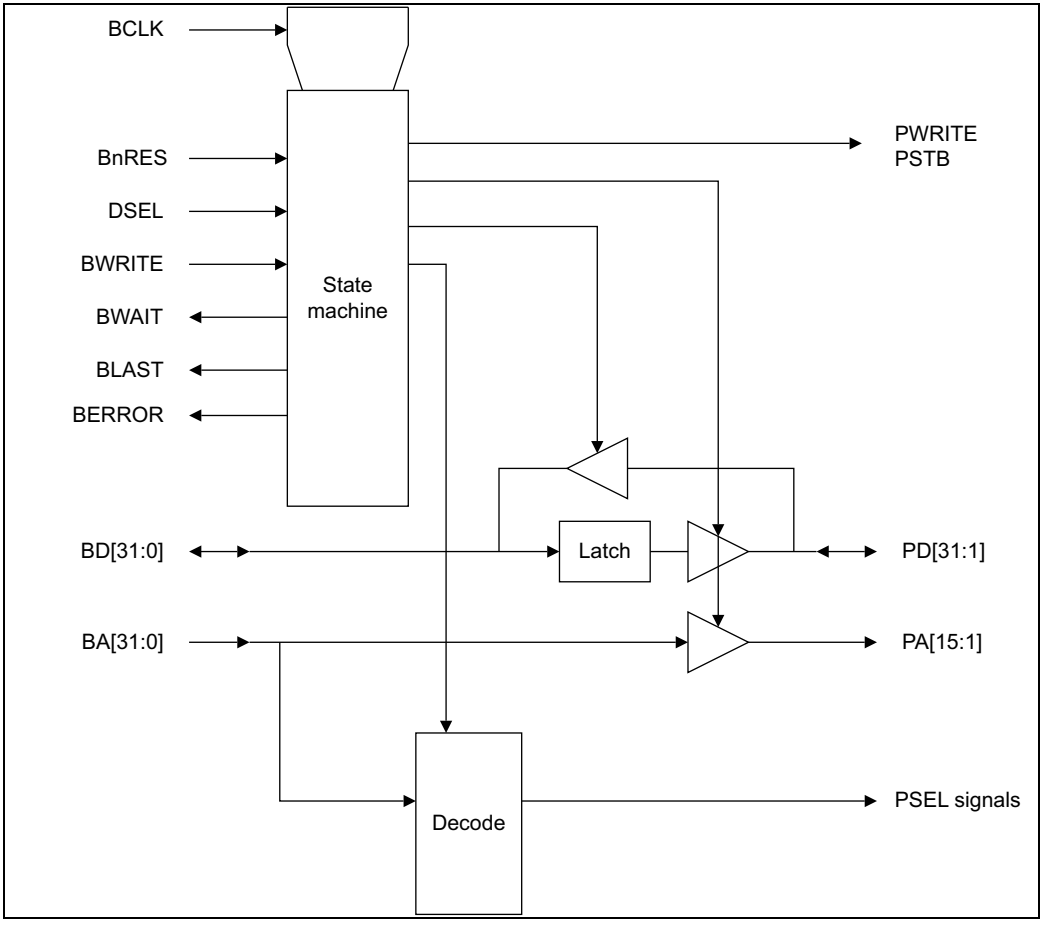

Figure 1-1 Block diagram of bridge module

The implementation of this block contains:

- a state machine, which is independent of the device memory map
- combinatorial address decoding logic to produce PSELxx signals

To add new peripherals or alter the system memory map only this section needs to be modified.

1.2 Hardware Interface and Signal Description

This module converts ASB transactions to APB transactions, as described in the following tables:

- Table 1-1 describes the ASB signals used in this module.
- Table 1-2 on page 1-4, describes the APB signals produced.
- Table 1-3 on page 1-4, describes the signals produced by the APB address decoding sub-module.

Table 1-1 ASB signal descriptions

Name	Type	Source/ Destination	Description
BCLK	In		System (bus) clock. This clock times all bus transfers. The clock has two distinct phases—phase 1 in which **BCLK** is LOW and phase 2 in which **BCLK** is HIGH.
BD[31:0]	InOut	Bus master	This is the bidirectional system data bus. The data bus is driven by the current bus master during write transfers, and by this block during read transfers from the peripheral bus.
BnRES	In	Reset controller	This active LOW signal indicates the reset status of the bus and is driven by the reset controller.
BWAIT	Out	System decoder and current bus master	This signal is driven by the selected bus slave to indicate if the current transfer may complete. If **BWAIT** is HIGH, a further bus cycle is required. If **BWAIT** is LOW, the transfer may complete in the current bus cycle. When no bus transfer is taking place, this signal is driven by the system decoder. When selected, the peripheral bus controller drives it in the LOW phase of **BCLK** and it is valid set up to the rising edge of **BCLK**.
BLAST	Out	System decoder and current bus master	This signal is driven by the selected bus slave to indicate if the current transfer should be the last of a burst sequence. It is always driven low. When no bus transfer is taking place, this signal is driven by the bus decoder. When selected, the peripheral bus controller drives it in the LOW phase of **BCLK** and it is valid set up to the rising edge of **BCLK**.
DSEL	In	From Bus Decoder	This signal indicates that the peripheral bus controller has been selected. It becomes valid during the **BCLK** HIGH phase before the data transfer and remains active until the last **BCLK** HIGH phase of the transfer.

Table 1-1 ASB signal descriptions (continued)

Name	Type	Source/ Destination	Description
BERROR	Out	System decoder and current bus master	A transfer error is indicated by the selected bus slave using the **BERROR** signal. When **BERROR** is HIGH, a transfer error has occurred. When **BERROR** is LOW, the transfer is successful. When no bus transfer is taking place, it is driven by the system decoder. When selected, the peripheral bus controller drives this signal in the LOW phase of **BCLK** and it is valid set up to the rising edge of **BCLK**.
BWRITE	In	Current bus master	This signal indicates a write cycle when HIGH and a read cycle when LOW. It has the same timing as the address bus and is driven by the bus master.

Table 1-2 APB signal descriptions

Name	Type	Source/ Destination	Description
PA	Out	APB Peripherals	This is the peripheral address bus, which is used by individual peripherals for decoding register accesses to that peripheral. The addresses become valid before **PSTB** goes HIGH and remain valid after **PSTB** goes LOW.
PD	InOut	APB Peripherals, B_D bus	This is the bidirectional peripheral data bus. The data bus is driven by this block during write cycles (when **PWRITE** is HIGH) and by the selected peripheral bus slave during read cycles (when **PWRITE** is LOW).
PSTB	Out	APB peripherals	This strobe signal is used to time all accesses on the peripheral bus. The falling edge of **PSTB** is coincident with the falling edge of **BCLK**.
PWRITE	Out	APB peripherals	This signal indicates a write to a peripheral when HIGH and a read from a peripheral when LOW. It has the same timing as the peripheral address bus. It becomes valid before **PSTB** goes HIGH and remains valid after **PSTB** goes LOW.

Table 1-3 Signal descriptions for address decoding block

Name	Type	Source/ Destination	Description
BA	In	Current bus master	This is the system address bus, which is driven by the current bus master. The addresses change during the **BCLK** HIGH phase before the transfer to which they refer and remain valid until the last **BCLK** HIGH phase of the transfer.

Table 1-3 Signal descriptions for address decoding block (continued)

Name	Type	Source/ Destination	Description
PSELx	Out	APB peripheral	There is one of these signals for each APB peripheral present in the system. The signal indicates that the slave device is selected and a data transfer is required. This signal has the same timing as the peripheral address bus. It becomes valid before **PSTB** goes HIGH and remains valid after **PSTB** goes LOW.

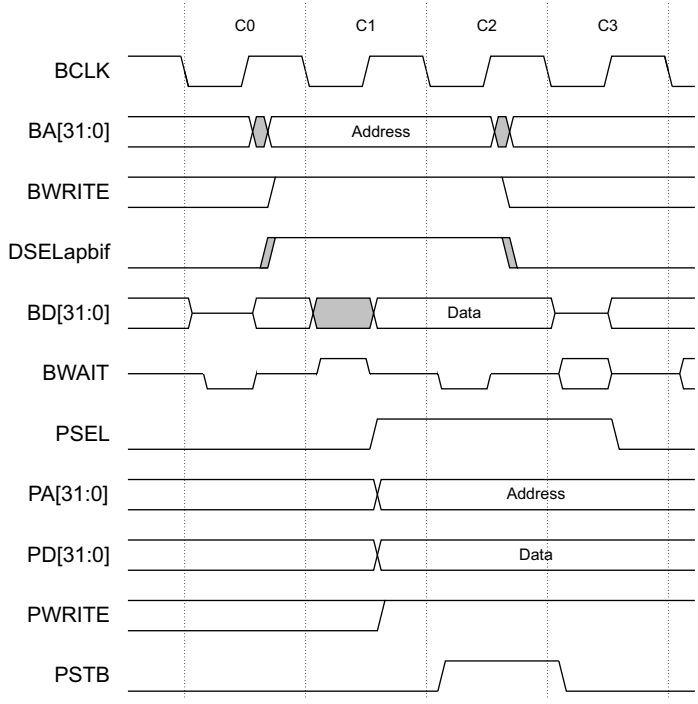

Figure 1-2 APB write cycle

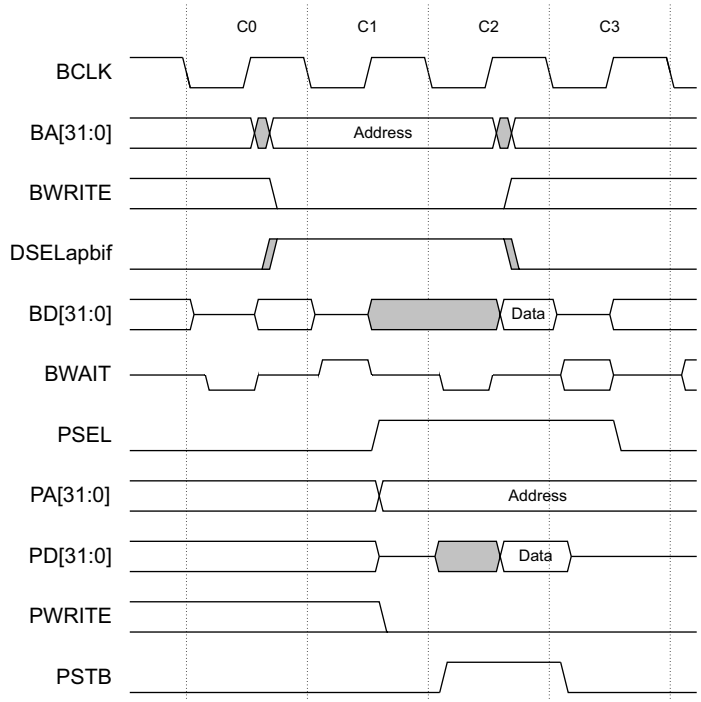

Figure 1-3 APB read cycle

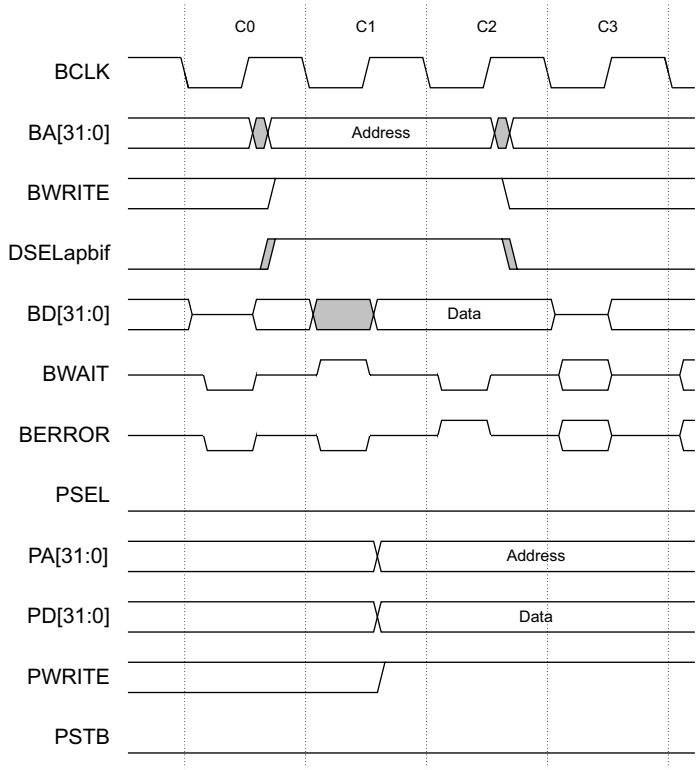

Figure 1-4 APB error

1.3 Peripheral Memory Map

The bridge controls the memory map for the peripherals and generates a select signal for each peripheral.

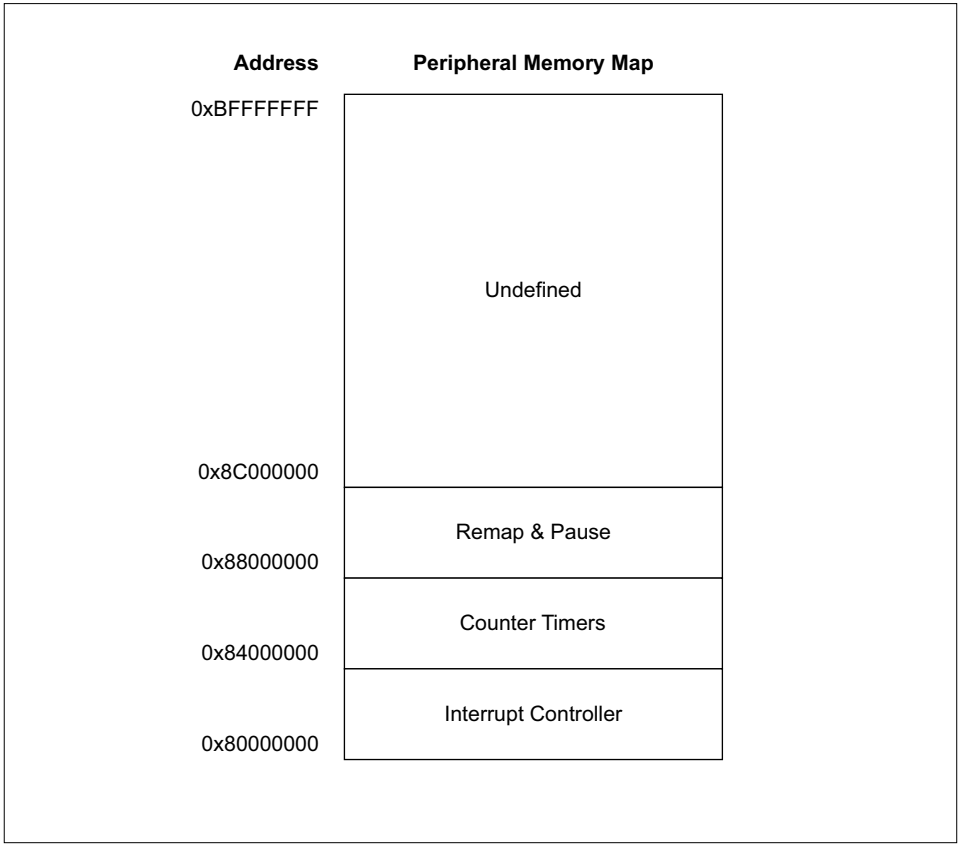

Figure 1-5 Peripheral Memory Map

1.4 Function and Operation of Block

The APB bridge responds to transaction requests from the currently enabled bus master. The ASB transactions are converted into APB transactions. The state machine, see Figure 1-6, controls the depipelining of the ASB transaction, and controls the latches and drivers for the PA, PD and BD buses, also producing the **PSTB** signal. This example design uses the **DSEL** signal from a centralised decoder to select the Peripheral bus controller as an ASB slave.

The individual **PSEL**xx signals are decoded from **BA**, using the state of the state machine to enable their output.

If an undefined location is accessed then **BERROR** is asserted and no peripheral is selected, see Figure 1-4 on page 1-7

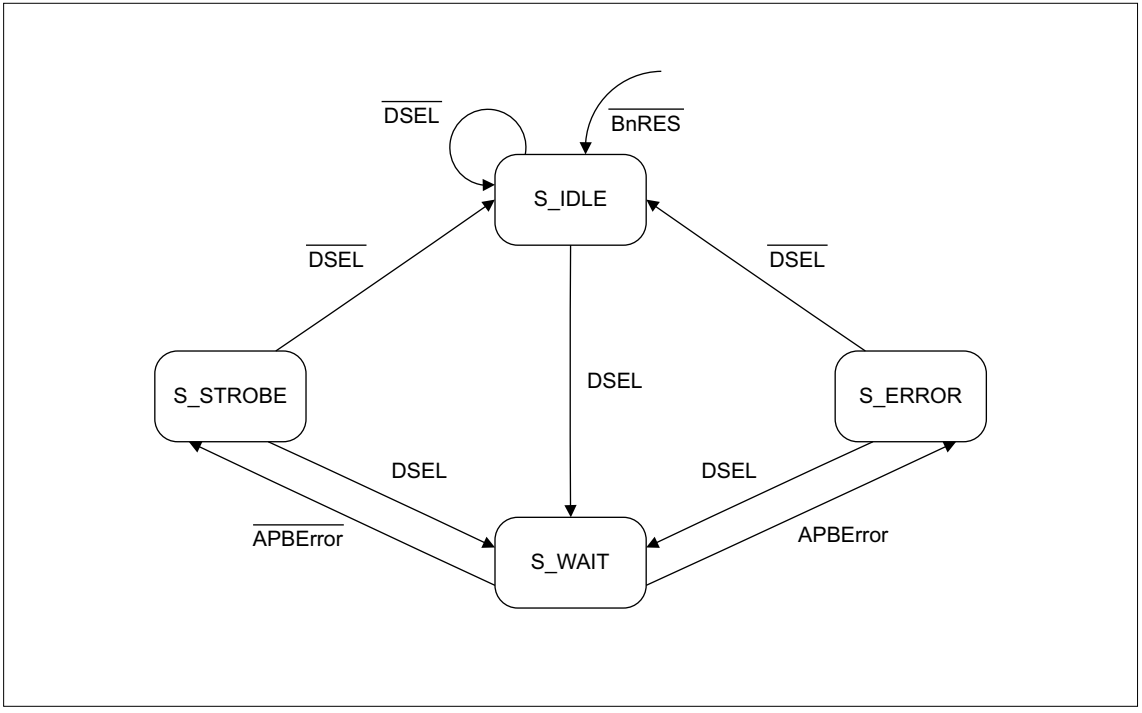

Figure 1-6 State machine for APB controller

The signal **APBError** is internal, and is asserted when the address points to an undefined APB area.

