

A Resource-Efficient 1024-Point MSC FFT Using Time-Multiplexed Constant Multiplication

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Abstract—This paper presents a resource-efficient architecture for a 1024-point FFT based on time-multiplexed constant multipliers. The proposed design reduces hardware cost while maintaining high throughput and numerical accuracy.

Index Terms—FFT, constant multiplication, time-multiplexing, FPGA, ASIC, low-complexity, signal processing.

I. INTRODUCTION

II. BACKGROUND AND RELATED WORK

III. PROPOSED ARCHITECTURE

IV. IMPLEMENTATION AND OPTIMIZATION

V. EXPERIMENTAL RESULTS

Table II demonstrates a comprehensive comparison of hardware resources and performance metrics for the proposed 4-parallel 1024-point FFT architecture against several state-of-the-art designs.

The metrics include the number of slice, LUT, flip-flop (FFs), DSP, Block-RAM, maximum clock frequency (f_{CLK}), throughput(Th.), latency (in cycles and microseconds), signal-to-quantization noise ratio (SQNR), power consumption (P), and normalized power (NP).

TABLE I
COMPARISON OF HARDWARE RESOURCES AND PERFORMANCE FOR 4-PARALLEL 1024-POINT FFT IMPLEMENTED ON FPGA

	[1]	[2]	[3]	[4]	[5]	Proposed
Architecture	MDC	MDC	MDC	CM	MSC	MSC
Radix	2^5	2^2	2	2^5	2^5	2^5
WL	16	16	16	16	16	16
Slices	1420	1351	-	2631	1615	1477
LUTs	-	-	4116	-	4682	4629
FFs	-	-	1920	-	5910	4887
DSPs	16	48	72	12	12	12
Block-RAMs	12	12	0	0	4	4
f_{CLK} (MHz)	253	227	380	680	420	493
Th. (MS/s)	1012	910	1520	2720	1680	1820
Latency (cyc.)	265	285	767	394	300	307
Latency (μ s)	1.04	1.25	2.02	0.58	0.71	0.62
SQNR (dB)	40.30	-	-	-	50.16	49.46
P (W)	-	-	-	1.68	0.98	1.16
NP ($\frac{mW}{MHz}$)	-	-	-	2.47	2.33	2.35

TABLE II
COMPARISON OF RESOURCE-DELAY PRODUCT (RDP) AND POWER-DELAY PRODUCT (PDP). $PDP = POWER \cdot T_{CLK}$ (mW·NS), $RDP = SLICES \cdot T_{CLK}$ (SLICES · NS)

	[1]	[2]	[3]	[4]	[5]	Proposed
Architecture	MDC	MDC	MDC	CM	MSC	MSC
Radix	2^5	2^2	2	2^5	2^5	2^5
PDP(mW·ns)	-	-	-	2470.61	2333.38	2352.94
RDP	5612.69	5951.56	-	3869.15	3845.32	2995.94

VI. CONCLUSION

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