A Resource-Efficient 1024-Point MSC FFT Using Time-Multiplexed Constant Multiplication

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***Abstract*—This paper presents a resource-efficient architecture for a 1024-point FFT based on time-multiplexed constant multipliers. The proposed design reduces hardware cost while maintaining high throughput and numerical accuracy [1].**

***Index Terms*—FFT, constant multiplication, time-multiplexing, FPGA, ASIC, low-complexity, signal processing.**

[1] A. Author, "A dummy reference for testing," *IEEE Transactions on Signal Processing*, vol. 73, pp. 1–10, 2025.

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