



- The devices contain from two to four TMs depending upon which device is selected with each TM having a reference name of **TM0, TM1, TM2 and TM3**.
- Each individual TM can be categorized as a certain type, namely **Compact** Type TM, **Standard** Type TM or **Enhanced** Type TM.

### TM Function Summary

Function	CTM	STM	ETM
Timer/Counter	✓	✓	✓
I/P Capture	—	✓	✓
Compare Match Output	✓	✓	✓
PWM Channels	1	1	2
Single Pulse Output	—	1	2
PWM Alignment	Edge	Edge	Edge & Centre
PWM Adjustment Period & Duty	Duty or Period	Duty or Period	Duty or Period

### TM Name/Type Reference

Device	TM0	TM1	TM2	TM3
HT66F20	10-bit CTM	10-bit STM	—	—
HT66F30	10-bit CTM	10-bit ETM	—	—
HT66F40	10-bit CTM	10-bit ETM	16-bit STM	—
HT66F50	10-bit CTM	10-bit ETM	16-bit STM	10-bit CTM
HT66F60	10-bit CTM	10-bit ETM	16-bit STM	10-bit CTM

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### TM Output Pins

All TM output pin names have an "\_n" suffix. Pin names that include a "\_1" or "\_2" suffix indicate that they are from a TM with multiple output pins

TM0 : CTM

TM1 : ETM/(STM only for HT66F20)

TM2 : STM

TM3 : CTM

Device	CTM	STM	ETM	Registers
HT66F20	TP0_0	TP1_0, TP1_1	—	TMPC0
HT66F30	TP0_0, TP0_1	—	TP1A, TP1B_0, TP1B_1	TMPC0
HT66F40	TP0_0, TP0_1	TP2_0, TP2_1	TP1A, TP1B_0, TP1B_1, TP1B_2	TMPC0, TMPC1
HT66F50	TP0_0, TP0_1 TP3_0, TP3_1	TP2_0, TP2_1	TP1A, TP1B_0, TP1B_1, TP1B_2	TMPC0, TMPC1
HT66F60	TP0_0, TP0_1 TP3_0, TP3_1	TP2_0, TP2_1	TP1A, TP1B_0, TP1B_1, TP1B_2	TMPC0, TMPC1

### TM Input/Output Pin Control Registers List

Registers	Device	Bit							
		7	6	5	4	3	2	1	0
TMPC0	HT66F20	—	—	T1CP1	T1CP0	—	—	—	T0CP0
TMPC0	HT66F30	T1ACP0	—	T1BCP1	T1BCP0	—	—	T0CP1	T0CP0
TMPC0	HT66F40 HT66F50 HT66F60	T1ACP0	T1BCP2	T1BCP1	T1BCP0	—	—	T0CP1	T0CP0
TMPC1	HT66F40	—	—	—	—	—	—	T2CP1	T2CP0
TMPC1	HT66F50 HT66F60	—	—	T3CP1	T3CP0	—	—	T2CP1	T2CP0

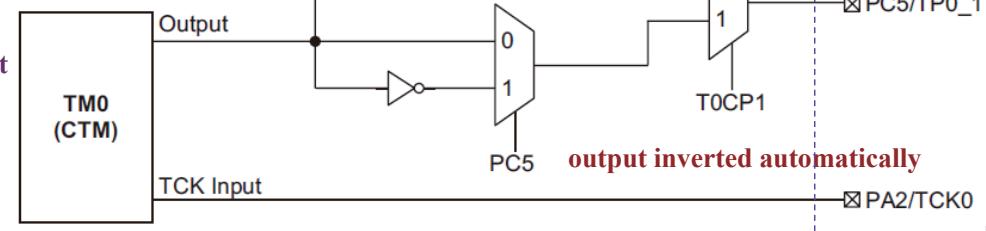
- Selecting to have a TM input/output or whether to retain its other shared function**, is implemented using one or two registers
- Setting the bit high** will setup the corresponding pin as a TM input/output, if reset to **zero** the pin will retain its original other function





Function	CTM
Timer/Counter	✓
I/P Capture	—
Compare Match Output	✓
PWM Channels	1
Single Pulse Output	—
PWM Alignment	Edge
PWM Adjustment Period & Duty	Duty or Period

The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the TM output pin is not used.



Note:

1. The I/O register data bits shown are used for TM output inversion control.
2. In the Capture Input Mode, the TM pin control register must never enable more than one TM input.

- This external TM input pin is shared with other functions but will be connected to the internal TM if selected using the TnCK2~TnCK0 bits. (110: TCKn rising edge clock ; 111: TCKn falling edge clock )
- The TM input pin can be chosen to have either a rising or falling active edge. ?!\_0 or \_1
- All TM output pin names have an \_n suffix. Pin names that include a \_1 or \_2 suffix indicate that they are from a TM with multiple output pins. This allows the TM to generate a complimentary output pair, selected using the I/O register data bits (i.e., \_pa0=0 → TP0\_0 normal output ; \_pa0=1 → TP0\_0 inverted output).

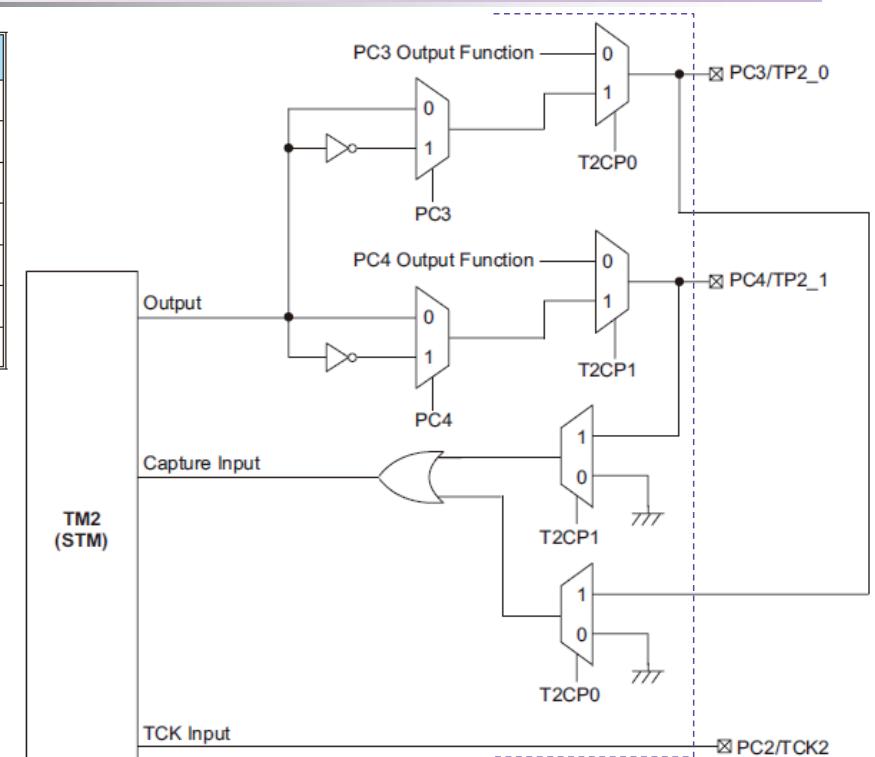


Function	STM
Timer/Counter	✓
I/P Capture	✓
Compare Match Output	✓
PWM Channels	1
Single Pulse Output	1
PWM Alignment	Edge
PWM Adjustment Period & Duty	Duty or Period

The Timer/Counter Mode operates in an identical way to the Compare Match Output Mode generating the same interrupt flags. The exception is that in the Timer/Counter Mode the TM output pin is not used.

Note:

1. The I/O register data bits shown are used for TM output inversion control.
2. In the Capture Input Mode, the TM pin control register must never enable more than one TM input.

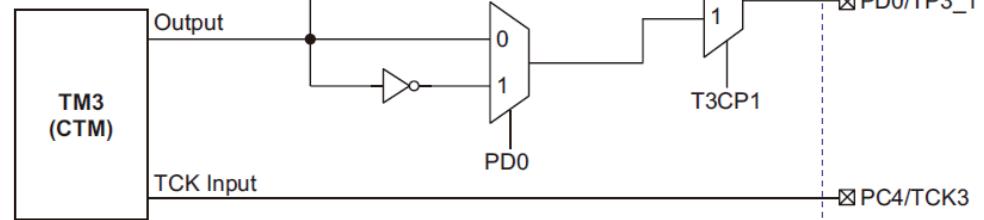


- This external TM input pin is shared with other functions but will be connected to the internal TM if selected using the TnCK2~TnCK0 bits. (110: TCKn rising edge clock ; 111: TCKn falling edge clock )
- The TM input pin can be chosen to have either a rising or falling active edge. ?!\_0 or \_1
- All TM output pin names have an \_n suffix. Pin names that include a \_1 or \_2 suffix indicate that they are from a TM with multiple output pins. This allows the TM to generate a complimentary output pair, selected using the I/O register data bits (i.e., \_pc4=0 → TP2\_1 normal output ; \_pc4=1 → TP2\_1 inverted output).



Function	CTM
Timer/Counter	✓
I/P Capture	—
Compare Match Output	✓
PWM Channels	1
Single Pulse Output	—
PWM Alignment	Edge
PWM Adjustment Period & Duty	Duty or Period

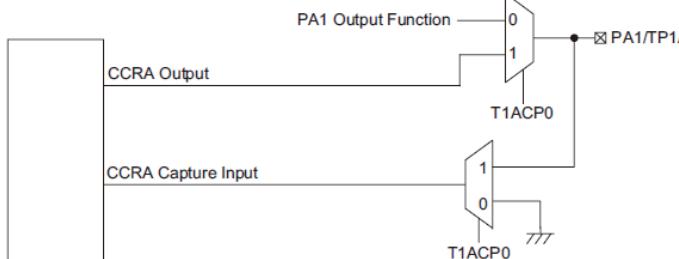
The **Timer/Counter Mode** operates in an identical way to the **Compare Match Output Mode** generating the same interrupt flags. The exception is that in the **Timer/Counter Mode** the TM output pin is not used.



Note:

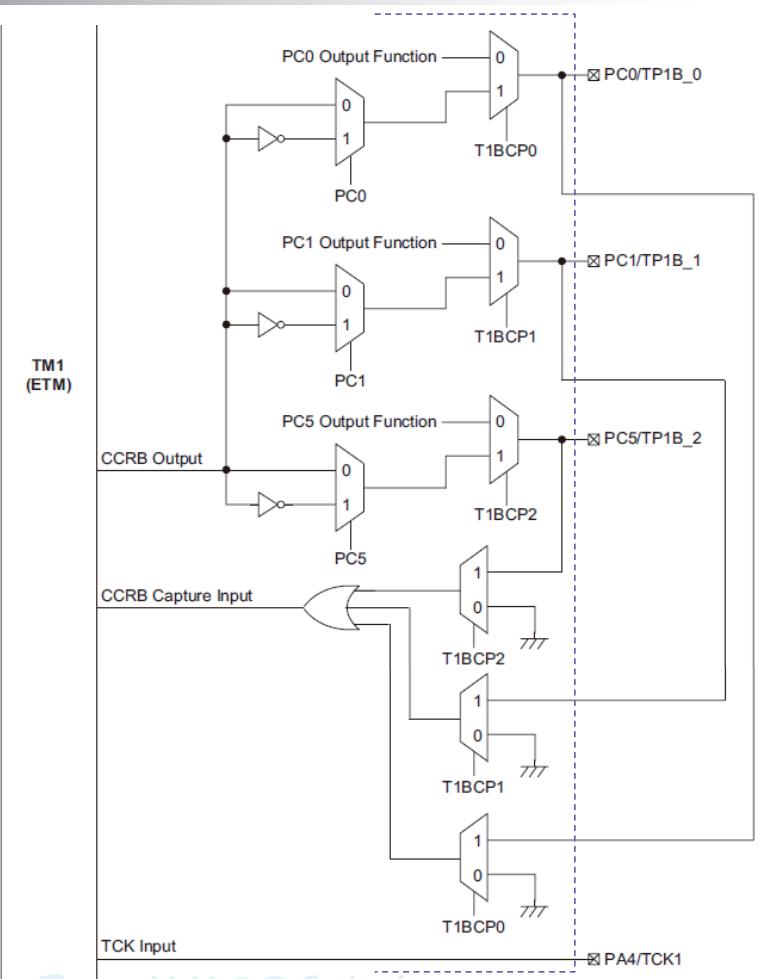
1. The I/O register data bits shown are used for TM output inversion control.
2. In the Capture Input Mode, the TM pin control register must never enable more than one TM input.

- This **external TM input pin** is shared with other functions but will be **connected to the internal TM if selected using the TnCK2~TnCK0 bits**. (110: TCKn rising edge clock ; 111: TCKn falling edge clock )
- The **TM input pin** can be chosen to have either a **rising or falling active edge**.
- All TM output pin names have an \_n suffix. Pin names that include a \_1 or \_2 suffix indicate that they are from a TM with multiple output pins. **This allows the TM to generate a complimentary output pair, selected using the I/O register data bits (i.e., \_pd3=0 → TP3\_0 normal output ; \_pd3=1 → TP3\_0 inverted output).**



Function	ETM
Timer/Counter	✓
I/P Capture	✓
Compare Match Output	✓
PWM Channels	2
Single Pulse Output	2
PWM Alignment	Edge & Centre
PWM Adjustment Period & Duty	Duty or Period

The **Timer/Counter Mode** operates in an identical way to the **Compare Match Output Mode** generating the same interrupt flags. The exception is that in the **Timer/Counter Mode** the TM output pin is not used.





- The TM Counter Registers and the Capture/Compare CCRA and CCRB registers, being either 10-bit or 16-bit, all have a **low and high byte structure**.
- The **high bytes can be directly accessed**, but as the **low bytes can only be accessed via an internal 8-bit buffer**, reading or writing to these register pairs must be carried out in a specific way.

The following steps show the read and write procedures:

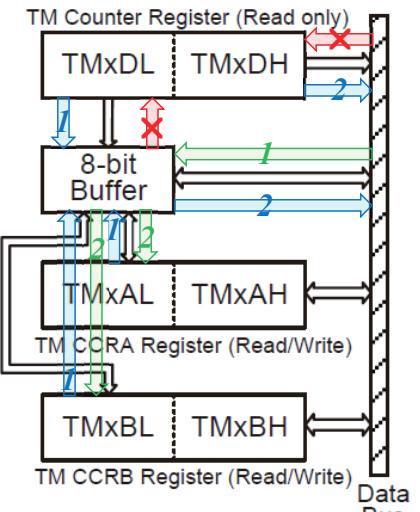
#### • Writing Data to CCRB or CCRA

- ◆ Step 1. **Write data to Low Byte** TMxAL or TMxBL
  - note that here **data is only written to the 8-bit buffer**.
- ◆ Step 2. **Write data to High Byte** TMxAH or TMxBH
  - here **data is written directly to the high byte registers** and **simultaneously data is latched from the 8-bit buffer to the Low Byte registers**.

#### • Reading Data from the Counter Registers and CCRB or CCRA

- ◆ Step 1. **Read data from the High Byte** TMxDH, TMxAH or TMxBH
  - here **data is read directly from the High Byte registers** and **simultaneously data is latched from the Low Byte register into the 8-bit buffer**.
- ◆ Step 2. **Read data from the Low Byte** TMxDL, TMxAL or TMxBL
  - this step **reads data from the 8-bit buffer**.

*Low & high bytes are accessed simultaneously but low bytes can only be accessed via an internal 8-bit buffer*



## Holtek – Compact Type TM / CTM (for TM0 or TM3)

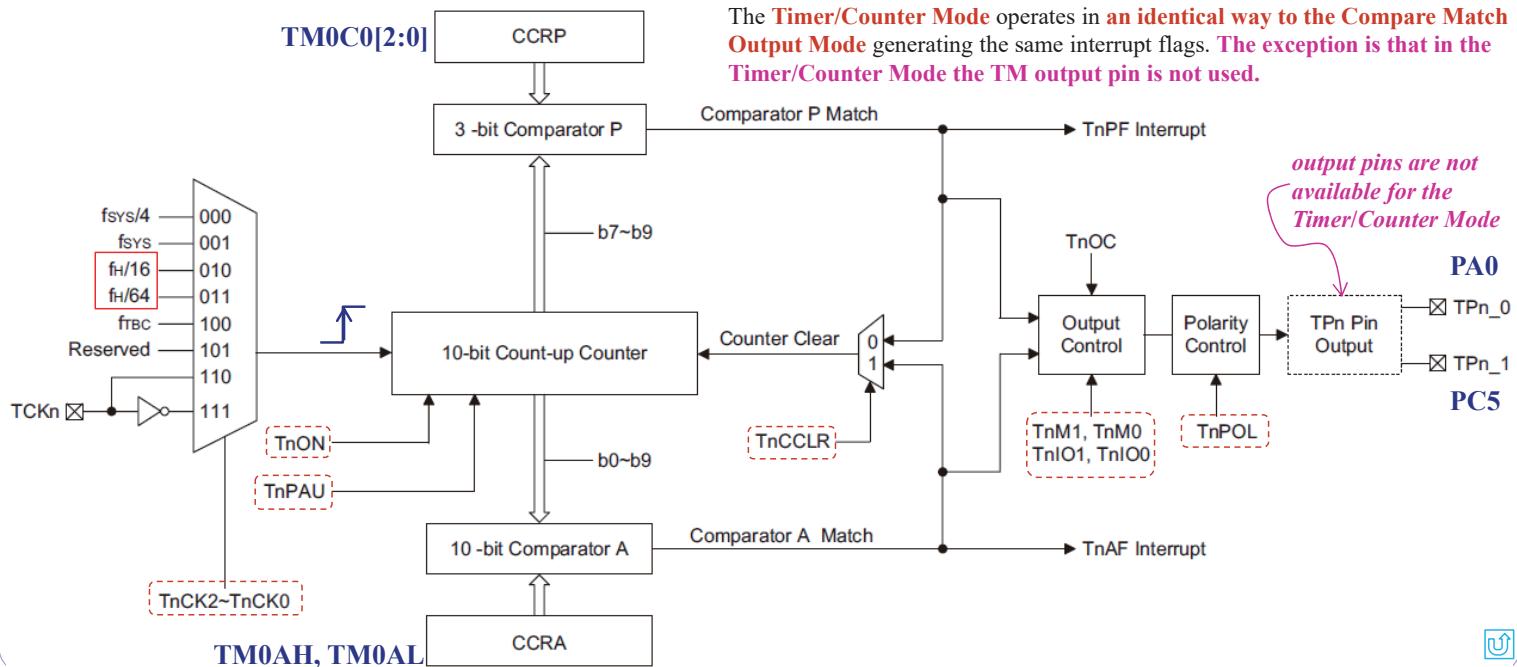


- Although the **simplest form of the three TM types**, the **Compact TM type** still contains **three operating modes**, which are **Compare Match Output**, **Timer/Event Counter** and **PWM Output modes**.
- The **Compact TM** can also be controlled with an external input pin and can drive one or two external output pins.
  - These **two external output pins** can be the **same signal or the inverse signal**. (depends on the value of pin's data register)
- Its **core** is a **10-bit count-up counter** which is driven by a user selectable internal or external clock source.
  - There are also **two internal comparators** with the names, **Comparator A** and **Comparator P**.
  - These comparators will **compare the value in the counter with CCRP and CCRA registers**.
    - The **CCRP** is **three bits wide** whose value is **compared with the highest three bits in the counter** while the **CCRA** is the **ten bits** and therefore **compares with all counter bits**.
  - The **only way of changing the value of the 10-bit counter** using the application program, is to **clear the counter by changing the TnON bit from low to high**. Read Only
  - The **counter will also be cleared automatically** by a **counter overflow** or a **compare match with one of its associated comparators**.
  - When **these match conditions occur**, a **TM interrupt** signal will also usually be generated.
- Overall operation of the Compact TM is controlled using six registers.
  - **Two control registers** which setup the **different operating and control modes** as well as the **three CCRP bits**.

(n=0 or 3)	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	CCPP
R/W	TMnC0	TnPAU	TnCK2	TnCK1	TnCK0	TnON	TnRP2	TnRP1	TnRP0	0x00
R/W	TMnC1	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR	0x00
R	TMnDL	D7	D6	D5	D4	D3	D2	D1	D0	0x00
R	TMnDH	—	—	—	—	—	—	D9	D8	0x00
R/W	TMnAL	D7	D6	D5	D4	D3	D2	D1	D0	0x00
R/W	TMnAH	—	—	—	—	—	—	D9	D8	0x00



CTM	Name	TM No.	TM Input Pin	TM Output Pin
HT66F20	10-bit CTM	0	TCK0	TP0_0
HT66F30	10-bit CTM	0	TCK0	TP0_0, TP0_1
HT66F40	10-bit CTM	0	TCK0	TP0_0, TP0_1
HT66F50	10-bit CTM	0, 3	TCK0, TCK3	TP0_0, TP0_1, TP3_0, TP3_1
HT66F60	10-bit CTM	0, 3	TCK0, TCK3	TP0_0, TP0_1, TP3_0, TP3_1



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## Holtek – Compact Type TM / TMnC0 Register (for TM0 or TM3)



Bit	7	6	5	4	3	2	1	0
Name	TnPAU	TnCK2	TnCK1	TnCK0	TnON	TnRP2	TnRP1	TnRP0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

**Bit 7 TnPAU:** TMn Counter Pause Control

- 0: Run
- 1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the TM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

**Bit 6~4 TnCK2~TnCK0:** Select TMn Counter clock

- 000: f<sub>SYS</sub>
- 001: f<sub>SYS</sub>
- 010: f<sub>H</sub>/16
- 011: f<sub>H</sub>/64
- 100: f<sub>TBC</sub>
- 101: Undefined
- 110: TCKn rising edge clock
- 111: TCKn falling edge clock

These three bits are used to select the clock source for the TM. Selecting the Reserved clock input will effectively disable the internal counter. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source f<sub>SYS</sub> is the system clock, while f<sub>H</sub> and f<sub>TBC</sub> are other internal clocks.

**Bit 3 TnON:** TMn Counter On/Off Control

- 0: Off → internal counter resets to 0
- 1: On      output pin=initial condition specified by TnOC

This bit controls the overall on/off function of the TM. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value. If the TM is in the Compare Match Output Mode then the TM output pin will be reset to its initial condition, as specified by the TnOC bit, when the TnON bit changes from low to high.

**Bit 2~0 TnRP2~TnRP0:** TMn CCRP 3-bit register, compared with the TMn Counter bit 9~bit 7. Comparator P Match Period :

- |                      |                     |
|----------------------|---------------------|
| 000: 1024 TMn clocks | 001: 128 TMn clocks |
| 010: 256 TMn clocks  | 011: 384 TMn clocks |
| 100: 512 TMn clocks  | 101: 640 TMn clocks |
| 110: 768 TMn clocks  | 111: 896 TMn clocks |

These three bits are used to setup the value on the internal CCRP 3-bit register, which are then compared with the internal counter's highest three bits. The result of this comparison, i.e. match, can be selected to clear the internal counter if the TnCCLR bit is set to zero. Clearing all three bits to zero is in effect allowing the counter to overflow at its maximum value.

# Holtek – Compact Type TM / TMnC1 Register



Bit	7	6	5	4	3	2	1	0
Name	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

**Bit 7~6 TnM1~TnM0:** Select TMn Operating Mode

- 00: Compare Match Output Mode *The TM output pin is controlled only by the TnAF interrupt flag*
- 01: Undefined
- 10: PWM Mode
- 11: Timer/Counter Mode

These bits setup the required operating mode for the TM. To ensure reliable operation, the TM should be switched off before any changes are made to the TnM1 and TnM0 bits. In the Timer/Counter Mode, the TM output pin control must be disabled. (TMPC0:T0CP0, T3CP0; TMPC1:T0CP1, T3CP1)

**Bit 5~4 TnIO1~TnIO0:** Select TPn\_0, TPn\_1 output function

**Compare Match Output Mode** *因為輸出架構預設自動反相*

- 00: No change
- 01: Output low *high*
- 10: Output high *low*
- 11: Toggle output

**PWM Mode** *因為輸出架構預設自動反相*

- 00: PWM output inactive state *與[3]設定的level相同*
- 01: PWM output active state *與[3]設定的level相反*
- 10: PWM output

**11: Undefined**

**Timer/counter Mode**

**Unused**

These two bits are used to determine how the TM output pin changes state when a certain condition is reached.

The function that these bits select depends upon in which mode the TM is running.

In the Compare Match Output Mode, the TnIO1 and TnIO0 bits determine how the TM output pin changes state when a compare match occurs from the Comparator A. The TM output pin can be setup to switch high, switch low or to toggle its present state when a compare match occurs from the Comparator A. When the bits are both zero, then no change will take place on the output. The initial value of the TM output pin should be setup using the TnOC bit in the TMnC1 register. Note that the output level requested by the TnIO1 and TnIO0 bits must be different from the initial value setup using the TnOC bit otherwise no change will occur on the TM output pin when a compare match occurs. After the TM output pin changes state it can be reset to its initial level by changing the level of the TnON bit from low to high.

In the PWM Mode, the TnIO1 and TnIO0 bits determine how the TM output pin changes state when a certain compare match condition occurs. The PWM output function is modified by changing these two bits. It is necessary to change the values of the TnIO1 and TnIO0 bits only after the TMn has been switched off. Unpredictable PWM outputs will occur if the TnIO1 and TnIO0 bits are changed when the TM is running.

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# Holtek – Compact Type TM / TMnC1 Register



Bit	7	6	5	4	3	2	1	0
Name	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

*因為輸出架構自動反相*

**Bit 3 TnOC:** TPn\_0, TPn\_1 Output control bit

**Compare Match Output Mode**

- 0: Initial low *high*
- 1: Initial high *low*

**PWM Mode** *因為輸出架構預設自動反相*

- 0: Active low *high* *active等同turn-on initial*
- 1: Active high *low*

This is the output control bit for the TM output pin. Its operation depends upon whether TM is being used in the Compare Match Output Mode or in the PWM Mode. It **has no effect if the TM is in the Timer/Counter Mode**.

**In the Compare Match Output Mode it determines the logic level of the TM output pin before a compare match occurs. In the PWM Mode it determines if the PWM signal is active high or active low.** (initial state)

**Bit 2 TnPOL:** TPn\_0, TPn\_1 Output polarity Control

- 0: Non-invert
- 1: Invert

This bit controls the polarity of the TPn\_0 or TPn\_1 output pin. When the bit is set high the TM output pin will be inverted and not inverted when the bit is zero. **It has no effect if the TM is in the Timer/Counter Mode**.

**Bit 1 TnDPX:** TMn PWM period/duty Control

0: CCRP - period; CCRA - duty *CCRA~CCRP才是active level*

1: CCRP - duty; CCRA - period *CCRP-CCRA才是active level*

This bit, determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

**Bit 0 TnCCLR:** Select TMn Counter clear condition

- 0: TMn Comparatr P match
- 1: TMn Comparatr A match

This bit is used to select the method which clears the counter. Remember that the Compact TM contains two comparators, either of which can be selected to clear the internal counter. With the TnCCLR bit set high, the counter will be cleared when a compare match occurs from the Comparator A. When the bit is low, the counter will be cleared when a compare match occurs from the Comparator P or with a counter overflow. *A counter overflow clearing method can only be implemented if the CCRP bits are all cleared to zero. The TnCCLR bit is not used in the PWM Mode.*

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## Holtek – Compact Type TM / TMPC0 Register



Bit	7	6	5	4	3	2	1	0
Name	T1ACP0	T1BCP2	T1BCP1	T1BCP0	—	—	T0CP1	T0CP0
R/W	R/W	R/W	R/W	R/W	—	—	R/W	R/W
POR	1	0	0	1	—	—	0	1

**Bit 7 T1ACP0:** TP1A pin Control

0: Disable

1: Enable

**Bit 6 T1BCP2:** TP1B\_2 pin Control

0: Disable

1: Enable

**Bit 5 T1BCP1:** TP1B\_1 pin Control

0: Disable

1: Enable

**Bit 4 T1BCP0:** TP1B\_0 pin Control

0: Disable

1: Enable

**Bit 3~2** Unimplemented, read as “0”**Bit 1 T0CP1:** TP0\_1 pin Control

0: Disable

1: Enable

**Bit 0 T0CP0:** TP0\_0 pin Control

0: Disable

1: Enable

**Default Setting :**t1acp0=1;t1bcp2=0;t1bcp1=0;t1bcp0=0;t0cp1=0;t0cp0=1;

For the pin labelled as “0”, its related control bit has a default value of “1”. This means that the pin has a default state of acting as a TM input/output pin.

For the pin labelled as a value other than “0”, its related control bit has a default value of “0”. This means that the pin has a default state of retaining its original function other than a TM input/output pin.



## Holtek – Compact Type TM / TMPC1 Register



Bit	7	6	5	4	3	2	1	0
Name	—	—	T3CP1	T3CP0	—	—	T2CP1	T2CP0
R/W	—	—	R/W	R/W	—	—	R/W	R/W
POR	—	—	0	1	—	—	0	1

Bit 7~6 Unimplemented, read as “0”

**Bit 5 T3CP1:** TP3\_1 pin Control

0: Disable

1: Enable

**Bit 4 T3CP0:** TP3\_0 pin Control

0: Disable

1: Enable

Bit 3~2 Unimplemented, read as “0”

**Bit 1 T2CP1:** TP2\_1 pin Control

0: Disable

1: Enable

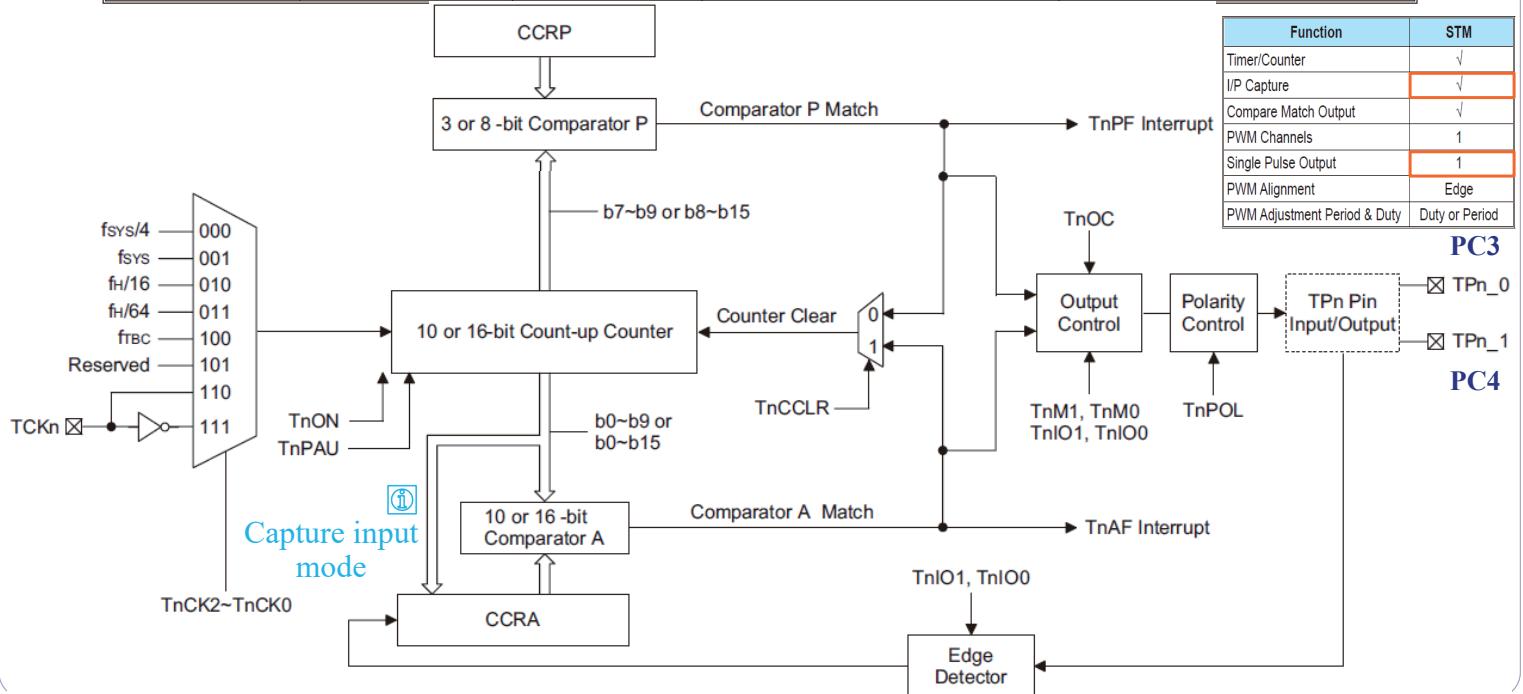
**Bit 0 T2CP0:** TP2\_0 pin Control

0: Disable

1: Enable



STM	Name	TM No.	TM Input Pin	TM Output Pin
HT66F20	10-bit STM	1	TCK1	TP1_0, TP1_1
HT66F30	—	—	—	—
HT66F40	16-bit STM	2	TCK2	TP2_0, TP2_1
HT66F50	16-bit STM	2	TCK2	TP2_0, TP2_1
HT66F60	16-bit STM	2	TCK2	TP2_0, TP2_1



- Overall operation of the **Standard TM** is controlled using a series of registers.
- A read only register pair exists to store the **internal counter 10 (TM1) or 16-bit (TM2) value**, while a read/write register pair exists to store the **internal 10 or 16-bit CCRA value**.
- The remaining two registers are control registers which setup the different operating and control modes as well as the three or eight CCRP bits.

**TM2**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TM2C0	T2PAU	T2CK2	T2CK1	T2CK0	T2ON	—	—	—
TM2C1	T2M1	T2M0	T2IO1	T2IO0	T2OC	T2POL	T2DPX	T2CCLR
TM2DL	D7	D6	D5	D4	D3	D2	D1	D0
TM2DH	D15	D14	D13	D12	D11	D10	D9	D8
TM2AL	D7	D6	D5	D4	D3	D2	D1	D0
TM2AH	D15	D14	D13	D12	D11	D10	D9	D8
TM2RP	D7	D6	D5	D4	D3	D2	D1	D0

**TM0, 3**

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
TMnC0	TnPAU	TnCK2	TnCK1	TnCK0	TnON	TnRP2	TnRP1	TnRP0
TMnC1	TnM1	TnM0	TnIO1	TnIO0	TnOC	TnPOL	TnDPX	TnCCLR
TMnDL	D7	D6	D5	D4	D3	D2	D1	D0
TMnDH	—	—	—	—	—	—	D9	D8
TMnAL	D7	D6	D5	D4	D3	D2	D1	D0
TMnAH	—	—	—	—	—	—	D9	D8



Bit	7	6	5	4	3	2	1	0
Name	T2PAU	T2CK2	T2CK1	T2CK0	T2ON	—	—	—
R/W	R/W	R/W	R/W	R/W	R/W	—	—	—
POR	0	0	0	0	0	—	—	—

**Bit 7 T2PAU:** TM2 Counter Pause Control

0: Run                            1: Pause

The counter can be paused by setting this bit high. Clearing the bit to zero restores normal counter operation. When in a Pause condition the TM will remain powered up and continue to consume power. The counter will retain its residual value when this bit changes from low to high and resume counting from this value when the bit changes to a low value again.

**Bit 6~4 T2CK2, T2CK1, T2CK0:** Select TM2 Counter clock000:  $f_{SYS}$ 001:  $f_{SYS}$ 010:  $f_H/16$ 011:  $f_H/64$ 100:  $f_{TBC}$ 

101: Undefined

110: TCK2 rising edge clock

111: TCK2 falling edge clock

These three bits are used to select the clock source for the TM. Selecting the Reserved clock input will effectively disable the internal counter. The external pin clock source can be chosen to be active on the rising or falling edge. The clock source  $f_{SYS}$  is the system clock, while  $f_H$  and  $f_{TBC}$  are other internal clocks.

**Bit 3 T2ON:** TM2 Counter On/Off Control

0: Off                            1: On

This bit controls the overall on/off function of the TM. Setting the bit high enables the counter to run, clearing the bit disables the TM. Clearing this bit to zero will stop the counter from counting and turn off the TM which will reduce its power consumption. When the bit changes state from low to high the internal counter value will be reset to zero, however when the bit changes from high to low, the internal counter will retain its residual value until the bit returns high again. If the TM is in the Compare Match Output Mode then the TM output pin will be reset to its initial condition, as specified by the T2OC bit, when the T2ON bit changes from low to high.

**Bit 2~0** Unimplemented, read as “0”

Bit	7	6	5	4	3	2	1	0
Name	T2M1	T2M0	T2IO1	T2IO0	T2OC	T2POL	T2DPX	T2CCLR
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

**Bit 7~6 T2M1~T2M0:** Select TM2 Operating Mode

00: Compare Match Output Mode

01: Capture Input Mode

10: PWM Mode or **Single Pulse Output Mode**

11: Timer/Counter Mode

These bits setup the required operating mode for the TM.

To ensure reliable operation the TM should be switched off before any changes are made to the T2M1 and T2M0 bits. In the Timer/Counter Mode, the TM output pin control must be disabled. (TMPC1 : T2CP0, T2CP1)

**Bit 5~4 T2IO1~T2IO0:** Select TP2\_0, TP2\_1 output function

Compare Match Output Mode

00: No change	01: Output low
10: Output high	11: Toggle output

PWM Mode/Single Pulse Output Mode

00: PWM output inactive state	
01: PWM output active state	
10: PWM output	11: Single pulse output

**Capture Input Mode**

00: Input capture at rising edge of TP2_0, TP2_1	
01: Input capture at falling edge of TP2_0, TP2_1	
10: Input capture at falling/rising edge of TP2_0, TP2_1	
11: Input capture disabled	

Timer/counter Mode:

Unused

These two bits are used to determine how the TM output pin changes state when a certain condition is reached. The function that these bits select depends upon in which mode the TM is running.

**Bit 3 T2OC: TP2\_0, TP2\_1 Output control bit**

Compare Match Output Mode

0: Initial low	1: Initial high
PWM Mode/ Single Pulse Output Mode <i>active 等同turn-on initial</i>	
0: Active low	1: Active high

**It has no effect if the TM is in the Timer/Counter Mode.****Bit 2 T2POL: TP2\_0, TP2\_1 Output polarity Control**

0: Non-invert

1: Invert

**It has no effect if the TM is in the Timer/Counter Mode.****Bit 1 T2DPX: TM2 PWM period/duty Control**

0: CCRP - period; CCRA - duty

1: CCRP - duty; CCRA - period

This bit, determines which of the CCRA and CCRP registers are used for period and duty control of the PWM waveform.

**Bit 0 T2CCLR: Select TM2 Counter clear condition**

0: TM2 Comparator P match      1: TM2 Comparator A match



## ♦ TM2DL Register - 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0      **TM2DL:** TM2 Counter Low Byte Register bit 7~bit 0

TM2 16-bit Counter bit 7~bit 0

## ♦ TM2DH Register - 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R	R	R	R	R	R	R	R
POR	0	0	0	0	0	0	0	0

Bit 7~0      **TM2DH:** TM2 Counter High Byte Register bit 7~bit 0

TM2 16-bit Counter bit 15~bit 8

## ♦ TM2AL Register - 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0      **TM2AL:** TM2 CCRA Low Byte Register bit 7~bit 0

TM2 16-bit CCRA bit 7~bit 0



## ♦ TM2AH Register - 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D15	D14	D13	D12	D11	D10	D9	D8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0      **TM2AH:** TM2 CCRA High Byte Register bit 7~bit 0

TM2 16-bit CCRA bit 15~bit 8

## ♦ TM2RP Register - 16-bit STM

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0      **TM2RP:** TM2 CCRP Register bit 7 ~ bit 0

TM2 CCRP 8-bit register, compared with the TM2 Counter bit 15 ~ bit 8. Comparator P Match Period

**0: 65536 TM2 clocks****1~255: 256 x (1~255) TM2 clocks**

These eight bits are used to setup the value on the internal CCRP 8-bit register, which are then compared with the internal counter's highest eight bits. The result of this comparison can be selected to clear the internal counter if the T2CCLR bit is set to zero. Setting the T2CCLR bit to zero ensures that a compare match with the CCRP values will reset the internal counter. As the CCRP bits are only compared with the highest eight counter bits, the compare values exist in 256 clock cycle multiples. **Clearing all eight bits to zero is in effect allowing the counter to overflow at its maximum value.**

# Holtek – Standard Type TM / PWM Output Mode



- 10-bit STM, PWM Mode, Edge-aligned Mode, TnDPX=0

CCRP	001b	010b	011b	100b	101b	110b	111b	000b
Period	128	256	384	512	640	768	896	1024
Duty	CCRA							

If  $f_{SYS} = 16MHz$ , TM clock source is  $f_{SYS}/4$ , CCRP = 100b and CCRA =128,

The STM PWM output frequency =  $(f_{SYS}/4) / 512 = f_{SYS}/2048 = 7.8125 kHz$ , duty =  $128/512 = 25\%$ .

If the Duty value defined by the CCRA register is equal to or greater than the Period value, then the PWM output duty is 100%.

- 10-bit STM, PWM Mode, Edge-aligned Mode, TnDPX=1

CCRP	001b	010b	011b	100b	101b	110b	111b	000b
Period	CCRA							
Duty	128	256	384	512	640	768	896	1024

The PWM output period is determined by the CCRA register value together with the TM clock while the PWM duty cycle is defined by the CCRP register value.

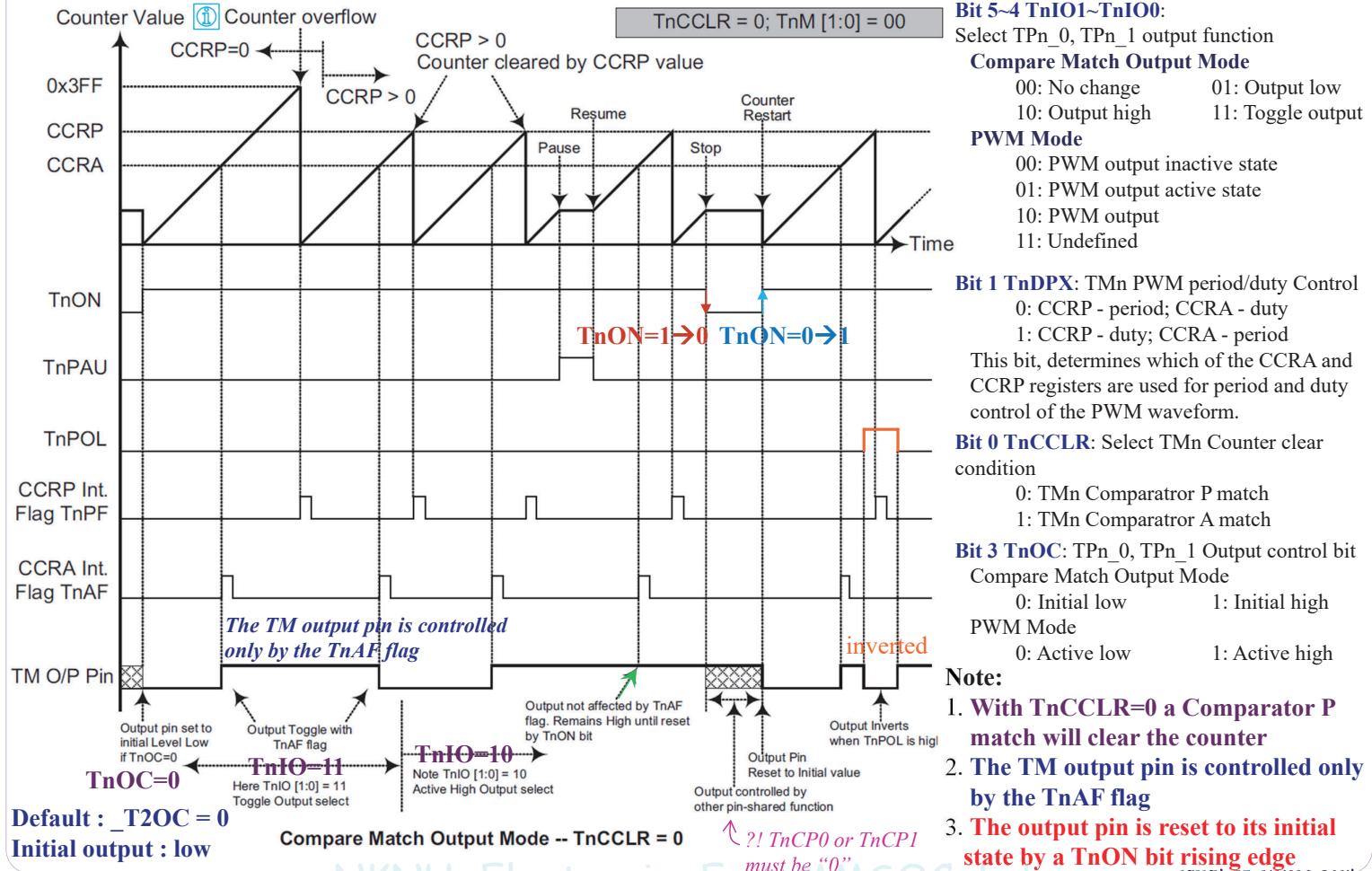
- 16-bit STM, PWM Mode, Edge-aligned Mode, TnDPX=0

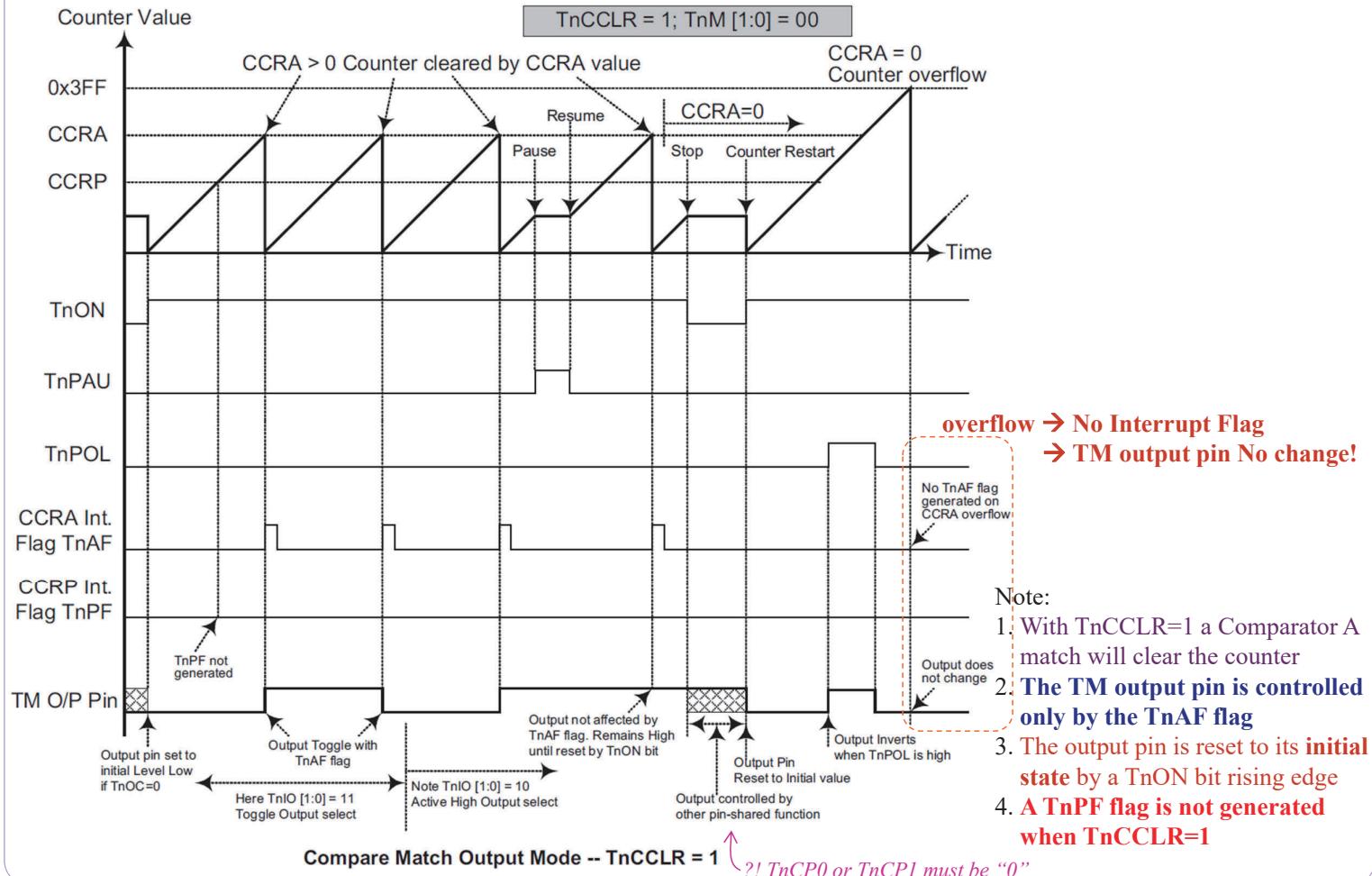
CCRP	1~255	0
Period	CCRP × 256	65536
Duty	CCRA	

- 16-bit STM, PWM Mode, Edge-aligned Mode, TnDPX=1

CCRP	1~255	0
Period	CCRA	
Duty	CCRP × 256	65536

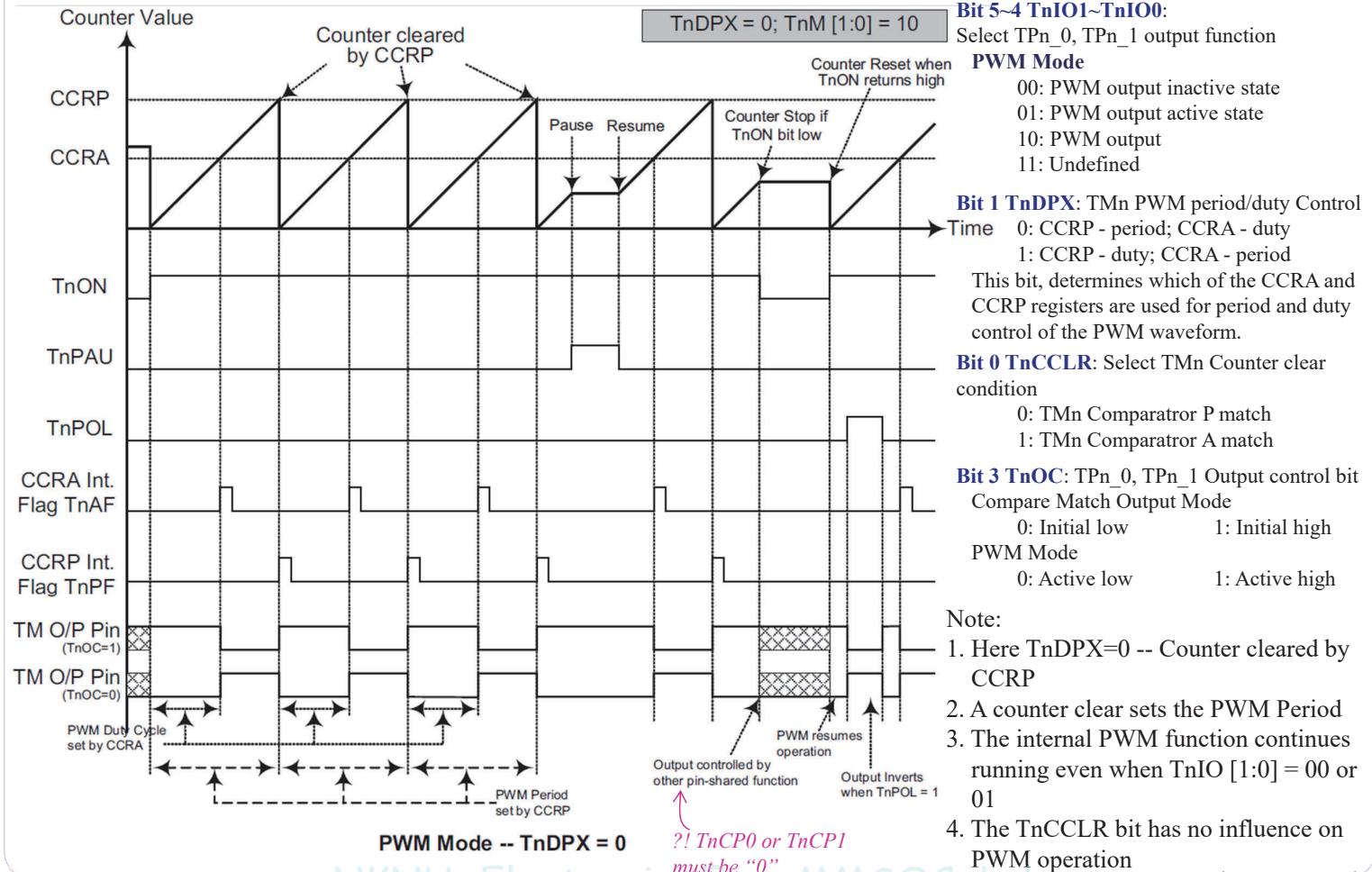
# Holtek – Timer Module / Compare Match Output Mode



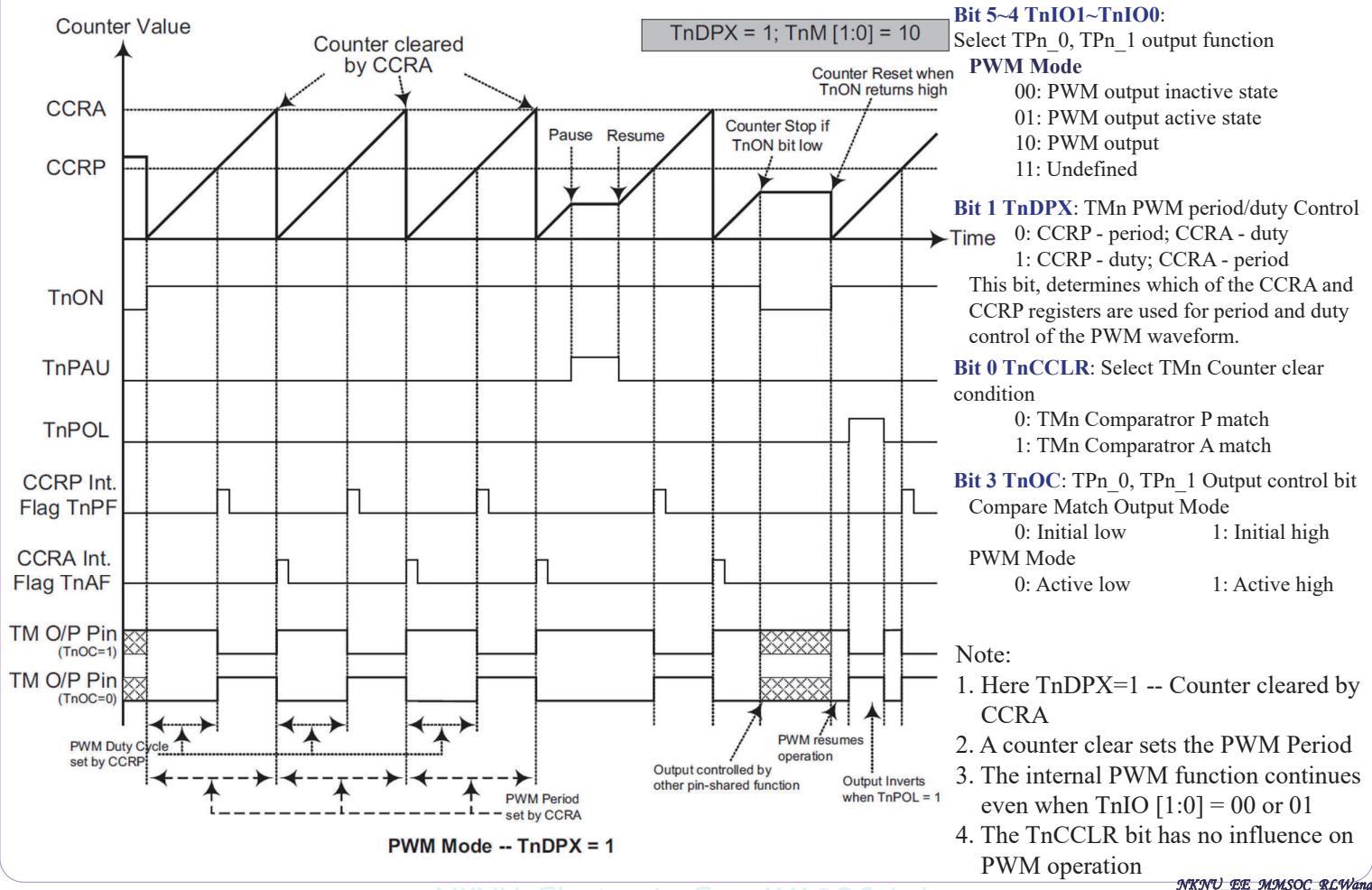


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# Holtek – Timer Module / PWM



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## Holtek – Standard Type TM / Single Pulse Output Mode



- To select this mode, bits **TnM1** and **TnM0** in the **TMnC1** register should be set to **10** respectively and also the **TnIO1** and **TnIO0** bits should be set to **11** respectively.
- The **Single Pulse Output Mode**, as the name suggests, will generate a **single shot pulse** on the TM output pin.
  - ⇒ The **trigger for the pulse output leading edge** is a **low to high transition of the TnON bit**, which can be implemented using the application program.
  - ⇒ However in the **Single Pulse Mode**, the **TnON bit can also be made to automatically change from low to high using the external TCKn pin**, which will in turn initiate the Single Pulse output.
  - ⇒ When the TnON bit transitions to a high level, the counter will start running and the pulse leading edge will be generated.
- The **TnON** bit should **remain high** when the pulse is in its active state.
  - ⇒ The **generated pulse trailing edge** will be generated **when the TnON bit is cleared to zero**, which can be implemented using the application program **or when a compare match occurs from Comparator A**.

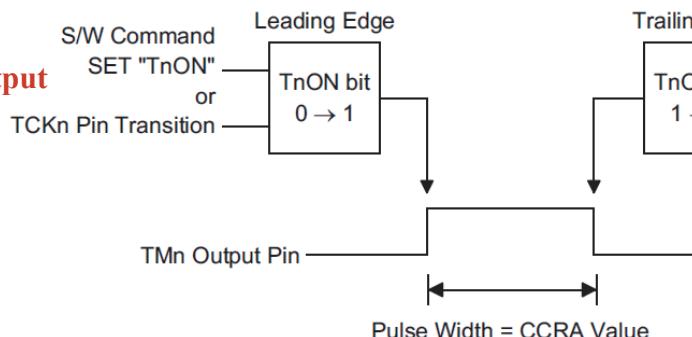
**Trigger for the pulse output leading edge:**

(1)TnON: 0→1

or

(2)TCKn Pin Transition

→TnON: 0→1

**Trigger for the pulse output trailing edge:**

(1)TnON: 1→0

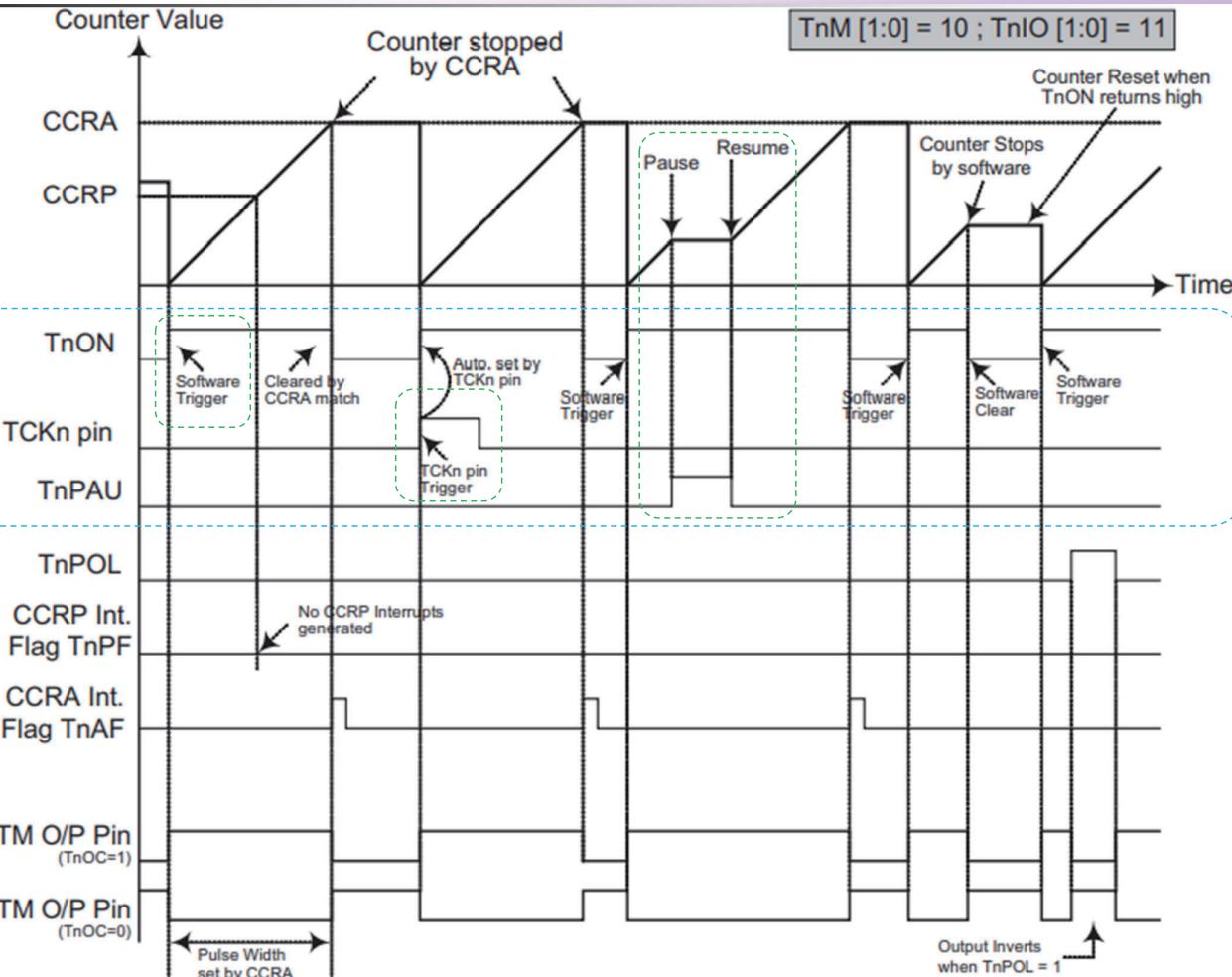
or

(2)CCRA Match Compare

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## Holtek – Standard Type TM / Single Pulse Output Mode



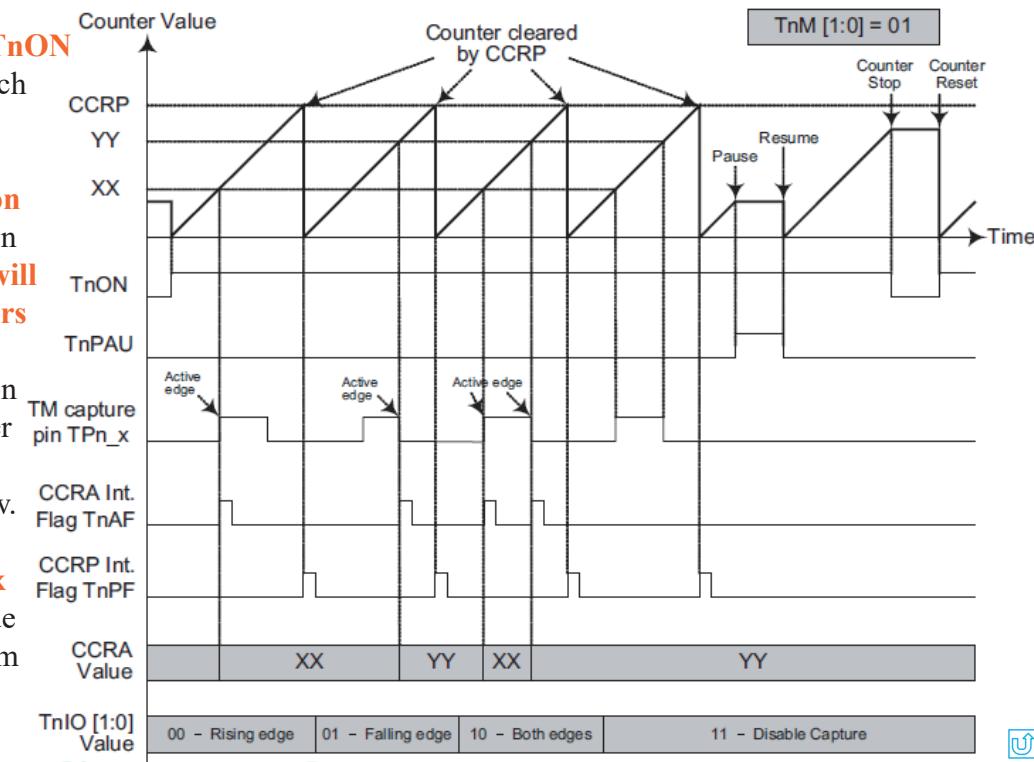
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## Holtek – Standard Type TM / Input Capture Mode

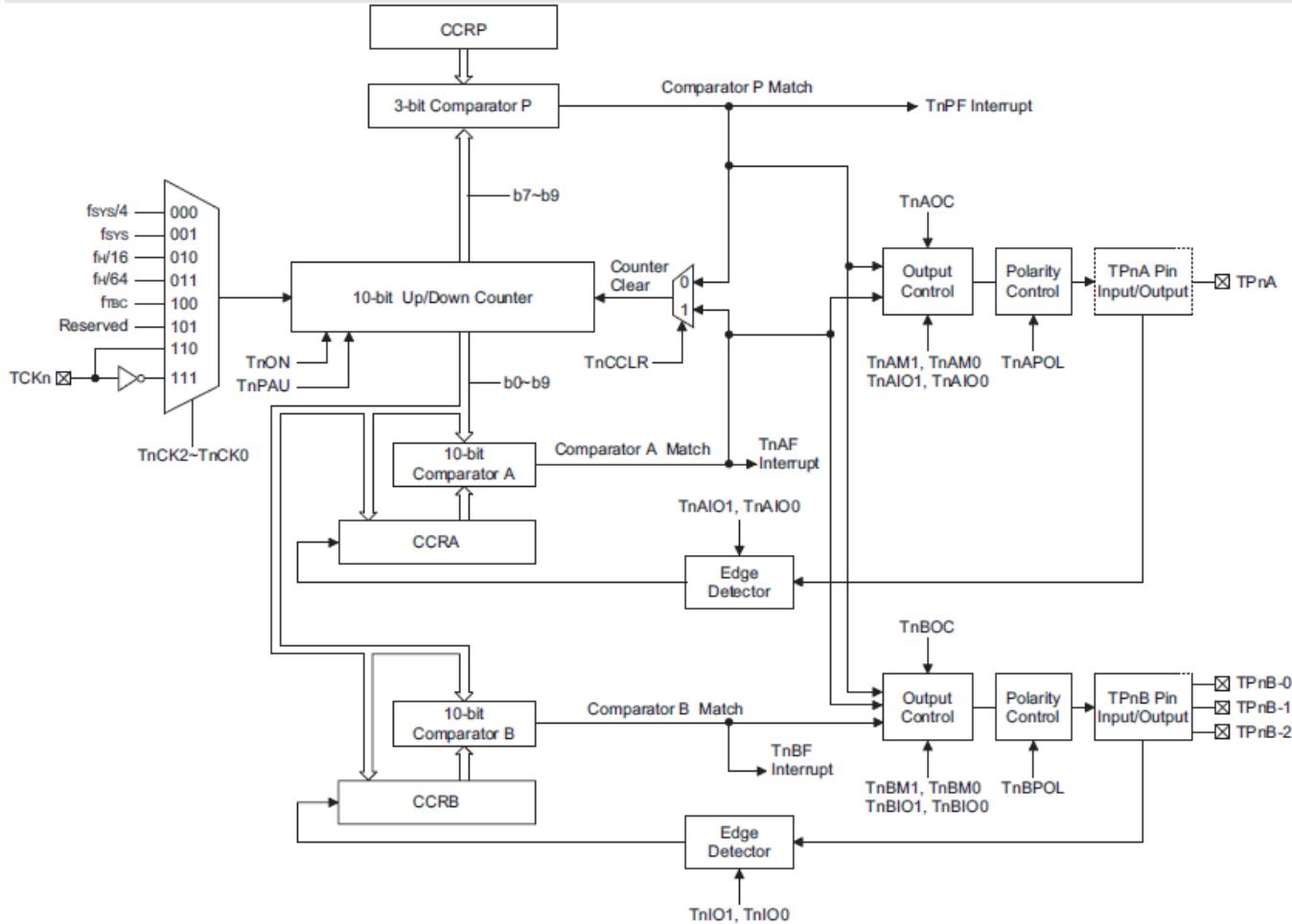


- To select this mode bits **TnM1** and **TnM0** in the **TMnC1** register should be set to **01** respectively. This mode enables external signals to capture and store the present value of the internal counter and can therefore be used for applications such as pulse width measurements.
- The **external signal** is supplied on the **TPn\_0** or **TPn\_1** pin, whose active edge can be either a rising edge, a falling edge or both rising and falling edges; the **active edge transition type** is selected using the **TnIO1** and **TnIO0** bits in the **TMnC1** register.
- The **counter is started when the TnON bit changes from low to high** which is initiated using the application program.
- When the required edge transition appears** on the **TPn\_0** or **TPn\_1** pin **the present value in the counter will be latched into the CCRA registers** and a **TM interrupt generated**.
- Irrespective of what events occur on the **TPn\_0** or **TPn\_1** pin the counter will continue to free run until the **TnON** bit changes from high to low.
- When a **CCRP compare match occurs** the **counter will reset back to zero**; in this way the CCRP value can be used to control the maximum counter value.



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## Holtek – PIN Function



PA0/C0X/TP0_0/AN0	1	48	PA1/TP1A/AN1
PF1/[C1X]	2	47	PA2/TCK0/C0+/AN2
PF0/[C0X]	3	46	PA3/INT0/C0-/AN3
PE7/[INT1]	4	45	PA4/INT1/TCK1/AN4
PE6/[INT0]	5	44	PA5/C1X/SDO/AN5
VSS&AVSS	6	43	PA6/SDI/SDA/AN6
PB4/XT2	7	42	PA7/SCK/SCL/AN7
PB3/XT1	8	41	PB5/SCS/VREF
PB2/OSC2	9	40	PB6/[SDO]
PB1/OSC1	10	39	PB7/[SDI/SDA]
VDD&AVDD	11	38	PD6/[SCK/SCL]
PB0/RES	12	37	PD7/[SCS]
PE5/[TP3_0]	13	36	PC4/[INT0]/[PINT]/TP2_1
PE4/[TP1B_2]	14	35	NC
PC1/TP1B_1/SCOM1	15	34	NC
PC0/TP1B_0/SCOM0	16	33	NC
NC	17	32	PC2/TCK2/PCK/C1+
PC7/[TP1A]/SCOM3	18	31	PC3/PINT/TP2_0/C1-
PC6/[TP0_0]/SCOM2	19	30	PC5/[INT1]/TP0_1/TP1B_2/[PCK]
PE3/[TP3_1]	20	29	PD0/[TCK2]/[SCS]
PE2	21	28	PD1/[TP2_0]/[SDO]/[SCK/SCL]
PE1	22	27	PD2/[TCK0]/[SDI/SDA]
PE0	23	26	PD3/[TCK1]/[SDO]
PD5/[TP0_1]	24	25	PD4/[TP2_1]

HT66F50

48 SSOP-A

- Note:
- Bracketed pin names indicate non-default pinout remapping locations.
  - If the pin-shared pin functions have multiple outputs simultaneously, its pin names at the right side of the / sign can be used for higher priority.
  - VDD&AVDD means the VDD and AVDD are the double bonding.

- MPU的每個接腳均具有多重功能，優先順序為由右至左，也就是說，接腳名稱最右邊的功能，為預設功能，若要將接腳做為純粹數位I/O，必須將其右邊的所有功能關掉。針對目前實驗用到的數位I/O接腳之使用設定，做一些說明。
  - POR(Power on reset)全部預設為ADC的輸入，屬於類比接腳。必須利用指令下列將PORT A八個接腳的AN功能disable。  
`_acerl=0;`  
⇒ PA2, PA3第二優先功能為比較器0的輸入(無pull-high configuration)，若希望規劃是為一般I/O輸出。因此，必須以下列指令關掉此輸入功能。  
`_c0sel=0;`  
// pa2 and pa3 are disconnected c0+ and c0-, respectively, and act as I/O pins  
⇒ PA0第二、三優先功能為TM0輸出與比較器0的輸出，若希望規劃是為一般I/O輸出。因此，必須以下列指令關掉此輸入功能。  
`_c0os=1; // pa0 is disconnected to c0x and purly acts as an I/Opin  
_t0cp0=0; // pa0 is disconnected to TM0 and purly acts as an I/Opin`  
⇒ PA5第二、三優先功能為SDO輸出與比較器1的輸出，若希望規劃規劃是為一般I/O輸出。POR的SDO為浮接狀態，不影響PA5的I/O功能。因此，必須以下列指令關掉此輸入功能。  
`_c1os=1; // pa5 is disconnected to c1x and purly acts as an I/Opin  
_t1cp0=0; // pa5 is disconnected to TM1 and purly acts as an I/Opin`  
⇒ PA1第二優先功能為TM1輸出，若希望規劃是為一般I/O輸出。因此，必須以下列指令關掉此輸入功能。  
`_t1acp0=0;`
  - PC3: POR的預設為比較器1的輸入。若希望規劃是為一般I/O輸出，必須利用下列指令使此功能disable。第二優先功能為TM2輸出，預設是開啟的，若希望規劃為一般I/O輸出，也必須關掉此輸入功能。  
`_c1sel=0;  
_t2cp0=0; // 0: turn off, 1: turn on`
  - PC4: POR的預設為TM2的輸出，但是，預設是關閉。可以直接做為一般I/O輸出。若希望做為TM2的輸出使用，也必須開啟此功能。  
`_t2cp1=1;`

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1. "single pulse output"範例，正常時，無任何脈波輸出，持續按著" F"鍵，每2~3秒輸出單一脈波(\_tm2rp=90)。本實作作業，延續範例功能，加入一個如下功能，持續按著" B"鍵，輸出的脈波寬度較短(\_tm2rp=10)。

2. 請將電子鐘範例中，"時"與"分"的十位數為"0"時，讓該位數的七段顯示數字為全暗。

◆加分題: 延續電子鐘範例，設計一個可切換12H/24H的電子鐘電路，PC0的LED每兩秒閃爍一次，主要有兩個功能，(1)12H顯示模式，PC7的LED暗，表示"12H"模式，AM(中午前)時，四位數七段顯示器僅顯示"時"與"分"；PM(中午後)時，四位數七段顯示器顯示"時"與"分"，且每個數字的小數點持續亮著，以表示"PM"；(2)24H顯示模式，PC7的LED亮，表示"24H"模式，四位數七段顯示器顯示"時"與"分"，且每個數字的小數點持續暗著。

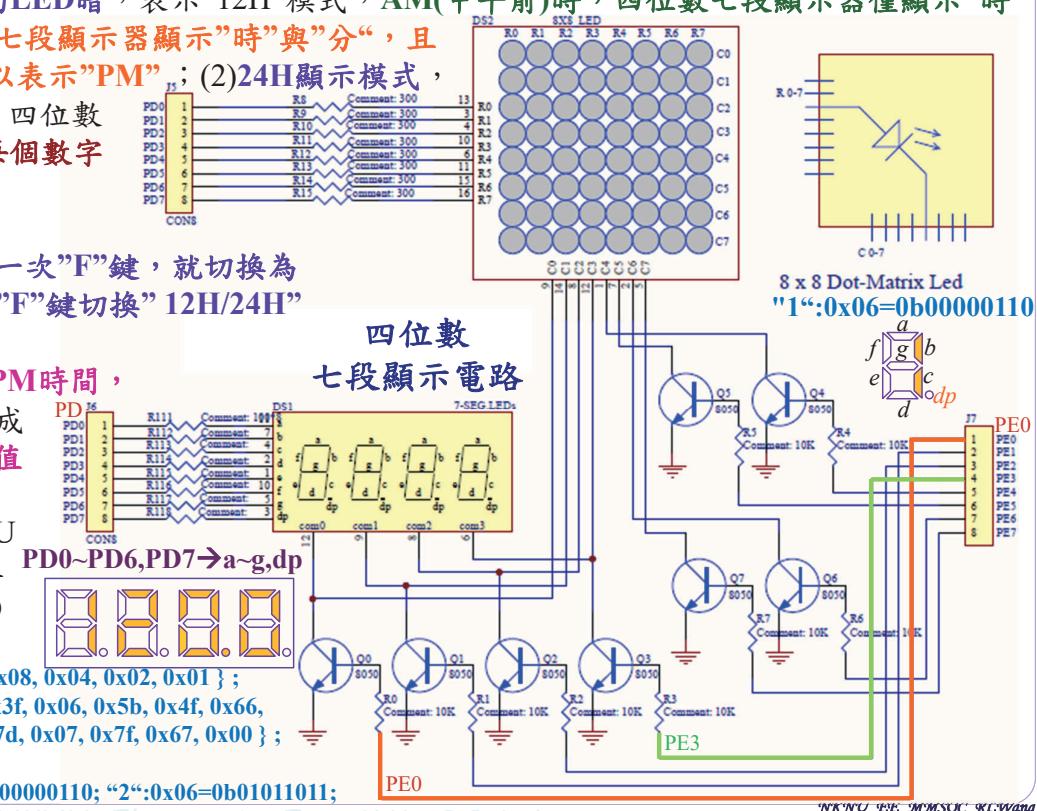
Hint:

(1)起始狀態為"12H"模式，每按一次" F"鍵，就切換為"12H"或"24H"，也就是，以" F"鍵切換"12H/24H"的模式。

(2)當從12H轉成24H模式，若為PM時間，要將"hour"加12。當從24H轉成12H模式，若為時間的小時數值大於11，要將"hour"減12。

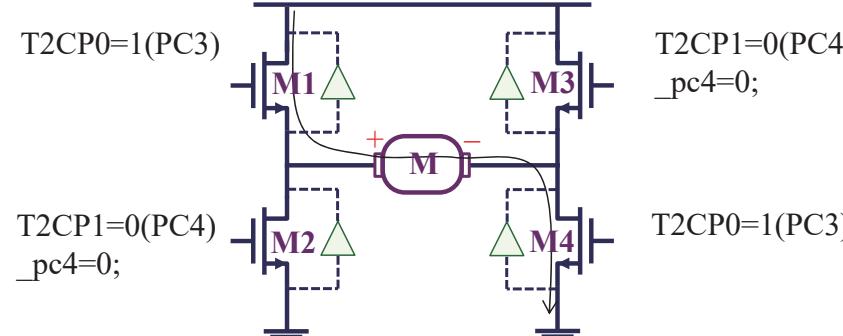
NOTE: 將鍵盤的PA2與PA3接至CPU那邊的PA2與PA3，記得接VCC與GND的接腳，並要將短路到GND的接腳用jump短路。

```
const unsigned char led7com[4] = { 0x08, 0x04, 0x02, 0x01 } ;
const unsigned char led7seg[11]= { 0x3f, 0x06, 0x5b, 0x4f, 0x66,
                                0x6d, 0x7d, 0x07, 0x7f, 0x67, 0x00 } ;
//7-LED: (dp or h)gfedcba
//0":0x3f=0b00111111; "1":0x06=0b000000110; "2":0x06=0b01011011;
```



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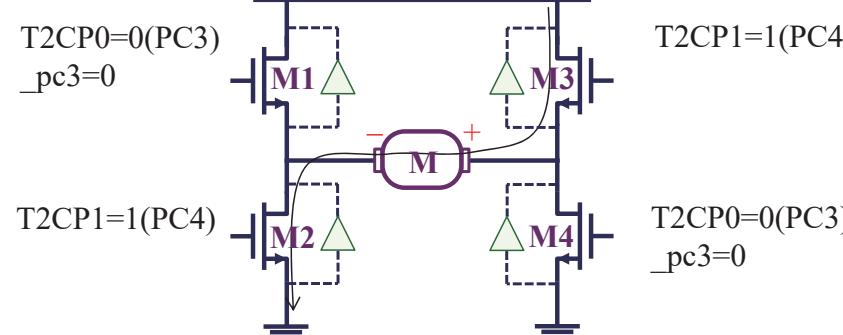
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slower rotation



Faster rotation



快速逆向恢復(fast recovery)二極體作用是在轉動方向切換時，能快速將原來運轉的馬達反電動勢之磁能快速透過二極體釋放掉。(如，M2,M3 ON → M1,M4 ON，反電動勢的磁能能快速透過M1並接的二極體釋放)。

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