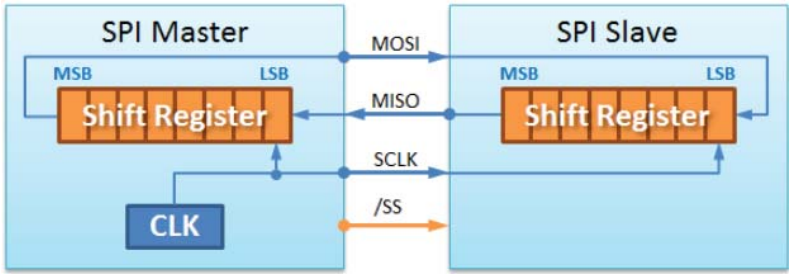
Holtek – Serial Interface Module / SIM

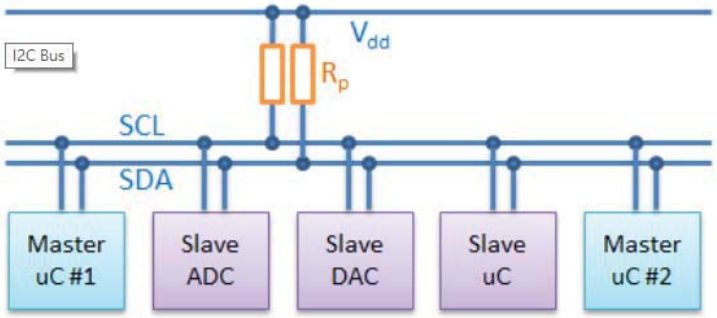
隨著科技的演進, 在單晶片微控制器及 SoC 的領域中, SPI (Serial Peripheral Interface) 及 I²C (Inter-Integrated Circuit)這二種串列 (序列) 介面變得十分常見. 這二者與主機間通訊用的**非同步串列通訊埠** RS-232 (UART) 非常不一樣

- 二個都是**同步傳輸**介面, 主要是用於 CPU 和週邊晶片之間.
- SPI 及 I²C 二者設計的主要目的在於減少 CPU 和週邊晶片之間的接腳數.
- SPI 一般需要 4 條接線 (至少三條), 而 I²C 則只要二條線, 這和早期常用的並列匯流排動輒十數條接線有著明顯的差異.

SPI 的硬體結構簡單而且傳輸速度快, 一般是 5M/10M/20Mbps 或是更快 (可以到 200Mbps), I²C 的傳輸速度則只有 100Kbps/400Kbps/1Mbps(/3.4Mbps/單向5Mbps).

- SPI 是全雙工, I²C 則是半雙工





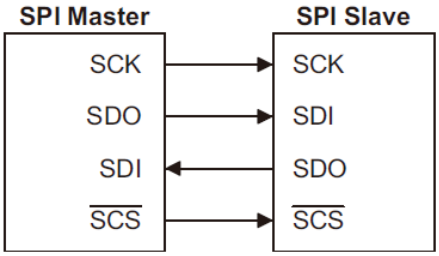
Holtek – Serial Interface Module / SIM

- These devices contain a **Serial Interface Module**, which includes both the **four line SPI interface** or the **two line I²C interface** types, to allow an easy method of communication with external peripheral hardware.
- Having relatively simple communication protocols, these serial interface types **allow the microcontroller to interface to external SPI or I²C based hardware such as sensors, Flash or EEPROM memory**, etc.
- The **SIM interface pins** are **pin-shared with other I/O pins** therefore the **SIM interface function must first be selected using a configuration option**.
- As **both interface types share the same pins and registers**, the **choice** of whether the **SPI or I2C type** is used is made **using the SIM operating mode control bits, named SIM2~SIM0, in the SIMC0 register**.
- These **pull-high resistors** of the SIM pin-shared I/O are selected using **pull-high control registers**, and also if the SIM function is enabled.

- The **four line SPI interface** is a **synchronous serial data interface** that has a relatively simple communication protocol simplifying the programming requirements when communicating with external hardware devices.
  - The **SPI** interface is a **full duplex synchronous serial data link** and operates as a slave/master type, where **the device can be either master or slave**.
  - Although **the SPI interface specification can control multiple slave devices** from a single master, but this device provided **only one SCS pin**.
    - If the master needs to **control multiple slave devices** from a single master, the **master can use I/O pin to select the slave devices**.
  - It is a four line interface with pin names **SDI, SDO, SCK and SCS**.
    - Pins SDI and SDO are the Serial Data Input and Serial Data Output lines, SCK is the Serial Clock line and SCS is the Slave Select line.
    - As the device **only contains a single SCS pin only one slave device can be utilized**.
    - The SCS pin is **controlled by software**, **set CSEN bit to 1 to enable SCS pin function**, **set CSEN bit to 0 the SCS pin will be floating state**.

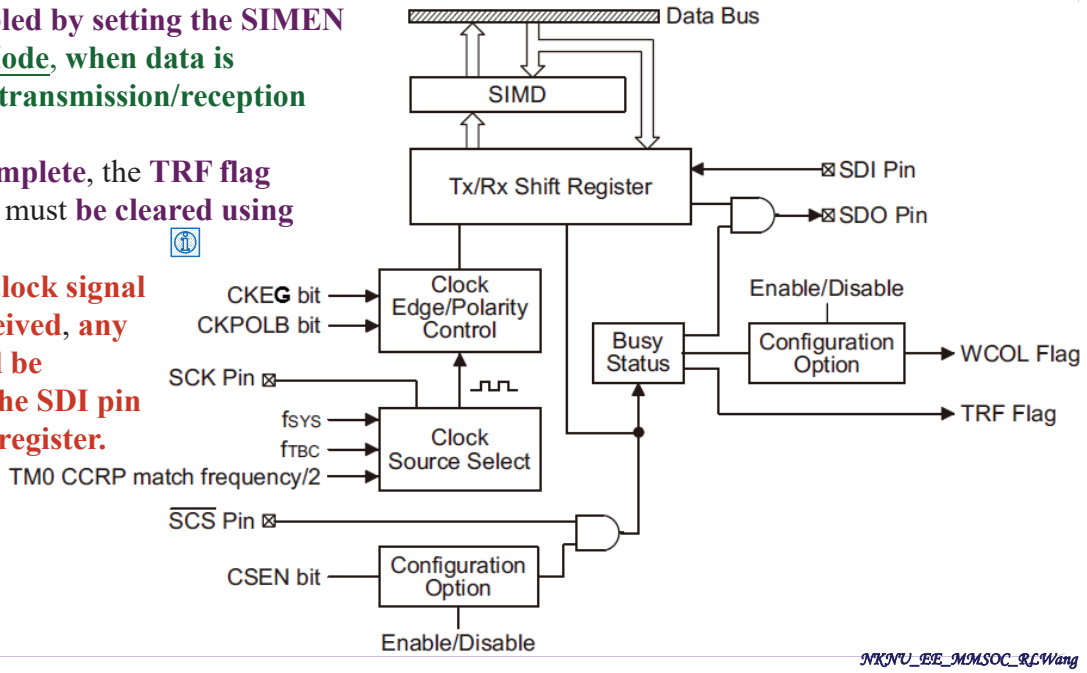
Holtek – Serial Interface Module / SPI

- The SPI function in this device offers the following features:
  - **Full duplex** synchronous data transfer
  - Both Master and Slave modes
  - **LSB first or MSB first** data transmission modes
  - **Transmission complete flag**
  - Rising or falling active clock edge
  - **WCOL and CSEN bit enabled or disable select**



SPI Communication

- After the **SPI interface is enabled by setting the SIMEN bit high**, then **in the Master Mode, when data is written to the SIMD register, transmission/reception will begin simultaneously**.
  - ⇨When the **data transfer** is **complete**, the **TRF flag** will be **set automatically**, but must **be cleared using the application program**.
- **In the Slave Mode**, when the **clock signal from the master has been received**, **any data in the SIMD register will be transmitted** and **any data on the SDI pin will be shifted into the SIMD register.**

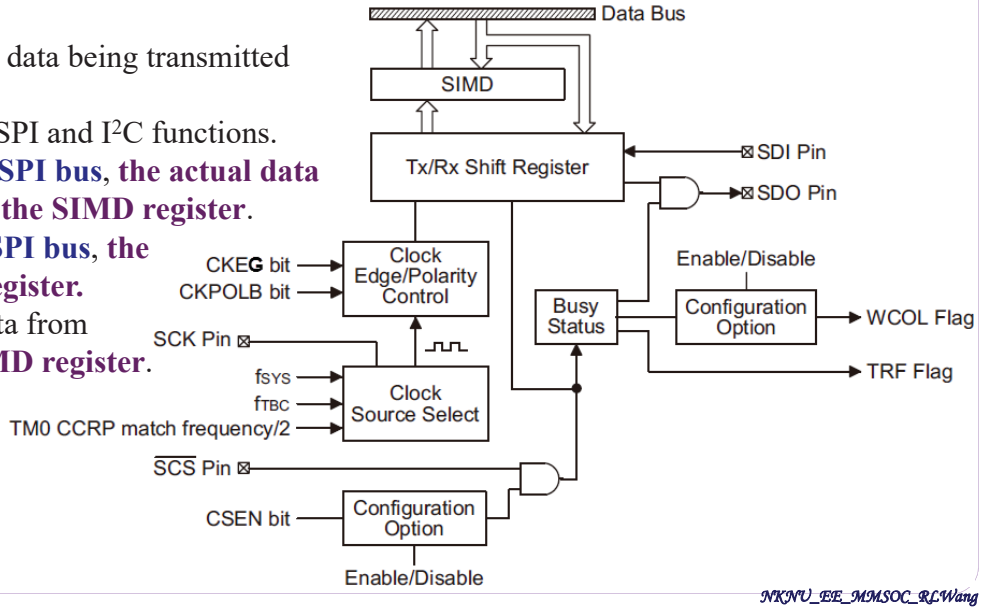


Holtek – Serial Interface Module / SPI Registers

- There are **three internal registers** which control the overall operation of the SPI interface.
  - These are the **SIMD data register** and **two registers SIMC0 and SIMC2**. Note that the **SIMC1 register is only used by the I²C interface**.

Register Name	Bit							
	7	6	5	4	3	2	1	0
SIMC0	SIM2	SIM1	SIM0	PCKEN	PCKP1	PCKP0	SIMEN	—
SIMD	D7	D6	D5	D4	D3	D2	D1	D0
SIMC2	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF

- The **SIMD register** is used to store the data being transmitted and received.
  - The same register is used by both the SPI and I²C functions.
  - **Before the device writes data to the SPI bus, the actual data to be transmitted must be placed in the SIMD register**.
  - **After the data is received from the SPI bus, the device can read it from the SIMD register.**
  - **Any transmission or reception** of data from the SPI bus must be made **via the SIMD register**.



Holtek – Serial Interface Module / SIMC0 Registers

Bit	7	6	5	4	3	2	1	0
Name	SIM2	SIM1	SIM0	PCKEN	PCKP1	PCKP0	SIMEN	—
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	—
POR	1	1	1	0	0	0	0	—

Bit 7~5 SIM2, SIM1, SIM0: SIM Operating Mode Control
000: SPI master mode; SPI clock is $f_{SYS}/4$
001: SPI master mode; SPI clock is $f_{SYS}/16$
010: SPI master mode; SPI clock is $f_{SYS}/64$
011: SPI master mode; SPI clock is f_{TBC}
100: SPI master mode; SPI clock is TM0 CCRP match frequency/2
101: SPI slave mode
110: I²C slave mode
111: Unused mode

These bits **setup the overall operating mode of the SIM function**. As well as selecting if the I²C or SPI function, they are used to **control the SPI Master/Slave selection and the SPI Master clock frequency**. The SPI clock is a function of the system clock but can also be chosen to be sourced from the TM0. If the **SPI Slave Mode is selected** then the **clock will be supplied by an external Master device**.

Bit 4 PCKEN: PCK Output Pin Control
0: Disable 1: Enable

Bit 3~2 PCKP1, PCKP0: Select PCK output pin frequency
00: f_{SYS} 01: $f_{SYS}/4$
10: $f_{SYS}/8$ 11: TM0 CCRP match frequency/2

Bit 1 SIMEN: SIM Control
0: Disable 1: Enable

The bit is the **overall on/off control for the SIM interface**. When the ***SIMEN bit is cleared to zero*** to ***disable the SIM interface***, the ***SDI, SDO, SCK and SCS, or SDA and SCL lines will be in a floating condition*** and the ***SIM operating current will be reduced to a minimum value***. When ***the bit is high the SIM interface is enabled***. The **SIM configuration option must have first enabled the SIM interface for this bit to be effective**. **If the SIM is configured to operate as an SPI interface via the *SIM2~SIM0 bits*, the contents of the SPI control registers will remain at the previous settings when the SIMEN bit changes from low to high and *should therefore be first initialized by the application program*. If the SIM is configured to operate as an I²C interface via the SIM2~SIM0 bits and the SIMEN bit changes from low to high, the contents of the I²C control bits such as HTX and TXAK will remain at the previous settings and should therefore be first initialized by the application program while the relevant I²C flags such as HCF, HAAS, HBB, SRW and RXAK will be set to their default states.**

Bit 0 Unimplemented, read as "0"

Holtek – Serial Interface Module / SIMC2 Registers

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	CKPOLB	CKEG	MLS	CSEN	WCOL	TRF
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~6 Undefined bit

Bit 5 CKPOLB: Determines the **base condition of the clock line**
0: The **SCK** line will be **high** when the **clock is inactive**
1: The **SCK** line will be **low** when the **clock is inactive**
The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive.

Bit 4 CKEG: Determines **SPI SCK active clock edge type**
CKPOLB=0
0: SCK is high base level and **data capture** at SCK **rising edge**
1: SCK is high base level and **data capture** at SCK **falling edge**
CKPOLB=1
0: SCK is low base level and **data capture** at SCK **falling edge**
1: SCK is low base level and **data capture** at SCK **rising edge**
The **CKEG and CKPOLB** bits **are used to setup the way** that the **clock signal outputs** and **inputs data on the SPI bus**. ***These two bits must be configured before data transfer is executed otherwise an erroneous clock edge may be generated.*** The CKPOLB bit determines the base condition of the clock line, if the bit is high, then the SCK line will be low when the clock is inactive. When the CKPOLB bit is low, then the SCK line will be high when the clock is inactive.
The CKEG bit determines active clock edge type which depends upon the condition of CKPOLB bit.

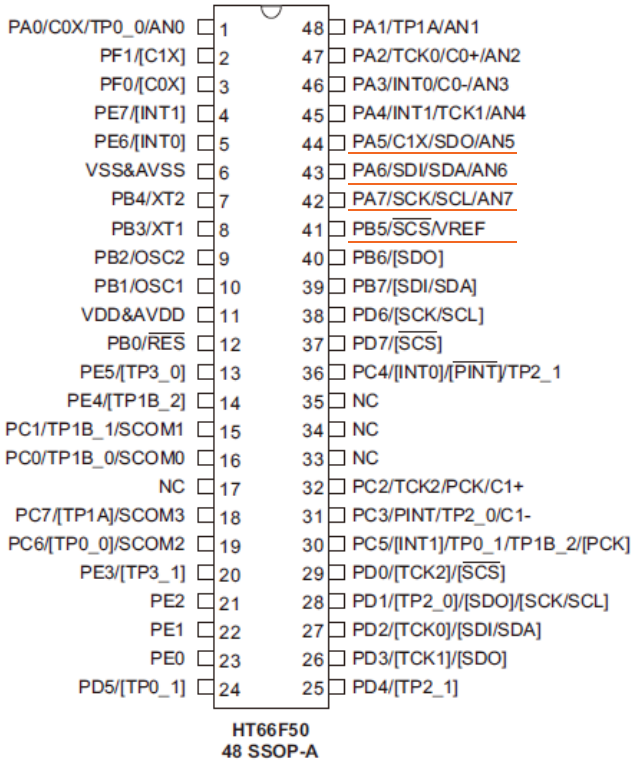
Bit 3 MLS: SPI Data shift order
0: LSB 1: MSB
This is the data shift select bit and is used to select how the data is transferred, **either MSB or LSB first**. Setting the bit high will select MSB first and low for LSB first.

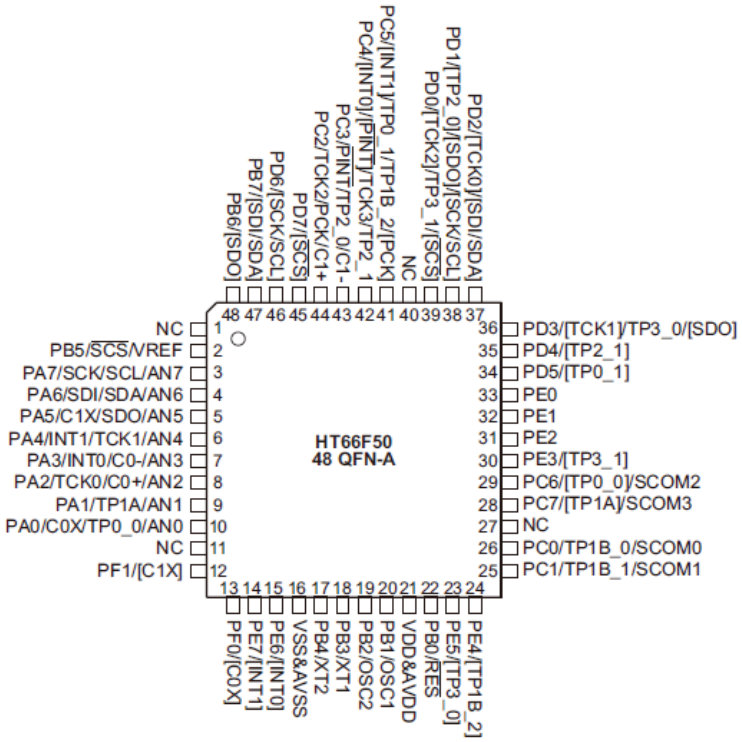
Bit 2 CSEN: SPI $\overline{SCS}$ (SPI Slave Select) pin Control
0: Disable 1: Enable
The CSEN bit is used as an enable/disable for the $\overline{SCS}$ pin. If **this bit is low**, then the $\overline{SCS}$ pin will be disabled and placed into a **floating condition**. If **the bit is high** the $\overline{SCS}$ pin will be enabled and **used as a select pin**. **Note that using the CSEN bit can be disabled or enabled via configuration option**.

Bit 1 WCOL: SPI Write Collision flag
0: No collision 1: Collision
If this bit is **high** it means that **data has been attempted to be written to the SIMD register during a data transfer operation**. This **writing** operation will be **ignored** if data is being transferred.

Bit 0 TRF: SPI Transmit/Receive Complete flag
0: Data is being transferred
1: SPI data transmission is completed
The TRF **bit must set to 0 by the application program**.

Holtek – HT66F50 Pins





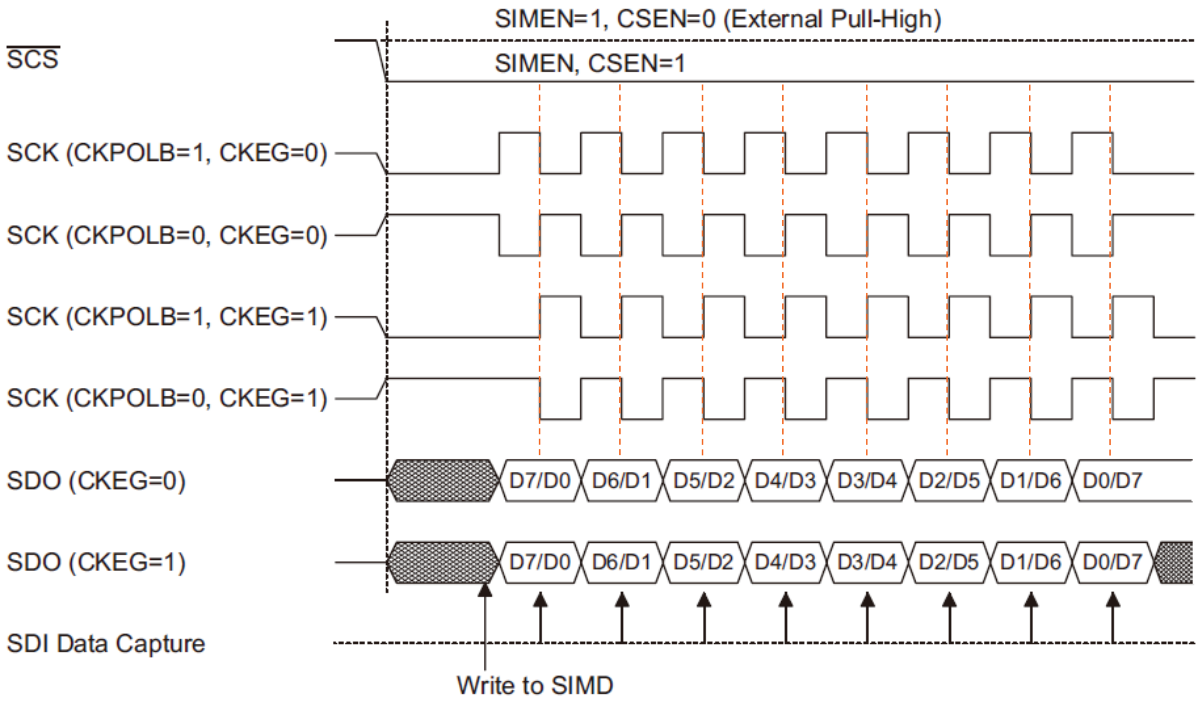
Note:

1. **Bracketed pin names** indicate **non-default pinout remapping locations**.
2. If the pin-shared pin functions have multiple outputs simultaneously, **its pin names at the right side of the / sign can be used for higher priority**.
3. VDD&AVDD means the VDD and AVDD are the double bonding.

Holtek – Serial Interface Module / SPI Master Mode Timing

After the **SPI interface** is enabled by **setting the SIMEN bit high**, then in **the Master Mode**, ***when data is written to the SIMD register, transmission/reception will begin simultaneously***.

- When the data **transfer is complete**, the **TRF flag will be set automatically**, but must be **cleared using the application program**.

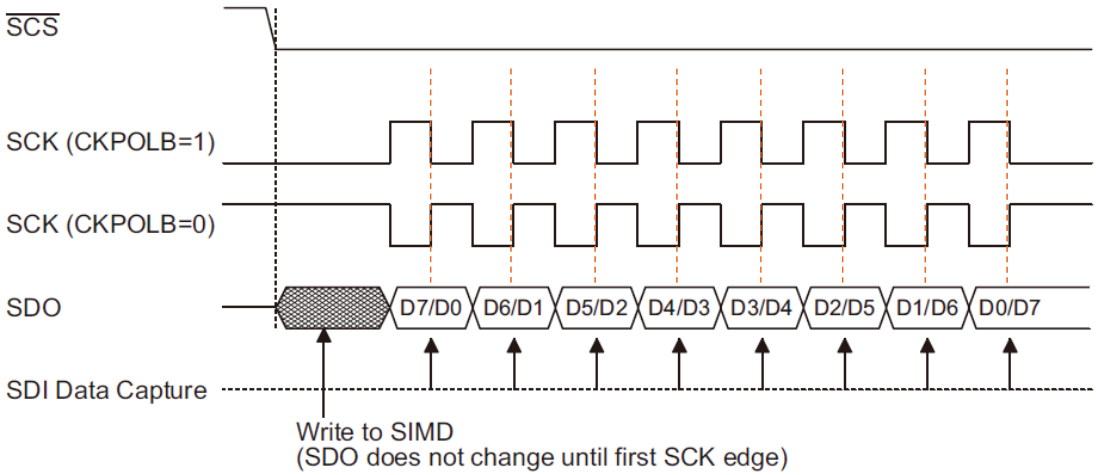


Holtek – Serial Interface Module / SPI Slave Mode Timing

After the **SPI interface** is enabled by **setting the SIMEN bit high**, then in **the Slave Mode**, when **the clock signal from the master has been received, any data in the SIMD register will be transmitted and any data on the SDI pin will be shifted into the SIMD register.**

- The **master should output an $\overline{SCS}$ signal to enable the slave device before a clock signal is provided**.
- The **slave data to be transferred should be well prepared at the appropriate moment relative to the $\overline{SCS}$ signal** depending upon the configurations of the CKPOLB bit and CKEG bit.
- The accompanying timing diagram shows the relationship between the slave data and $\overline{SCS}$ signal for various configurations of the CKPOLB and CKEG bits.
- The **SPI will continue to function even in the IDLE Mode**.

CKEG=0



Note: For SPI slave mode, if SIMEN=1 and CSEN=0, SPI is always enabled and ignores the $\overline{SCS}$ level.

Holtek – Serial Interface Module / SPI Slave Mode Timing

After the **SPI interface** is enabled by **setting the SIMEN bit high**, then in **the Slave Mode**, when the clock signal from the master has been received, any data in the SIMD register will be transmitted and any data on the SDI pin will be shifted into the SIMD register.

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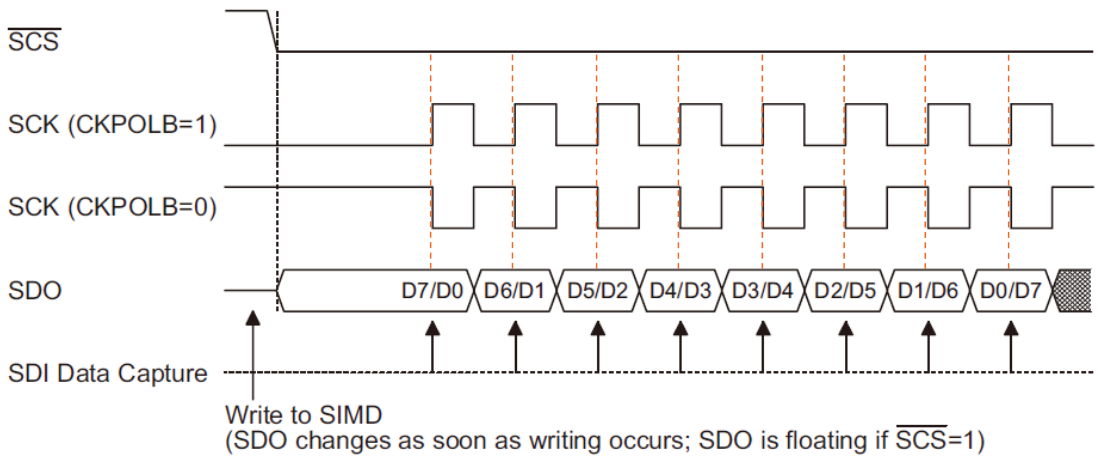
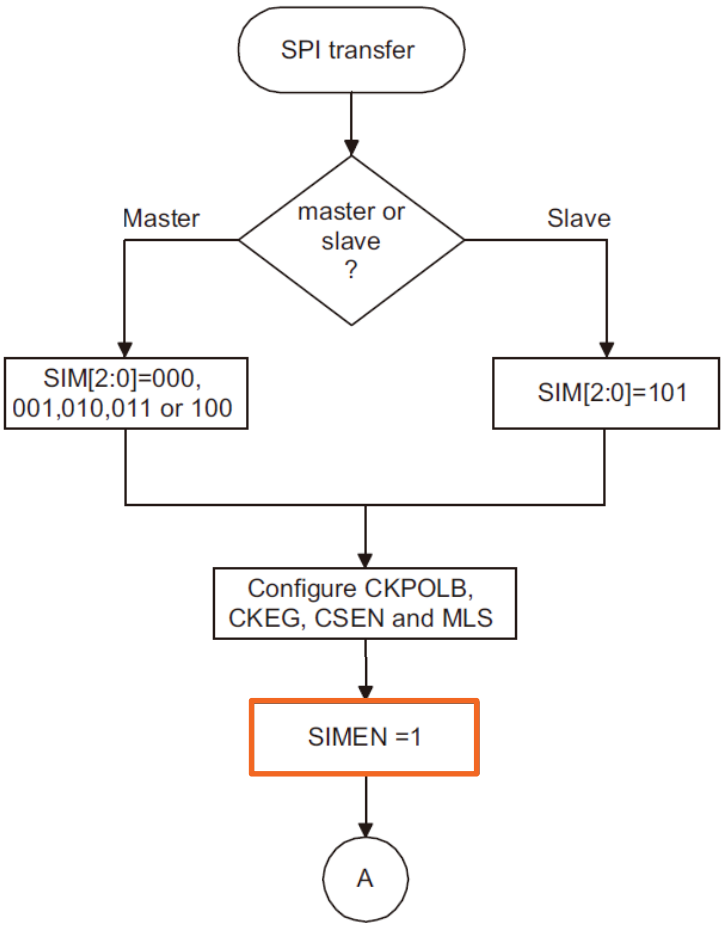
- The accompanying timing diagram shows the relationship between the slave data and $\overline{SCS}$ signal for various configurations of the CKPOLB and CKEG bits.
- The **SPI will continue to function even in the IDLE Mode**.

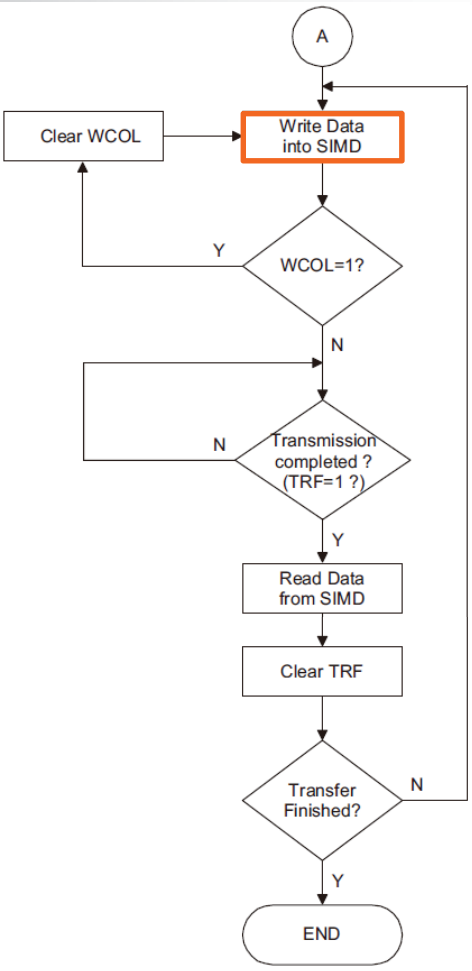
CKEG=1



Note: For SPI slave mode, if SIMEN=1 and CSEN=0, SPI is always enabled and ignores the $\overline{SCS}$ level.

Holtek – Serial Interface Module / SPI Slave Mode Timing





Holtek – Interrupt Structure

- When **an interrupt is generated**, the **Program Counter**, which ***stores the address of the next instruction to be executed***, will **be transferred onto the stack**.

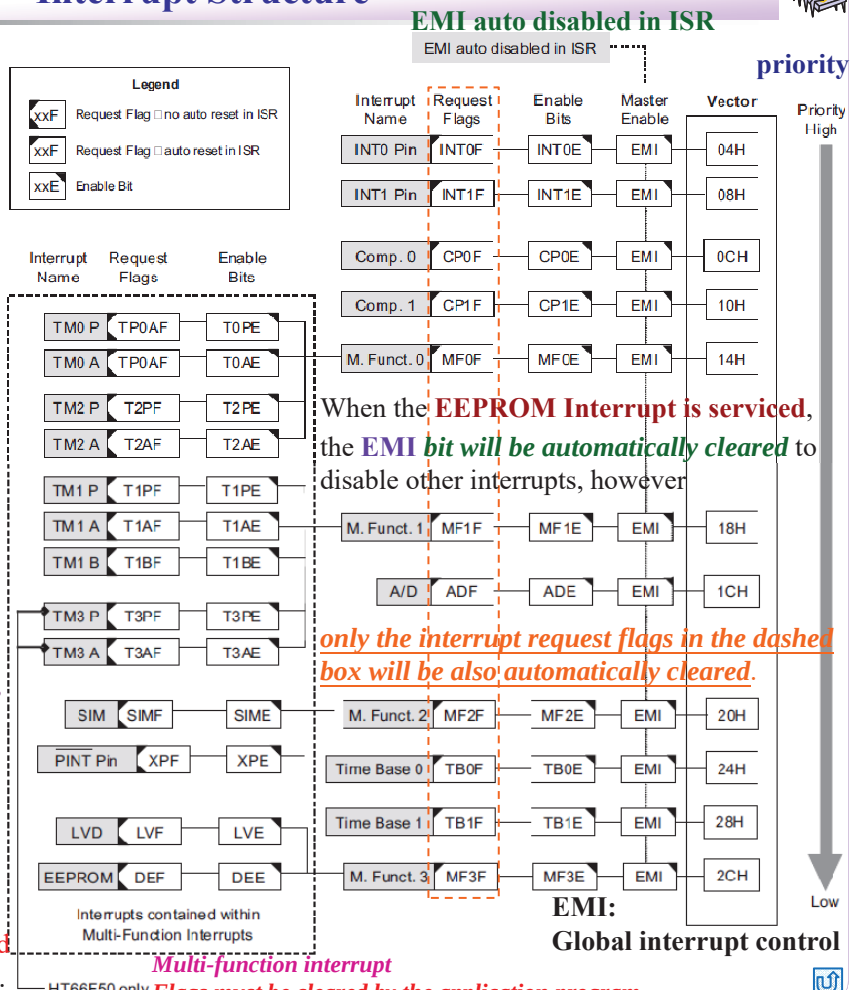
⇨ The **Program Counter** will ***then be loaded with a new address*** which will be the value of the ***corresponding interrupt vector***.

⇨ The microcontroller will then fetch its next instruction from this interrupt vector.

⇨ The ***instruction at this vector will usually be a JMP which will jump to another section of program*** which is known as the ***interrupt service routine***. Here is located the code to control the appropriate interrupt.

⇨ The ***interrupt service routine must be terminated with a RETI***, which ***retrieves the original Program Counter address from the stack and allows the microcontroller to continue with normal execution*** at the point where the interrupt occurred.

The **RETI** instruction in addition to **executing a return to the main program also automatically sets the EMI bit high to allow further interrupts**. The **RET** instruction however only executes a return to the main program ***leaving the EMI bit in its present zero state*** and therefore **disabling the execution of further interrupts**.



When the **EEPROM Interrupt is serviced**, the **EMI** ***bit will be automatically cleared*** to disable other interrupts, however

only the interrupt request flags in the dashed box will be also automatically cleared.