Holtek – Analog to Digital Converter

- **The need of interface to real world of analog signals is a common requirement for many electronic systems.**
  - ⇨However, to properly process these signals by a microcontroller, they must first be converted into digital signals by A/D converters.
  - ⇨By integrating the A/D conversion electronic circuitry into the microcontroller, the need for external components is reduced significantly with the corresponding follow-on benefits of lower costs and reduced component space requirements.

A/D Converter Register Description

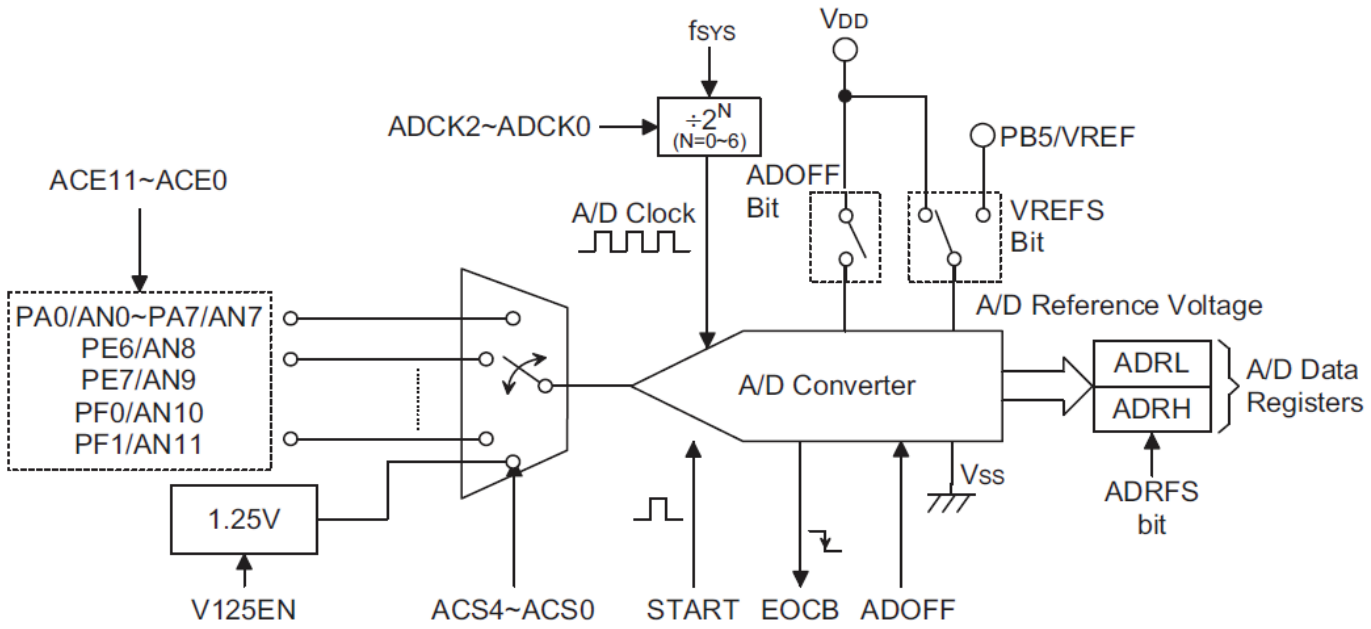
- Overall operation of the A/D converter is **controlled using six registers**.
  - ⇨**A read only register pair** exists to **store the ADC data 12-bit value**.
  - ⇨The **remaining three or four registers** are control registers which setup the operating and control function of the A/D converter.

Part No.	Input Channels	A/D Channel Select Bits	Input Pins
HT66F20 HT66F30 HT66F40 HT66F50	8	ACS4, ACS2~ACS0	AN0~AN7
HT66F60	12	ACS4, ACS3~ACS0	AN0~AN11

Register Name	Bit							
	7	6	5	4	3	2	1	0
ADRL(ADRFS=0)	D3	D2	D1	D0	—	—	—	—
ADRL(ADRFS=1)	D7	D6	D5	D4	D3	D2	D1	D0
ADRH(ADRFS=0)	D11	D10	D9	D8	D7	D6	D5	D4
ADRH(ADRFS=1)	—	—	—	—	D11	D10	D9	D8
ADCR0	START	EOCB	ADOFF	ADRFS	ACS3	ACS2	ACS1	ACS0
ADCR1	ACS4	V125EN	—	VREFS	—	ADCK2	ADCK1	ADCK0
ACERL	ACE7	ACE6	ACE5	ACE4	ACE3	ACE2	ACE1	ACE0
ACERH	—	—	—	—	ACE11	ACE10	ACE9	ACE8

ACERH only available for HT66F60

Holtek – Analog to Digital Converter



Maximum conversion speed (bit/sec) : $f_{ADCK,max}$ is 2MHz

- As the **minimum value of permissible A/D clock period**, t_{ADCK}, is **0.5 μs (i.e. 2MHz)**, care must be taken for system clock frequencies **equal to or greater than 4MHz**.

Holtek – Analog to Digital Converter / ADCR0 Register

Bit	7	6	5	4	3	2	1	0
Name	START	EOCB	ADOFF	ADRFS	ACS3	ACS2	ACS1	ACS0
R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	1	0	0	0	0	0

Bit 7 START: Start the A/D conversion

0→1→0 : start

0→1 : reset the A/D converter and set EOCB to 1

This bit is used to initiate an A/D conversion process.

The bit is normally low but if set high and then cleared low again, the A/D converter will initiate a conversion process.

When the bit is set high the A/D converter will be reset.

Bit 6 EOCB: End of A/D conversion flag

0 : A/D conversion ended

1 : A/D conversion in progress

This read only flag is used to **indicate when an A/D conversion process has completed**.

When the conversion process is running the bit will be high.

Bit 5 ADOFF : ADC module power on/off control bit

0 : ADC module power on

1 : ADC module power off

As the A/D converter will consume a limited amount of power, even when not executing a conversion, this may be an important consideration in power sensitive battery powered applications.

Note: 1. **it is recommended to set ADOFF=1 before entering IDLE/SLEEP Mode for saving power.**

2. **ADOFF=1 will power down the ADC module.**

Bit 4 ADRFS: ADC Data Format Control

0 : ADC Data MSB is ADRH bit 7, LSB is ADRL bit 4

1 : ADC Data MSB is ADRH bit 3, LSB is ADRL bit 0

This bit controls the format of the 12-bit converted A/D value in the two A/D data registers.

Bit 3 unimplemented, read as 0 (only usable for HT66F60)

Bit 2~0 ACS2, ACS1, ACS0: Select A/D channel (when ACS4 is 0)

000: AN0
001: AN1
010: AN2
011: AN3
100: AN4
101: AN5
110: AN6
111: AN7
1000: AN8
1001: AN9
1010: AN10
1011: AN11
1100~1111: undefined, cant be used

These are the A/D channel select control bits.

As there is only one internal hardware A/D converter each of the eight A/D inputs must be routed to the internal converter using these bits.

If bit ACS4 in the ADCR1 register is set high then the internal 1.25V will be routed to the A/D Converter.

Holtek – Analog to Digital Converter / ADCR1 Register

Bit	7	6	5	4	3	2	1	0
Name	ACS4	V125EN	—	VREFS	—	ADCK2	ADCK1	ADCK0
R/W	R/W	R/W	—	R/W	—	R/W	R/W	R/W
POR	0	0	—	0	—	0	0	0

Bit 7 ACS4: Selecte Internal 1.25V as ADC input Control

0: Disable

1: Enable

This bit enables 1.25V to be connected to the A/D converter.

The V125EN bit must first have been set to enable the bandgap circuit 1.25V voltage to be used by the A/D converter.

When the ACS4 bit is set high, the bandgap 1.25V voltage will be routed to the A/D converter and **the other A/D input channels disconnected.**

Bit 6 V125EN: Internal 1.25V Control

0: Disable

1: Enable

This bit controls the internal Bandgap circuit on/off function to the A/D converter.

When the bit is set high, the bandgap voltage 1.25V can be used by the A/D converter.

If 1.25V is not used by the A/D converter and the LVR/LVD function is disabled then the bandgap reference circuit will be automatically switched off to conserve power.

When 1.25V is switched on for use by the A/D converter, a time t_{BG} ($t_{BGS} \geq 200\mu s$) should be allowed for the bandgap circuit to stabilise before implementing an A/D conversion.

Bit 5 unimplemented, read as 0

Bit 4 VREFS: Selecte ADC reference voltage

0: Internal ADC power

1: VREF pin

This bit is used to select the reference voltage for the A/D converter. If the bit is **high**, then the A/D converter reference voltage is supplied on the **external VREF pin**.

If the pin is **low**, then the internal reference is used which is taken from the **power supply pin VDD**.

Bit 3 unimplemented, read as 0

Bit 2~0 ADCK2, ADCK1, ADCK0: Select ADC clock source

000: fSYS
001: fSYS/2
010: fSYS/4
011: fSYS/8
100: fSYS/16
101: fSYS/32
110: fSYS/64
111: Undefined

These three bits are used to select the clock source for the A/D converter.ADC module.

Holtek – Analog to Digital Converter / ACERL Register

ACERL Register

Bit	7	6	5	4	3	2	1	0
Name	ACE7	ACE6	ACE5	ACE4	ACE3	ACE2	ACE1	ACE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7~0 **ACE7~ACE0 : Define PA7~PA0 is A/D input or not**
0: Not A/D input
1: A/D input

ACERH Register

Bit	7	6	5	4	3	2	1	0
Name	—	—	—	—	ACE11	ACE10	ACE9	ACE8
R/W	—	—	—	—	R/W	R/W	R/W	R/W
POR	—	—	—	—	1	1	1	1

Bit 7~4 unimplemented, read as 0
Bit 3~0 ACE11~ACE8 : Define PF1, PF0, PE7, PE6 is A/D input or not
0: Not A/D input
1: A/D input, AN11

NOTE: ACERH Register only usable in HT66F60

Holtek – Analog to Digital Converter / A/D Converter Characteristics

- Pins can be changed under program control to change their function between A/D inputs and other functions.
- **All pull-high resistors**, which are setup through register programming, will **be automatically disconnected if the pins are setup as A/D inputs**.
- Note that **it is not necessary to first setup the A/D pin as an input in the PAC, PEC or PFC port control register** to enable the A/D input as **when the ACE11~ ACE0 bits enable an A/D input, the status of the port control register will be overridden.**
- The **A/D converter has its own reference voltage pin**, **VREF**, however the **reference voltage can also be supplied from the power supply pin**, a choice which is made through the **VREFS bit in the ADCR1** register.
- **The analog input values must not be allowed to exceed the value of VREF.**

A/D Transfer Function

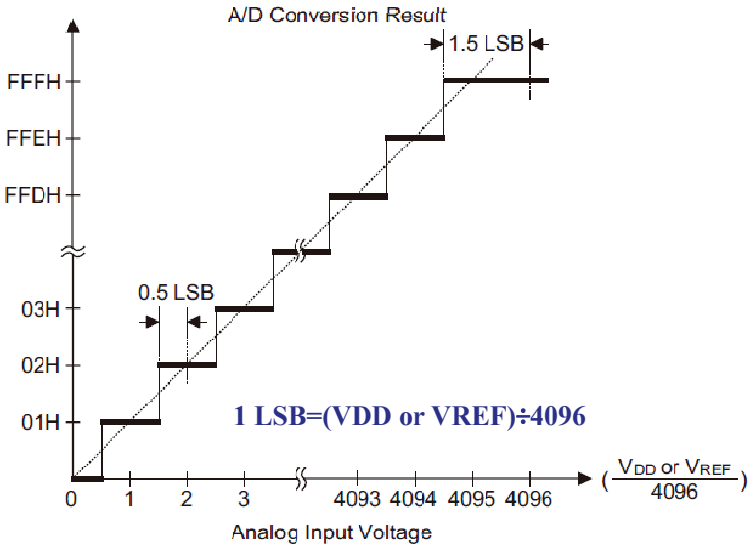
- As the devices contain a **12-bit A/D converter**, its full-scale converted digitized value is equal to FFFH.
- Since the **full-scale analog input value** is equal to the **VDD or VREF** voltage, this gives **a single bit analog input value of VDD or VREF divided by 4096**.

1 LSB=(VDD or VREF)÷4096

- The A/D Converter input voltage value can be calculated using the following equation:

A/D input voltage=
A/D output digital value×(VDD or VREF)÷4096

- The diagram shows the ideal transfer function between the analog input value and the digitized output value for the A/D converter. Except for the digitized zero value, the subsequent **digitized values will change at a point 0.5 LSB below** where they would change without the offset, and the **last full scale digitized value will change at a point 1.5 LSB below the VDD or VREF level**.



Holtek – Analog to Digital Converter / A/D Clock Period

f_{SYS}	A/D Clock Period (t_{ADCK})							
	ADCK2, ADCK1, ADCK0 = 000 (f_{SYS})	ADCK2, ADCK1, ADCK0 = 001 ($f_{SYS}/2$)	ADCK2, ADCK1, ADCK0 = 010 ($f_{SYS}/4$)	ADCK2, ADCK1, ADCK0 = 011 ($f_{SYS}/8$)	ADCK2, ADCK1, ADCK0 = 100 ($f_{SYS}/16$)	ADCK2, ADCK1, ADCK0 = 101 ($f_{SYS}/32$)	ADCK2, ADCK1, ADCK0 = 110 ($f_{SYS}/64$)	ADCK2, ADCK1, ADCK0 = 111
1MHz	1μs	2μs	4μs	8μs	16μs	32μs	64μs	Undefined
2MHz	500ns	1μs	2μs	4μs	8μs	16μs	32μs	Undefined
4MHz	250ns*	500ns	1μs	2μs	4μs	8μs	16μs	Undefined
8MHz	125ns*	250ns*	500ns	1μs	2μs	4μs	8μs	Undefined
12MHz	83ns*	167ns*	333ns*	667ns	1.33μs	2.67μs	5.33μs	Undefined

Maximum conversion speed (bit/sec) : $f_{ADCK,max}$ is 2MHz

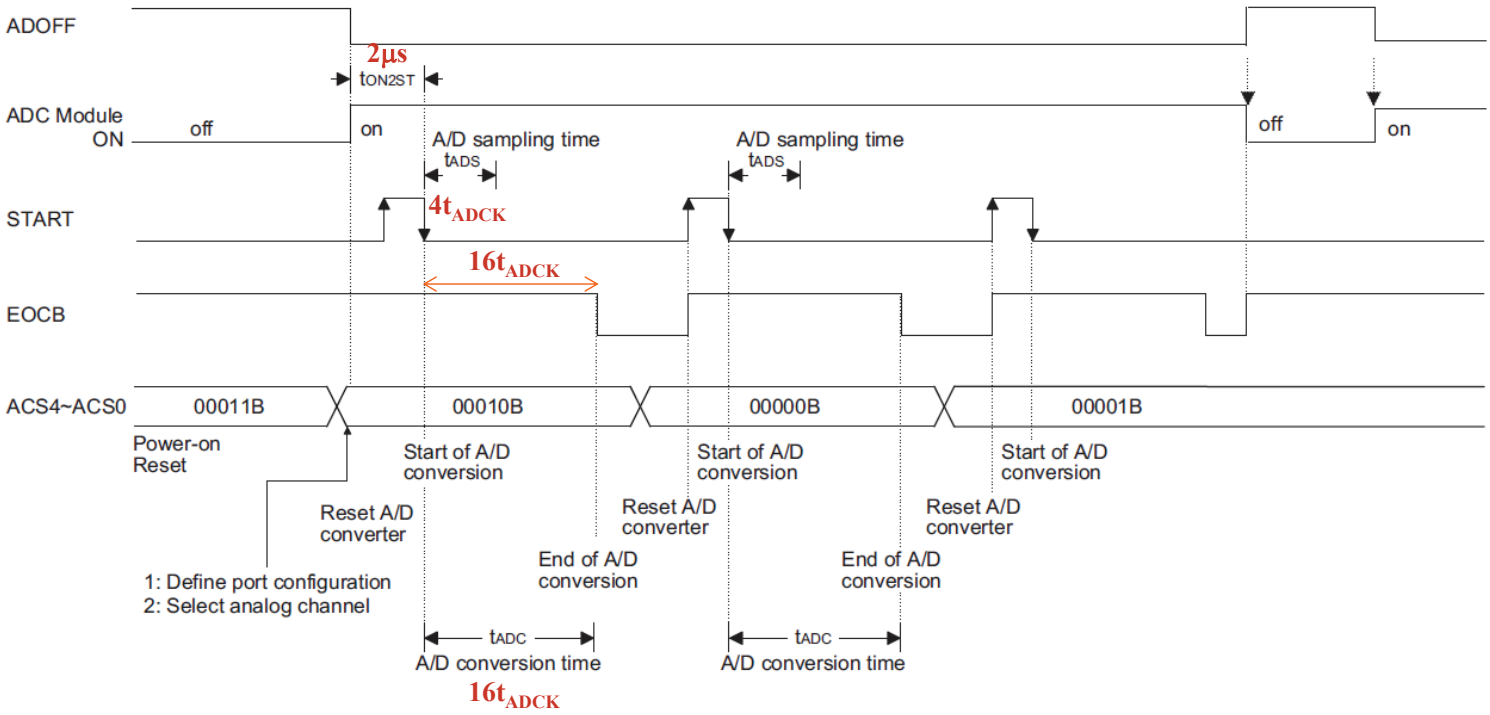
- As **the minimum value of permissible A/D clock period, t_{ADCK}, is 0.5 μs, care must be taken for system clock frequencies equal to or greater than 4MHz.**

Holtek – Analog to Digital Converter / A/D conversion process

- **Step 1** : **Select the required A/D conversion clock** by correctly programming bits **ADCK2~ADCK0 in the ADCR1 register**.
- **Step 2** : **Enable the A/D by clearing the ADOFF bit** in the **ADCR0** register to zero.
- **Step 3** : **Select which channel is to be connected to the internal A/D converter** by correctly programming the **ACS4~ACS0 bits** which are also contained in the **ADCR1 and ADCR0 register**.
- **Step 4** : **Select which pins are to be used as A/D inputs** and configure them by correctly programming the **ACE11~ACE0 bits in the ACERH and ACERL registers**. (ACERH only usable for HT66F50)
- **Step 5** : **If the interrupts are to be used, the interrupt control registers must be correctly configured** to ensure the A/D converter interrupt function is active.
  - ⇨The master interrupt control bit, **EMI**, and the A/D converter interrupt bit, **EADI**, must both be **set high** to do this.
- **Step 6** : The analog to digital **conversion process can now be initialized by setting the START bit in the ADCR0 register from low to high and then low again**.
  - ⇨Note that this bit should have been originally cleared to zero.

- **Step 7** : **To check when the analog to digital conversion process is complete, the EOCB bit in the ADCR0 register can be polled**.
  - ⇨The **conversion process is complete when this bit goes low**.
    - When this occurs the A/D data registers ADRL and ADRH can be read to obtain the conversion value.
  - ⇨As **an alternative method, if the interrupts are enabled and the stack is not full, the program can wait for an A/D interrupt to occur**.
    - Note: When checking for the end of the conversion process, if the method of polling the EOCB bit in the ADCR0 register is used, the interrupt enable step above can be omitted.

Holtek – Analog to Digital Converter / A/D Clock Period



Holtek – Analog to Digital Converter / A/D Converter Characteristics

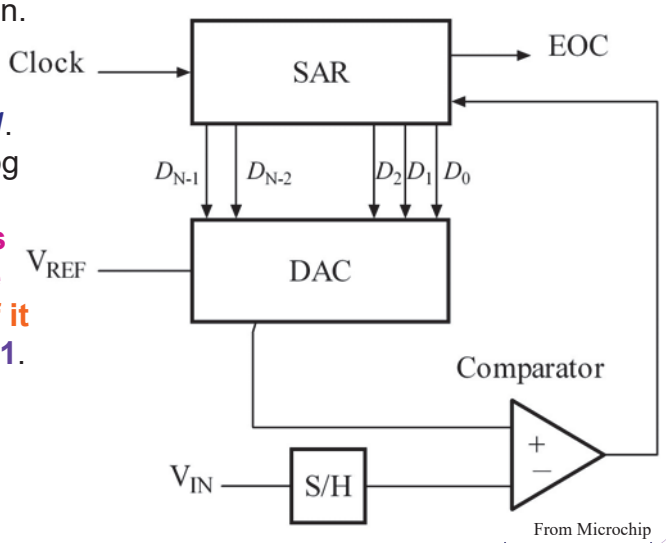
Ta=25°C

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
		V_{DD}	Conditions				
AV_{DD}	A/D Converter Operating Voltage	—	—	2.7	—	5.5	V
V_{ADI}	A/D Converter Input Voltage	—	—	0	—	VREF	V
V_{REF}	A/D Converter Reference Voltage	—	—	2	—	AV_{DD}	V
DNL	Differential Non-linearity	5V	t_{ADCK}= 1.0μs	—	±1	±2	LSB
INL	Integral Non-linearity	5V	t_{ADCK}= 1.0μs	—	±2	±4	LSB
I_{ADC}	Additional Power Consumption if A/D Converter is Used	3V	No load, t_{ADCK}= 0.5μs	—	0.90	1.35	mA
		5V	No load, t_{ADCK}= 0.5μs	—	1.20	1.80	mA
t_{ADCK}	A/D Converter Clock Period	—	—	0.5	—	10	μs
t_{ADC}	A/D Conversion Time (Include Sample and Hold Time)	—	12-bit A/D Converter	—	16	—	t_{ADCK}
t_{ADS}	A/D Converter Sampling Time	—	—	—	4	—	t_{ADCK}
t_{ON2ST}	A/D Converter On-to-Start Time	—	—	2	—	—	μs

12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE

- A **successive approximation ADC** is a type of analog-to-digital converter that converts a **continuous analog waveform** into a **discrete digital representation** via a **binary search through all possible quantization levels** before finally converging upon a digital output for each conversion.
- The successive approximation Analog to digital converter circuit typically consists of four chief subcircuits:
- A **sample and hold circuit** to acquire the input voltage (Vin).
- An **analog voltage comparator** that compares Vin to the output of the **internal DAC** and outputs the result of the comparison to the **successive approximation register (SAR).**
- A **successive approximation register subcircuit** designed to supply an approximate digital code of Vin to the internal DAC.
- An **internal reference DAC** that supplies the comparator with an analog voltage equivalent of the digital code output of the SAR for comparison with Vin.

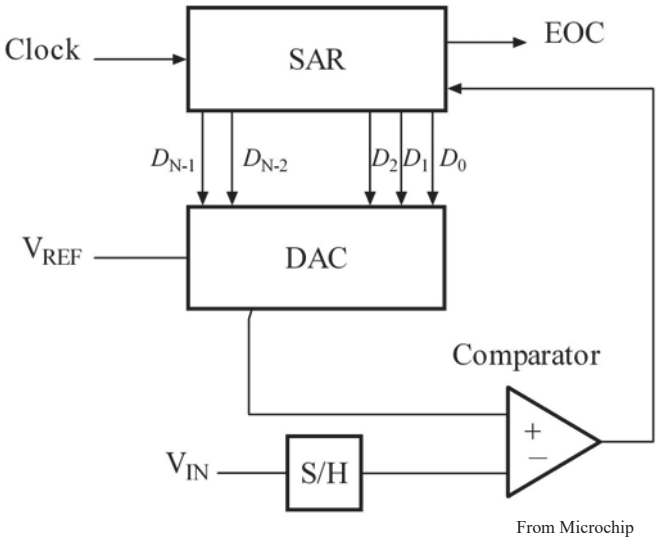
The **successive approximation register *is initialized so that the most significant bit (MSB) is equal to a digital 1***. This code is fed into the DAC which then supplies the analog equivalent of this digital code (Vref/2) into the comparator circuit for comparison with the sampled input voltage**. If this analog voltage exceeds Vin, the comparator causes the SAR to reset this bit and set the next bit to a digital 1. If it is lower, then the bit is left a 1 and the next bit is set to 1**. This **binary search continues until every bit in the SAR has been tested**. The resulting code is the digital approximation of the sampled input voltage and is finally output by the ADC at the **end of the conversion** (**EOC**).



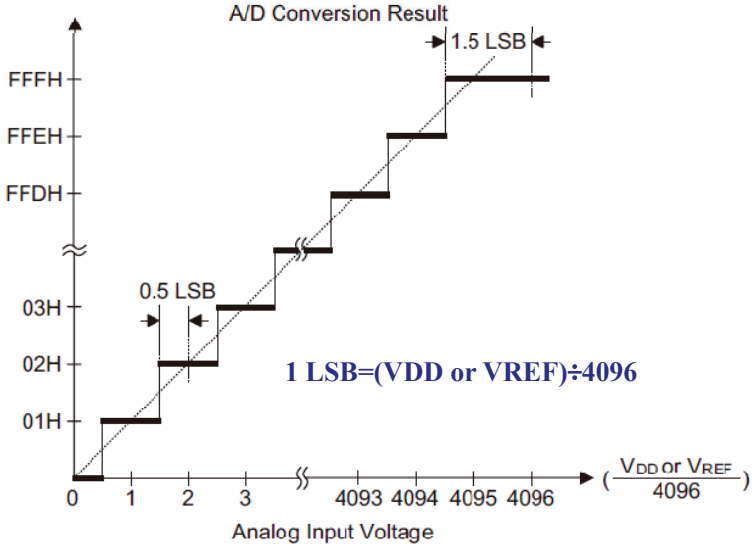
From Microchip

NKNU_EE_MMSOC

12-BIT ANALOG-TO-DIGITAL CONVERTER (A/D) MODULE



From Microchip



Assuming V_{in} = 1.5626V and V_{ref} = 2.5V,
LSB=2.5/4096=0.00061035
[1.5626+(2.5/4096/2)]/(2.5/4096)=2560=101000000000

1~4 t_{clk} : sample input
5 t_{clk} : 100000000000 → 1.5626 > 1.25 → 100000000000
6 t_{clk} : 110000000000 → 1.5626 < (1.25+0.625=1.875) → 100000000000
7 t_{clk} : 101000000000 → 1.5626 > (1.25+0+0.3125=1.5625) → 101000000000
8 t_{clk} : 101100000000 → 1.5626 < (1.25+0+0.3125+0.15625=1.71875) → 101000000000

•
•
•

16 t_{clk} : 101000000001 → 1.5626 < (1.25+0+0.3125+0+0+0+0+0+0+0+0+0.00061=1.56321) → 101000000000

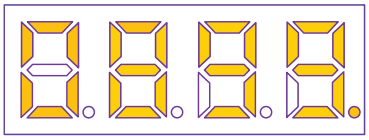
Holtek – Exercise Lab06

▸▸此次的”ADC”範例，CPU針對PA0(可變電阻VR0分壓器輸出)及PA2(光敏電阻CDS分壓器輸出)進行ADC轉換，然後判斷PA2之ADC數位數值是否大於PA0之ADC數位數值的2倍，若是的話，就啟動Timer module 0 (TM0)驅動蜂鳴器警報聲，否則關閉TM0。若PA2之ADC數位數值小於PA0之ADC數位數值，關閉使用的周遭硬體(如，ADC、七段顯示器、LED)，並使系統進入”sleep mode”模式。按下“7”鍵，可喚醒系統。

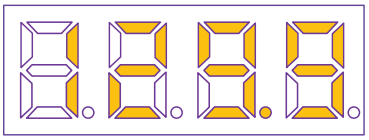
▸▸正常模式下，七段顯示器會依序顯示PA0與PA2的ADC數位數值(每個ADC數值維持一段時間就自動切換)。為了辨識所顯示的數值是哪一個的，利用小數點(“DP”)亮的位置來呈現目前是哪一個信號的ADC數位數值，個位數的小數點亮表示現在的數值為PA0的ADC數位數值，十位數的小數點亮表示現在的數值為PA2的ADC數位數值。”sleep mode”模式時，七段顯示器的LED燈全暗。

NOTE:以adc_no變數累加重複while(1)迴圈的次數，每50次就更換七段顯示器的顯示內容，也就是，用adc_no/50的商來判斷是哪一個輸入的ADC數位數值要被顯示，且增加對應數字位置的小數點顯示。

▸▸若PA2之ADC數位數值在PA0之ADC數位數值(含)與兩倍PA0之ADC數位數值(含)範圍，_pc0的LED亮，否則_pc0的LED暗。



adc_no/50=0
(PA0)=0899



adc_no/50=1
(PA2)=1099

作業要求的規格:

1.加入PA1(可變電阻VR1分壓器輸出)，進行ADC轉換。七段顯示器會依序顯示PA0、PA1與PA2的ADC數位數值(每個ADC數值維持一段時間就自動切換)。 為了辨識所顯示的數值是哪一個的，利用小數點(“DP”)亮的位置來呈現，個位數的小數點亮表示現在的數值為PA0的ADC數位數值，十位數的小數點亮表示現在的數值為PA1的ADC數位數值，百位數的小數點亮表示現在的數值為PA2的ADC數位數值。

2.以(PA2)表示，PA2透過ADC轉換的數位數值，若(PA2)>(PA1)或(PA1)<=(PA0)，蜂鳴器聲響，否則關閉蜂鳴器。

3.若(PA0) ≤(PA2)≤(PA1) ，_pc0的LED亮，否則_pc0的LED暗。

4.若(PA2)<(PA0)，關閉使用的周遭硬體(如，ADC、七段顯示器、LED)，並使系統進入”sleep mode”模式。按下“7”鍵，可喚醒系統。

5.追加功能:按下”B”鍵，可直接顯示PA0的ADC數位數值。按下”F”鍵，可直接顯示PA1的ADC數位數值。

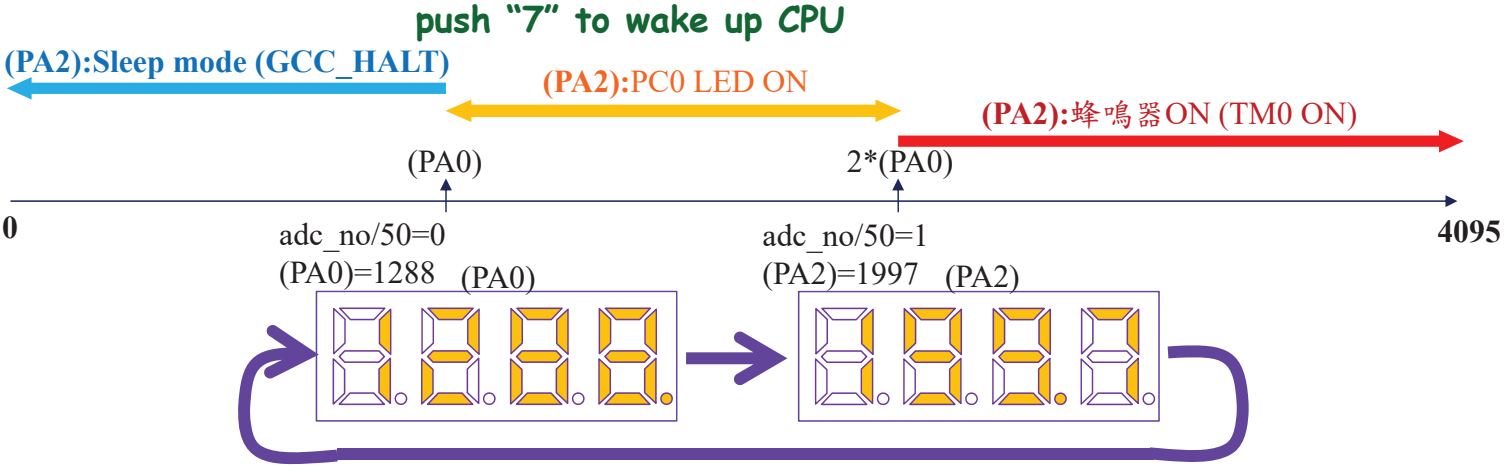
Holtek – Exercise Lab06 / Example Demo

▸▸此次的”ADC”範例，CPU針對PA0(可變電阻VR0分壓器輸出)及PA2(光敏電阻CDS分壓器輸出)進行ADC轉換，然後判斷PA2之ADC數位數值是否大於PA0之ADC數位數值的2倍，若是的話，就啟動Timer module 0 (TM0)驅動蜂鳴器警報聲，否則關閉TM0。若PA2之ADC數位數值小於PA0之ADC數位數值，關閉使用的周遭硬體(如，ADC、七段顯示器、LED)，並使系統進入”sleep mode”模式。按下“7”鍵，可喚醒系統。

▸▸正常模式下，七段顯示器會依序顯示PA0與PA2的ADC數位數值(每個ADC數值維持一段時間就自動切換)。為了辨識所顯示的數值是哪一個的，利用小數點(“DP”)亮的位置來呈現目前是哪一個信號的ADC數位數值，個位數的小數點亮表示現在的數值為PA0的ADC數位數值，十位數的小數點亮表示現在的數值為PA2的ADC數位數值。”sleep mode”模式時，七段顯示器的LED燈全暗。

NOTE:以adc_no變數累加重複while(1)迴圈的次數，每50次就更換七段顯示器的顯示內容，也就是，用adc_no/50的商來判斷是哪一個輸入的ADC數位數值要被顯示，且增加對應數字位置的小數點顯示。

▸▸若PA2之ADC數位數值在PA0之ADC數位數值(含)與兩倍PA0之ADC數位數值(含)範圍，_pc0的LED亮，否則_pc0的LED暗。



Holtek – Exercise Lab06 / SPECS (Specifications)

作業要求的規格:

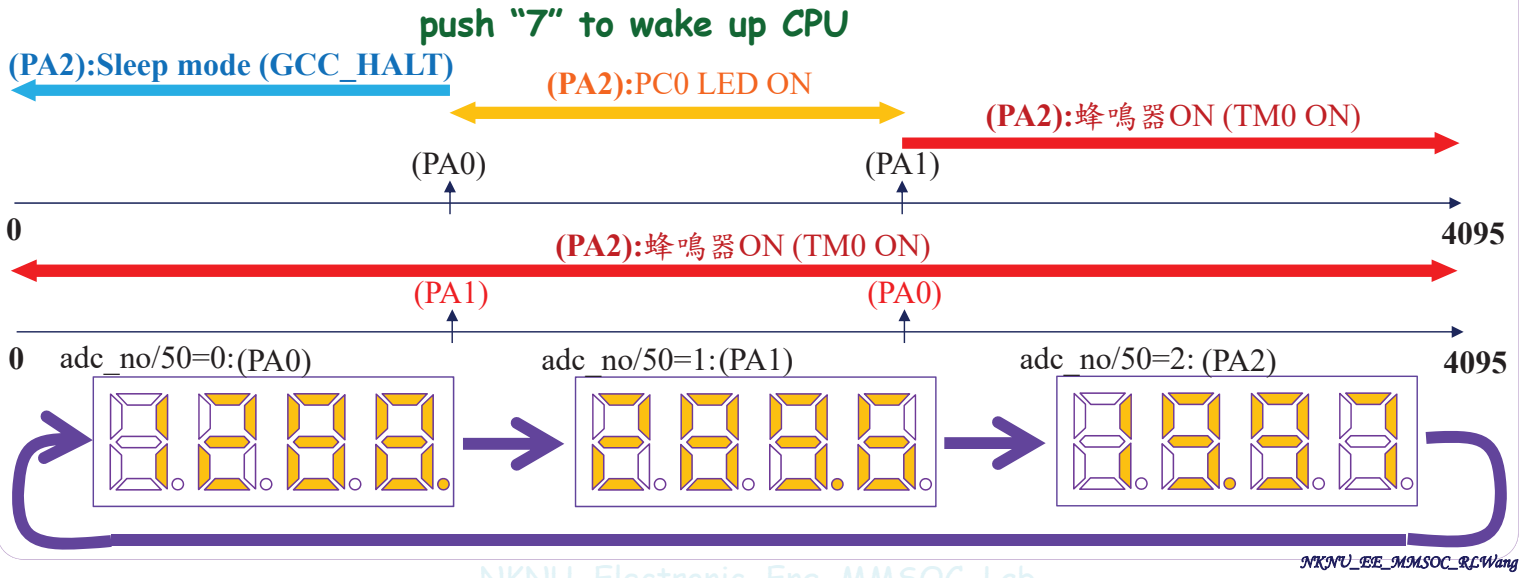
1.**加入PA1(**可變電阻VR1分壓器輸出)，進行ADC轉換。七段顯示器會依序顯示PA0、PA1與PA2的ADC數位數值(每個ADC數值維持一段時間就自動切換)。 為了辨識所顯示的數值是哪一個的，利用小數點(“DP”)亮的位置來呈現，個位數的小數點亮表示現在的數值為PA0的ADC數位數值，十位數的小數點亮表示現在的數值為PA1的ADC數位數值，百位數的小數點亮表示現在的數值為PA2的ADC數位數值。

2.以(PA2)表示，PA2透過ADC轉換的數位值，若(PA2)>(PA1)或**(PA1)<=(PA0)**，**蜂鳴器**響，否則關閉蜂鳴器。

3.若(PA0) ≤(PA2)≤(PA1) ，**_pc0的LED亮**，否則_pc0的LED暗。

4.若(PA2)<(PA0)，**關閉使用的周遭硬體(如，ADC、七段顯示器、LED)，並使系統進入”sleep mode”模式。按下“7”鍵，可喚醒系統**。

5.追加功能:按下”B”鍵，可直接顯示PA0的ADC數位數值。按下”F”鍵，可直接顯示PA1的ADC數位數值。



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