Holtek – Configuration Options

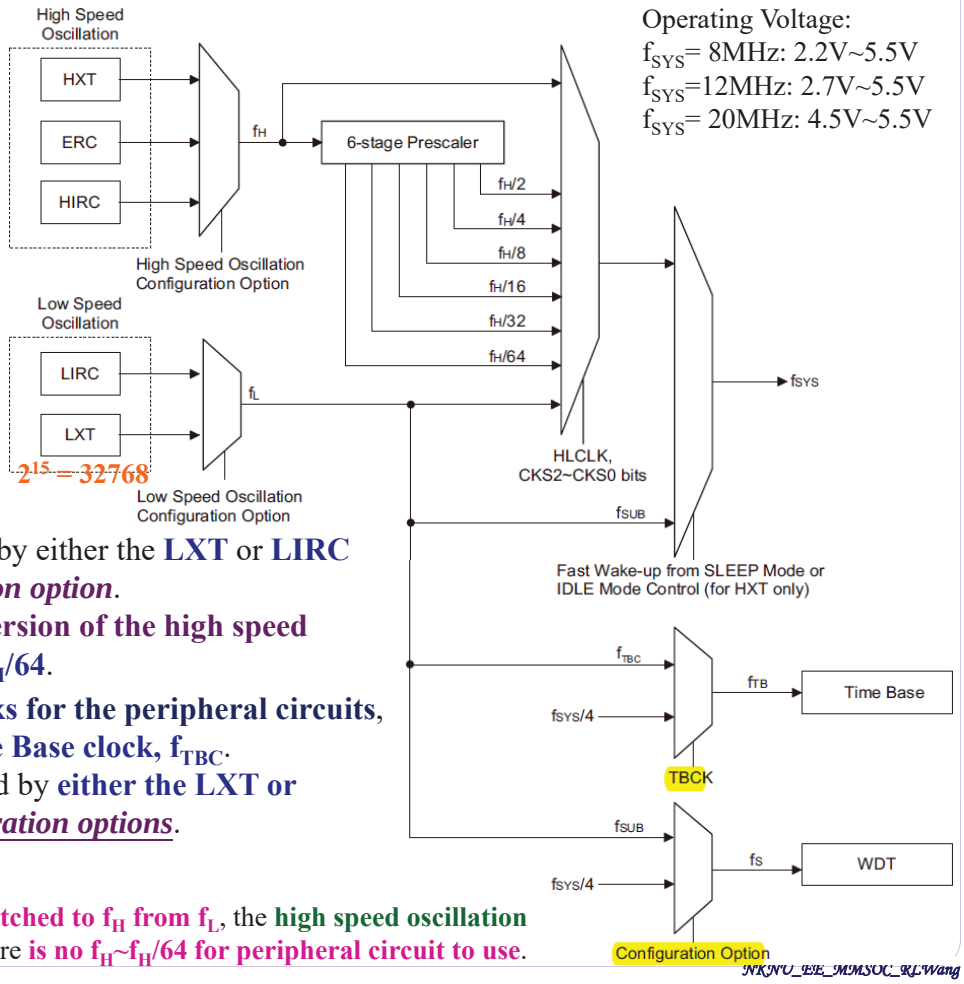
Configuration options refer to certain options within the CU that are **programmed into the device during the programming process**. During the development process, these options are selected using the HT-IDE software development tools. As these options are programmed into the device using the hardware programming tools, **once they are selected they cannot be changed later using the application program**

No.	Options
Oscillator Options	
1	High Speed System Oscillator Selection - fH: 1. HXT 2. ERC 3. HIRC
2	Low Speed System Oscillator Selection - fL: 1. LXT 2. LIRC
3	WDT Clock Selection - fS: 1. f_{SUB} 2. $f_{SYS}/4$
4	HIRC Frequency Selection: 1. 4MHz 2. 8MHz 3. 12MHz
Note: The f_{SUB} and the f_{TBC} clock source are LXT or LIRC selection by the f_L configuration option.	
Reset Pin Options	
5	PB0/RES Pin Options: 1. RES pin 2. I/O pin
Watchdog Options	
6	Watchdog Timer Function: 1. Enable 2. Disable
7	CLRWDT Instructions Selection: 1. 1 instructions 2. 2 instructions

No.	Options
LVR Options (Low Voltage Reset)	
8	LVR Function: 1. Enable 2. Disable
9	LVR Voltage Selection: 1. 2.10V 2. 2.55V 3. 3.15V 4. 4.20V
SIM Options	
10	SIM Function: 1. Enable 2. Disable
11	SPI - WCOL bit: 1. Enable 2. Disable
12	SPI - CSEN bit: 1. Enable 2. Disable
13	I²C Debounce Time Selection: 1. No debounce 2. 2 system clock debounce 3. 4 system clock debounce

Holtek – System Clock Sources

- The device has **many different clock sources for** both the **CPU** and **peripheral function** operation.
- The **main system clock**, can come from either a **high frequency, f_H**, or **low frequency, f_L**, source, and is **selected using the HLCLK bit and CKS2~CKS0 bits in the SMOD register**.
  - The **high speed system clock** can be sourced from either an **HXT**, **ERC** or **HIRC oscillator**, ***selected via a configuration option***.
  - The **low speed system clock** source can be sourced from **internal clock f_L**.
    - If **f_L** is selected then it can be sourced by either the **LXT** or **LIRC oscillators**, ***selected via a configuration option***.
  - The **other choice**, which is a **divided version of the high speed system oscillator** has a range of **$f_H/2$~$f_H/64$**.
- There are **two additional internal clocks for the peripheral circuits**, the **substitute clock, f_{SUB}**, and the **Time Base clock, f_{TBC}**.
  - Each of these internal clocks are sourced by **either the LXT or LIRC oscillators**, ***selected via configuration options***.

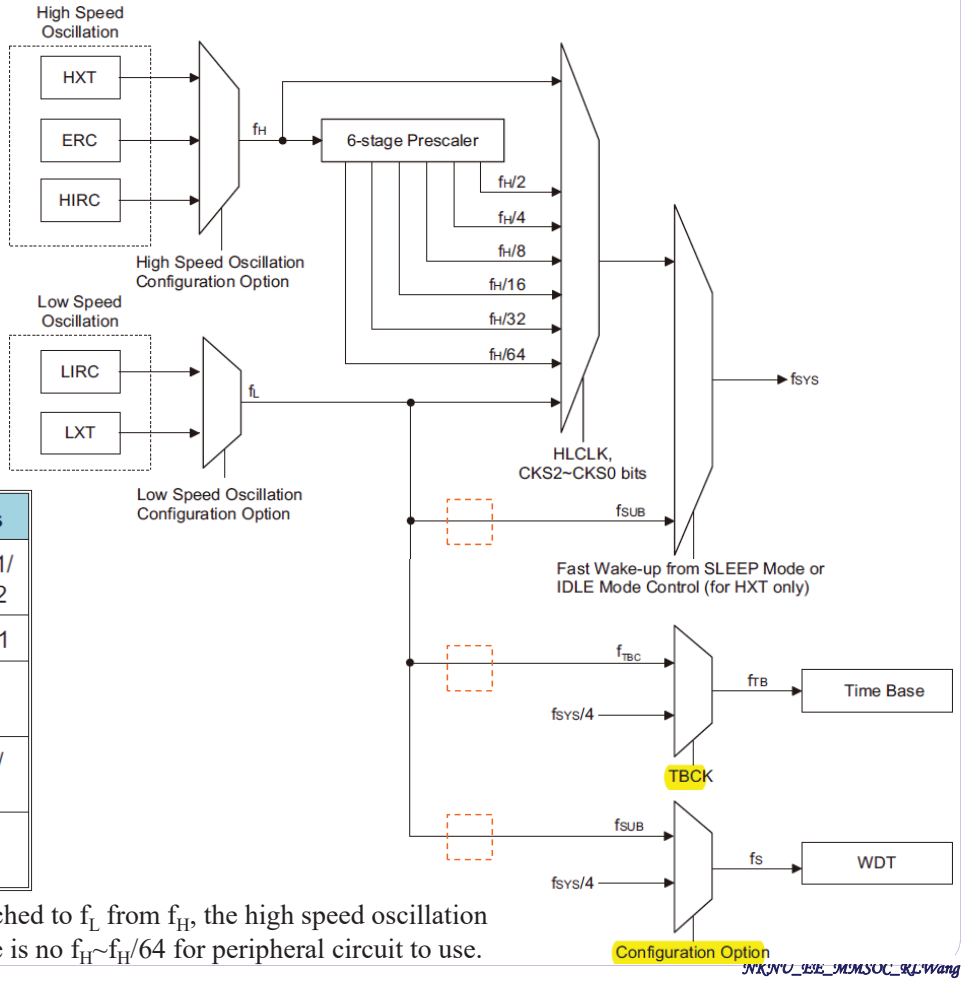


Operating Voltage:
f_{SYS}= 8MHz: 2.2V~5.5V
f_{SYS}=12MHz: 2.7V~5.5V
f_{SYS}= 20MHz: 4.5V~5.5V

Note: **When the system clock source f_{SYS} is switched to f_H from f_L**, the **high speed oscillation will stop to conserve the power**. Thus there **is no f_H~$f_H/64$ for peripheral circuit to use**.

Holtek – System Clock Sources

- The f_{SUB} clock is used to *provide a substitute clock for the microcontroller just after a wake-up has occurred to enable faster wake-up times*.
  - Together with $f_{SYS}/4$ it is also used as one of the clock sources for the Watchdog timer.
- The f_{TBC} clock is used as a source *for the Time Base interrupt functions and for the TMs*.

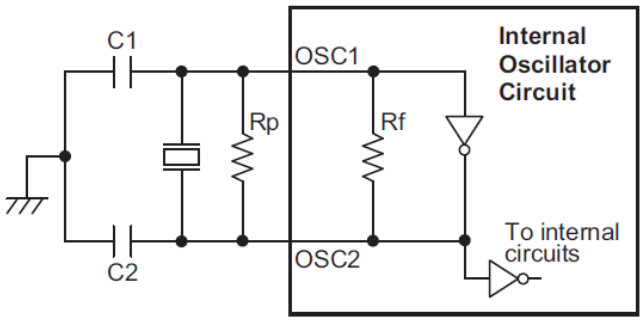


Type	Name	Freq.	Pins
External Crystal	HXT	400kHz~ 20MHz	OSC1/ OSC2
External RC	ERC	8MHz	OSC1
Internal High Speed RC	HIRC	4, 8 or 12MHz	—
External Low Speed Crystal	LXT	32.768kHz	XT1/ XT2
Internal Low Speed RC	LIRC	32kHz	—

Note: When the system clock source f_{SYS} is switched to f_L from f_H, the high speed oscillation will stop to conserve the power. Thus there is no f_H~$f_H/64$ for peripheral circuit to use.

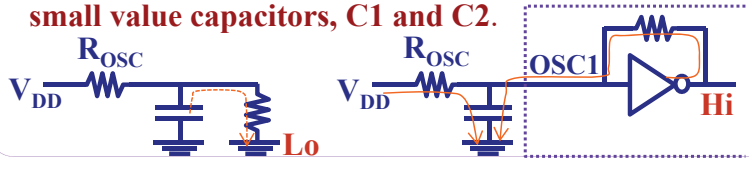
Holtek – System Clock Sources

Crystal/Resonator Oscillator HXT



1. Rp is normally not required.C1 and C2 are required.
2. Although not shown OSC1/OSC2 pins have a parasitic capacitance of around 7 pF.

- The **External** Crystal/ Ceramic System Oscillator is one of the **high frequency oscillator choices**, which is **selected via configuration option**.
- For most crystal oscillator configurations, the **simple connection of a crystal across OSC1 and OSC2** will **create the *necessary phase shift and feedback for oscillation***, without requiring external capacitors.
- However, for some crystal types and frequencies, **to ensure oscillation**, it may be **necessary to add two small value capacitors, C1 and C2**.

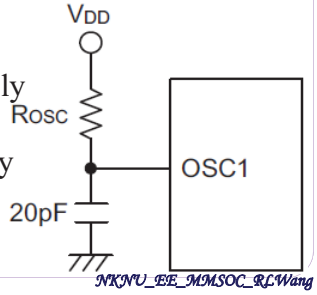


Crystal Oscillator C1 and C2 Values		
Crystal Frequency	C1	C2
12MHz	0pF	0pF
8MHz	0pF	0pF
4MHz	0pF	0pF
1MHz	100pF	100pF
Note: C1 and C2 values are for guidance only.		

Crystal Recommended Capacitor Values

External RC Oscillator ERC

- Using the ERC **oscillator only requires that a resistor, with a value between 56k and 2.4M, is connected between OSC1 and VDD**, and a capacitor is connected between OSC1 and ground, providing a low cost oscillator configuration.
- As a resistance/frequency reference point, it can be noted that with an external **120k** resistor connected and with a 5V voltage power supply and temperature of 25C degrees, the oscillator will have a frequency of **8MHz** within a tolerance of 2%.



Holtek – System Clock Sources

Internal RC Oscillator HIRC

- The internal RC oscillator is **a fully integrated system oscillator requiring no external components**.
- The internal RC oscillator has **three fixed frequencies of either 4MHz, 8MHz or 12MHz.**

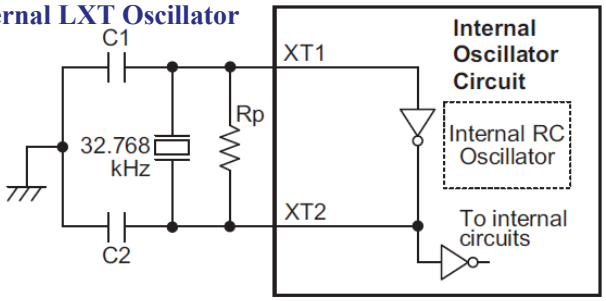
External 32.768kHz Crystal Oscillator LXT

- The **External 32.768kHz Crystal System Oscillator** is one of the low frequency oscillator choices, which is **selected via configuration option**.
- This clock source has a fixed frequency of 32.768kHz **and requires a 32.768kHz crystal to be connected between pins XT1 and XT2**.
- The external resistor and capacitor components connected to the 32.768kHz crystal are necessary to provide oscillation.

Internal 32kHz Oscillator LIRC

- The **Internal 32kHz System Oscillator is one of the low frequency oscillator choices**, which is **selected via configuration option**.
- It is a fully integrated RC oscillator with a typical frequency of 32kHz at 5V, requiring no external components for its implementation. at a power supply of 5V and at a temperature of 25C degrees, the fixed oscillation frequency of 32kHz will have a tolerance within 10%.

External LXT Oscillator



Note: 1. Rp, C1 and C2 are required.
2. Although not shown pins have a parasitic capacitance of around 7pF.

LXT Oscillator C1 and C2 Values		
Crystal Frequency	**C1**	**C2**
32.768kHz	10pF	10pF
Note: 1. C1 and C2 values are for guidance only. 2. R_P=5M~10MΩ is recommended.		

- The **LXT oscillator** can function in one of **two modes**, the **Quick Start Mode** and the **Low Power Mode**. **The mode selection is executed using the LXTLP bit in the TBC register**.
- **After power on**, the **LXTLP bit** will be automatically cleared to **zero** ensuring that the **LXT oscillator is in the Quick Start operating mode**.
- However, **after the LXT oscillator has fully powered up it can be placed into the Low-power mode by setting the LXTLP bit high**

Holtek – System Operation Modes

- There are **six different modes of operation** for the microcontroller, each one with its own special characteristics and which can be chosen according to the specific performance and power requirements of the application.
- There are **two modes allowing normal operation** of the microcontroller, the **NORMAL Mode** and **SLOW Mode**.
- The remaining four modes, the **SLEEP0**, **SLEEP1**, **IDLE0** and **IDLE1 Mode** are used when the microcontroller CPU is switched off to conserve power.

Depend on WDT clock source (f_s) selection
If f_s=f_{SUB}, f_s is on, else f_s=f_{SYS}/4 and f_s is off

Operating Mode	Description				
	CPU	f_{SYS}	f_{SUB}	f_S	f_{TBC}
NORMAL Mode	On	f_H~f_H/64	On	On	On
SLOW Mode	On	f_L	On	On	On
IDLE0 Mode	Off	Off	On	On/Off	On
IDLE1 Mode	Off	On	On	On	On
SLEEP0 Mode	Off	Off	Off	Off	Off
SLEEP1 Mode	Off	Off	On	On	Off

SMOD[1] IDLEN bit=1

IDLEN bit=0

WDT or LVD on/off

IDLE mode: WDT is still on

- **FSYSON(=WDTC[7]) bit ='1' :** in the **IDLE1** mode, the **CPU will stop running but the system clock will continue to keep the peripheral functions operational.**
- **FSYSON(=WDTC[7]) bit = '0':** in **IDLE0** mode, the **CPU and the system clock will all stop**.

Holtek – System Operation Modes / SMOD Register

A single register, **SMOD**, is used **for overall control of the internal clocks within the device**.

Bit	7	6	5	4	3	2	1	0
Name	CKS2	CKS1	CKS0	FSTEN	LTO	HTO	IDLEN	HLCLK
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
POR	0	0	0	0	0	0	1	1

Bit 7~5 CKS2~CKS0: The system clock selection when **HLCLK is "0"**

000: f_L (f_{LXT} or f_{LIRC}) 001: f_L (f_{LXT} or f_{LIRC})
010: $f_H/64$ 011: $f_H/32$
100: $f_H/16$ 101: $f_H/8$
110: $f_H/4$ 111: $f_H/2$

These three bits are used to select which clock is used as the system clock source. In addition to the system clock source, which can be either the LXT or LIRC, a divided version of the high speed system oscillator can also be chosen as the system clock source.

Bit 4 FSTEN: Fast Wake-up Control (**only for HXT**)

0: Disable 1: Enable

This is the **Fast Wake-up Control bit** which **determines if the f_{SUB} clock source is initially used after the device wakes up. When the bit is high, the f_{SUB} clock source can be used as a temporary system clock** to provide a faster wake up time as the f_{SUB} clock is available.

Bit 3 LTO: Low speed system oscillator ready flag

0: Not ready
1: Ready

This is the low speed system oscillator ready flag which indicates when the low speed system oscillator is stable after power on reset or a wake-up has occurred. The **flag will be low when in the SLEEP0 Mode** but **after a wake-up has occurred, the flag will change to a high level after 1024 clock cycles if the LXT oscillator is used** and **1~2 clock cycles if the LIRC oscillator is used**.

Holtek – System Operation Modes / SMOD Register

A single register, **SMOD**, is used **for overall control of the internal clocks within the device**.

Bit	7	6	5	4	3	2	1	0
Name	CKS2	CKS1	CKS0	FSTEN	LTO	HTO	IDLEN	HLCLK
R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W
POR	0	0	0	0	0	0	1	1

Bit 2 HTO: High speed system oscillator ready flag

0: Not ready
1: Ready

This is the high speed system oscillator ready flag which indicates when the high speed system oscillator is stable. **This flag is cleared to "0" by hardware when the device is powered on and then changes to a high level after the high speed system oscillator is stable**. Therefore this flag will always be read as "1" by the application program after device power-on. **The flag will be low when in the SLEEP or IDLE0 Mode** but **after a wake-up has occurred**, the flag will **change to a high level after 1024 clock cycles if the HXT oscillator is used** and **after 15~16 clock cycles if the ERC or HIRC oscillator is used**.

Bit 1 IDLEN: IDLE Mode control

0: Disable (→ SLEEP mode)
1: Enable (→ IDLE mode)

This is the **IDLE Mode Control bit** and ***determines what happens when the* HALT *instruction is executed***. **If this bit is high**, when a HALT instruction is executed the device will **enter the IDLE Mode**. In the **IDLE1** Mode the **CPU will stop running but the system clock will continue** to keep the peripheral functions operational, if **FSYSON(=WDTC[7]) bit is high**. **If FSYSON bit is low**, the CPU and the system clock will all stop in **IDLE0** mode. **If the bit is low** the device will **enter the SLEEP Mode** when a HALT instruction is executed.

Bit 0 HLCLK: system clock selection

0: $f_H/2$~$f_H/64$ or f_L 1: f_H

This bit is used to select if the f_H clock or the $f_H/2$~$f_H/64$ or f_L clock is used as the system clock**. When the bit is high the f_H clock will be selected** and **if low the $f_H/2$~$f_H/64$ or f_L clock will be selected**. When **system clock switches from the f_H clock to the f_L clock and the f_H clock will be automatically switched off to conserve power.**

Holtek – Input/Output Ports

Register Name	Bit							
	7	6	5	4	3	2	1	0
PAWU	D7	D6	D5	D4	D3	D2	D1	D0
PAPU	D7	D6	D5	D4	D3	D2	D1	D0
PA	D7	D6	D5	D4	D3	D2	D1	D0
PAC	D7	D6	D5	D4	D3	D2	D1	D0
PBPU	D7	D6	D5	D4	D3	D2	D1	D0
PB	D7	D6	D5	D4	D3	D2	D1	D0
PBC	D7	D6	D5	D4	D3	D2	D1	D0
PCPU	D7	D6	D5	D4	D3	D2	D1	D0
PC	D7	D6	D5	D4	D3	D2	D1	D0
PCC	D7	D6	D5	D4	D3	D2	D1	D0
PDPU	D7	D6	D5	D4	D3	D2	D1	D0
PD	D7	D6	D5	D4	D3	D2	D1	D0
PDC	D7	D6	D5	D4	D3	D2	D1	D0
PEPU	D7	D6	D5	D4	D3	D2	D1	D0
PE	D7	D6	D5	D4	D3	D2	D1	D0
PEC	D7	D6	D5	D4	D3	D2	D1	D0
PFPU	—	—	—	—	—	—	D1	D0
PF	—	—	—	—	—	—	D1	D0
PFC	—	—	—	—	—	—	D1	D0

Holtek – Input/Output Ports

Register	Reset (Power-on)	$\overline{\text{RES}}$ or LVR Reset	WDT Time-out (Normal Operation)	WDT Time-out (IDLE)
BP	---- --00	---- --00	---- --00	---- --uu
ACC	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
PCL	0000 0000	0000 0000	0000 0000	0000 0000
TBLP	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBLH	xxxx xxxx	uuuu uuuu	uuuu uuuu	uuuu uuuu
TBHP	---x xxxx	---u uuuu	---u uuuu	---u uuuu
STATUS	--00 xxxx	--uu uuuu	--1u uuuu	--11 uuuu
SMOD	0000 0011	0000 0011	0000 0011	uuuu uuuu
INTEG	---- 0000	---- 0000	---- 0000	---- uuuu
WDTC	0111 1010	0111 1010	0111 1010	uuuu uuuu
PAWU	0000 0000	0000 0000	0000 0000	uuuu uuuu
PAPU	0000 0000	0000 0000	0000 0000	uuuu uuuu
PA	1111 1111	1111 1111	1111 1111	uuuu uuuu
PAC	1111 1111	1111 1111	1111 1111	uuuu uuuu
TM0C0	0000 0000	0000 0000	0000 0000	uuuu uuuu
TM0C1	0000 0000	0000 0000	0000 0000	uuuu uuuu
TM0DL	0000 0000	0000 0000	0000 0000	uuuu uuuu
TM0DH	---- --00	---- --00	---- --00	---- --uu
TM0AL	0000 0000	0000 0000	0000 0000	uuuu uuuu
TM0AH	---- --00	---- --00	---- --00	---- --uu
TMPC0	1001 --01	1001 --01	1001 --01	uuuu --uu
TMPC1	--01 --01	--01 --01	--01 --01	--uu --uu

Holtek – Input/Output Ports

- **ACERL Register**

Bit	7	6	5	4	3	2	1	0
Name	ACE7	ACE6	ACE5	ACE4	ACE3	ACE2	ACE1	ACE0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

Bit 7 **ACE7: Define PA7 is A/D input or not**
0: Not A/D input
1: A/D input, AN7

Bit n **ACEn: Define PAn is A/D input or not**
0: Not A/D input
1: A/D input, Ann ; n=0~7

- **PAWU Register**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 **PAWU: Port A bit 7 ~ bit 0 Wake-up Control**
0: Disable 1:enable **wake up the microcontroller as one of the Port A pins changes from high to low.**

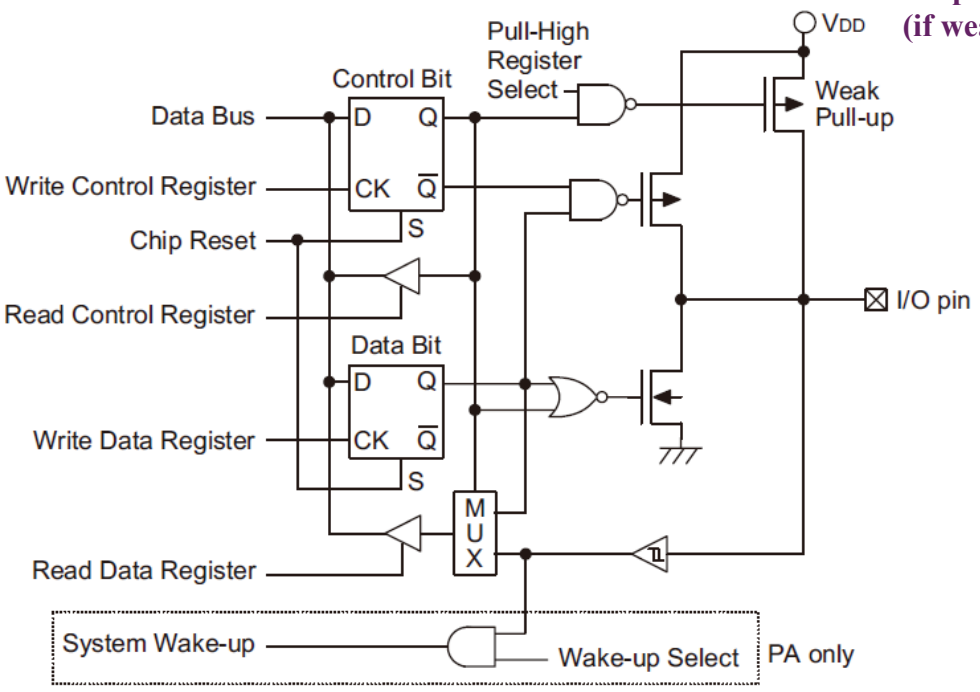
- **PAPU Register** **1: enable pull-up p-MOSFET**

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Holtek – I/O Structure

Write Control register : PAC
Data register : PA

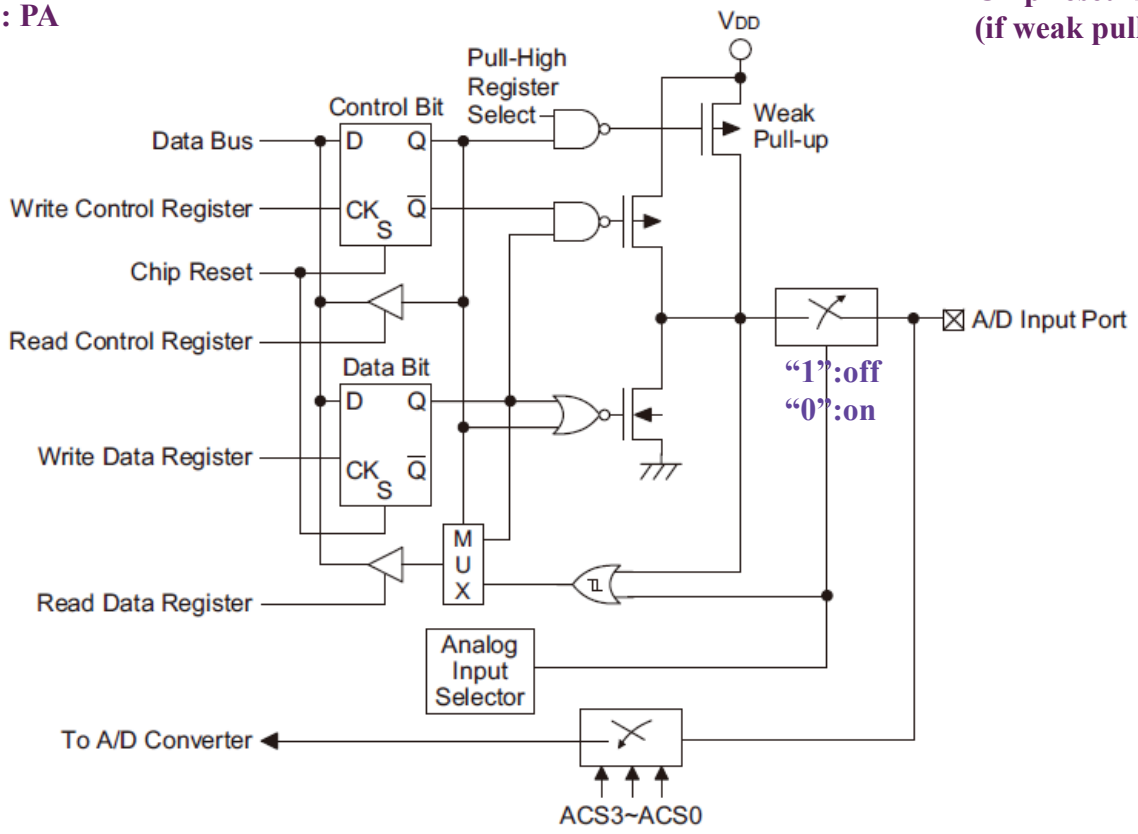
Chip reset → I/O high-Z
(if weak pull-up is off)



Holtek – I/O Structure

Write Control register : PAC
Data register : PA

Chip reset → I/O high-Z
(if weak pull-up is off)



Holtek – I/O Structure (Pull-up Resistor & Port A Wake-up)

- **PAPU Register**

To eliminate the need for these external resistors, all I/O pins, when configured as an input have the capability of being connected to an **internal pull-high resistor**. These pull-high resistors are selected using registers PAPU~PGPU, and are implemented using weak PMOS transistors.

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

Bit 7~0 I/O Port bit 7 ~ bit 0 Pull-High Control
0: Disable 1: Enable

- **Port A Wake-up (PAWU Register)**

The **HALT instruction** forces the microcontroller **into the SLEEP or IDLE Mode which preserves power**, a feature that is important for battery and other low-power applications.

Various methods exist to wake-up the microcontroller, one of which is to change the logic condition on one of the Port A pins from high to low.

⇨ This function is especially suitable for applications that can be woken up via external switches.

⇨ Each pin on Port A can be selected individually to have this wake-up feature using the **PAWU register**.

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	0	0	0	0	0	0

0: Disable 1: Enable

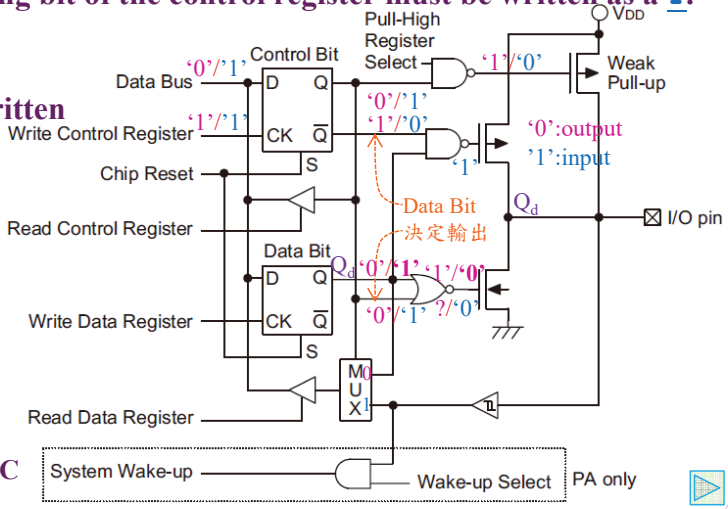
Holtek – I/O Structure (I/O Port Control Registers)

I/O Port Control Registers (PAC Register)

Bit	7	6	5	4	3	2	1	0
Name	D7	D6	D5	D4	D3	D2	D1	D0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	1	1	1	1	1	1	1	1

0: Output 1: Input

- Each I/O port has its own control register known as PAC~PGC, to control the input/output configuration.
  - ⇨ With this control register, each CMOS output or input can be reconfigured dynamically under software control.
- Each pin of the I/O ports is directly mapped to a bit in its associated port control register.
- **For the I/O pin to function as an input, the corresponding bit of the control register must be written as a 1.**
  - ⇨ This will then allow the logic state of the input pin to be directly read by instructions.
- **When the corresponding bit of the control register is written as a 0, the I/O pin will be setup as a CMOS output.**
- **If the pin is currently setup as an output, instructions can still be used to read the output register.**
  - ⇨ However, it should be noted that the program will in fact **only read the status of the output data latch** and **not the actual logic status of the output pin**.



Write Control register : PAC
Data register : PA

Holtek – Status Register (STATUS)

- This 8-bit register contains the **zero flag (Z)**, **carry flag (C)**, **auxiliary carry flag (AC)**, **overflow flag (OV)**, **power down flag (PDF)**, and **watchdog time-out flag (TO)**.
- These **arithmetic/logical operation** and **system management flags** are used to **record the status and operation of the microcontroller**.
- **With the exception of the TO and PDF flags, bits in the status register can be altered by instructions** like most other registers. **Any data written into the status register will not change the TO or PDF flag.**

Bit	7	6	5	4	3	2	1	0
Name	—	—	TO	PDF	OV	Z	AC	C
R/W	—	—	R	R	R/W	R/W	R/W	R/W
POR	—	—	0	0	x	x	x	x

"x" unknown

Bit 7, 6 Unimplemented, read as 0

Bit 5 TO: Watchdog Time-Out flag
0: After power up or executing the CLR WDT or HALT instruction
1: A watchdog time-out occurred.

Bit 4 PDF: Power down flag
0: After power up or executing the "CLR WDT" instruction
1: By **executing the "HALT" instruction**

Bit 3 OV: Overflow flag
0: no overflow
1: an operation results in **a carry into the highest-order bit** but **not a carry out of the highest-order bit** or vice versa.

Bit 2 Z: Zero flag
0: The result of an arithmetic or logical operation is not zero
1: The result of an arithmetic or logical operation is zero

Bit 1 AC: Auxiliary flag
0: no auxiliary carry
1: an operation results in **a carry out of the low nibbles** in addition, or **no borrow from the high nibble** into the low nibble in subtraction

Bit 0 C: Carry flag
0: no carry-out
1: an operation results in **a carry during an addition** operation or if **a borrow does not take place during a subtraction** operation

C is also affected by a rotate through carry instruction.

Holtek – Watchdog Timer / Watchdog Timer Control Register (WDTC)

- The **Watchdog Timer** is provided to **prevent program malfunctions or sequences from jumping to unknown locations**, due to certain **uncontrollable external events such as electrical noise**.
- The **Watchdog Timer clock source** is provided by the **internal clock, f_S**, which is in turn supplied by one of two sources selected by configuration option: **f_{SUB}** or **$f_{SYS}/4$**.
- The **f_{SUB}** clock can be sourced from either the **LXT or LIRC oscillators**, again chosen via a configuration option.
- The **Watchdog Timer source clock** is then **subdivided by a ratio of 2^8 to 2^{15} to give longer timeouts**, the actual value being chosen using the **WS2~WS0 bits in the WDTC register**.

Bit	7	6	5	4	3	2	1	0
Name	FSYSON	WS2	WS1	WS0	WDTEN3	WDTEN2	WDTEN1	WDTEN0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	1	1	1	1	0	1	0

Bit 7 FSYSON: f_{SYS} Control in IDLE Mode
0: Disable
1: Enable

Operating Mode	Description				
	CPU	f_{SYS}	f_{SUB}	f_S	f_{TBC}
NORMAL Mode	On	f_H~f_H/64	On	On	On
SLOW Mode	On	f_L	On	On	On
IDLE0 Mode	Off	Off	On	On/Off	On
IDLE1 Mode	Off	On	On	On	On
SLEEP0 Mode	Off	Off	Off	Off	Off
SLEEP1 Mode	Off	Off	On	On	Off

Bit 6~4 WS2, WS1, WS0: WDT time-out period selection
000: $256/f_S$ 001: $512/f_S$
010: $1024/f_S$ 011: $2048/f_S$
100: $4096/f_S$ 101: $8192/f_S$
110: $16384/f_S$ 111: $32768/f_S$
These three bits determine the division ratio of the Watchdog Timer source clock, which in turn determines the timeout period.

Bit 3~0 WDTEN3, WDTEN2, WDTEN1, WDTEN0: WDT Software Control
1010: Disable Other: Enable

Holtek – Watchdog Timer / Watchdog Timer Control Register (WDTC)

- **To disable the Watchdog Timer**, as well as the **configuration option being set to disable, the WDTEN3~WDTEN0 bits must also be set to a specific value of "1010".**
- **Any other values for these bits (i.e. WDTEN3~WDTEN0 bits) will keep the Watchdog Timer enabled, irrespective of the configuration enable/disable setting.**
- **After power on these bits will have the value of "1010". If the Watchdog Timer is used, it is recommended that they are set to a value of "0101" for maximum noise immunity**. Note that if the Watchdog Timer has been disabled, then any instruction relating to its operation will result in no operation.

WDT Configuration Option	WDTEN3~WDTEN0 Bits	WDT
WDT Enable	××××	Enable
WDT Disable	Except 1010	Enable
WDT Disable	1010	Disable

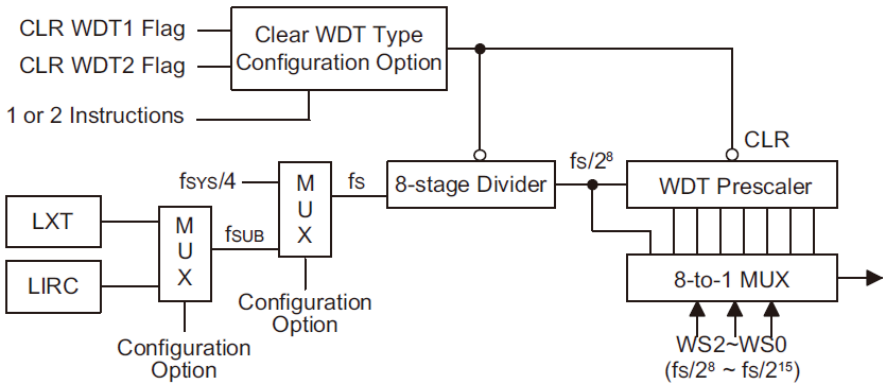
- **Under normal program operation, a Watchdog Timer time-out will initialize a device reset and set the status bit TO**. However, **if the system is in the SLEEP or IDLE Mode, when a Watchdog Timer time-out occurs, the TO bit in the status register will be set and only the Program Counter and Stack Pointer will be reset.**
- **Three methods** can be adopted to **clear the contents of the Watchdog Timer**.
  1. The first is an **external hardware reset**, which means a low level on the **RES** pin,
  2. the second is using the **Watchdog Timer software clear instructions** and
  3. the third is via **a HALT instruction**.

Other SFRs are not reset
CPU is waked up

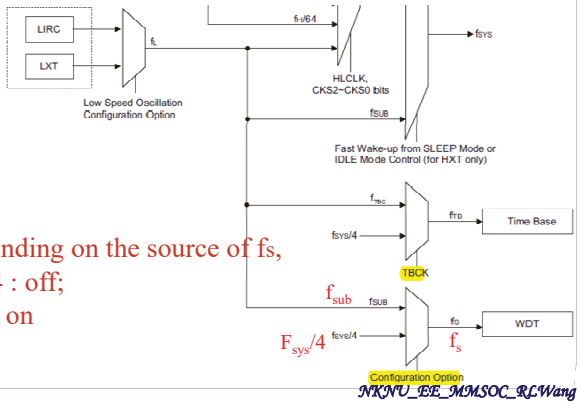
- There are **two methods of using software instructions** to clear the Watchdog Timer, **one of which must be chosen by configuration option**.
  1. The first option is to use the **single "CLR WDT" instruction** while
  2. the second is to use **the two commands "CLR WDT1" and "CLR WDT2".**
     (CLR WDT1 ……. CLR WDT2…… CLRWDT1 ……, i.e. to clear the Watchdog Timer by "CLR WDT1" and "CLR WDT2" by turns).

Holtek – Watchdog Timer / Watchdog Timer Control Register (WDTC)

- The **maximum time out period** is when the **2^{15} division ratio** is selected.
- As an example, with a **32.768kHz LXT** oscillator as its source clock, this will give **a maximum watchdog period of around 1 second for the 2^{15} division ratio**, and a **minimum timeout of 7.8ms for the 2^{8} division ratio**.
- If **the $f_{SYS}/4$ clock is used as the Watchdog Timer clock source**, it should be noted that when **the system enters the SLEEP or IDLE0 Mode, then the instruction clock is stopped and the Watchdog Timer may lose its protecting purposes**.
  - ⇨ For **systems that operate in noisy environments**, **using the f_{SUB} clock source is strongly recommended**.



32.768kHz —Div by 2^{15} = 32768→ 1Hz (1sec)



Operating Mode	Description				
	CPU	f_{SYS}	f_{SUB}	f_S	f_{TBC}
NORMAL Mode	On	f_H~f_H/64	On	On	On
SLOW Mode	On	f_L	On	On	On
IDLE0 Mode	Off	Off	On	On/Off	On
IDLE1 Mode	Off	On	On	On	On
SLEEP0 Mode	Off	Off	Off	Off	Off
SLEEP1 Mode	Off	Off	On	On	Off

Depending on the source of fs,
fsys/4 : off;
fsub : on

Fast wake-up WDT

Holtek – Wake up / Fast Wake-up

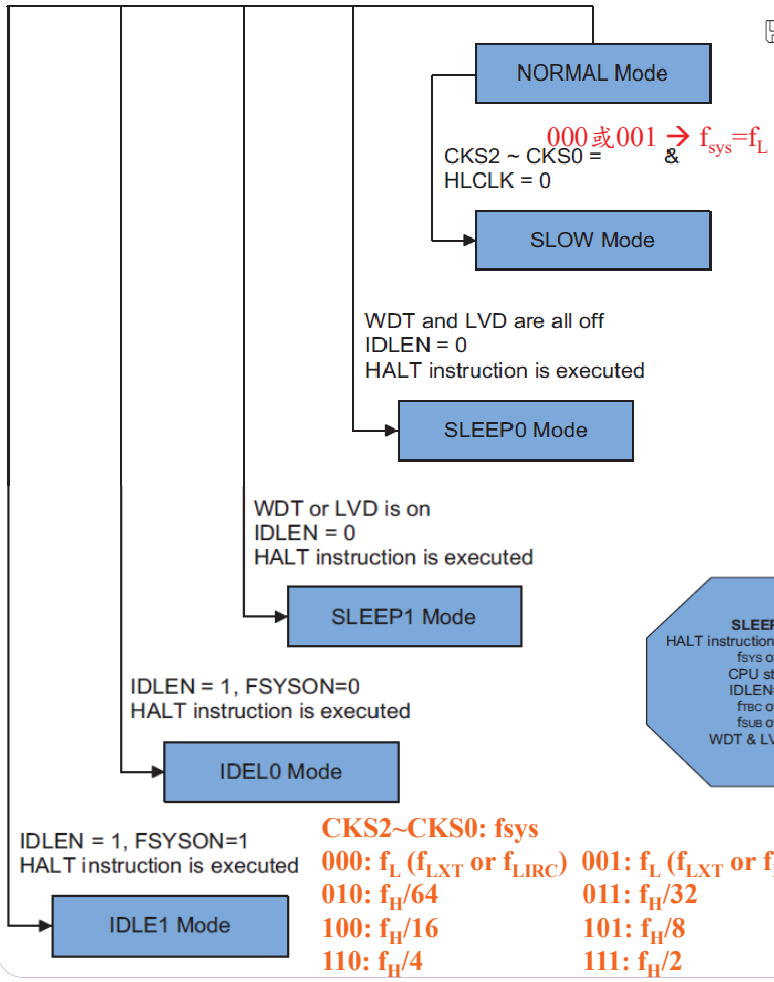
- **To minimize power consumption** the device can **enter the SLEEP or IDLE0 Mode**, where the **system clock source to the device will be stopped**.
- However **when the device is woken up again**, it can **take a considerable time for the original system oscillator (f_{SYS})to restart, stabilize and allow normal operation to resume**.
- **To ensure the device is up and running as fast as possible**, a **Fast Wake-up function** is provided, which **allows f_{SUB}, namely either the LXT or LIRC oscillator, to act as a temporary clock to first drive the system until the original system oscillator has stabilized**.
- As the **clock source for the Fast Wake-up function is f_{SUB}**, the **Fast Wake-up function is only available in the SLEEP1 and IDLE0 modes**. When the device is woken up from the **SLEEP0 mode**, the **Fast Wake-up function has no effect because the f_{SUB} clock is stopped**.
- The **Fast Wake-up enable/disable function** is controlled using the **FSTEN bit in the SMOD register**.

Operation Mode	Description				
	CPU	f_{SYS}	f_{SUB}	f_S	f_{TBC}
NORMAL Mode	On	f_H~f_H/64	On	On	On
SLOW Mode	On	f_L	On	On	On
IDLE0 Mode	Off	**Off**	**On**	On/Off	On
IDLE1 Mode	Off	On	On	On	On
SLEEP0 Mode	**Off**	**Off**	**Off**	**Off**	**Off**
SLEEP1 Mode	Off	**Off**	**On**	On	Off

SMOD[4]

System Oscillator	FSTEN Bit	Wake-up Time (SLEEP0 Mode)	Wake-up Time (SLEEP1 Mode)	Wake-up Time (IDLE0 Mode)	Wake-up Time (IDLE1 Mode)
HXT	0	1024 HXT cycles	1024 HXT cycles		1~2 HXT cycles
	1	1024 HXT cycles	1~2 f_{SUB} cycles (System runs with f_{SUB} first for 1024 HXT cycles and then switches over to run with the HXT clock)		1~2 HXT cycles
ERC	X	15~16 ERC cycles	15~16 ERC cycles		1~2 ERC cycles
HIRC	X	15~16 HIRC cycles	15~16 HIRC cycles		1~2 HIRC cycles
LIRC	X	1~2 LIRC cycles	1~2 LIRC cycles		1~2 LIRC cycles
LXT	X	1024 LTX cycles	1024 LXT cycles		1~2 LXT cycles

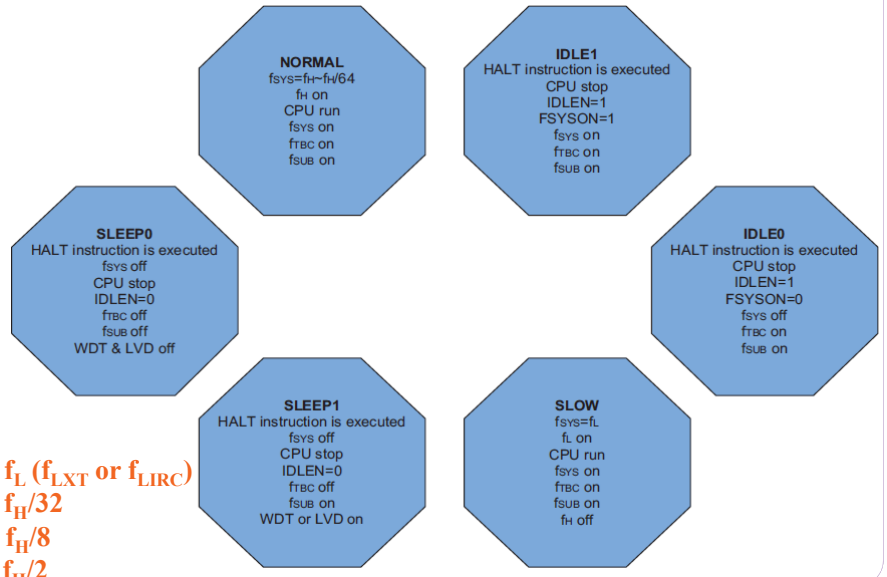
Holtek – Wake up / Fast Wake-up



Wake-up After the system enters the **SLEEP** or **IDLE** Mode, it can be woken up from one of various sources listed as follows:

- **An external reset**
- **An external falling edge on Port A**

  Port A pins from high to low.
- **A system interrupt**
- **A WDT overflow**



CKS2~CKS0: fsys

000: f_L (f_{LXT} or f_{LIRC}) 001: f_L (f_{LXT} or f_{LIRC})
010: $f_H/64$ 011: $f_H/32$
100: $f_H/16$ 101: $f_H/8$
110: $f_H/4$ 111: $f_H/2$

Lab program

Holtek – Low Voltage Detector (LVD)

❒ Each device has a **Low Voltage Detector** function, also known as **LVD**.

- This enabled the device to **monitor the power supply voltage, VDD**, and **provide a warning signal** should it fall below a certain level.
- This function may be especially useful in battery applications where the supply voltage will gradually reduce as the battery ages, as it allows an early warning battery low signal to be generated.
- The **Low Voltage Detector also has the capability of generating an interrupt signal**.

• **LVDC Register**

Bit	7	6	5	4	3	2	1	0
Name	—	—	LVDO	LVDEN	—	VLVD2	VLVD1	VLVD0
R/W	—	—	R	R/W	—	R/W	R/W	R/W
POR	—	—	0	0	—	0	0	0

Bit 7~6 unimplemented, read as 0

Bit 5 LVDO: LVD Output Flag
0: No Low Voltage Detect
1: Low Voltage Detect

Bit4 LVDEN: Low Voltage Detector Control
0: Disable
1: Enable

Bit 3 unimplemented, read as 0

Bit 2~0 VLVD2 ~ VLVD0: Select LVD Voltage
000: 2.0V 001: 2.2V
010: 2.4V 011: 2.7V
100: 3.0V 101: 3.3V
110: 3.6V 111: 4.4V

When the device is **powered down** the Low Voltage Detector will remain active if the **LVDEN bit is high**. In this case, the **LVF interrupt request flag will be set,** causing an interrupt to be generated **if VDD falls below the preset LVD voltage**. This will cause **the device to wake-up from the SLEEP or IDLE Mode, however if the Low Voltage Detector wake up function is not required then the LVF flag should be first set high before the device enters the SLEEP or IDLE Mode.**

Note : **Another reset** exists in the form of a **Low Voltage Reset, LVR**, where **a full reset, similar to the RES reset** is implemented in **situations where the power supply voltage falls below a certain threshold**.

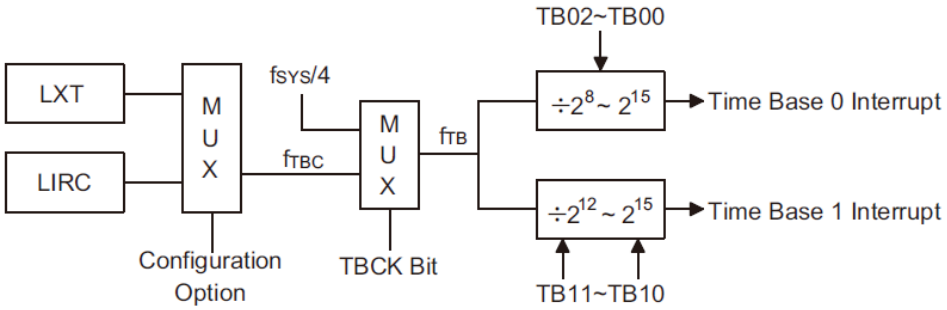
Holtek – Time Base Interrupt

The function of the Time Base Interrupts is to provide regular time signal in the form of an internal interrupt. They are controlled by the overflow signals from their respective timer functions.

TBC Register

Bit	7	6	5	4	3	2	1	0
Name	TBON	TBCK	TB11	TB10	LXTLP	TB02	TB01	TB00
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W
POR	0	0	1	1	0	1	1	1

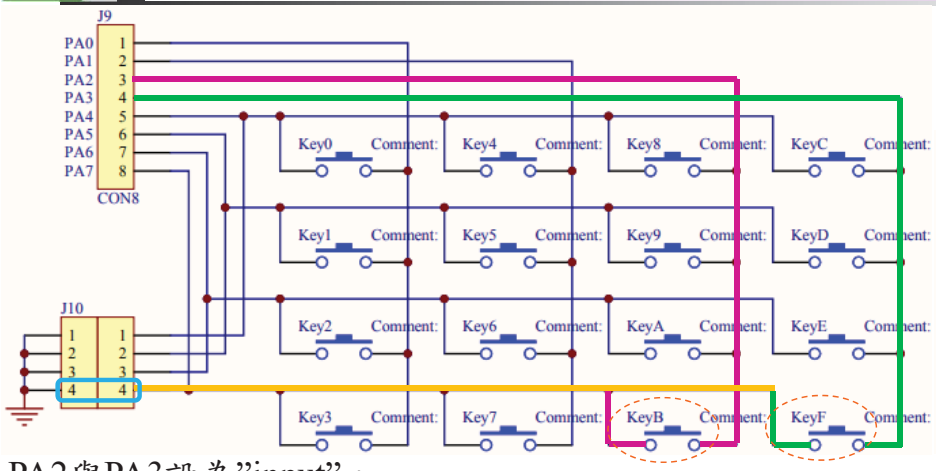
Bit 7 TBON: TB0 and TB1 Control
0: Disable; 1: Enable
Bit 6 TBCK: Select f_{TB} Clock
0: f_{TBC} ; 1: $f_{SYS}/4$
Bit 5~4 TB11~TB10: Select Time Base 1 Time-out Period
00: $4096/f_{TB}$; 01: $8192/f_{TB}$
10: $16384/f_{TB}$; 11: $32768/f_{TB}$
Bit 3 LXTLP: LXT Low Power Control
0: Disable; 1: Enable
Bit 2~0 TB02~TB00: Select Time Base 0 Time-out Period
000: $256/f_{TB}$
001: $512/f_{TB}$
010: $1024/f_{TB}$
011: $2048/f_{TB}$
100: $4096/f_{TB}$
101: $8192/f_{TB}$
110: $16384/f_{TB}$
111: $32768/f_{TB}$



Holtek – Operating Mode Switching

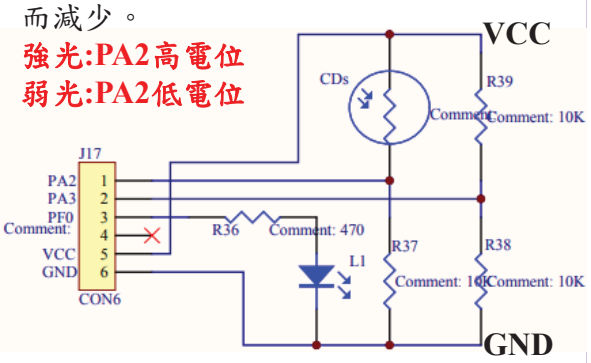
- The device can **switch between operating modes dynamically** allowing the user to **select the best performance/power ratio** for the present task in hand.
  - ⇨**Microcontroller operations** that **do not require high performance** can be **executed using slower clocks** thus requiring **less operating current and prolonging battery** life in **portable applications**.
  - ⇨**Mode Switching between the NORMAL Mode and SLOW Mode** is executed **using the HLCLK bit and CKS2~CKS0 bits in the SMOD register.**
  - ⇨**Mode Switching from the NORMAL/SLOW Modes to the SLEEP/IDLE Modes** is executed **via the HALT instruction**.
- When a **HALT** instruction is executed, whether the device **enters the IDLE Mode or the SLEEP Mode** is determined by the condition of **the IDLEN bit in the SMOD register** and **FSYSON in the WDTC register**.
- When the **HLCLK** bit switches to a **low level**, which implies that clock source is switched from the high speed clock source, f_H, to the **clock source, $f_H/2$~$f_H/64$ or f_L**.
  - ⇨**If the clock is from the f_L, the *high speed clock source will stop running*** to **conserve power**.
  - ⇨When this happens it must be noted that the **$f_H/16$ and $f_H/64$ internal clock sources will also stop running**, which may **affect the operation of other internal functions** such as the **TMs and** the **SIM**.
- **NORMAL Mode to SLOW Mode Switching :**
  The SLOW Mode is sourced from the LXT or the LIRC oscillators and therefore requires these oscillators to be **stable before full mode switching occurs**. This is **monitored using the LTO bit in the SMOD register**.
- **SLOW Mode to NORMAL Mode Switching :**
  As **a certain amount of time will be required for the high frequency clock to stabilize**, the **status of the HTO bit is checked**. The amount of time required for high speed system oscillator stabilization depends upon which high speed system oscillator type is used.

Holtek – Assignment / Exercise Lab03



CDS光敏電阻照光為低電阻狀態，未照光為高阻抗狀態，電阻值隨光強度增加而減少。

強光:PA2高電位
弱光:PA2低電位



PA2與PA3設為”input”，

- 按下按鈕”B”與”F”，分別將PA2與PA3透過J10的第四組端點的jump連接下地，等同輸入為”0”。
- 未按下按鈕”B”與”F”，PA2與PA3等同處於浮接的狀態，此次電路功能設計上，乃希望此時的PA2與PA3輸入為高準位”1”，因此，必須啟動PA2與PA3腳位內部的pull-up電路功能，讓PA2與PA3可透過PMOSFET連接至VDD。

Assignment: 兩種情況擇一即可，完成(1)或(2)，(2)的分數較高。

兩種情況: 基本上，以第一種為原則。第二種情況只是將CPU的PA2從接至按鍵那邊的PA2改接至CDS那邊PA2，但是，**要注意原來的PA2 pull-up電阻是否會跟未照光的CDS電阻並聯而呈現偏低電阻，導致PA2的輸出無法為”0”，若是如此情況，必須將PA2的pull-up電阻功能關閉。**

(1)鬆開PA2，讓系統進入IDLE狀態，按下PA2，喚醒系統，使系統正常運作。(不使用PA3)
檢查時，按住PA2(“B”鍵)，確保8x8 LEDs能正常依序顯示，“N”、“K”、“N”、“U”。然後鬆開以檢查是否系統休眠。接著，透過按與不按PA2檢查是否功能正常。

(2)將PA2改接至CDS的PA2，強光時，系統休眠。弱光時，8x8 LEDs能正常顯示。