LibreSilicon's 1st Test Wafer
(珠江芯片一号)

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Abstract

Document Revision History

VERSION	DATE	DESCRIPTION	TRACKING NOTES
Draft 0.0	2018-05-25	START with empty document, ADD Ring Oscillator	-

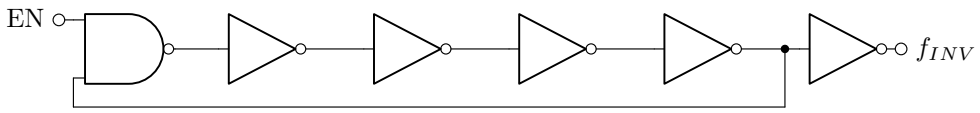
Chapter 1

Ring Oscillators

Ring Oscillators are the hidden Champions in case of qualifying a process.

Here is a example of a Ring Oscillator with 5 inverting stages (build with inverters).

Schematic (Ring Oscillator with INV-Gates)



If $EN = 0$ the Ring Oscillator does nothing. But when EN becomes 1, the output of the most left NAND2 Gate depends on the other input. With both inputs for the NAND2 Gate are 1, the output goes to 0, otherwise the output is 1.

Hence we can describe EN as a high-active Enable signal.

Assuming now $EN = 1$, the Ring Oscillator is enabled, the NAND3 Gate delivers the inverted input value from the long feedback line on his output. Assuming there was a level change, this edge propagates through every gate (which takes time t_D for every INV Gate). At $n \cdot t_D$ this edge cames back over the feedback line with inverted polarity, while using odd numbers only of inverting Gates.

While edges progagates once through the long line of inverting gates and arrives on the enabling gate again inverted, after 2 runs, this forms a waveform on f_{INV} which is similiar to a clock with a 50-50 duty cycle. The last buffer, between the feedback line and the output pin, is just a buffer to keep the driven capacaty on the output line low. Now we can say, that the frequency of the output signal depends just on the delay t_D over the inverting gates. The Equation for odd numbers of n is

$$f_{INV} = \frac{1}{2n \cdot t_D} \tag{1.1}$$

Usually, Ring Oscillators are build from 100..150 Gates in one row. The reason for that is the lowpass characteristic of PAD Cells - the output frequency on PAD cells should be below their cut-off frequency.

With a reasonable guessed value of t_D and equation 1.1 we can now adjust f_{INV} below the cut-off frequency.

At this point we should think about t_D which depends of course from different parameters, at least

1. the Supply Voltage for the inverting Gates,
2. the current Temperature,
3. and the Quality of the processed technology for every Gate.

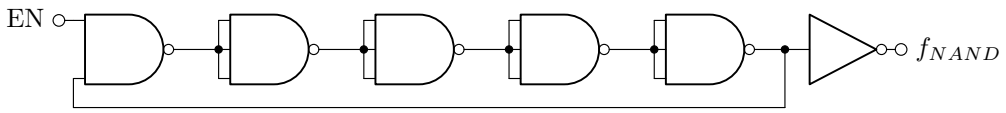
All three items matter for Process Evaluation and Process Calibration, just by indirect measurement of t_D under different test conditions. BTW, t_D follows equation 1.1 as

$$t_D = \frac{1}{2n \cdot f_{INV}} \tag{1.2}$$

If you are already familiar with cell design, you migth be knowing that the delay t_D over the gate differs for both edges. We assume here, that the transistor sizes for PMOS and NMOS transistors are well balanced with a relationship of $\gamma = 2$ and therefor t_D has the same value for both edges.

With knowledge of the Ring Oscillator build by simple Inverting Gates, we might think about more advanced cells with different transistor sizes. The schematic with NAND Gates looks quite similiar.

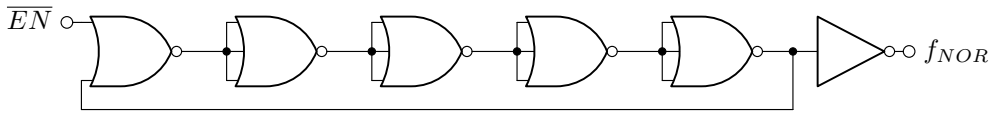
Schematic (Ring Oscillator with NAND3-Gates)



While using 3-input NAND Gates, all inputs on every gate are wired together. Using just 2-input NAND Gates would be possible also but not recommended as 3-input NAND Gates having one more stacked transisor and are heavier to process accuratly. Hence getting the oscillating output frequency on f_{NAND} means much more.

Adapting the same scheme on NOR3-Gates we get this third Ring Oscillator schematic.

Schematic (Ring Oscillator with NOR3-Gates)



Now please, make yourself familiar with the method of "Logical Effort" for calculating the transistor sizes to get well balanced cells. We still assume that $\gamma = 2$, where the PMOS transistors are 2 times bigger than the NMOS transistors.

As the logical effort differs for every type of Gate (and therefor there delay), we can calculate the relationship between all output frequencies f_{INV}, f_{NAND} and f_{NOR}.

The highest output frequency should have the INV Gate based Ring Oscillator (f_{INV}) with the lowest logical effort $g = \frac{3}{3}$, followed by the NAND3 Gate based Ring Oscillator (f_{NAND}) with logical effort $g = \frac{5}{3}$. The lowest frequency should have the NOR3 Gate based Ring Oscillator (f_{NOR}) with logical effort of $g = \frac{7}{3}$.

According the calculation of getting the delay from the logical effort, the relations can be expressed as

$$f_{INV} \approx f_{max} \tag{1.3}$$

$$f_{NAND} \approx \frac{9}{11} \cdot f_{INV} \tag{1.4}$$

$$f_{NOR} \approx \frac{9}{13} \cdot f_{INV} \tag{1.5}$$