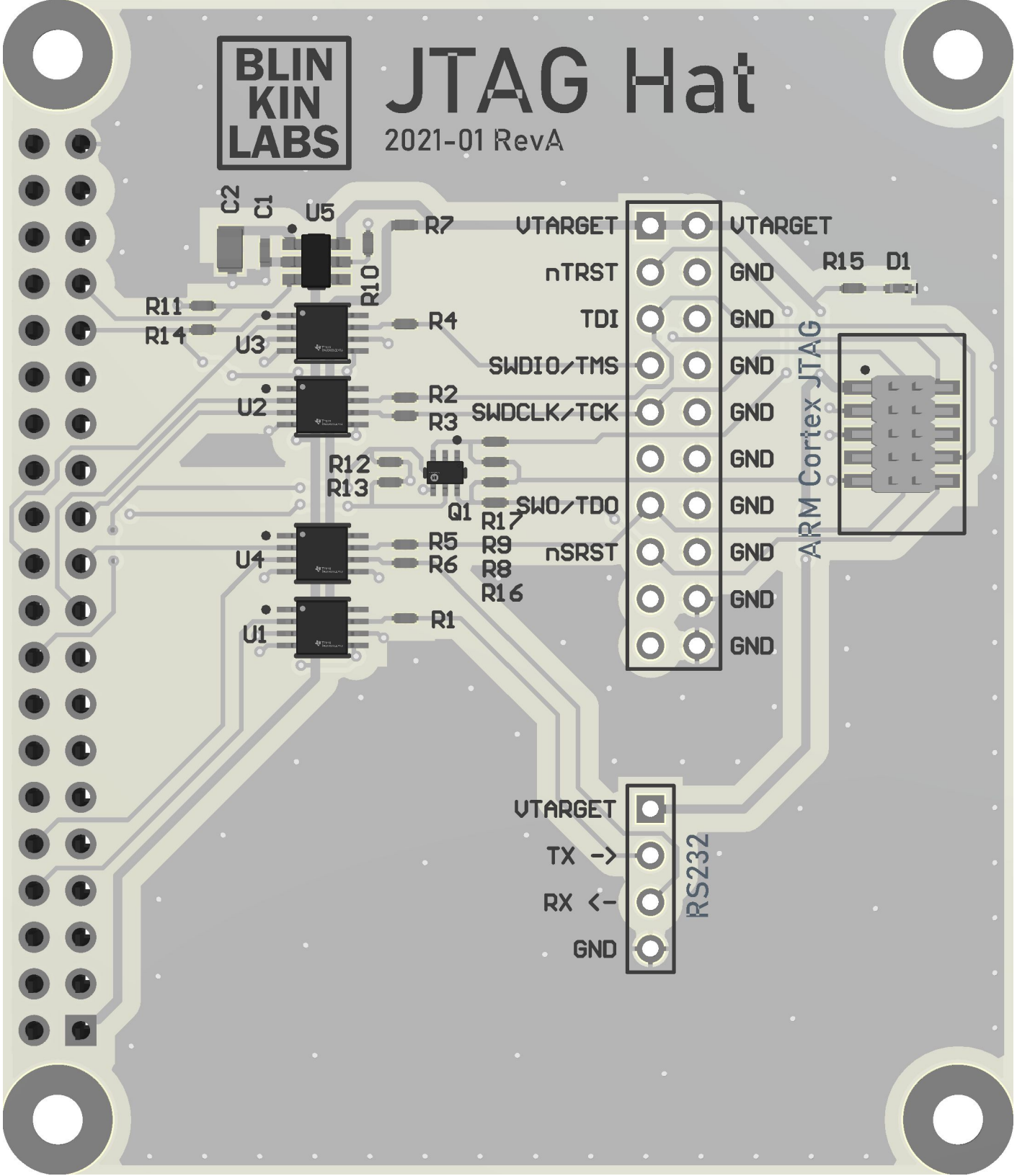
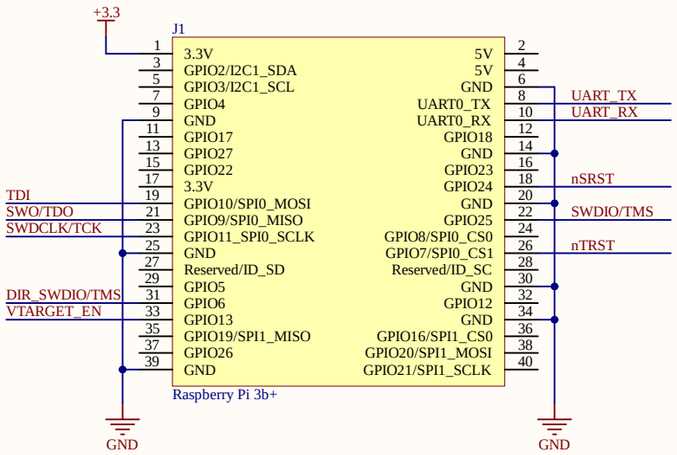

BLIN
KIN
LABS
JTAG Hat
2021-01 RevA
C2
C1
U5
R7
R10
R11
R14
U3
R4
U2
R2
R3
R12
R13
Q1
R17
R5
R9
R6
R8
R16
U4
U1
R1
VTARGET
nTRST
TDI
SWDIO/TMS
SWDCLK/TCK
SWO/TDO
nSRST
GND
R15
D1
ARM Cortex JTAG
VTARGET
TX ->
RX <-
GND
RS232

JTAG Hat

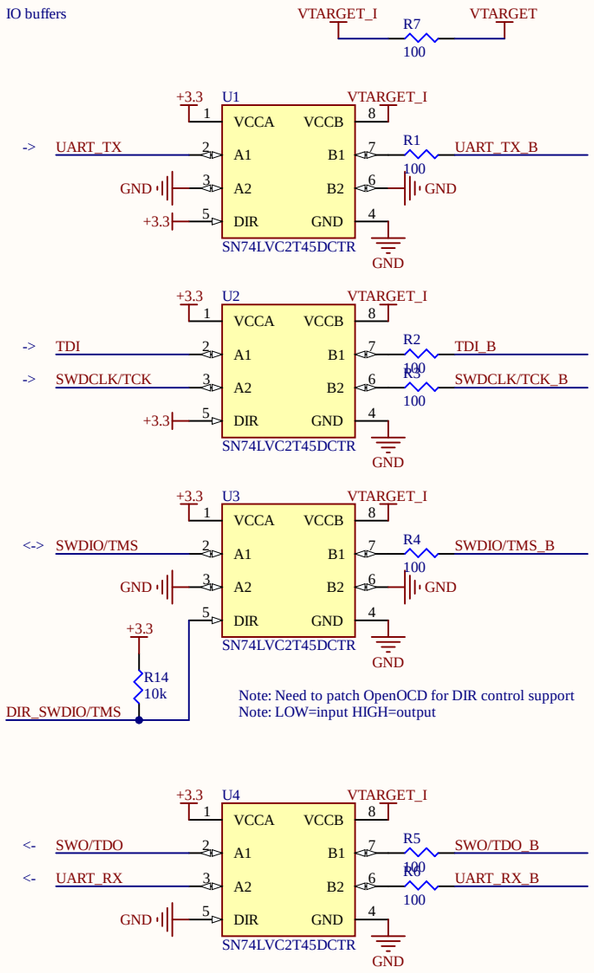
OpenOCD JTAG board for Raspberry Pi 2/3/4, with target voltage isolation

Raspberry Pi header

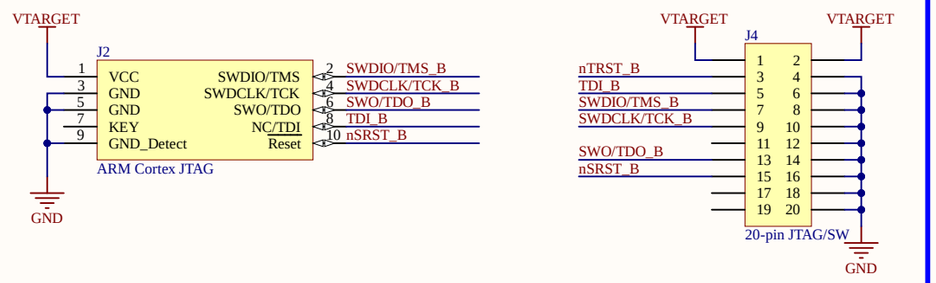



```
# Each of the JTAG lines need a gpio number set: tck tms tdi tdo
# Header pin numbers: 23 22 19 21
bcm2835gpio_jtag_nums 11 25 10 9

# Each of the SWD lines need a gpio number set: swclk swdio
# Header pin numbers: 23 22
bcm2835gpio_swd_nums 11 25

# If you define trst or srst, use appropriate reset_config
# Header pin numbers: TRST - 26, SRST - 18
```

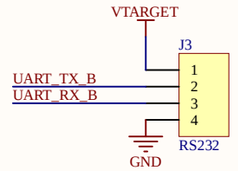
IO buffers



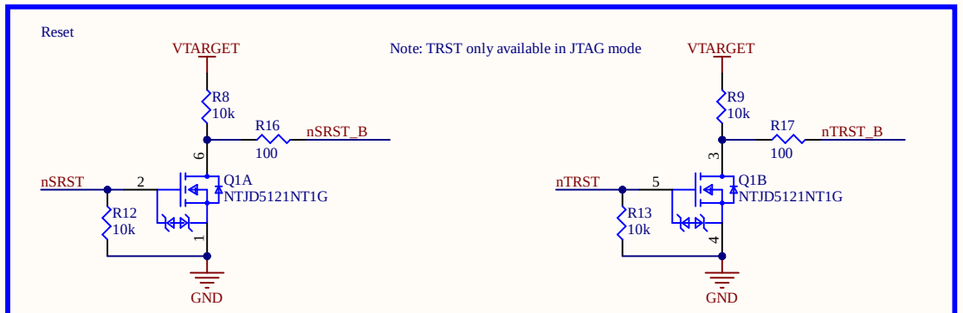
JTAG headers



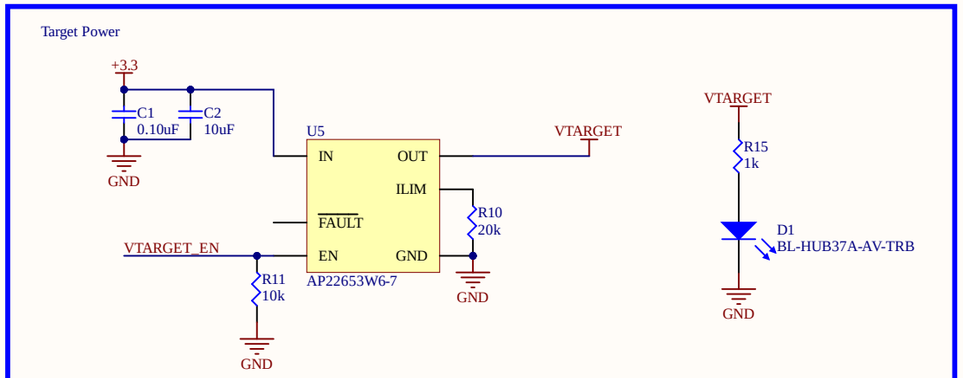
UART header



Reset



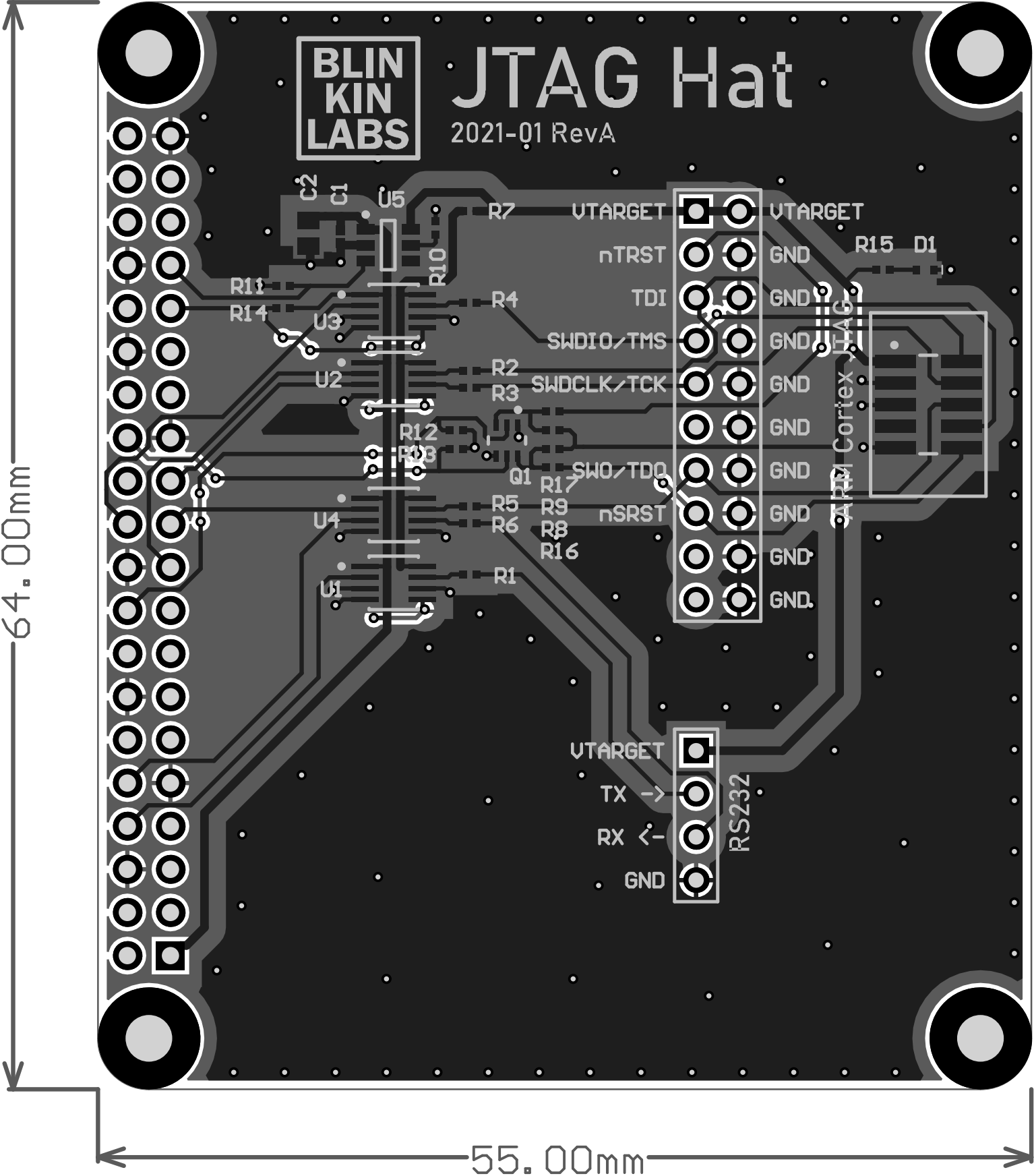
Target Power



BLIN KIN LABS

Title: *		
Project: JTAG Hat		Revision: RevA
Date: 1/21/2021	Time: 11:54:53 PM	Sheet * of *

BLIN KIN LABS


BLIN
KIN
LABS
JTAG Hat
2021-Q1 RevA
C2
C1
U5
R7
VTARGET
VTARGET
nTRST
GND
R15
D1
R10
R11
R14
U3
R4
TDI
GND
SWDIO/TMS
GND
ARM Cortex JTAG
U2
R2
R3
SWDCLK/TCK
GND
R12
R13
GND
Q1
SWO/TDO
GND
R17
R5
R9
nSRST
GND
U4
R6
R8
R16
GND
R1
U1
GND
VTARGET
TX ->
RX <-
GND
RS232
64.00mm
55.00mm

Design Rules Verification Report

Filename : C:\Users\blinkinlabs\Desktop\JTAG_hat\pcb\PCB1.PcbDoc

Warnings 0
Rule Violations 48

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=1mm) (InNamedPolygon('pg_gnd_fill')),(All)	0
Clearance Constraint (Gap=0.254mm) (All),(All)	1
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.508mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=6mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	22
Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)	15
Silk to Silk (Clearance=0.254mm) (All),(All)	1
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	9
Room Sheet1 (Bounding Region = (104.14mm, 41.656mm, 174.625mm, 122.301mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Prefered=12.7mm) (All)	0
Total	48

Clearance Constraint (Gap=0.254mm) (All),(All)
Clearance Constraint: (0.22mm < 0.254mm) Between Pad C1-1(14.3mm,49.81mm) on Top Layer And Pad

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm) Between Pad C1-1(14.3mm,49.81mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R10-1(19.9mm,51.1mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R1-1(21.527mm,30.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R11-1(10.5mm,47.3mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R12-1(21.5mm,38.8mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R13-1(21.5mm,37.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R14-1(10.5mm,46mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R15-1(46.65mm,48.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R16-1(26.4mm,36.6mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R17-1(26.4mm,39.9mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R2-1(21.527mm,42.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R3-1(21.527mm,41.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R4-1(21.527mm,46.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R5-1(21.527mm,34.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R6-1(21.527mm,33.315mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R7-1(21.5mm,51.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R8-1(26.4mm,37.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad R9-1(26.4mm,38.8mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-1(15.775mm,50.65mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-2(15.775mm,49.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-4(18.425mm,48.75mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm) Between Pad U5-5(18.425mm,49.7mm) on Top Layer And

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad D1-2(49.275mm,48.25mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-1(46.977mm,42.855mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-1(46.977mm,42.855mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-10(50.877mm,37.775mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-10(50.877mm,37.775mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.254mm) Between Pad J2-2(50.877mm,42.855mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-2(50.877mm,42.855mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-3(46.977mm,41.585mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-4(50.877mm,41.585mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-5(46.977mm,40.315mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-6(50.877mm,40.315mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-7(46.977mm,39.045mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-8(50.877mm,39.045mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-9(46.977mm,37.775mm) on Top Layer
And
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-9(46.977mm,37.775mm) on Top Layer
And

Silk to Silk (Clearance=0.254mm) (All),(All)
Silk To Silk Clearance Constraint: (Collision < 0.254mm) Between Text "R17" (26.2mm,35.2mm) on Top Overlay And Te›

Board Clearance Constraint (Gap=0mm) (All)
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(3mm,3mm) on
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(3mm,61mm) on
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(52mm,3mm) on
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(52mm,61mm) on
Board Outline Clearance(Outline Edge): (0.372mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.372mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.372mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.373mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.373mm < 0.508mm) Between Board Edge And Track

Electrical Rules Check Report

Class	Document	Message
Warning	Sheet1.SchDoc	Component Q1 NTJD5121NT1G at 10100mil,4400mil: Can't perform revision status validation: Revision not found.
Warning	Sheet1.SchDoc	Component Q1 NTJD5121NT1G: Can't perform revision status validation: Revision not found.
Warning	Sheet1.SchDoc	GND contains IO Pin and Power Pin objects (Pin U1-3, Pin U1-6, Pin U3-3, Pin U3-6, Pin J2-3, Pin J2-5, Pin J2-9, Pin U1-4, Pin U2-4, Pin U3-4, Pin U4-4)
Warning	Sheet1.SchDoc	Net DIR_SWDIO/TMS has no driving source (Pin J1-31, Pin R14-1, Pin U3-5)