

RPi GPIO	Signal
GPIO_25	SWDIO/TMS
GPIO_11	SWDCLK/TCK
GPIO_9	TDO
GPIO_10	TDI
GPIO_24	nSRST
GPIO_7	nTRST
GPIO_13	VTARGET_EN
GPIO_6	DIR_SWDIO

-  +5V
-  GND
-  +3.3V
-  GND



JTAG Hat

2021-05 RevB.1

Cortex Debug

VTARGET	SWDIO/TMS
GND	SWDCLK/TCK
GND	TDO
	TDI
GND	nSRST

VTARGET

nTRST

TDI

SWDIO/TMS

SWDCLK/TCK

N/C

TDO

nSRST

N/C

N/C

VTARGET

TX ->

RX <-

GND

UART

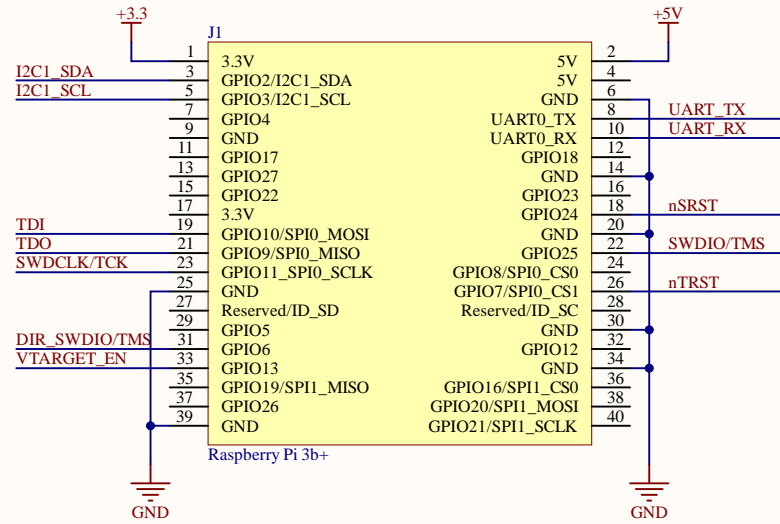
R15 D1

TARGET POWER

JTAG Hat

OpenOCD JTAG board for Raspberry Pi 2/3/4, with target voltage isolation

Raspberry Pi header

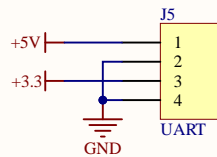


```
# Each of the JTAG lines need a gpio number set: tck tms tdi tdo
# Header pin numbers: 23 22 19 21
bcm2835gpio_jtag_nums 11 25 10 9

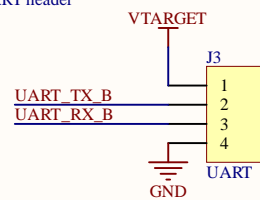
# Each of the SWD lines need a gpio number set: swclk swdio
# Header pin numbers: 23 22
bcm2835gpio_swd_nums 11 25

# If you define trst or srst, use appropriate reset_config
# Header pin numbers: TRST - 26, SRST - 18
```

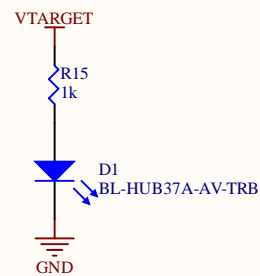
Extra Power



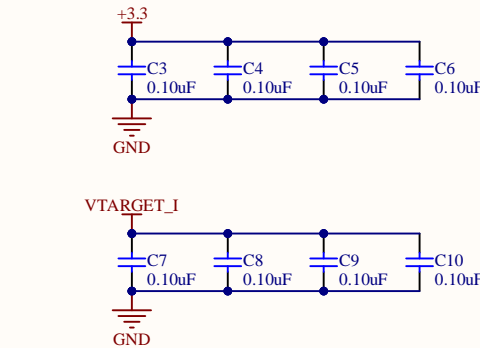
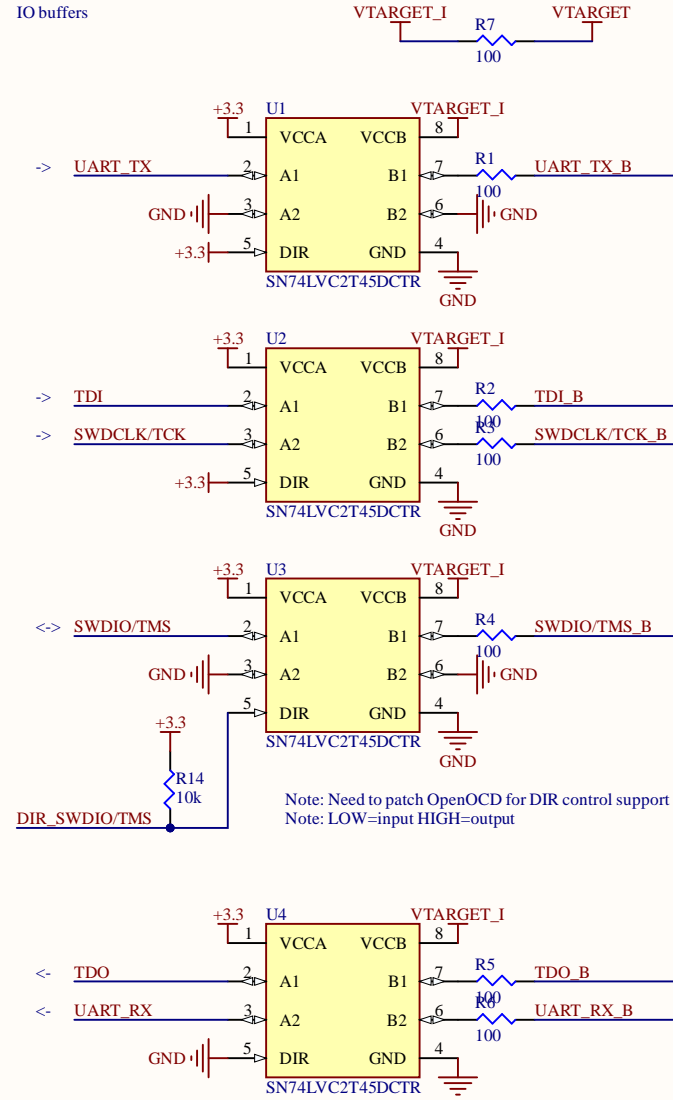
UART header



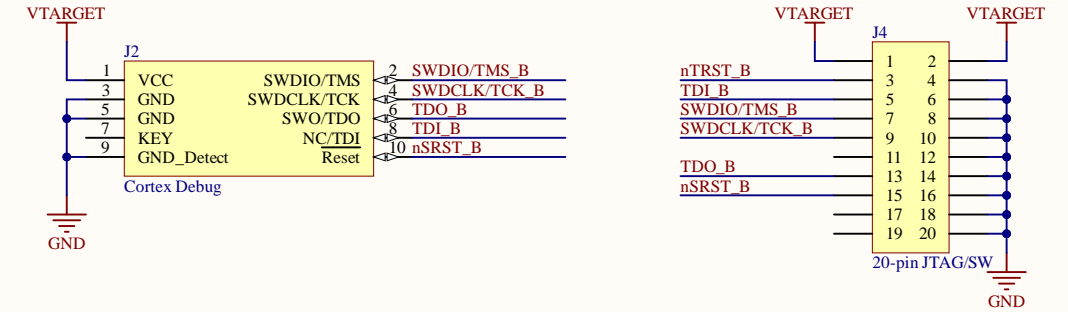
Target power indication



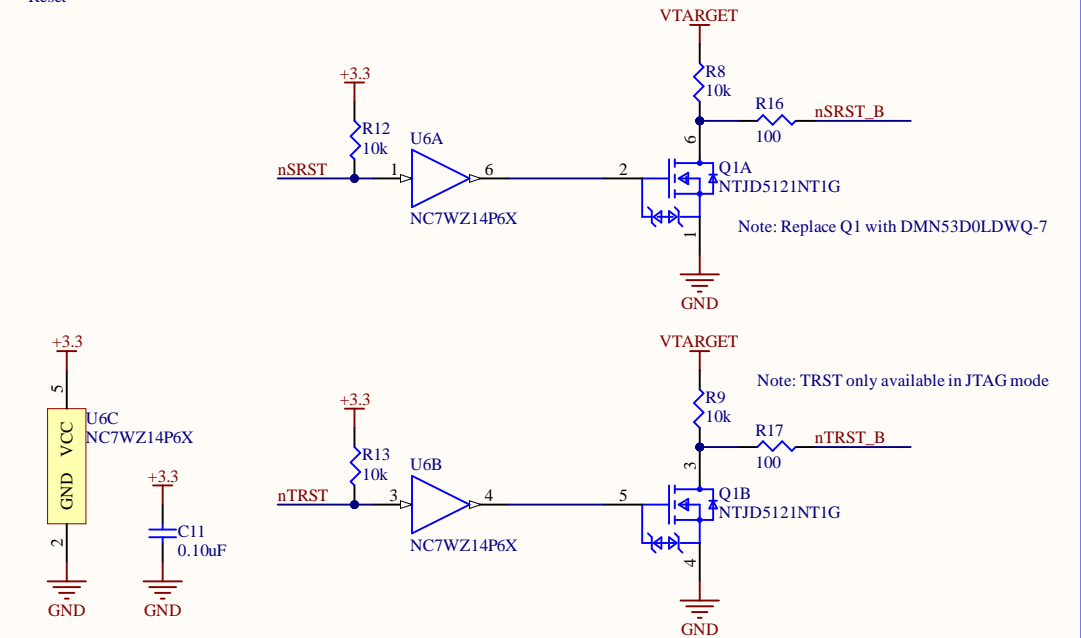
IO buffers



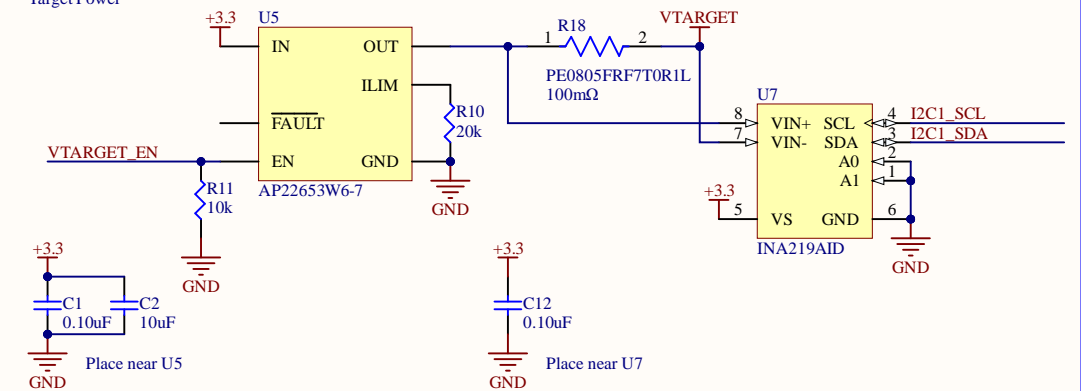
JTAG headers



Reset



Target Power



Design Rules Verification Report

Filename : C:\Users\matt\Blinkinlabs-Repos\JTAG_hat\pcb\PCB1.PcbDoc

Warnings 0
Rule Violations 79

Warnings	
Total	0

Rule Violations	
Clearance Constraint (Gap=1mm) (InNamedPolygon('pg_gnd_fill')),(All)	0
Clearance Constraint (Gap=0.254mm) (All),(All)	0
Short-Circuit Constraint (Allowed=No) (All),(All)	0
Un-Routed Net Constraint ((All))	0
Modified Polygon (Allow modified: No), (Allow shelved: No)	0
Width Constraint (Min=0.254mm) (Max=0.508mm) (Preferred=0.254mm) (All)	0
Power Plane Connect Rule(Relief Connect)(Expansion=0.508mm) (Conductor	0
Width=0.254mm)	0
Hole Size Constraint (Min=0.025mm) (Max=6mm) (All)	0
Hole To Hole Clearance (Gap=0.254mm) (All),(All)	0
Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	36
Silk To Solder Mask (Clearance=0.254mm) (Is Pad),(All)	20
Silk to Silk (Clearance=0.254mm) (All),(All)	14
Net Antennae (Tolerance=0mm) (All)	0
Board Clearance Constraint (Gap=0mm) (All)	9
Room Sheet1 (Bounding Region = (104.14mm, 41.656mm, 174.625mm, 122.301mm)	0
Height Constraint (Min=0mm) (Max=25.4mm) (Preferred=12.7mm) (All)	0
Total	79

Minimum Solder Mask Sliver (Gap=0.254mm) (All),(All)	
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C10-1(19.79mm,49.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C1-1(14.235mm,51.812mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C11-1(16mm,37.51mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C12-1(19.5mm,57.14mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C3-1(15.01mm,44.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C4-1(15.21mm,36.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C5-1(15.21mm,31.3mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C6-1(15.31mm,49.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C7-1(19.39mm,44.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C8-1(19.59mm,36.1mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.017mm < 0.254mm)	Between Pad C9-1(19.59mm,31.3mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R10-1(21mm,51.7mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R1-1(21.527mm,29.415mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R11-1(10.5mm,48.2mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R12-1(11mm,38.5mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R13-1(11mm,37.4mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R14-1(10.5mm,46.9mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R15-1(46.65mm,48.25mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R16-1(26.4mm,36.6mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R17-1(26.4mm,39.9mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R2-1(21.527mm,42.315mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R3-1(21.527mm,41.315mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R4-1(21.527mm,47.215mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R5-1(21.527mm,34.315mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R6-1(21.527mm,33.315mm) on Top Layer
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R7-1(20.2mm,50.6mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R8-1(26.4mm,37.7mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad R9-1(26.4mm,38.8mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U5-1(15.71mm,52.652mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U5-2(15.71mm,51.702mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U5-4(18.36mm,50.752mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.147mm < 0.254mm)	Between Pad U5-5(18.36mm,51.702mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad U6-1(13mm,38.95mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad U6-2(13mm,38.3mm) on Top Layer And Pad
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad U6-4(14.85mm,37.65mm) on Top Layer And
Minimum Solder Mask Sliver Constraint: (0.047mm < 0.254mm)	Between Pad U6-5(14.85mm,38.3mm) on Top Layer And
Pad	

Silk To Solder Mask (Clearance=0.254mm) (IsPad),(All)

Silk To Solder Mask Clearance Constraint: (0.242mm < 0.254mm) Between Arc (12.575mm,39.627mm) on Top Overlay And
Silk To Solder Mask Clearance Constraint: (0.225mm < 0.254mm) Between Pad D1-2(49.275mm,48.25mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-1(46.977mm,42.855mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-1(46.977mm,42.855mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-10(50.877mm,37.775mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-10(50.877mm,37.775mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.151mm < 0.254mm) Between Pad J2-2(50.877mm,42.855mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-2(50.877mm,42.855mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-3(46.977mm,41.585mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-4(50.877mm,41.585mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-5(46.977mm,40.315mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-6(50.877mm,40.315mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-7(46.977mm,39.045mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-8(50.877mm,39.045mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-9(46.977mm,37.775mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.15mm < 0.254mm) Between Pad J2-9(46.977mm,37.775mm) on Top Layer
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U6-1(13mm,38.95mm) on Top Layer Anc
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U6-3(13mm,37.65mm) on Top Layer Anc
Silk To Solder Mask Clearance Constraint: (0.25mm < 0.254mm) Between Pad U6-4(14.85mm,37.65mm) on Top Layer And
Silk To Solder Mask Clearance Constraint: (0.252mm < 0.254mm) Between Pad U6-6(14.85mm,38.95mm) on Top Layer

And

Silk to Silk (Clearance=0.254mm) (All),(All)

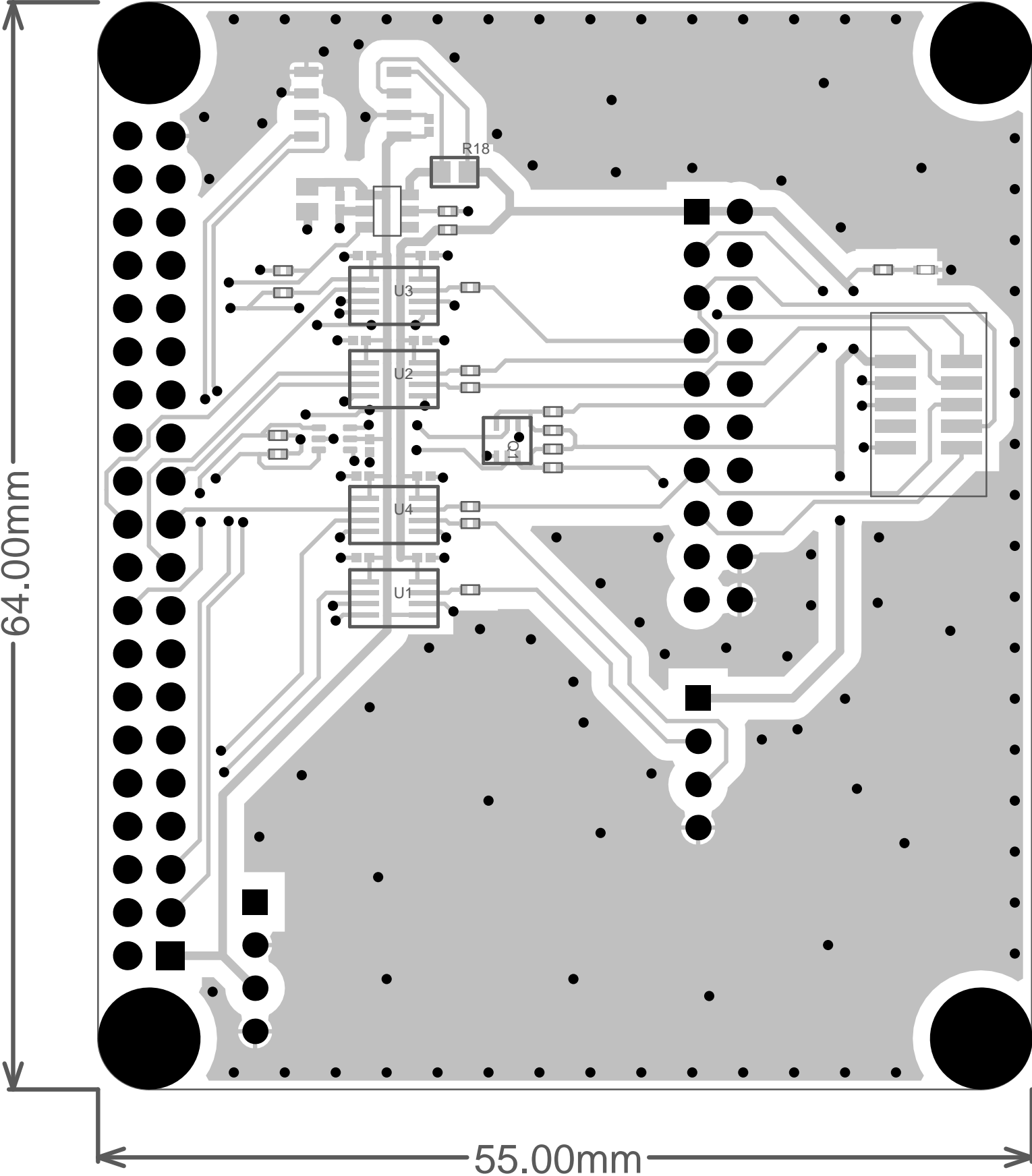
Silk To Silk Clearance Constraint: (0.254mm < 0.254mm) Between Text "Signal" (13.161mm,25.287mm) on Top Overlay And
Silk To Silk Clearance Constraint: (0.215mm < 0.254mm) Between Text "SWDCLK/TCK" (12.751mm,22.287mm) on Top
Silk To Silk Clearance Constraint: (0.201mm < 0.254mm) Between Text "SWDCLK/TCK" (12.751mm,22.287mm) on Top
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "SWDCLK/TCK" (12.751mm,22.287mm) on Top
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "SWDCLK/TCK" (12.751mm,22.287mm) on Top
Silk To Silk Clearance Constraint: (0.238mm < 0.254mm) Between Text "SWDCLK/TCK" (48.001mm,29.787mm) on Top
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "SWDCLK/TCK" (48.001mm,29.787mm) on Top
Silk To Silk Clearance Constraint: (0.215mm < 0.254mm) Between Text "SWDCLK/TCK" (48.001mm,29.787mm) on Top
Silk To Silk Clearance Constraint: (0.201mm < 0.254mm) Between Text "SWDCLK/TCK" (48.001mm,29.787mm) on Top
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "SWDIO/TMS" (13.161mm,23.787mm) on Top
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "SWDIO/TMS" (13.161mm,23.787mm) on Top
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "SWDIO/TMS" (48.411mm,31.287mm) on Top
Silk To Silk Clearance Constraint: (0.237mm < 0.254mm) Between Text "SWDIO/TMS" (48.411mm,31.287mm) on Top
Silk To Silk Clearance Constraint: (0.163mm < 0.254mm) Between Text "VTARGET" (43.463mm,31.389mm) on Top Overlay

Board Clearance Constraint (Gap=0mm) (All)

Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(3mm,3mm) on
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(3mm,61mm) on
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(52mm,3mm) on
Board Outline Clearance(Outline Edge): (Collision < 0.508mm) Between Board Edge And Pad J1-MNT(52mm,61mm) on
Board Outline Clearance(Outline Edge): (0.372mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.372mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.372mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.373mm < 0.508mm) Between Board Edge And Track
Board Outline Clearance(Outline Edge): (0.373mm < 0.508mm) Between Board Edge And Track

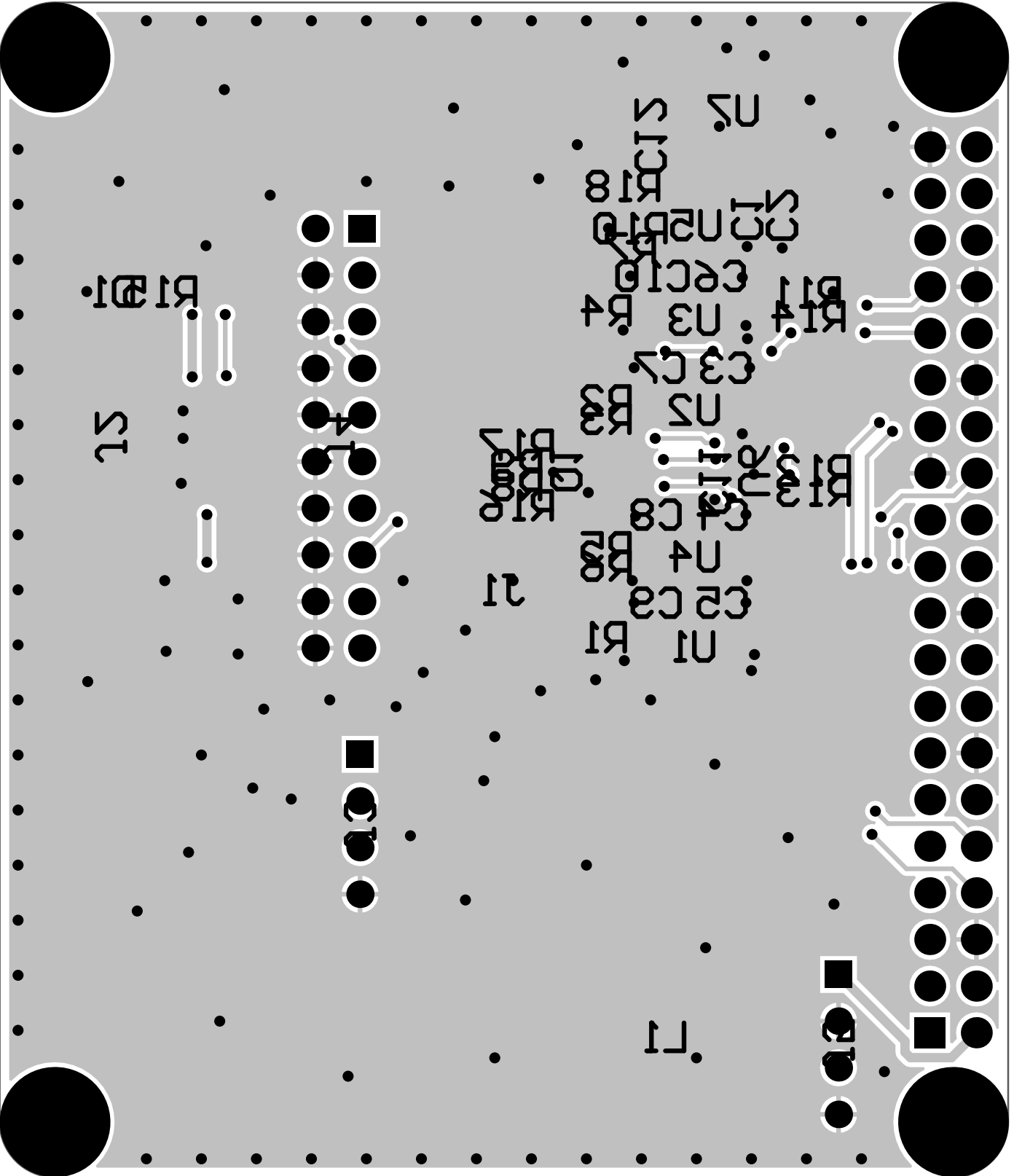
Electrical Rules Check Report

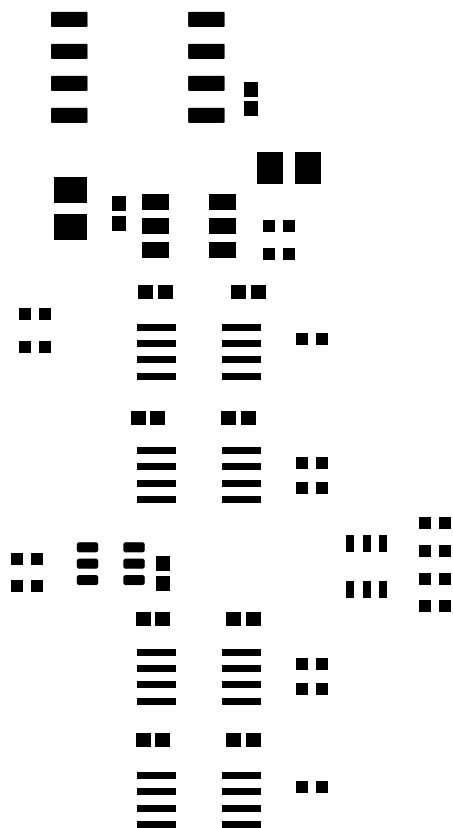
Class	Document	Message
Warning	Sheet1.SchDoc	Component Q1 NTJD5121NT1G at 12600mil,4400mil: Can't perform revision status validation: Revision not found.
Warning	Sheet1.SchDoc	Component Q1 NTJD5121NT1G: Can't perform revision status validation: Revision not found.
Warning	Sheet1.SchDoc	GND contains IO Pin and Power Pin objects (Pin U1-3, Pin U1-6, Pin U3-3, Pin U3-6, Pin J2-3, Pin J2-5, Pin J2-9, Pin U1-4, Pin U2-4, Pin U3-4, Pin U4-4, Pin U6-2, Pin U7-6).
Warning	Sheet1.SchDoc	Net DIR_SWDIO/TMS has no driving source (Pin J1-31, Pin R14-1, Pin U3-5)
Warning	Sheet1.SchDoc	Net nSRST has no driving source (Pin J1-18, Pin R12-2, Pin U6-1)
Warning	Sheet1.SchDoc	Net nTRST has no driving source (Pin J1-26, Pin R13-2, Pin U6-3)



Layer	Name	Material	Thickness	Constant	Gerber
	Top Overlay				GTO
	Top Solder	Solder Resist	0.40mil	3.5	GTS
1	Top Layer	Copper	1.40mil		GTL
	Dielectric 1	FR-4	12.60mil	4.8	
2	Bottom Layer	Copper	1.40mil		GBL
	Bottom Solder	Solder Resist	0.40mil	3.5	GBS
	Bottom Overlay				GBO

Total board thickness: 16.20mil





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