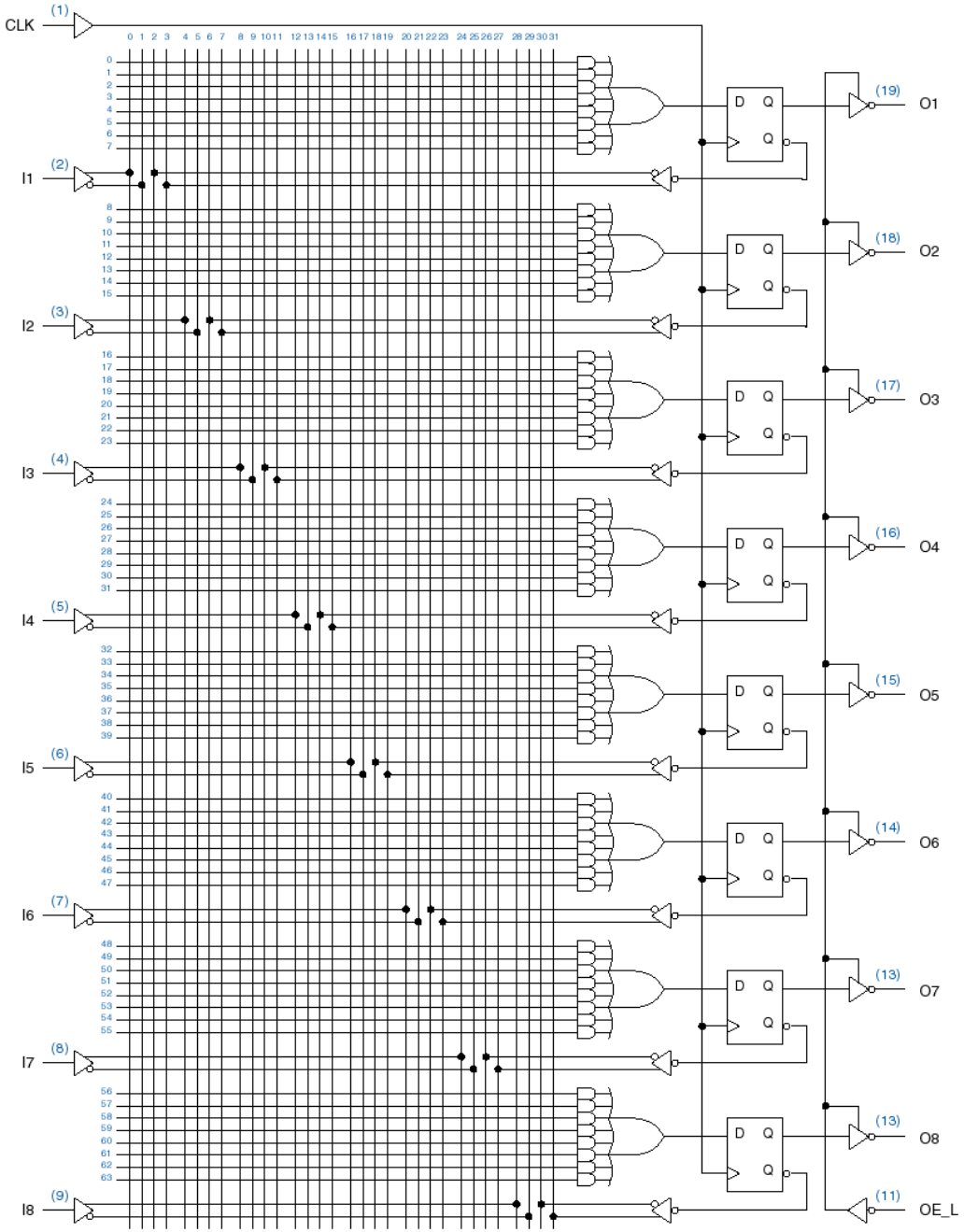
Sistemas Digitais

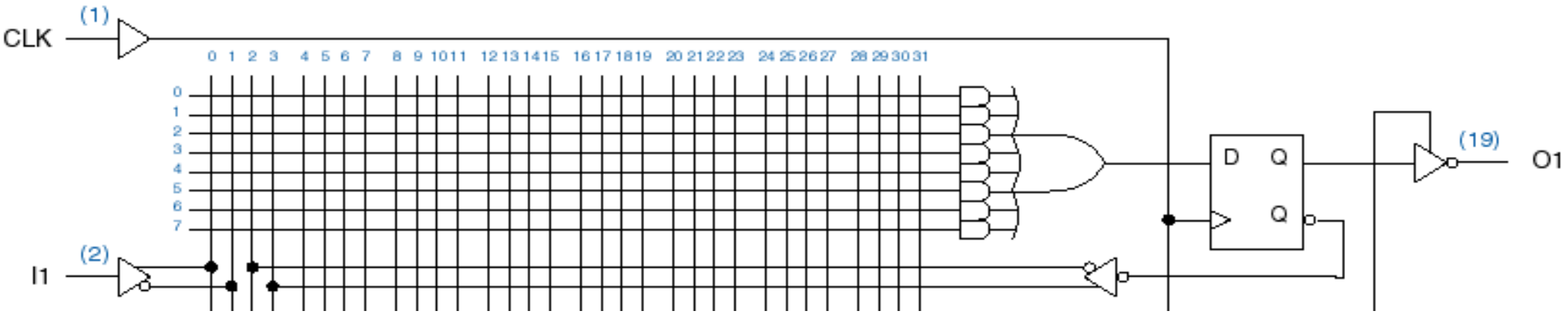
- PALs Sequenciais
- Parâmetros Temporais em PALs Sequenciais
- Registos
- Contadores
- Registos de Deslocamento (“Shift Registers”)



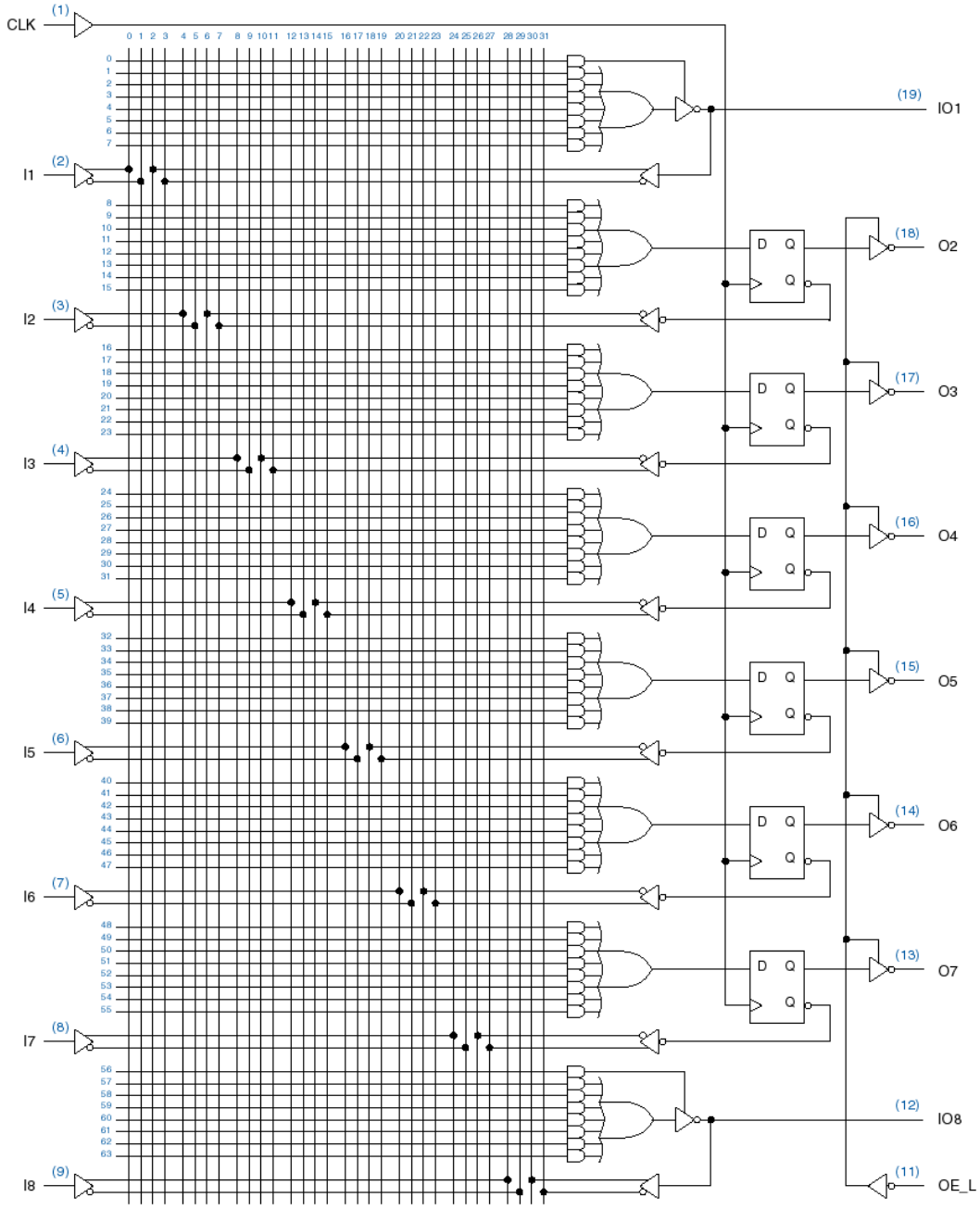
PALs Sequenciais

- 16R8

Uma Saída de 16R8



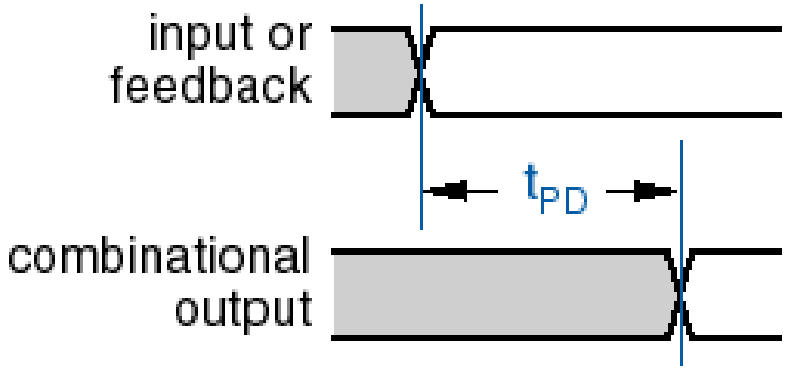
- 8 termos produto na entrada de flip-flop D
  - "positive edge triggered", relógio comum a todos FFs
- Saída Q é acessível na matriz AND
  - Necessário, por ex:, para máquinas de estados
- Saídas com 3 estados

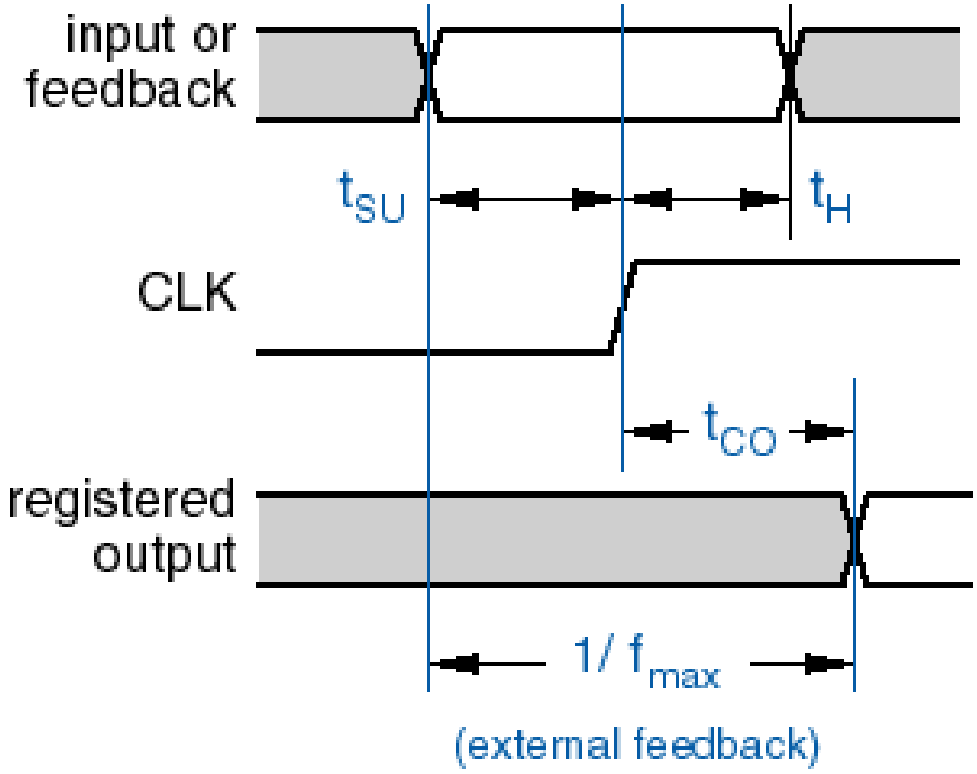


PAL16R6

- 6 saídas tipo “reg”
- 2 saídas combinacionais (como na 16L8’s)

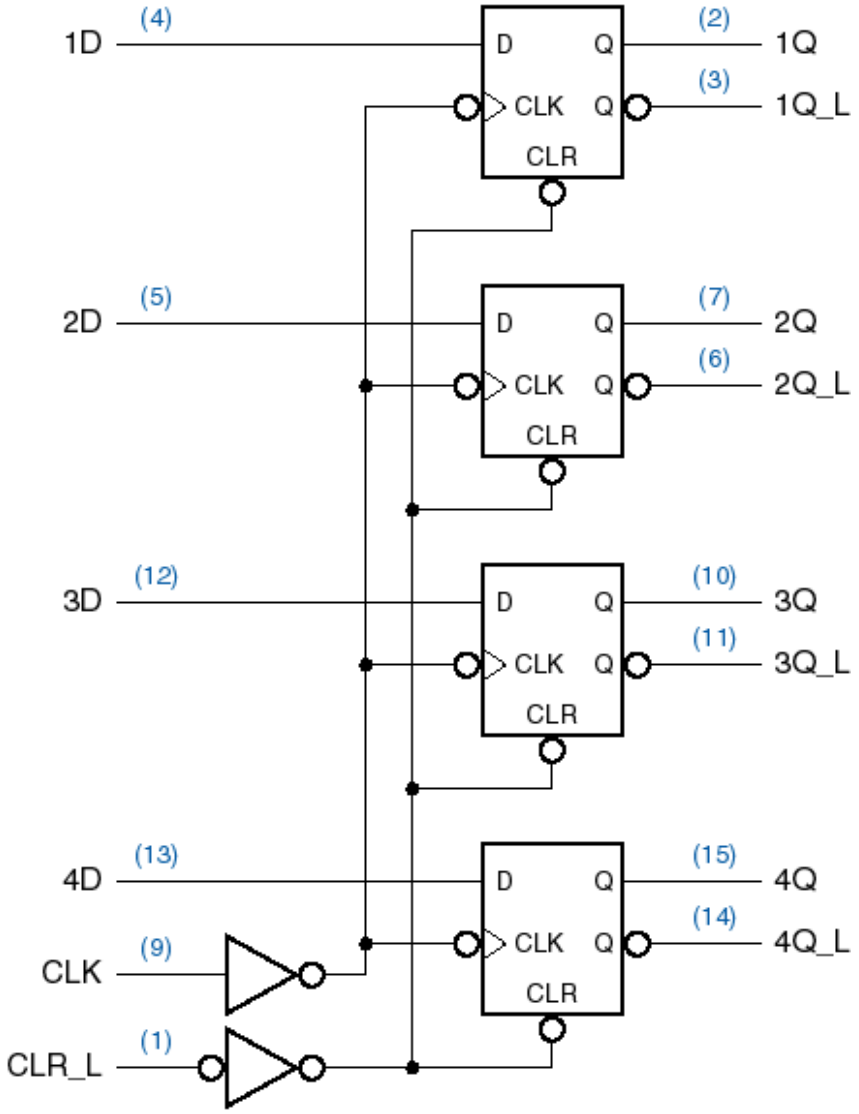
Parâmetros temporais de PLDs Sequenciais



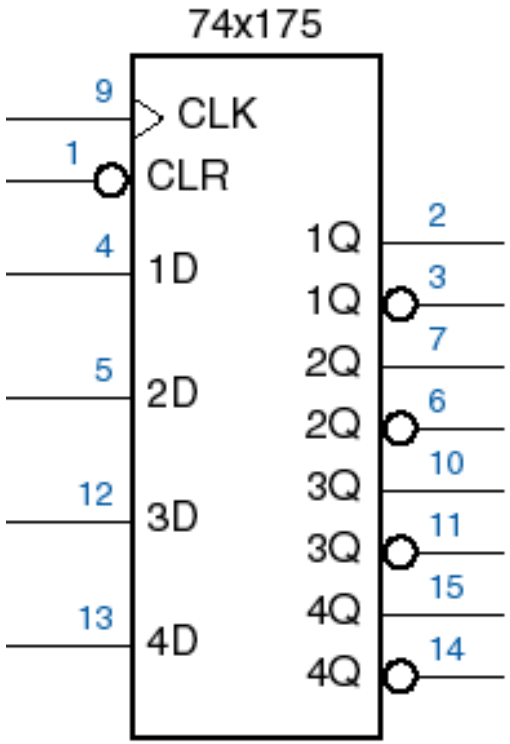


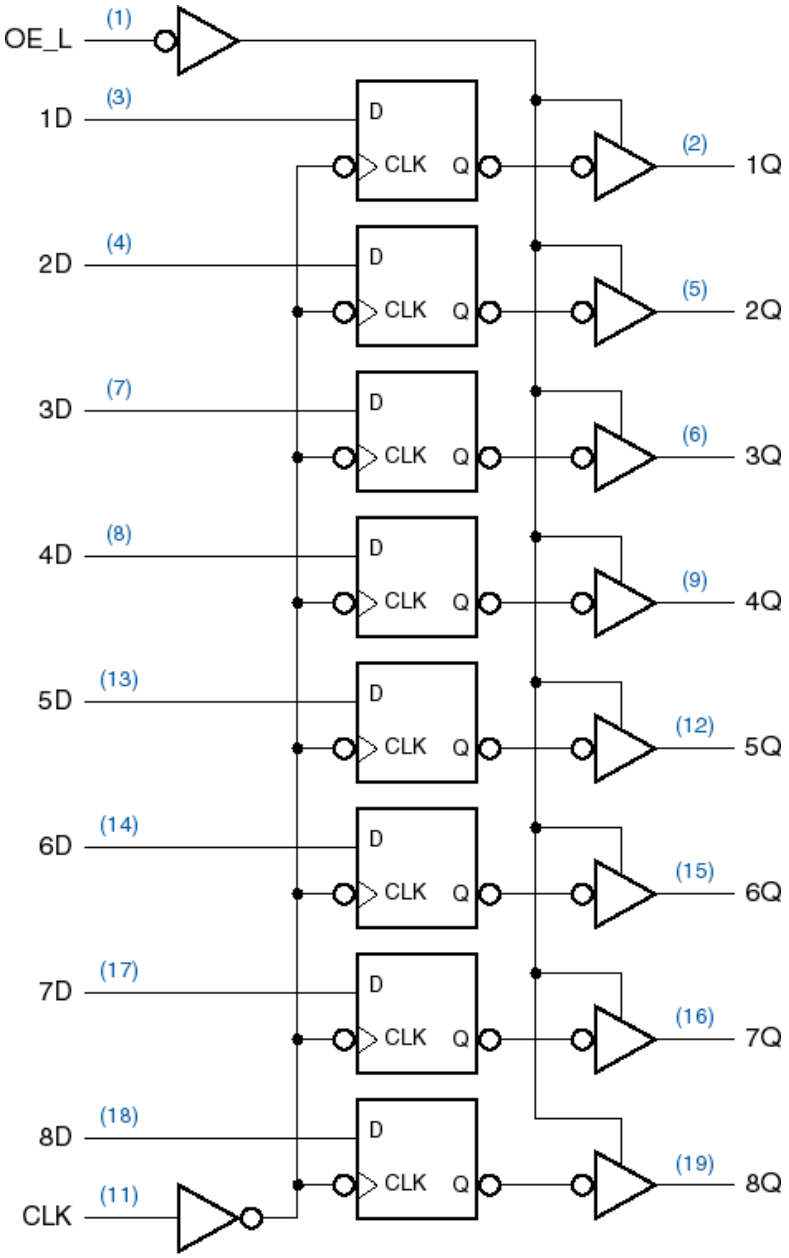
- t_{pd} -> t. propagação
- t_{su} -> t. setup
- t_{co} -> t. propagação desde clk
- t_H -> t. hold

Registos e Latches Multibit

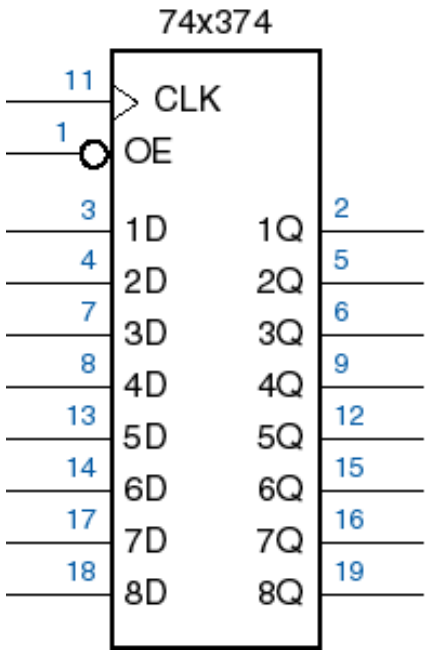


- 74x175





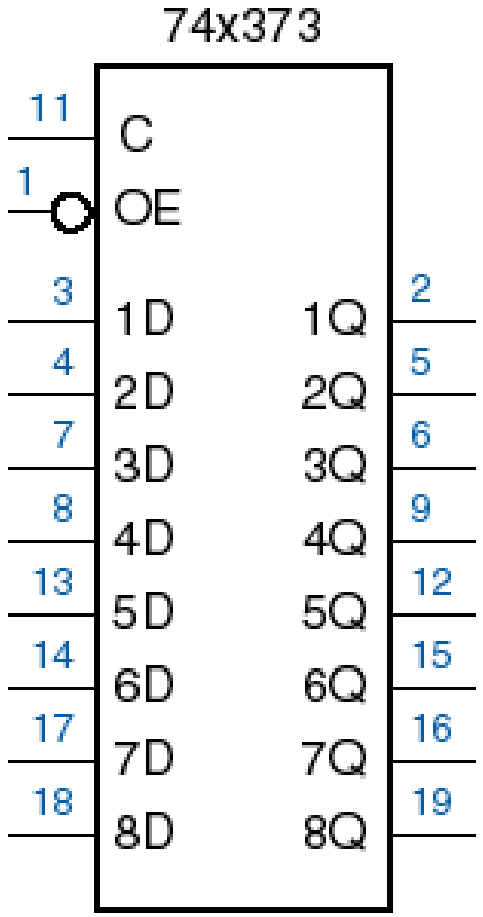
Registo 8-bit (octal)



- 74x374
  - 3 estados

“Latch” Octal

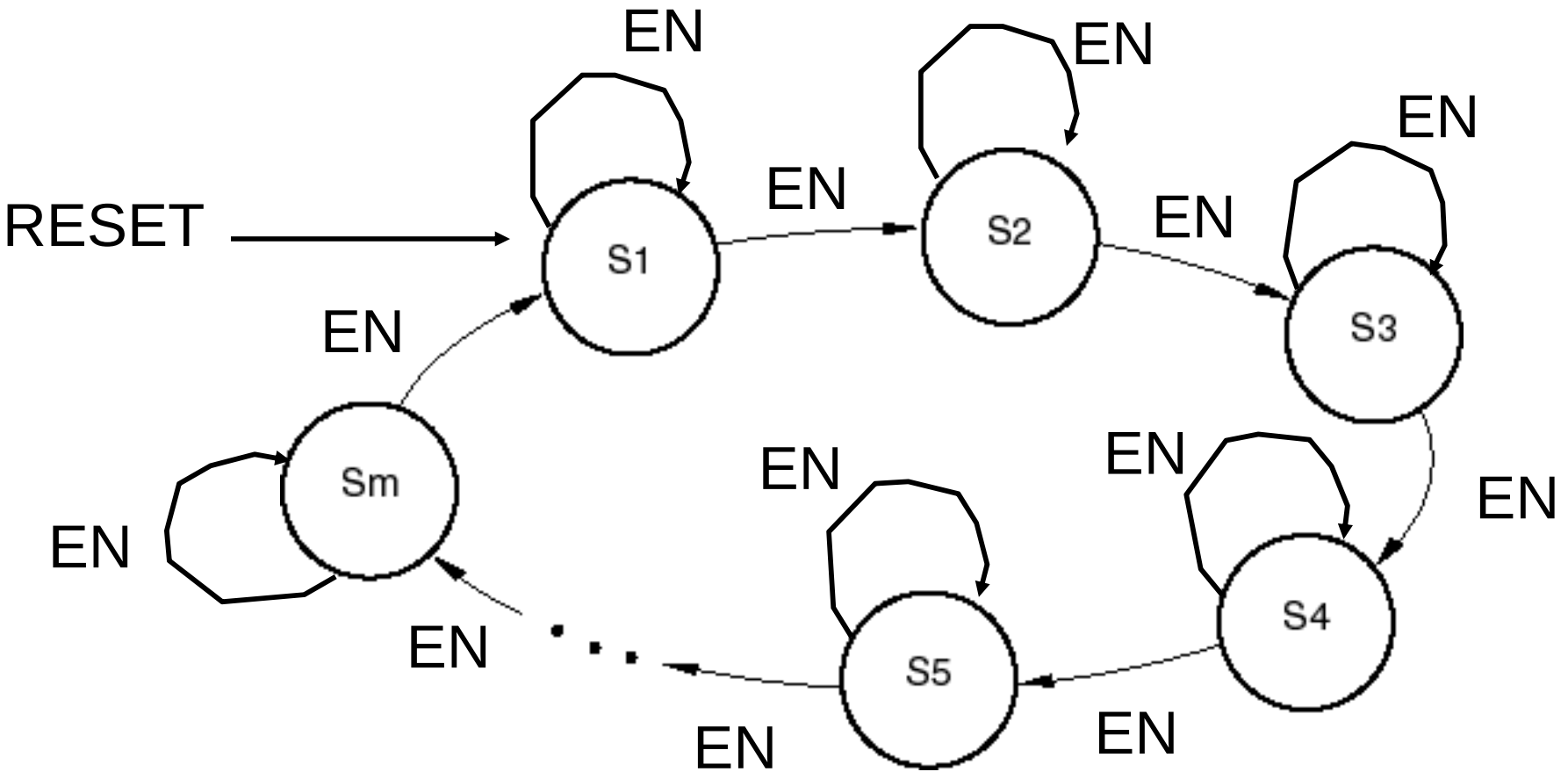
- 74x373
  - “Output enable”
  - Entrada “Latch-enable”, “C” ou “G”



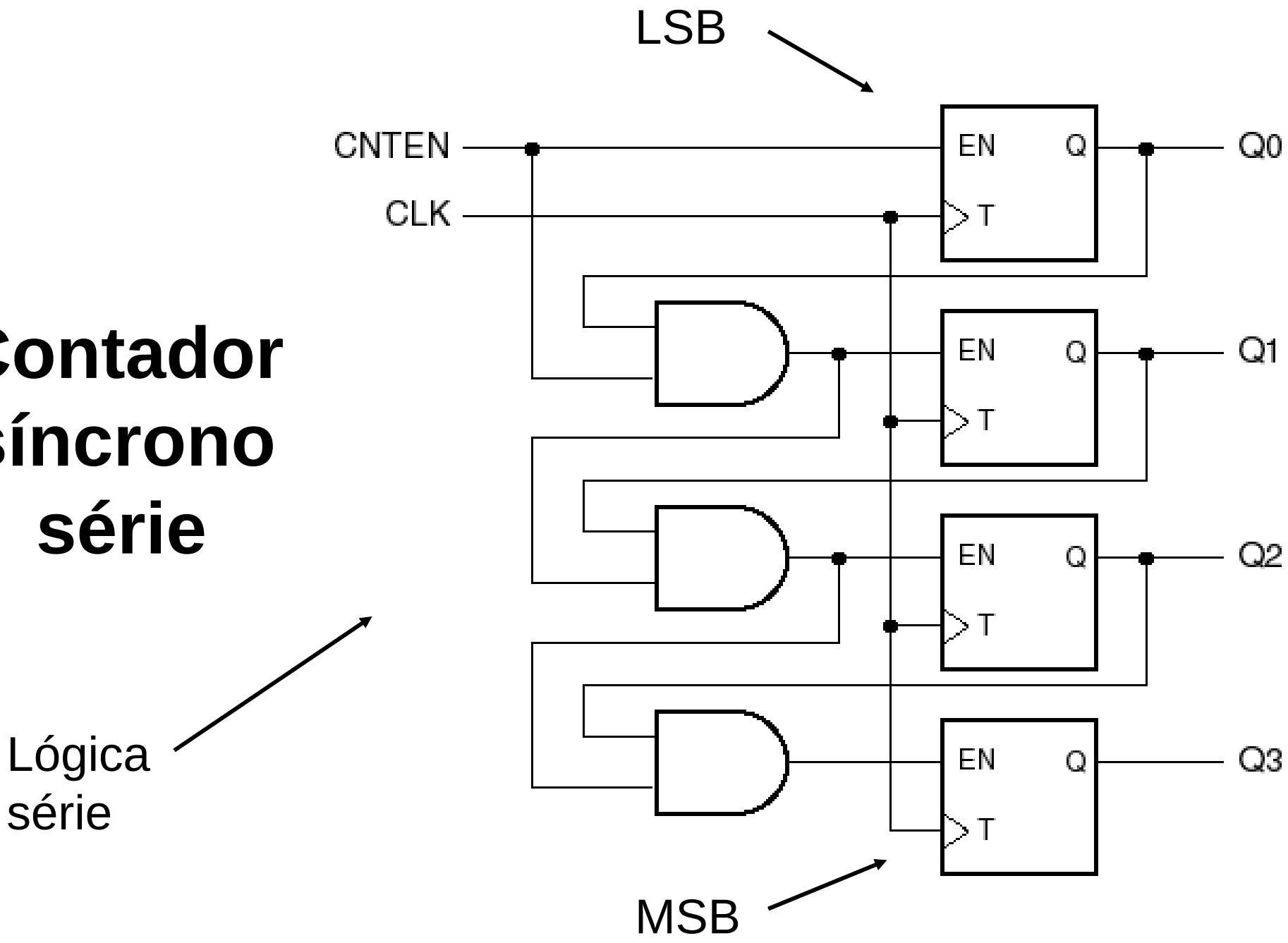
- Register vs. latch, qual a diferença?

Contadores

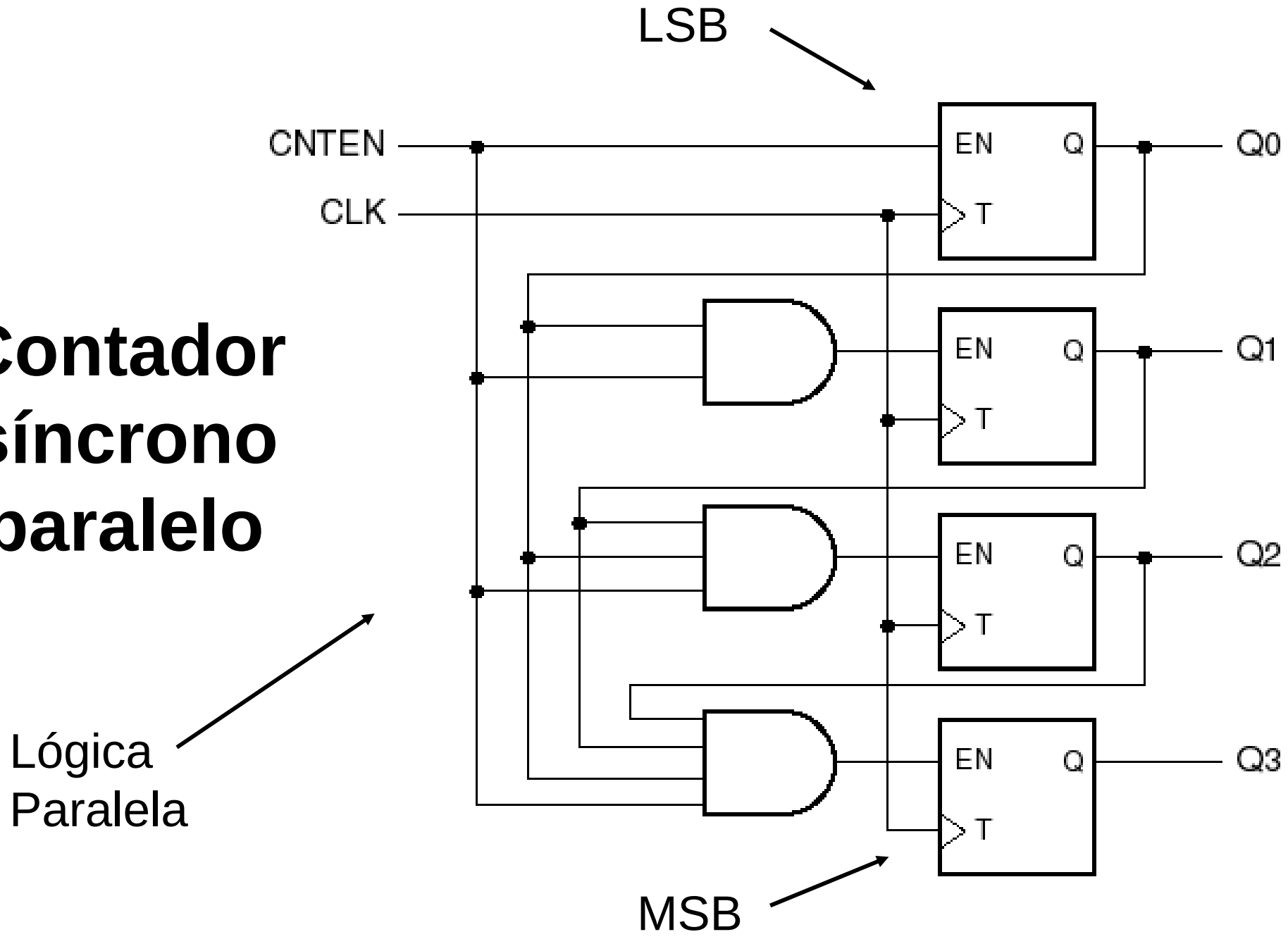
- Qualquer circuito sequencial cujo diagrama de estados é um ciclo.



Contador síncrono série

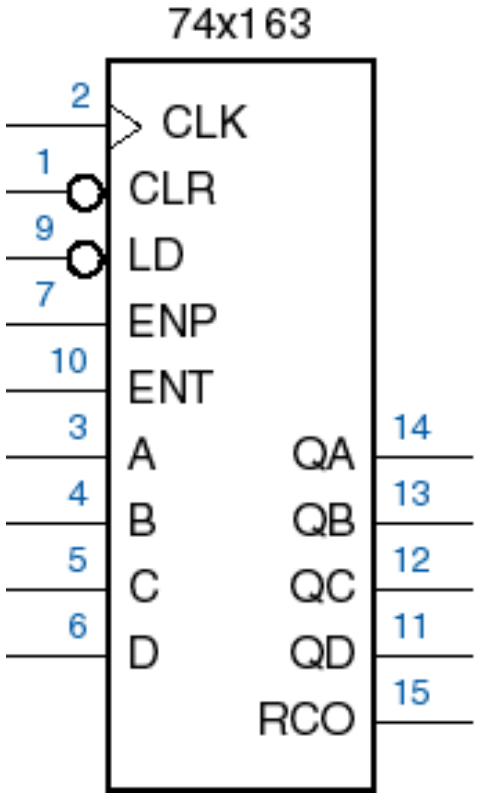


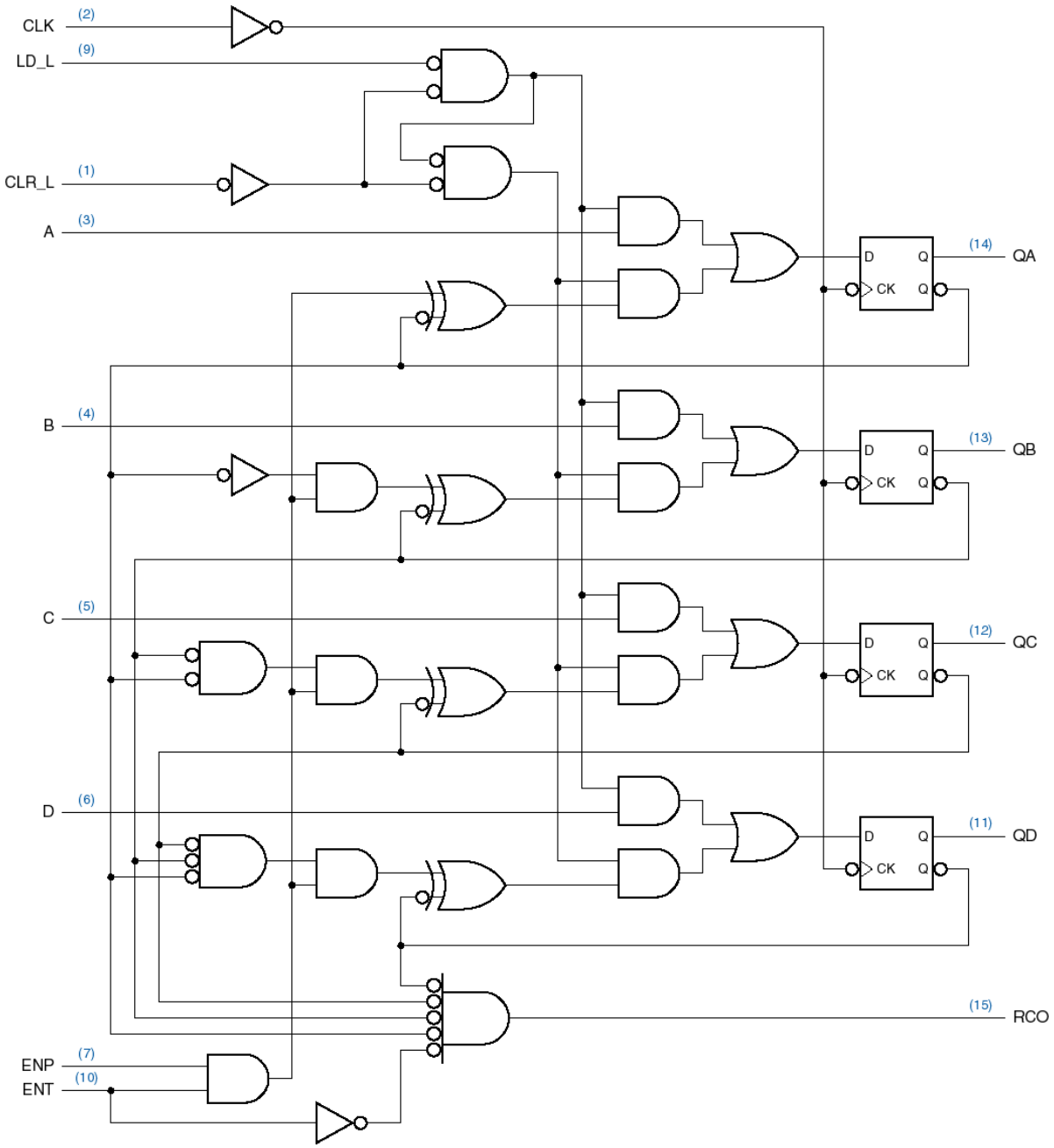
Contador síncrono paralelo



Contador MSI 4-bit 74x163

Inputs				Current State				Next State			
CLR_L	LD_L	ENT	ENP	QD	QC	QB	QA	QD*	QC*	QB*	QA*
0	x	x	x	x	x	x	x	0	0	0	0
1	0	x	x	x	x	x	x	D	C	B	A
1	1	0	x	x	x	x	x	QD	QC	QB	QA
1	1	x	0	x	x	x	x	QD	QC	QB	QA
1	1	1	1	0	0	0	0	0	0	0	1
1	1	1	1	0	0	0	1	0	0	1	0
1	1	1	1	0	0	1	0	0	0	1	1
1	1	1	1	0	0	1	1	0	1	0	0
1	1	1	1	0	1	0	0	0	1	0	1
1	1	1	1	0	1	0	1	0	1	1	0
1	1	1	1	0	1	1	0	0	1	1	1
1	1	1	1	0	1	1	1	1	0	0	0
1	1	1	1	1	0	0	0	1	0	0	1
1	1	1	1	1	0	0	1	1	0	1	0
1	1	1	1	1	0	1	0	1	0	1	1
1	1	1	1	1	0	1	1	1	1	0	0
1	1	1	1	1	1	0	0	1	1	0	1
1	1	1	1	1	1	0	1	1	1	1	0
1	1	1	1	1	1	1	0	1	1	1	1
1	1	1	1	1	1	1	1	0	0	0	0



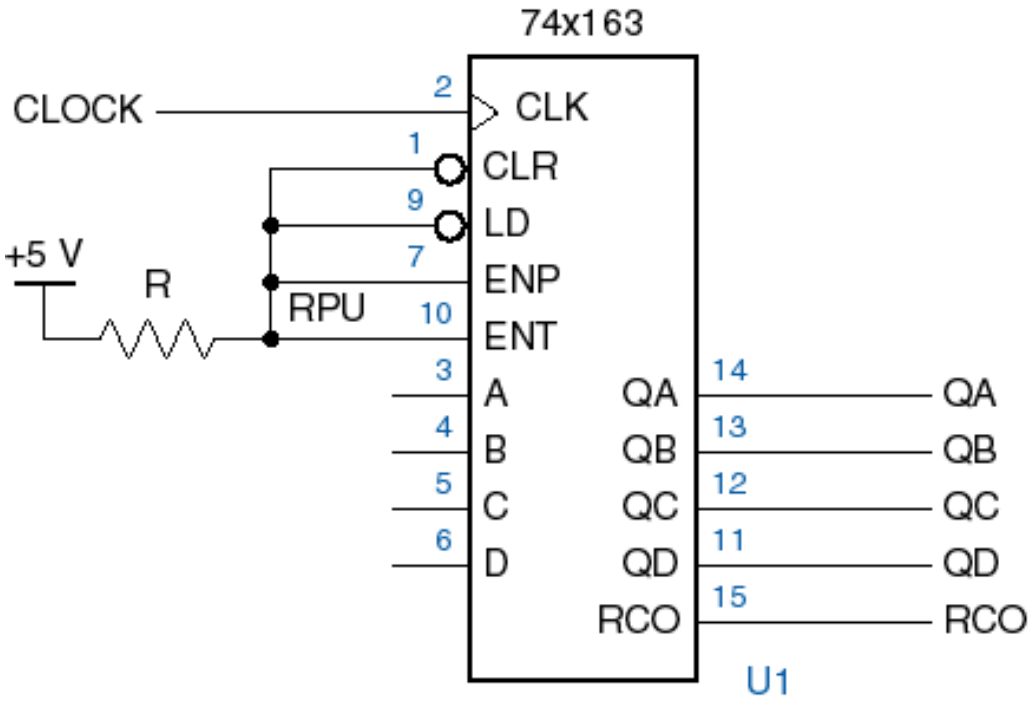


74x163

- Portas XOR formam a função “T”
- Estrutura como Mux para a carga

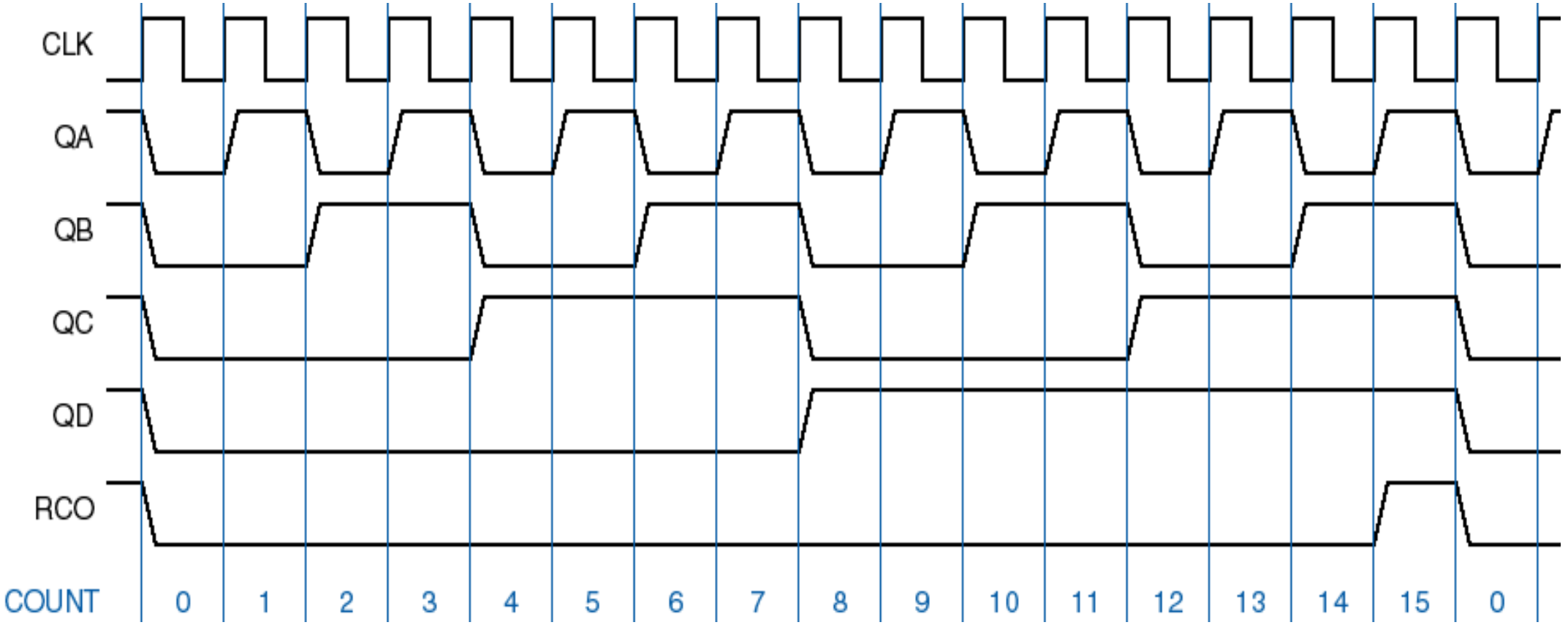
Operação do Contador

- Divisor por ÷16
- Conta se ENP e ENT activos.
- Carga se LD é activado
- Limpa se CLR é activado



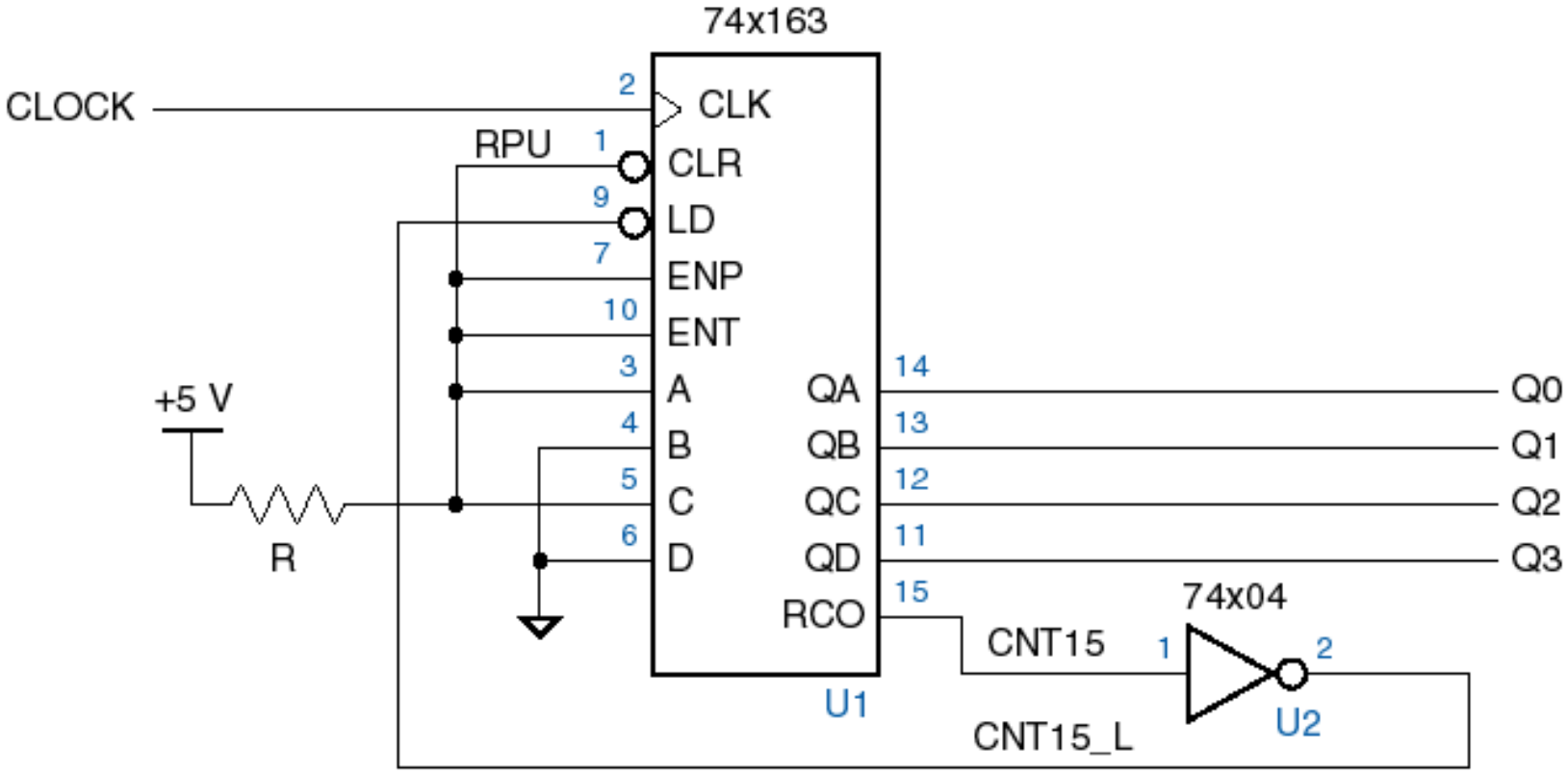
- Saídas mudam após transição positiva do CLK.
- RCO é activado se ENT é activado e QD,QC,QB,QA = 15.

Contador 4-bit ’163 (“Free-running”)



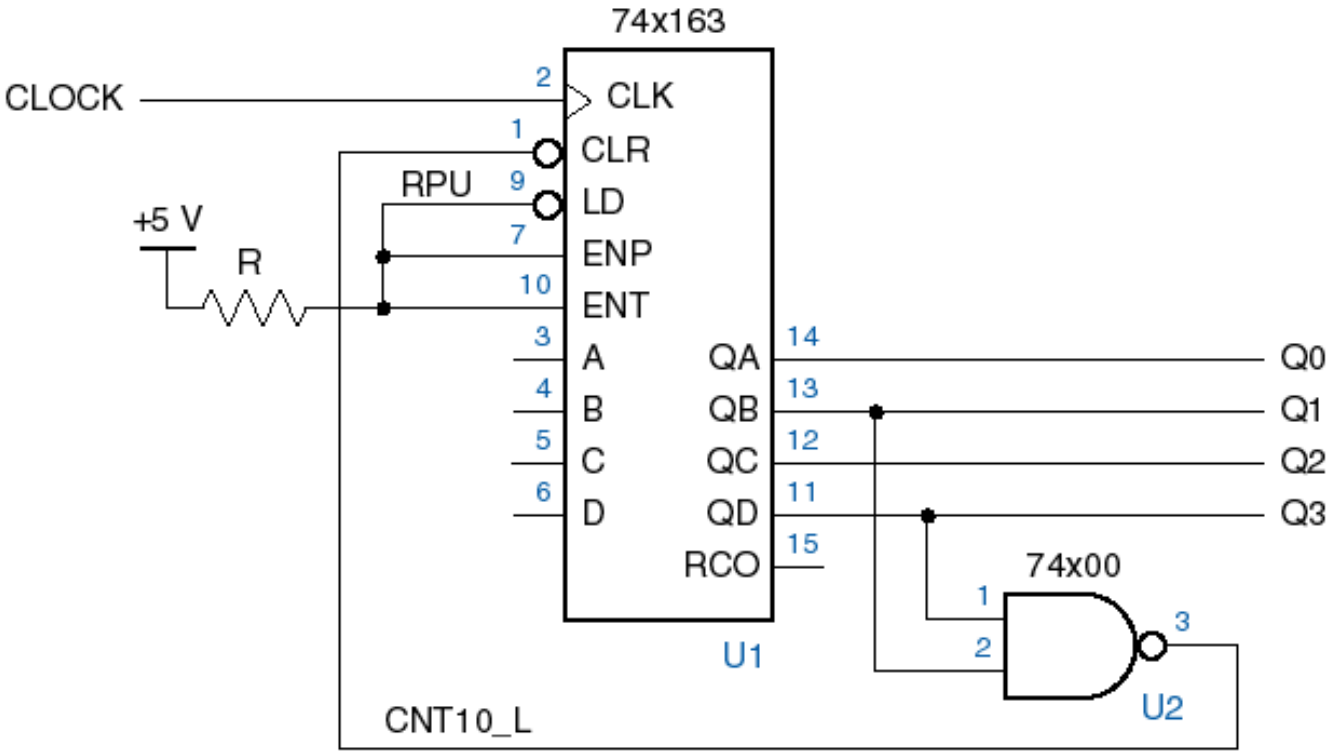
- Contador “divide-by-16”

Sequência de contagem modificada



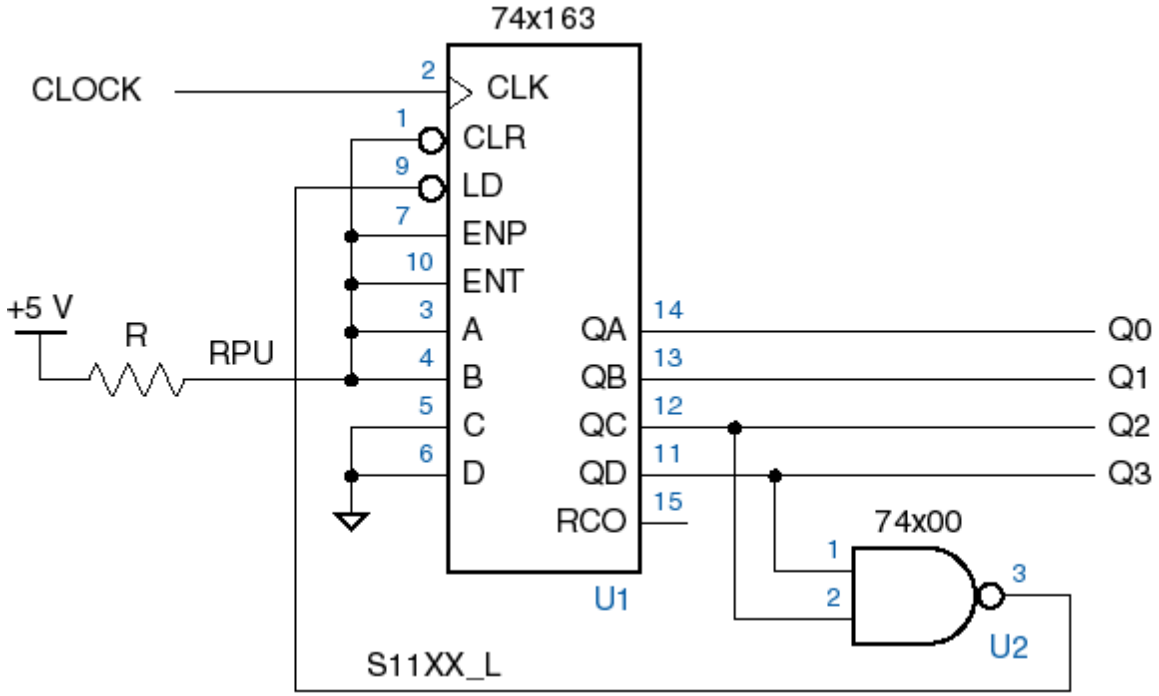
- Carga 0101 (5) após Count = 15
- 5, 6, 7, 8, 9, 10, 11, 12, 13, 14, 15, 5, 6, …
- Contador “divide-by-11”

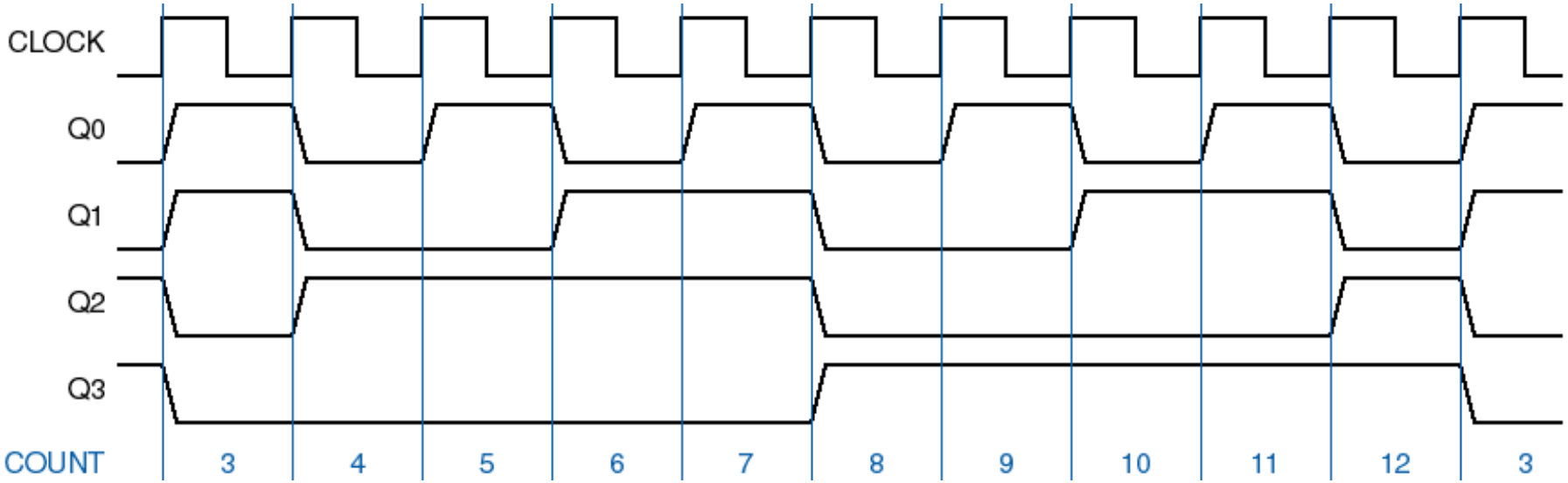
Outra solução



- Limpa após Count = 1010 (10)
- 0, 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 0, 1, 2, 3, …
- Contador “modulo-11” or “divide-by-11”

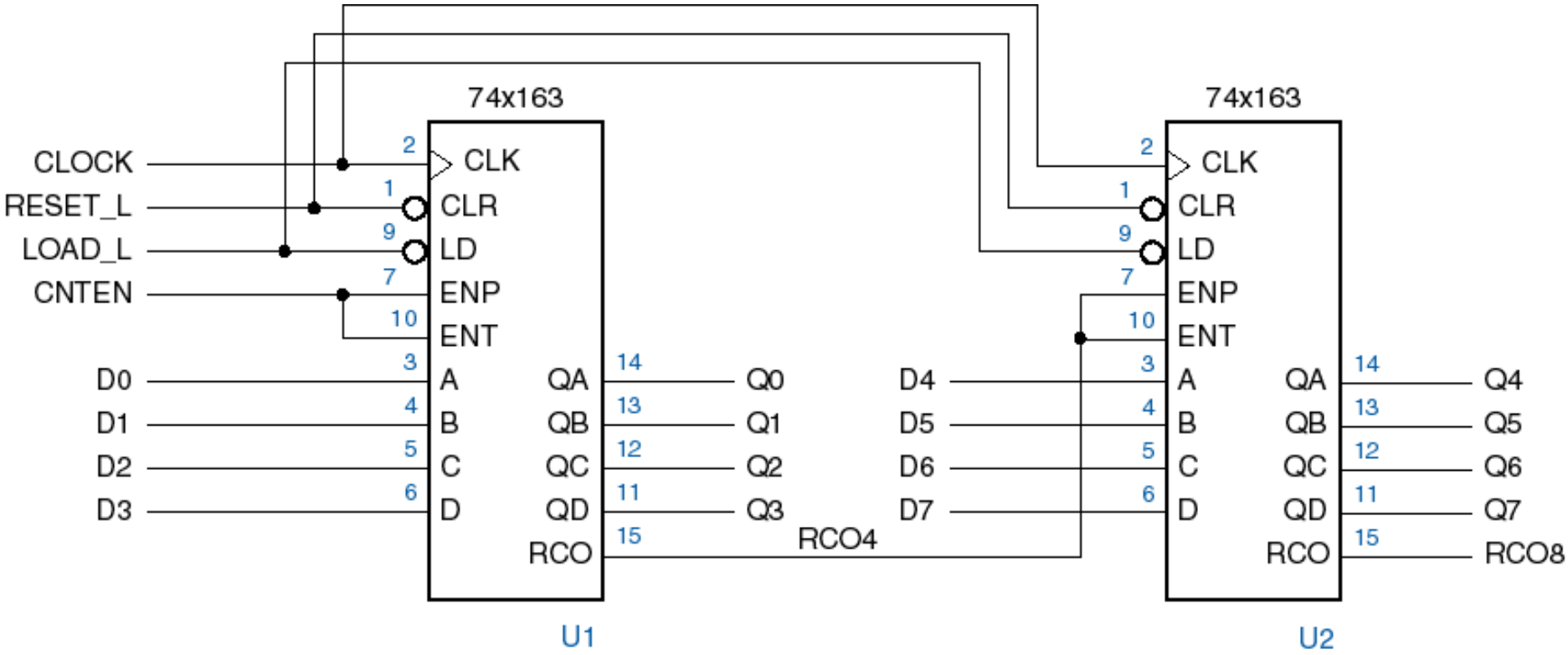
Contagem de 3 a 12



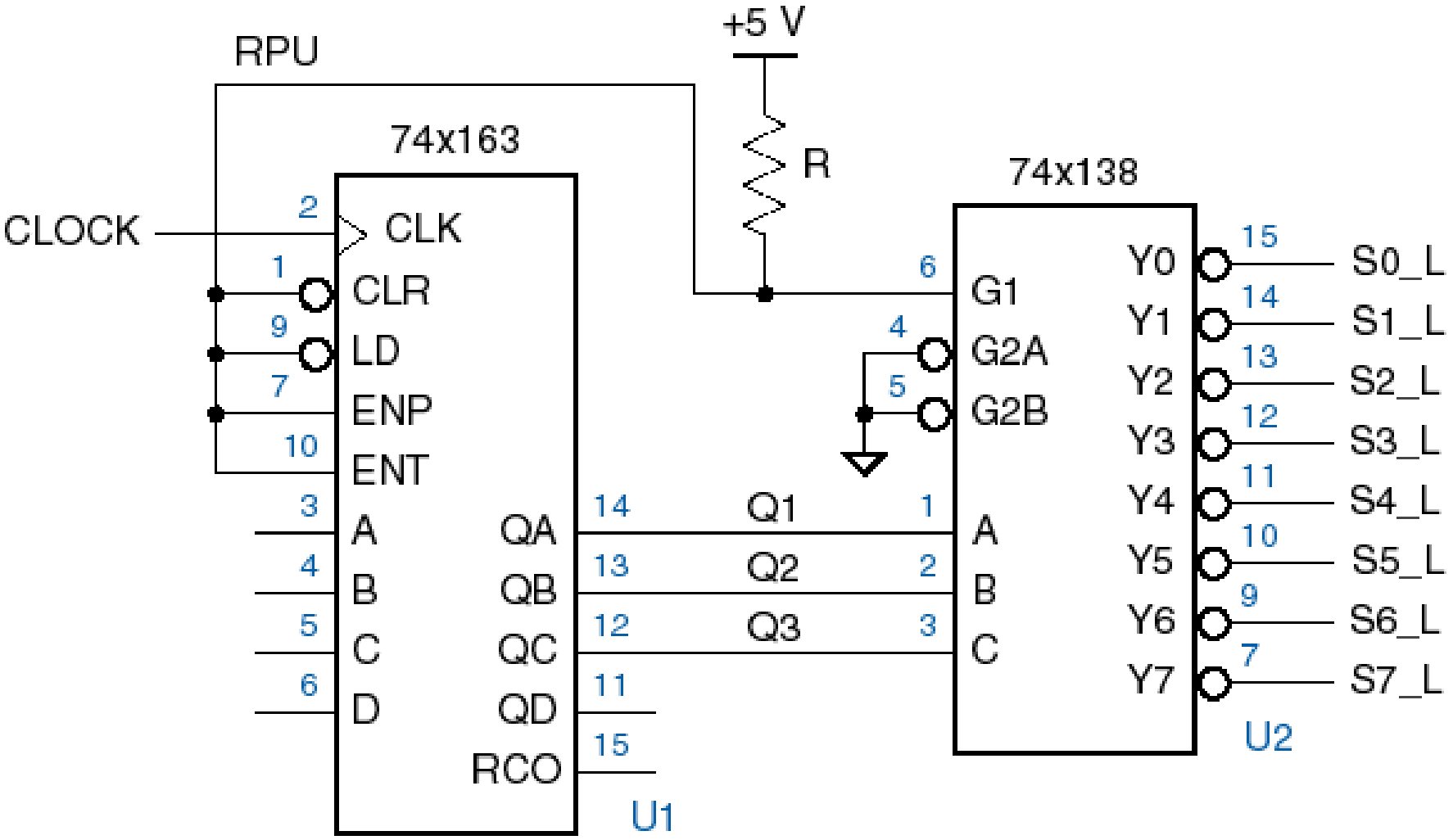


Cascata de Contadores

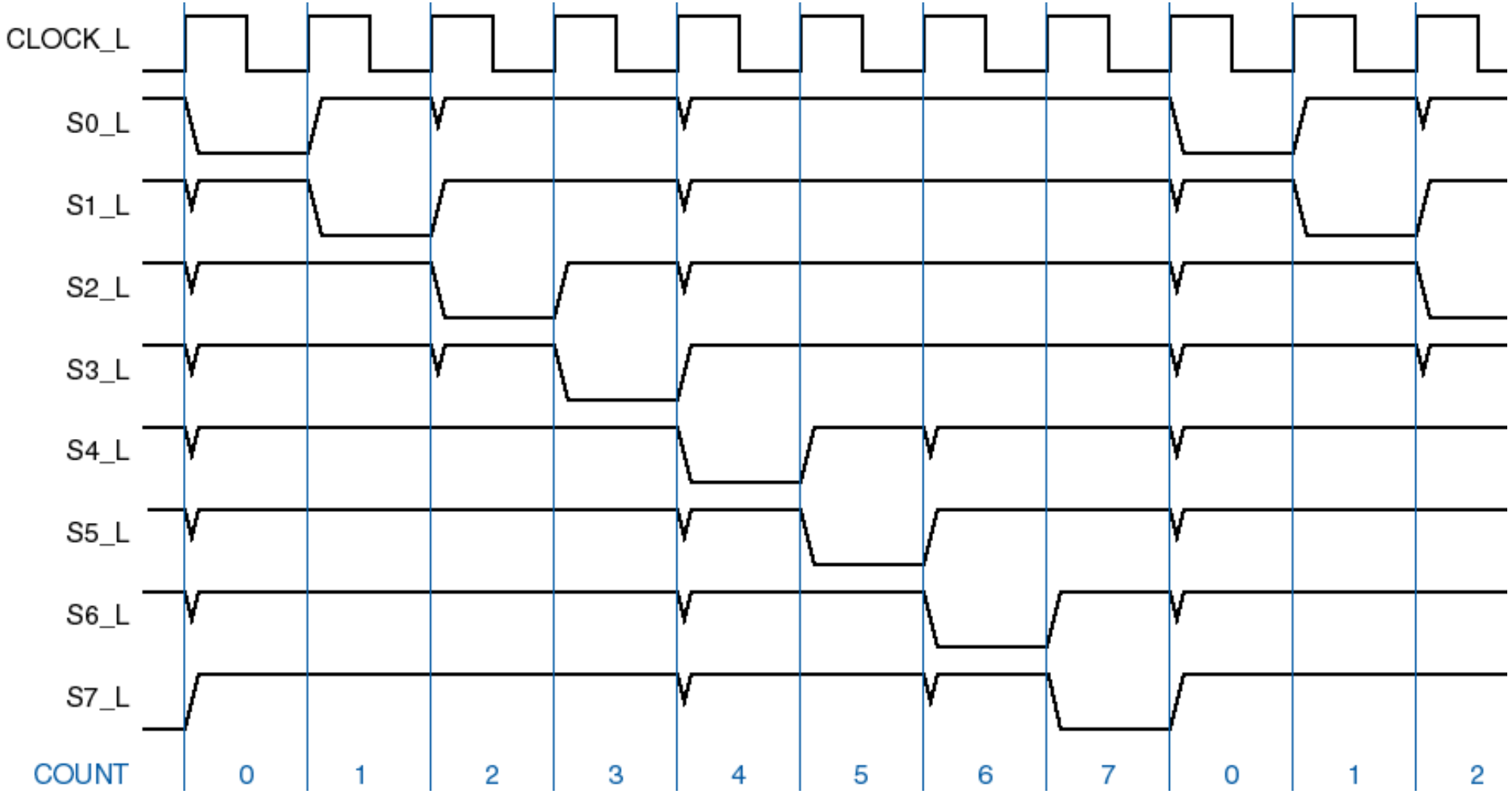
- RCO (“ripple carry out”) é activado no estado 15, se ENT está activo



Descodificação de estados

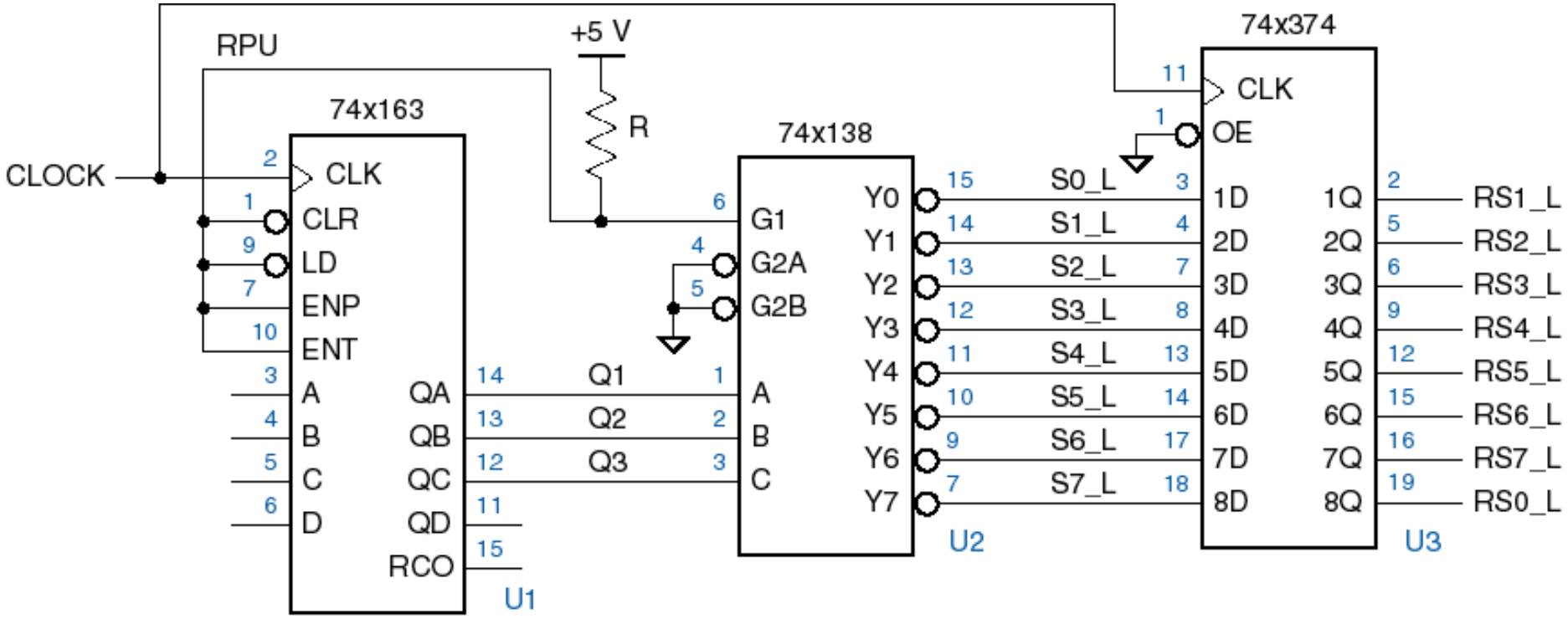


Formas de onda do Descodificador



- “Glitches” podem ser uma preocupação .

Saídas “Glitch-free”

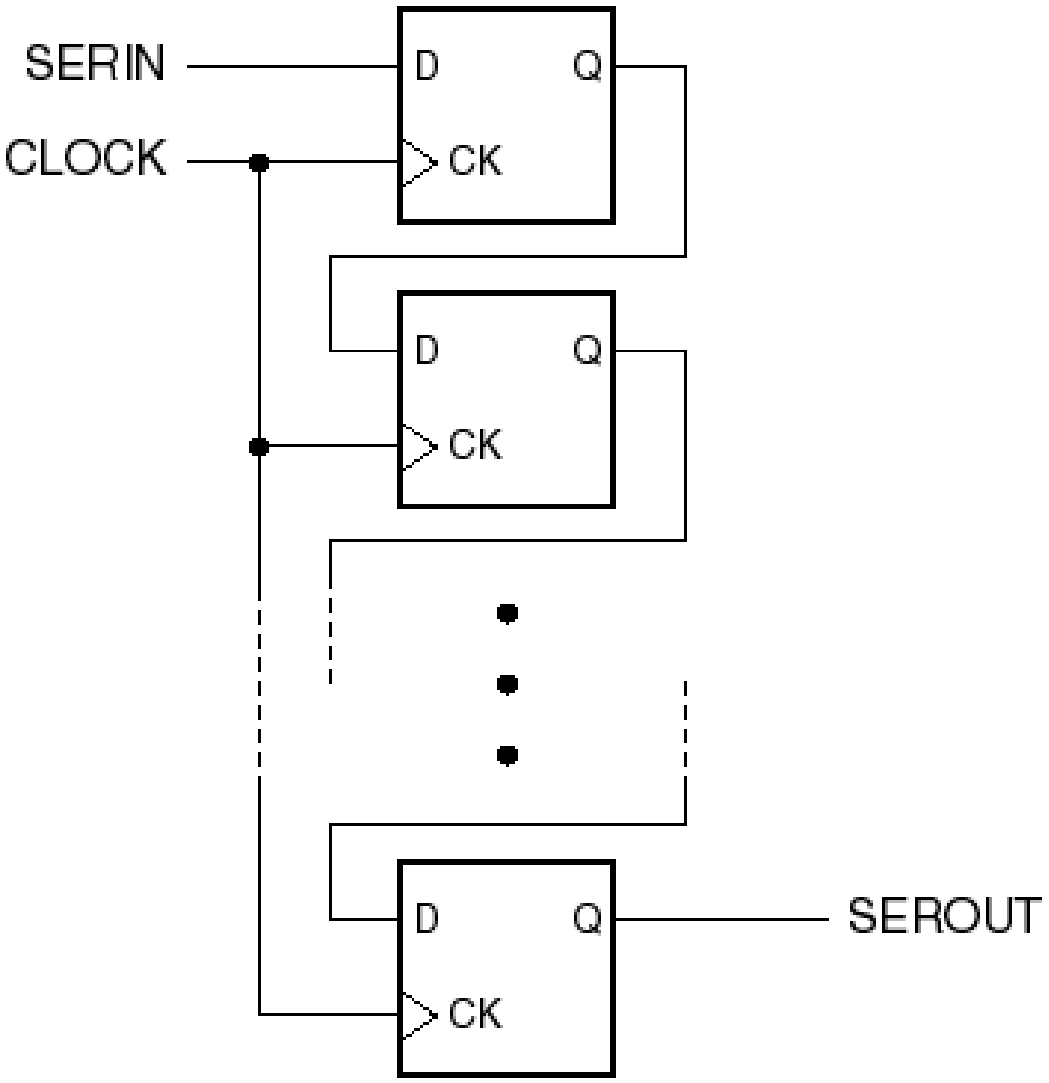


- Saídas dos registos atrasadas um pulso de clk.

Registos de deslocamento "Shift Registers"

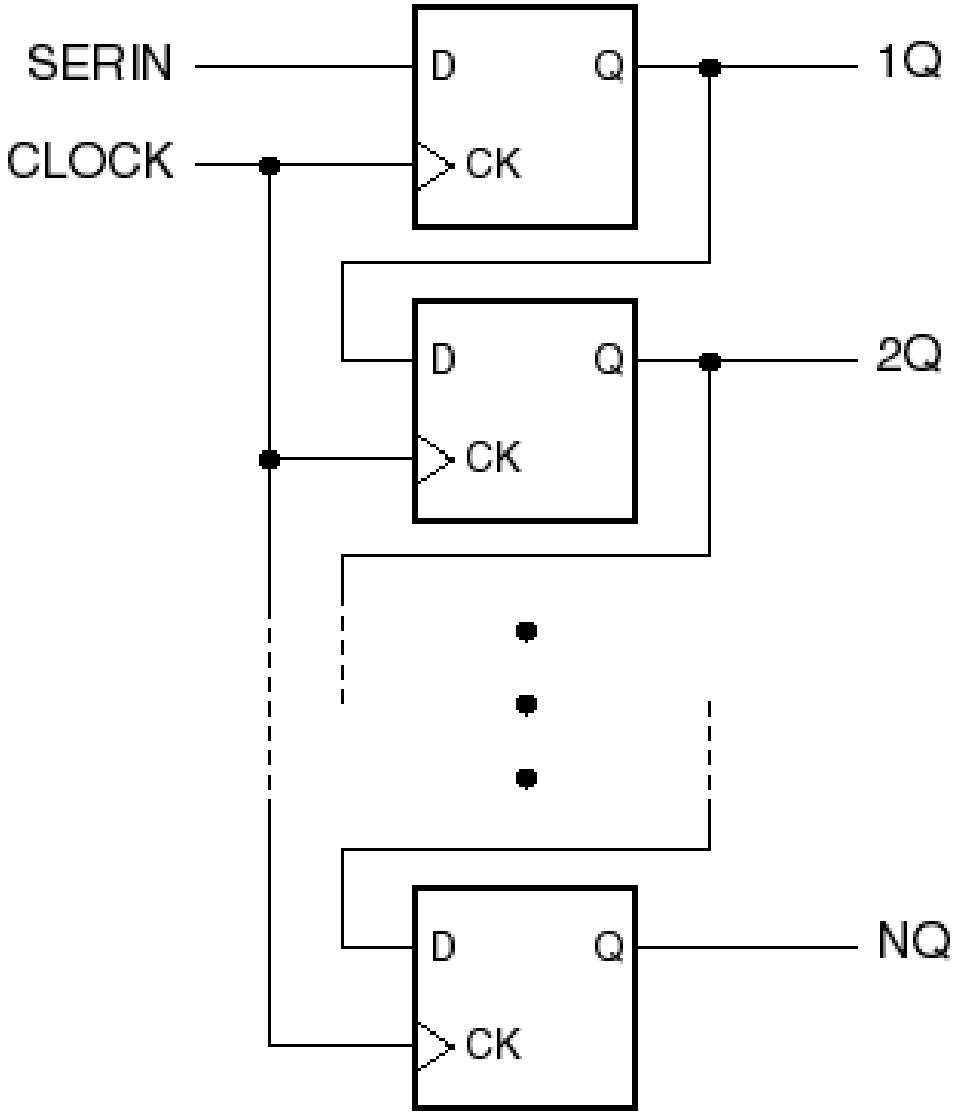
- Manipulação de bits em série, tal como: RS-232, transmissão e recepção via modem, Ethernet, USB, etc.

- Serial-in, Serial-out (SISO)



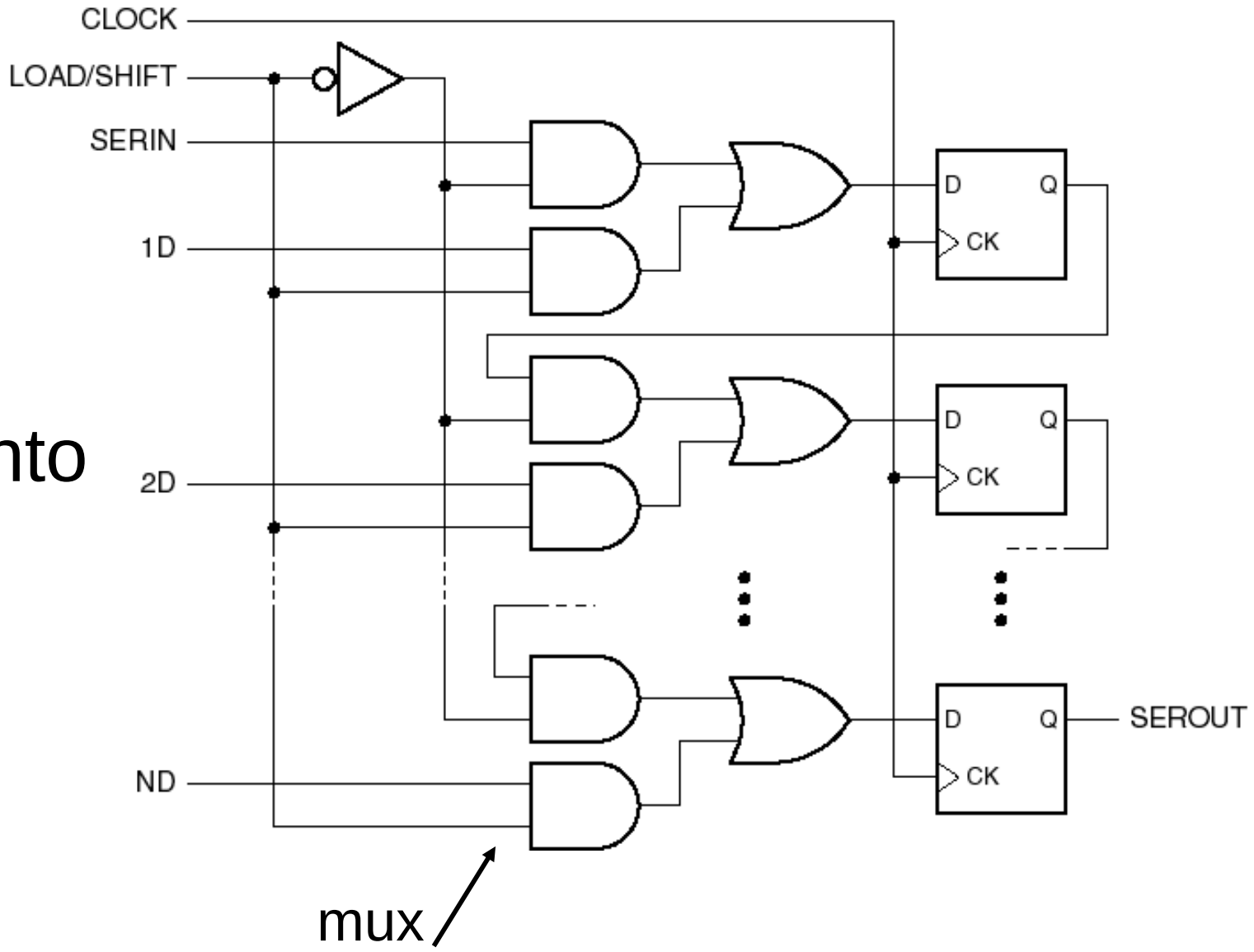
Conversão Série - Paralelo

- Usando um registo de deslocamento “serial-in, parallel-out” (SIPO)



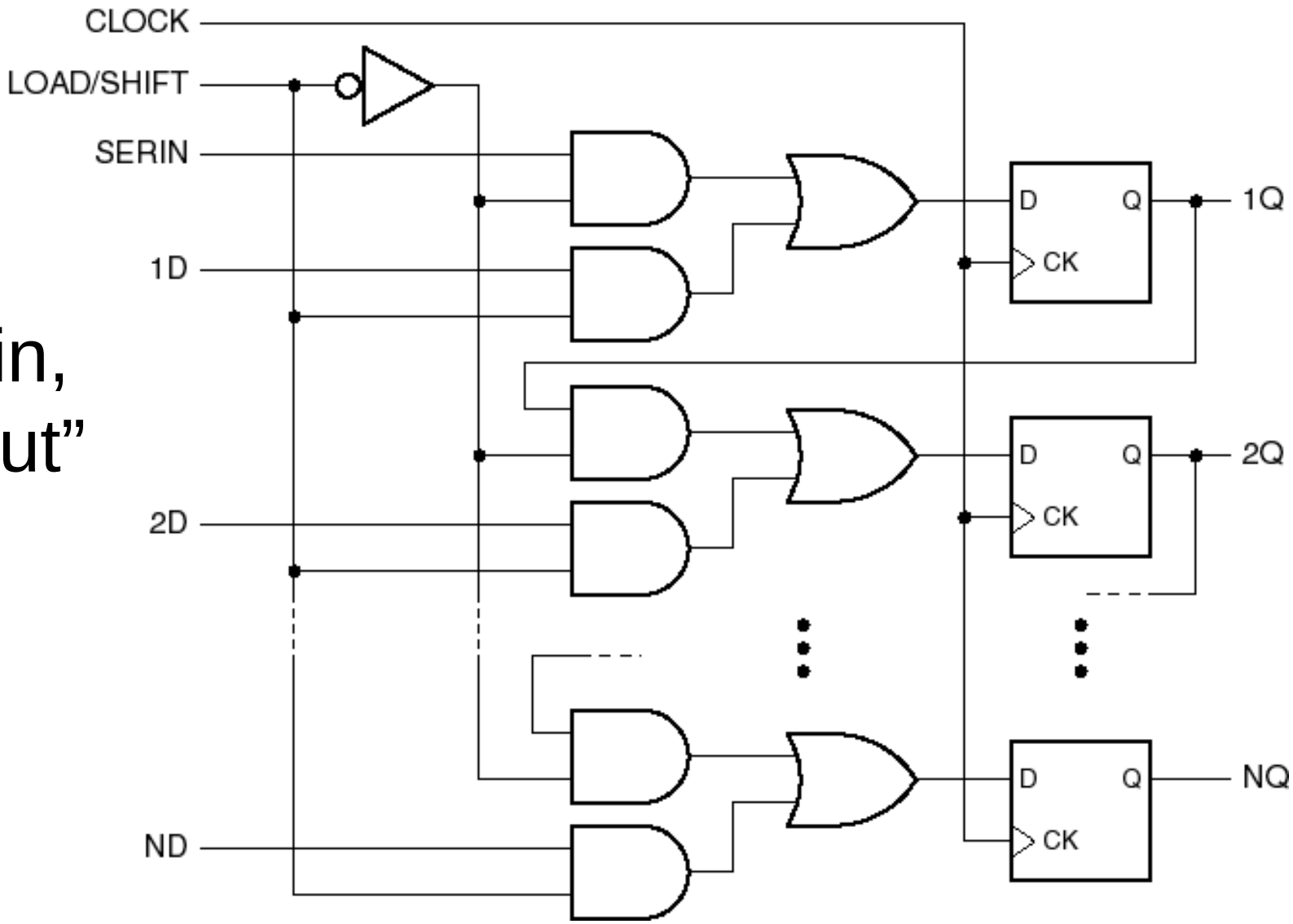
Conversão Paralelo - Série

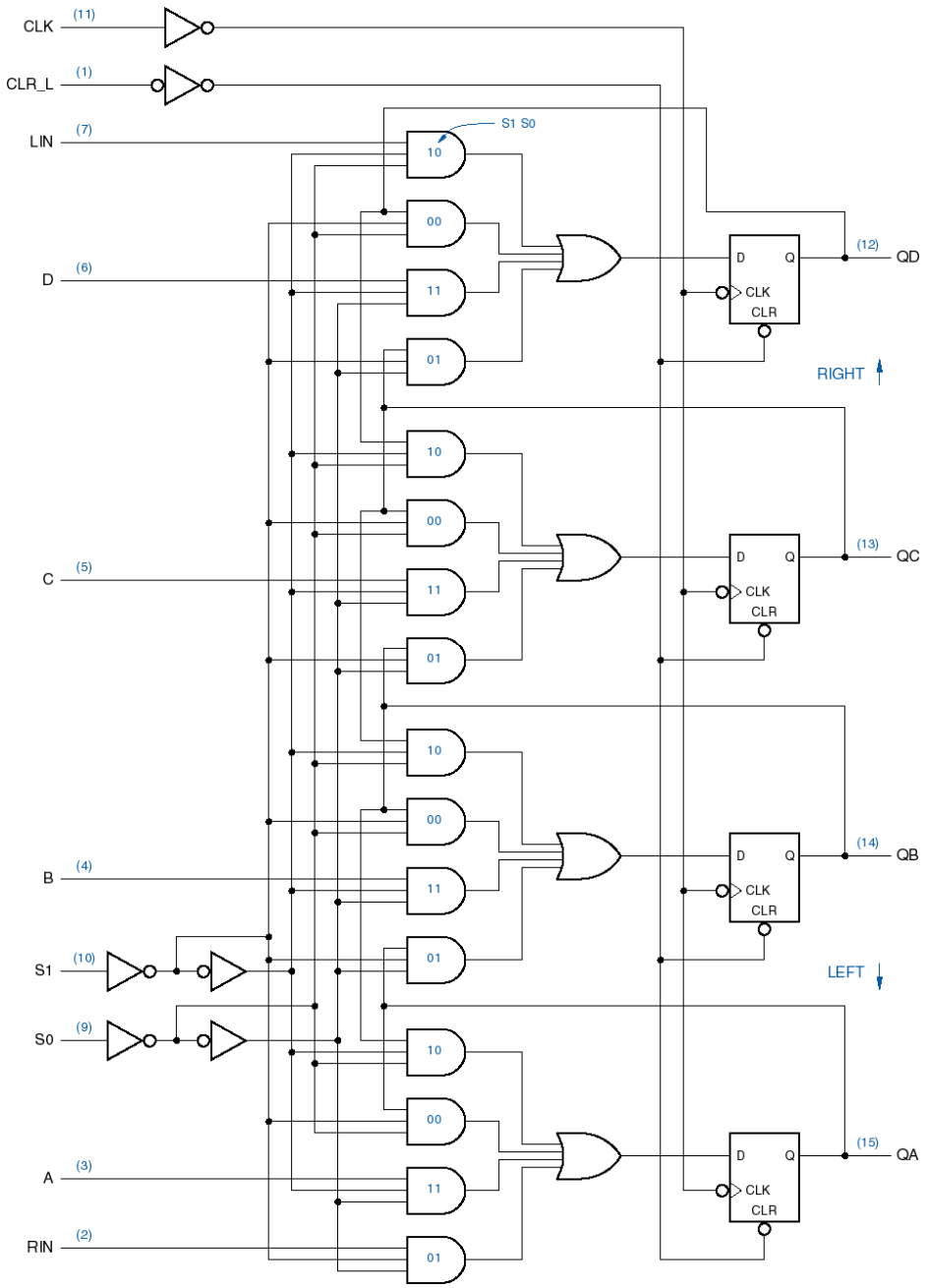
- Usando um registo de deslocamento “parallel-in, serial-out” (PISO)



Conversor Universal

- "Parallel-in, parallel-out" (PIPO)

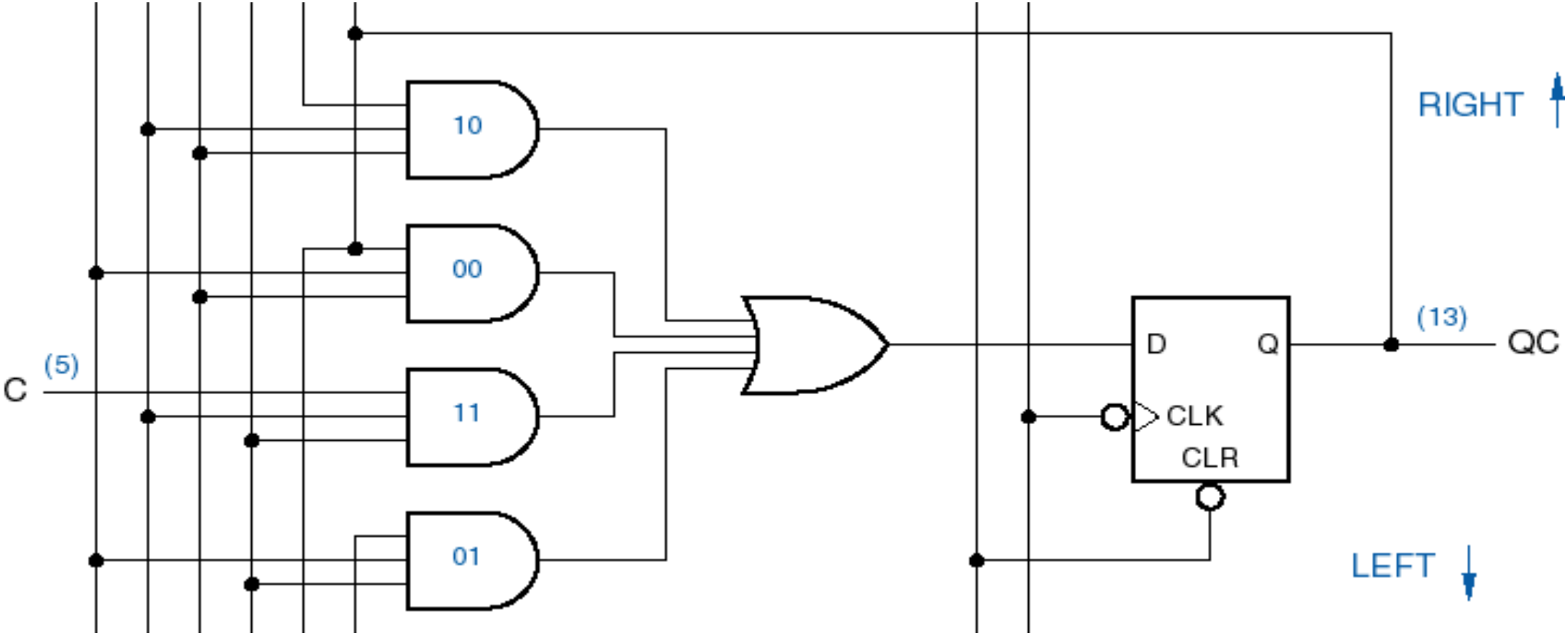


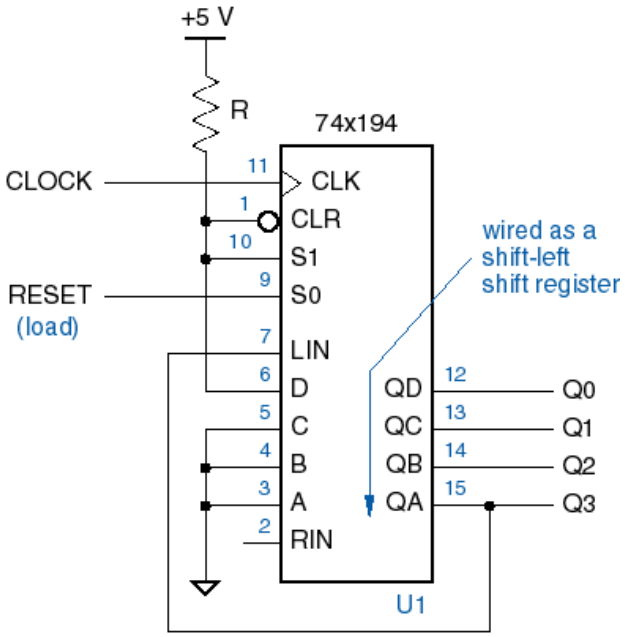


74x194 Universal Shift - Register

- “Shift left”
- “Shift right”
- “Load”
- “Hold”

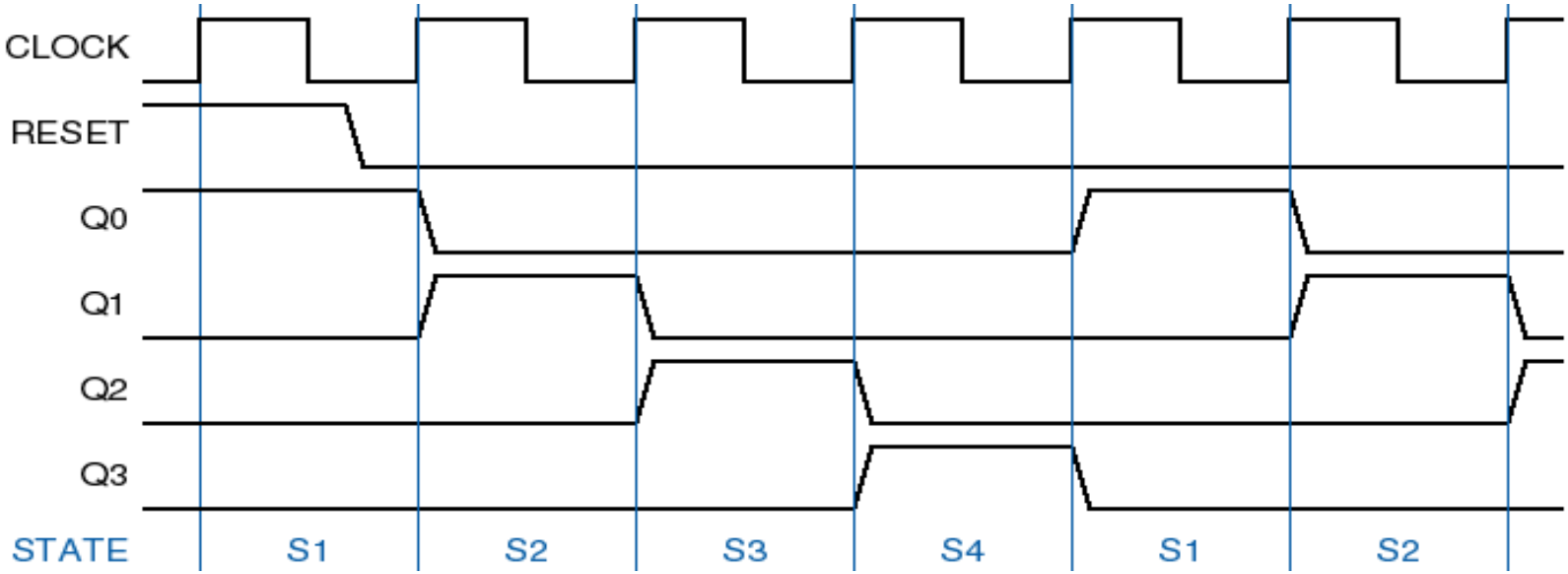
Um estágio do IC ’194

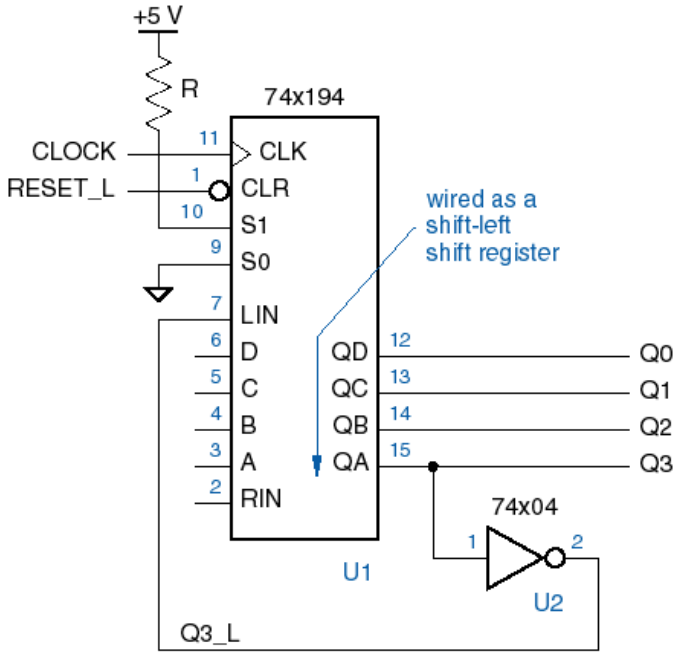




Contadores “Shift-register”

- Contador em Anel “Ring counter”





Contador “Johnson”

- Contador “Twisted ring”