Circuitos Sequenciais

- Saída não depende apenas das entradas actuais mas também do passado destas.

- "Estado" engloba toda a informação necessária acerca do passado para prever a saída actual tendo em conta as entradas actuais.
  - *Variáveis de Estado*, um ou mais bits de informação.

Descrição Circuitos Sequenciais

- Tabela de Estados
  - Para cada estado actual, especifica-se o próximo estado em função das entradas actuais.
  - Para cada estado actual, especificam-se saídas em função das entradas actuais

- Diagrama de Estados
  - Versão Gráfica da Tabela de Estados

Estrutura duma Máquina de Estados

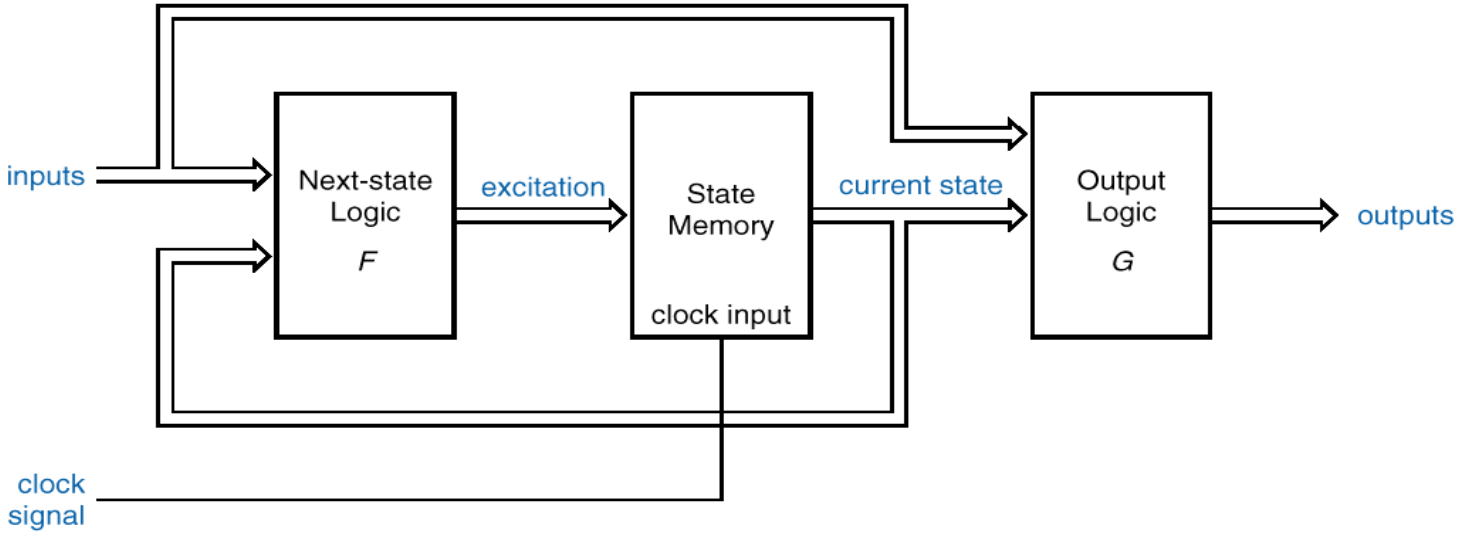


Figure 7–32 Clocked synchronous state-machine structure (Mealy machine).

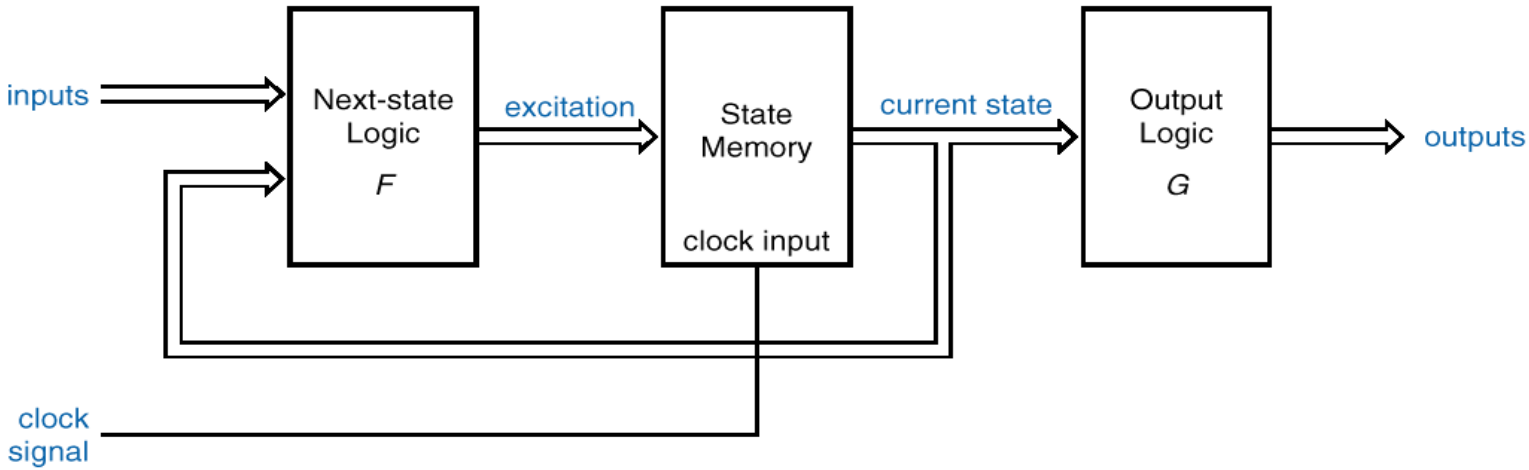
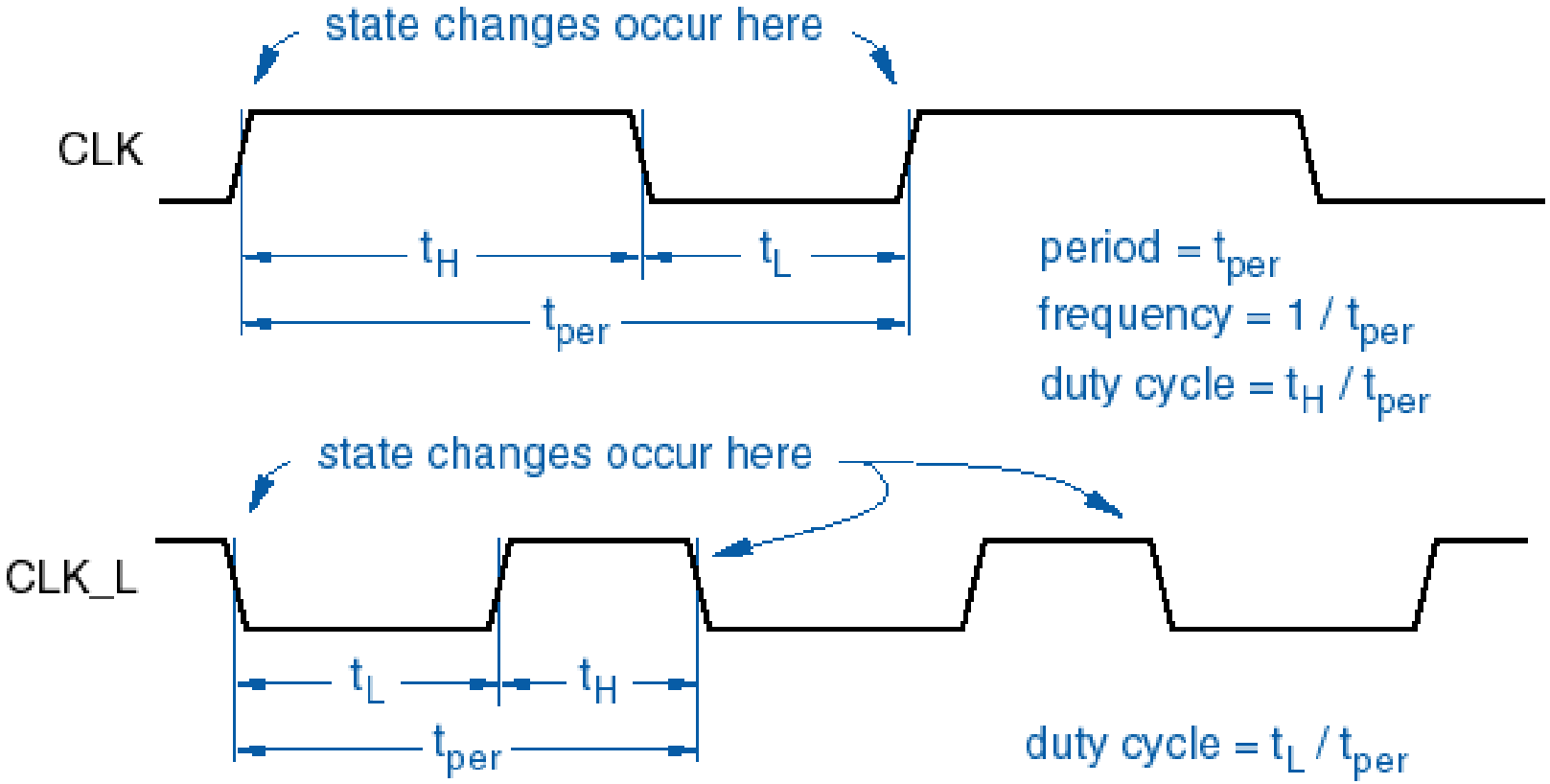


Figure 7–33 Clocked synchronous state-machine structure (Moore machine).

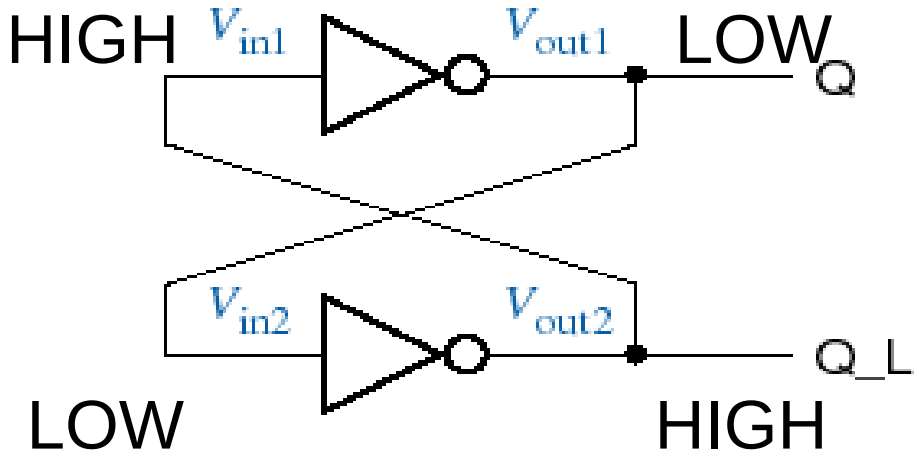
Sinais de Relógio

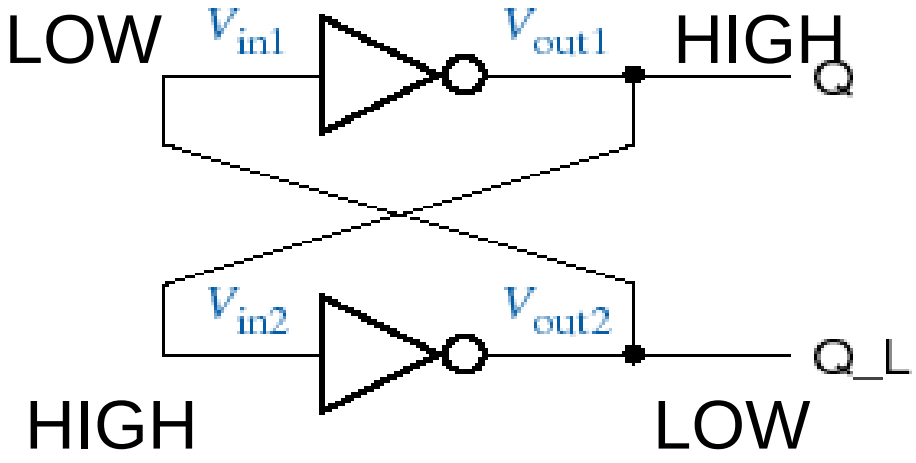
- Muito importante nos circuitos sequenciais
  - Variáveis de Estado mudam na transição do sinal de relógio (transição negativa e positiva).



Elemento Bi-estável

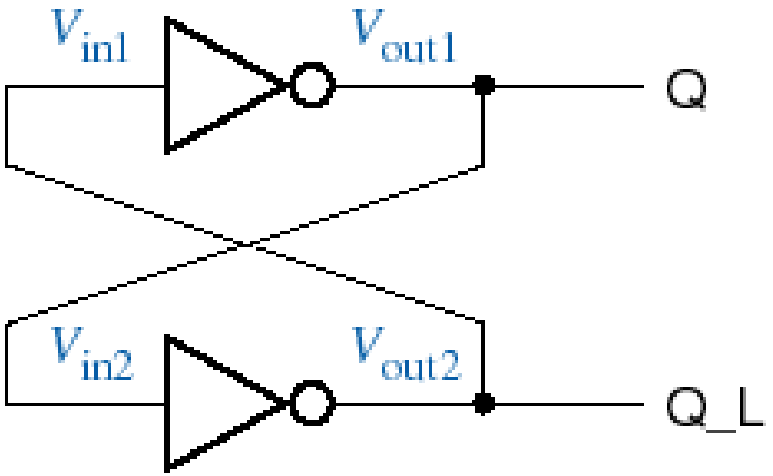
- Circuito sequencial mais simples
- Dois Estados
  - Uma variável de estado, por exemplo: Q



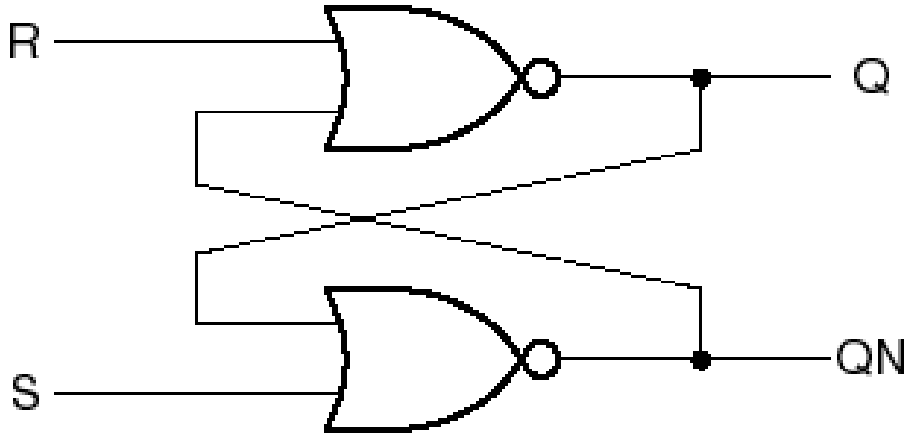


Elementos Bi-estáveis

- Como controlá-los?

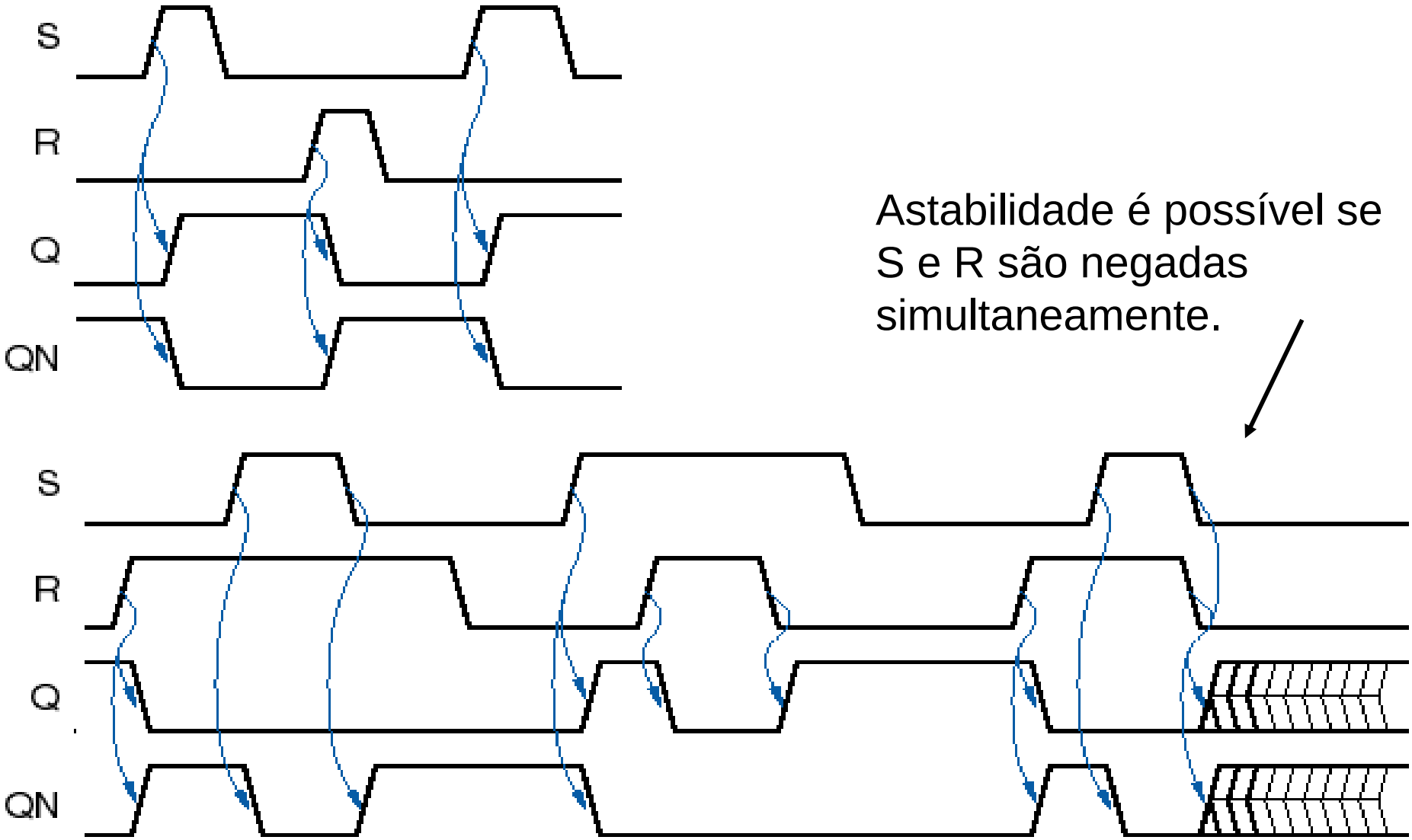


- Latch S-R



S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

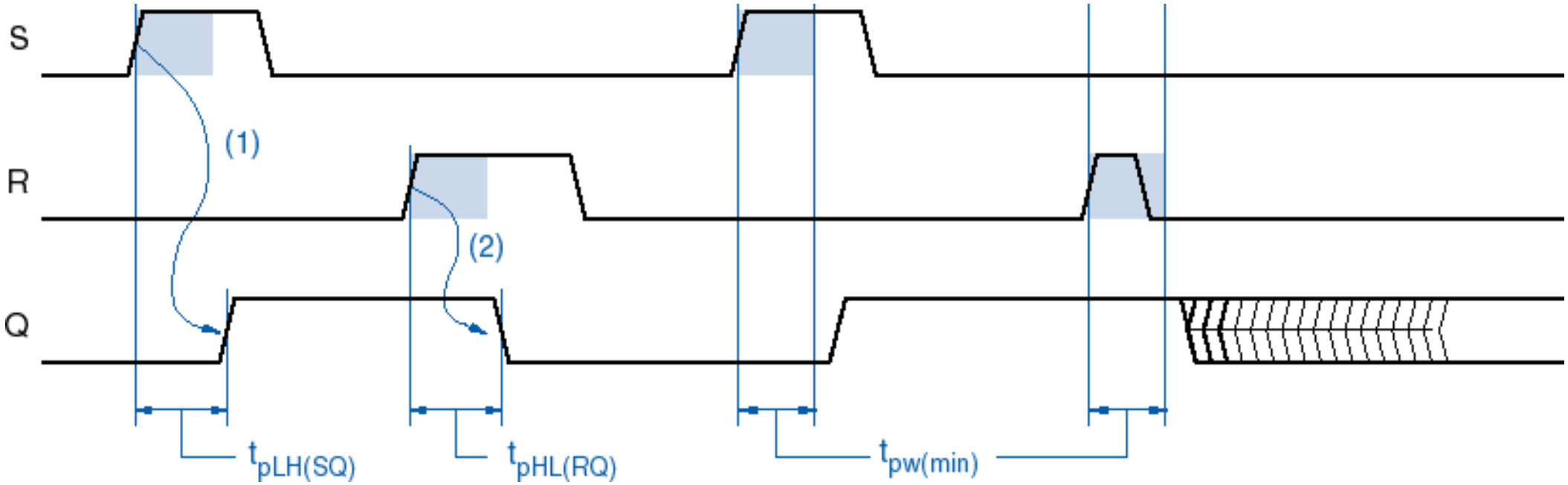
Funcionamento Latch S-R



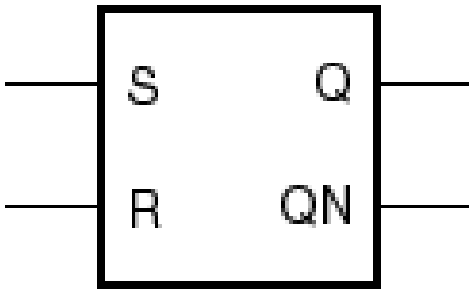
Astabilidade é possível se S e R são negadas simultaneamente.

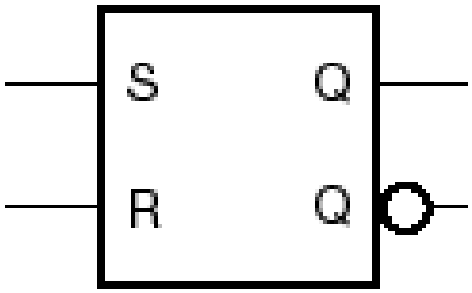
Param. Temporais Latch S-R

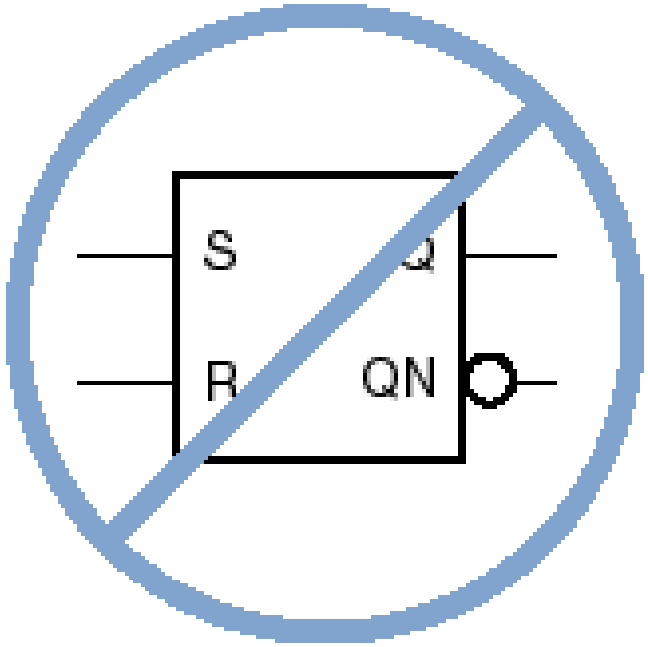
- Tempo de atraso de propagação.
- Largura mínima de pulso.



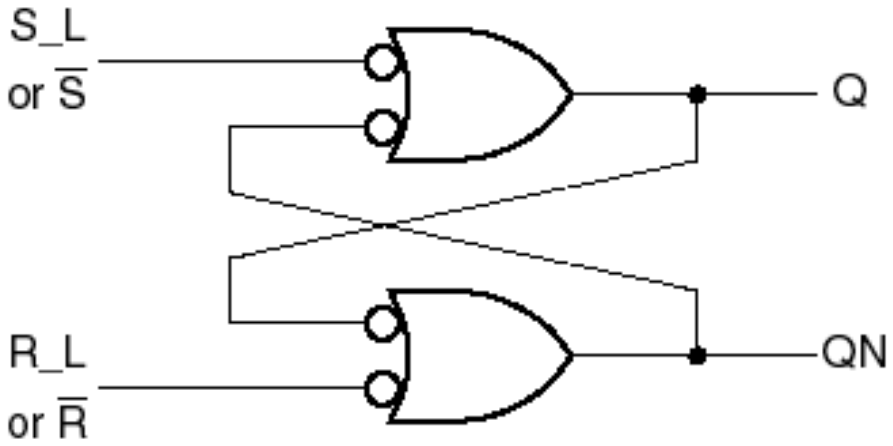
Símbolos da Latch S-R

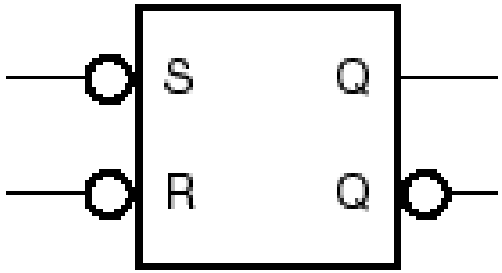






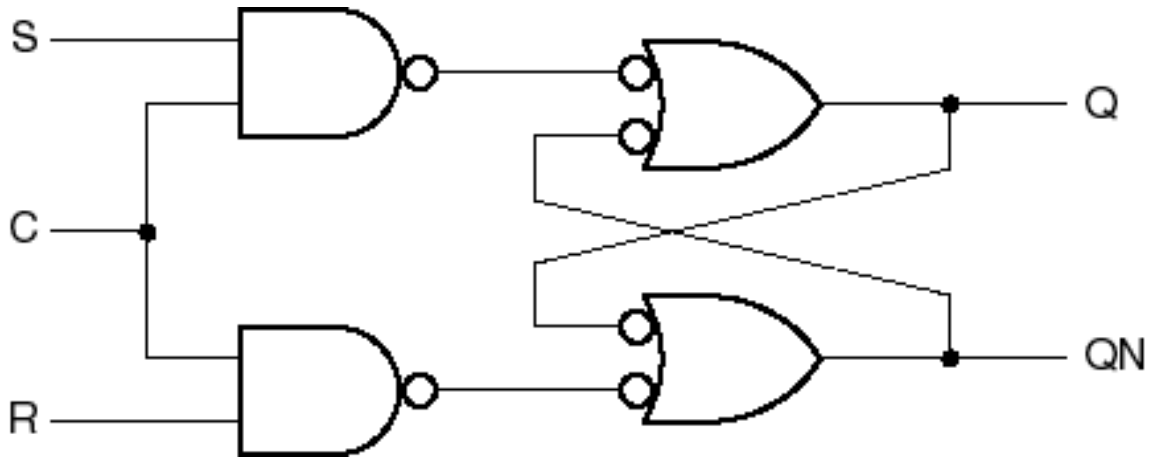
Latch S-R com NANDs





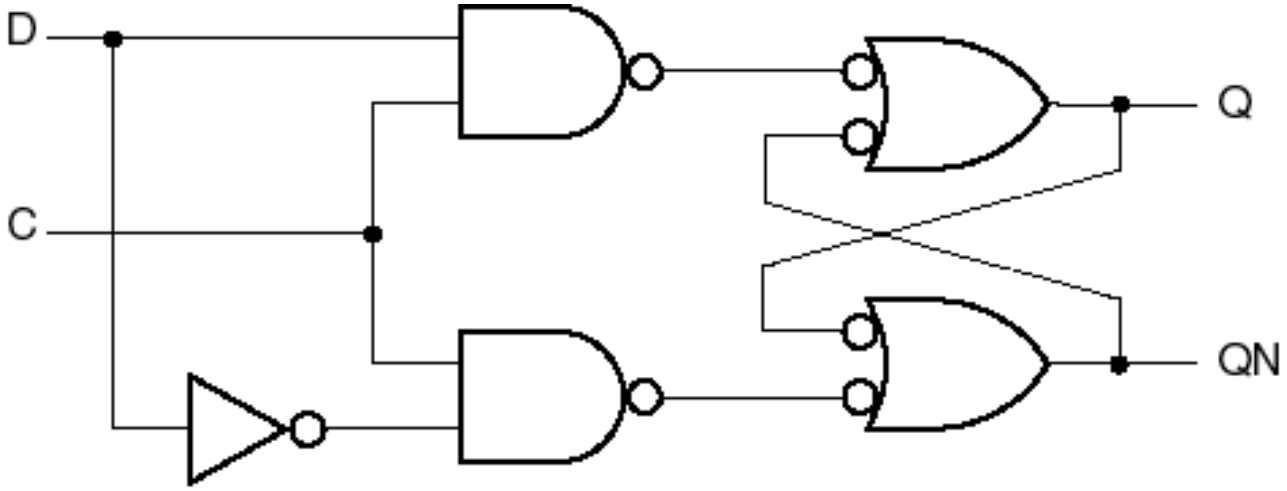
S_L	R_L	Q	QN
0	0	1	1
0	1	1	0
1	0	0	1
1	1	last Q	last QN

Latch S-R com “Enable”



S	R	C	Q	QN
0	0	1	last Q	last QN
0	1	1	0	1
1	0	1	1	0
1	1	1	1	1
x	x	0	last Q	last QN

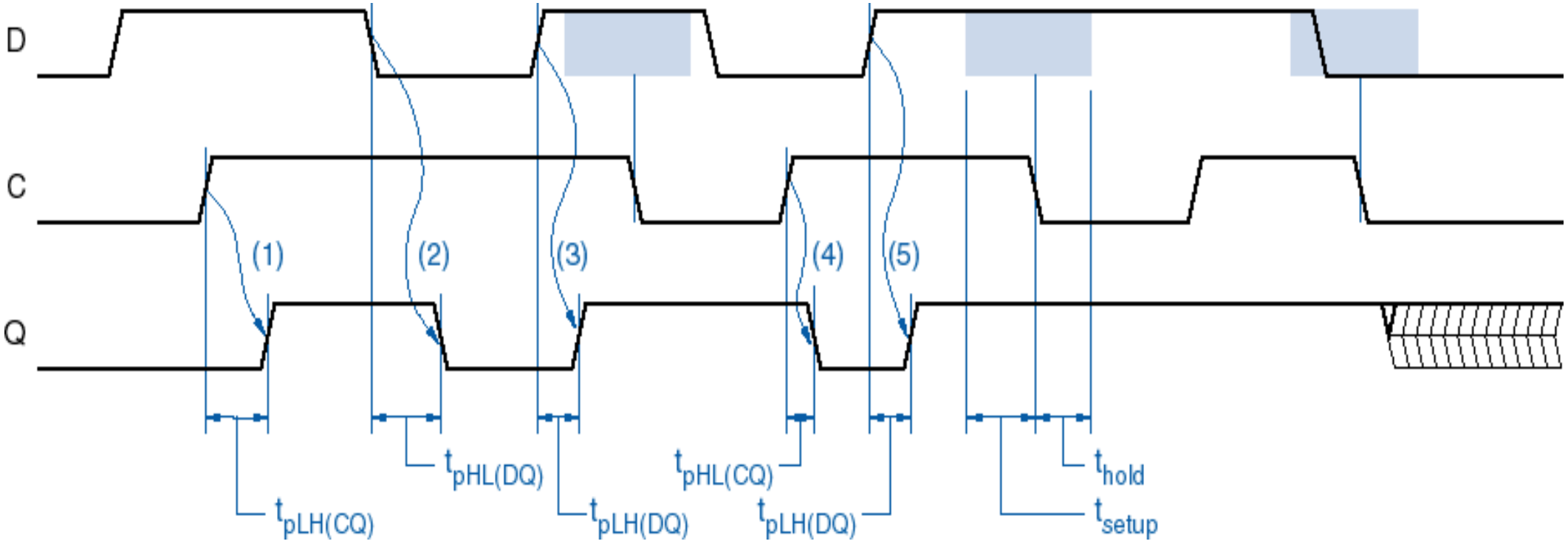
Latch tipo D



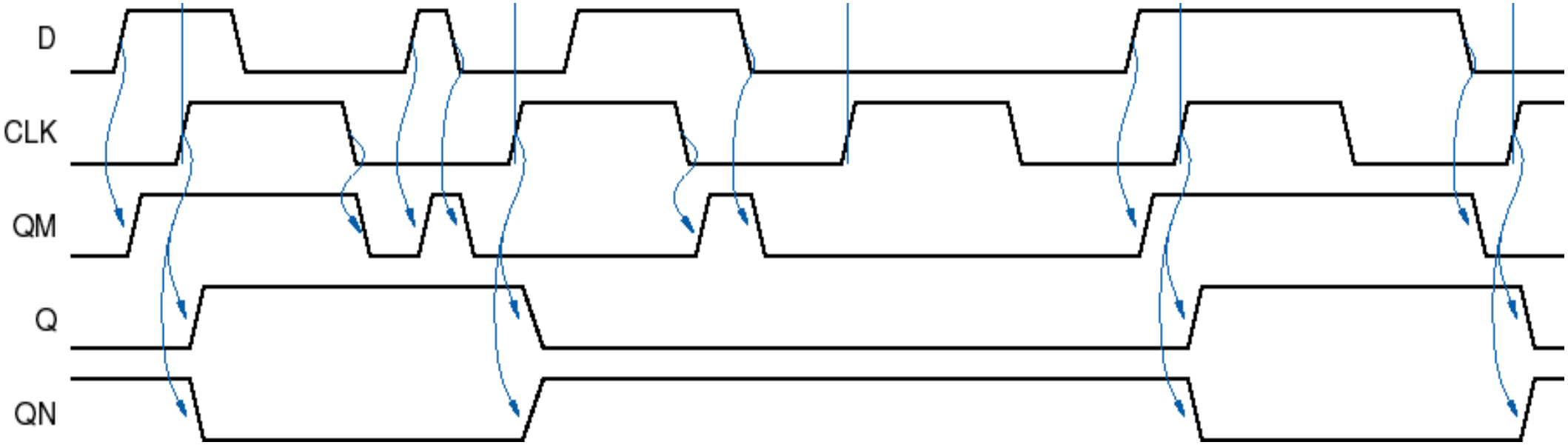
C	D	Q	QN
1	0	0	1
1	1	1	0
0	x	last Q	last QN

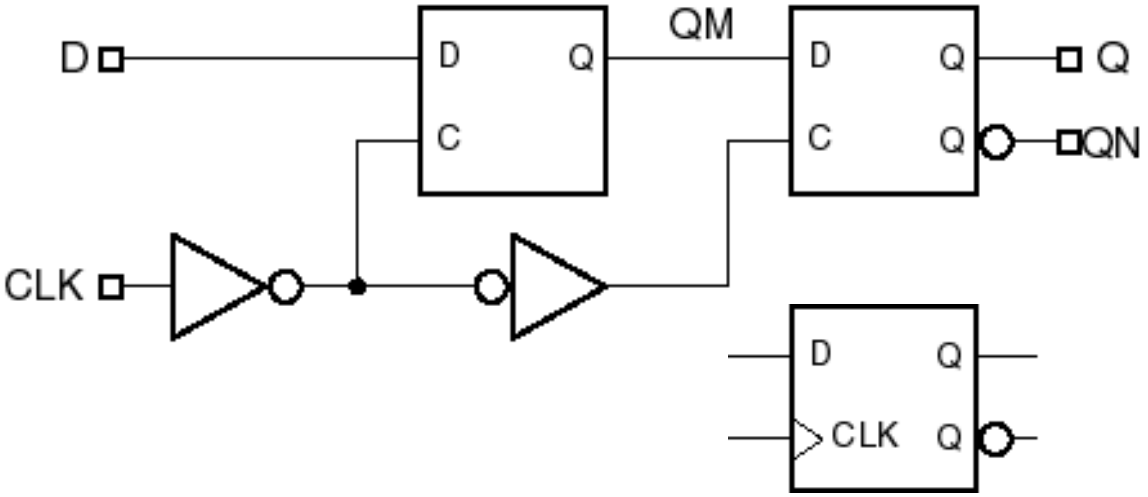
Param. Temporais Latch tipo D

- Atraso de Propagação (de C ou D)
- Tempo de “Setup” (D antes da transição de C)
- Tempo de “Hold” (D após transição de C)



“Edge-triggered” D flip-flop

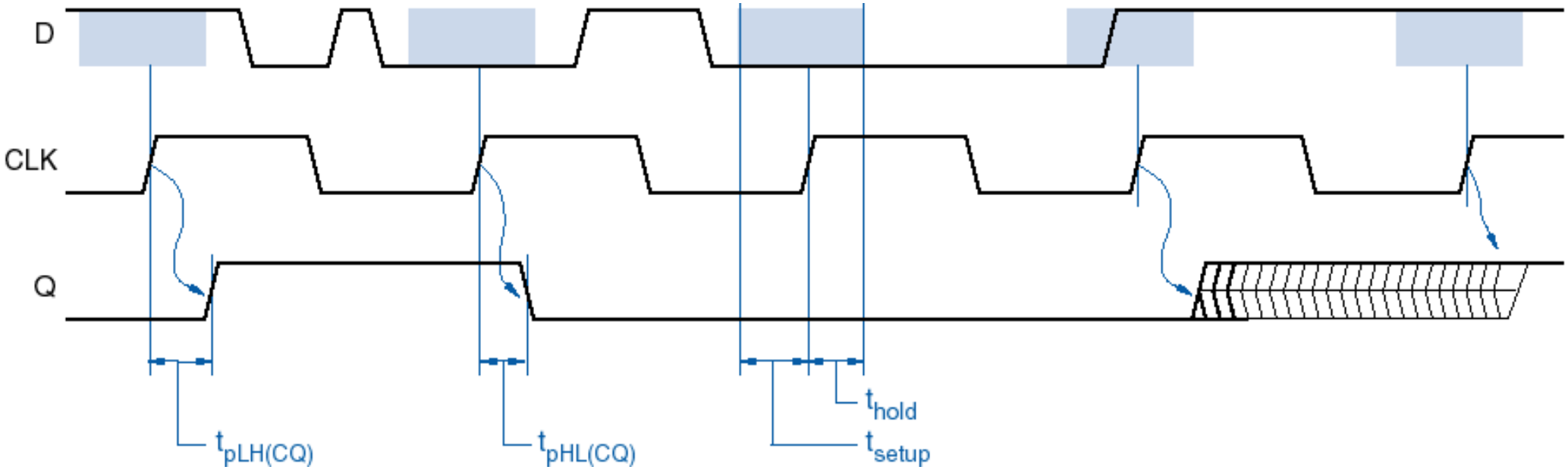




D	CLK	Q	QN
0	↑	0	1
1	↑	1	0
x	0	last Q	last QN
x	1	last Q	last QN

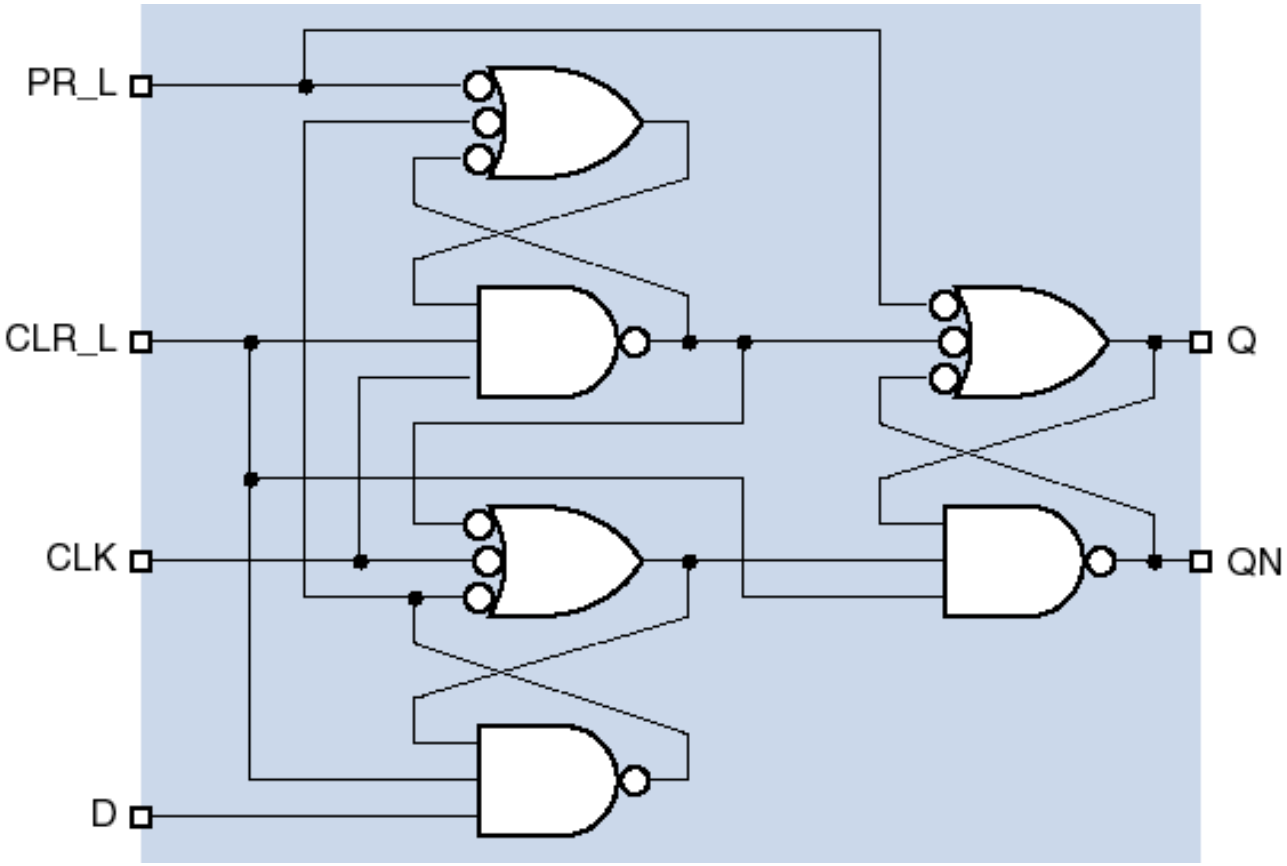
Param. Temp. “Edge-triggered” D flip-flop

- Atraso de Propagação (desde CLK)
- Tempo de “Setup” (D antes da transição de CLK)
- Tempo de “Hold” (D após transição de CLK)

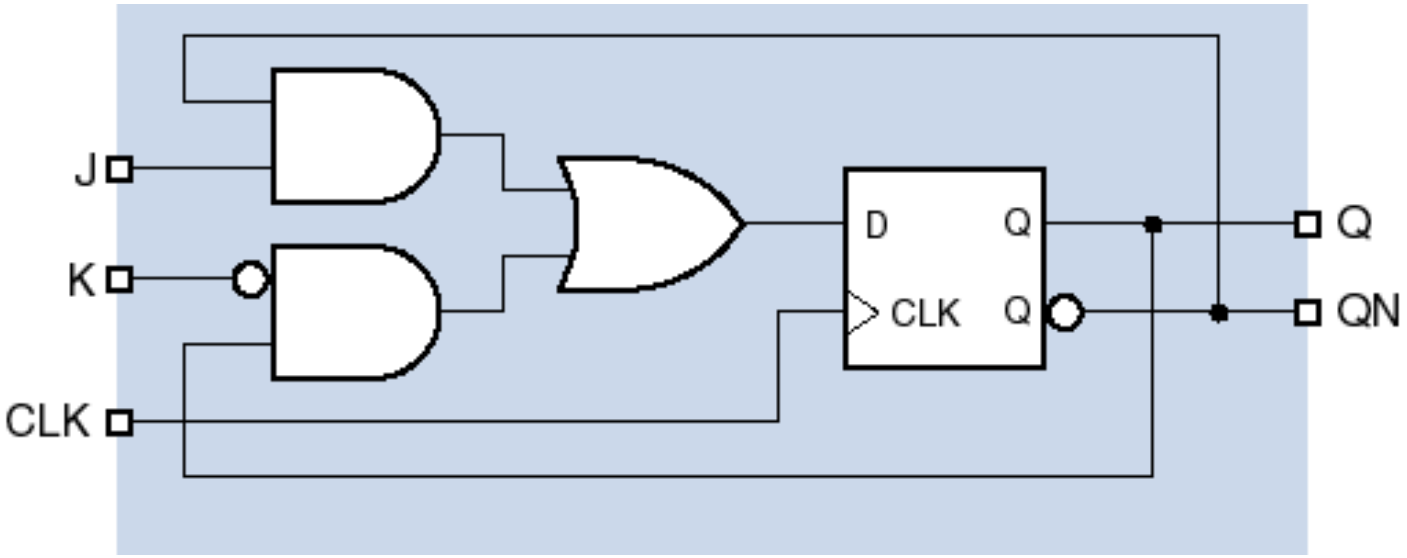


TTL edge-triggered D flip-flop

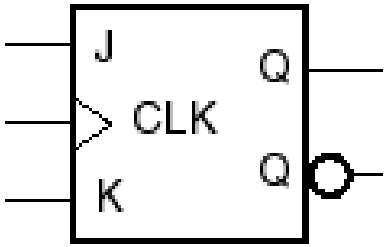
- Entradas de “Preset” e “clear”
  - como latch S-R
- 3 anéis de “feedback”
- Carga em D e CLK muito leve



Flip-flops J-K

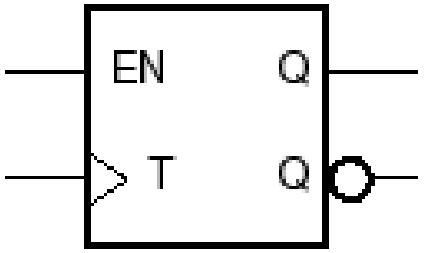


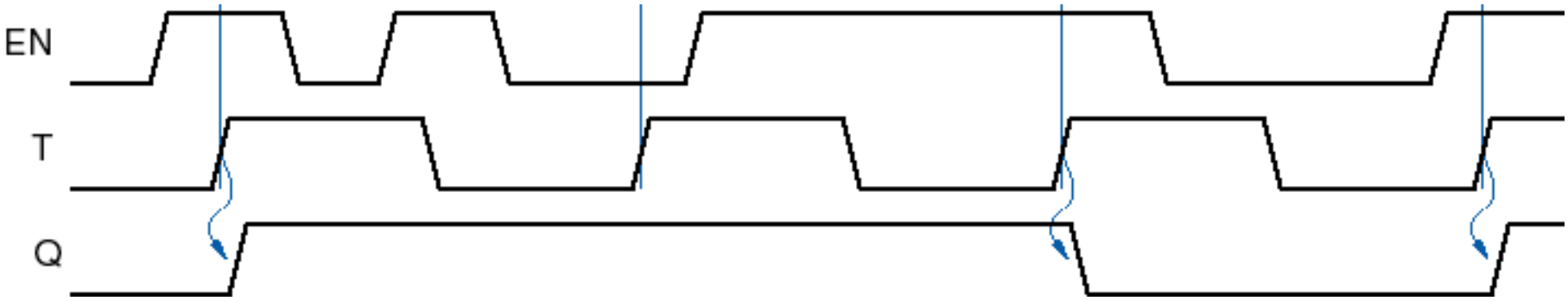
J	K	CLK	Q	QN
x	x	0	last Q	last QN
x	x	1	last Q	last QN
0	0	↓	last Q	last QN
0	1	↓	0	1
1	0	↓	1	0
1	1	↓	last QN	last Q

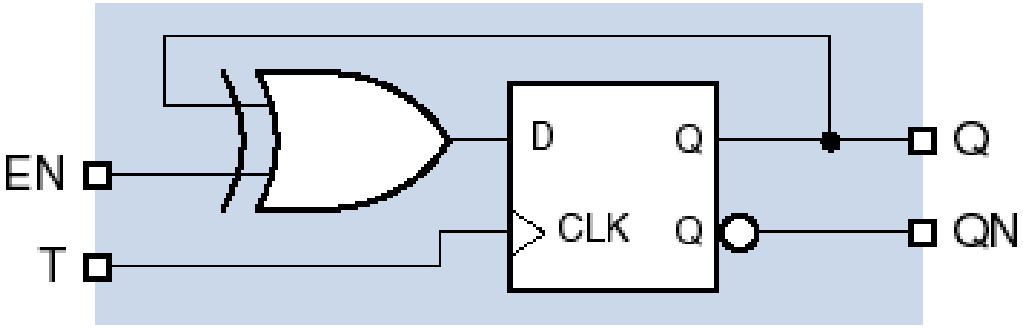


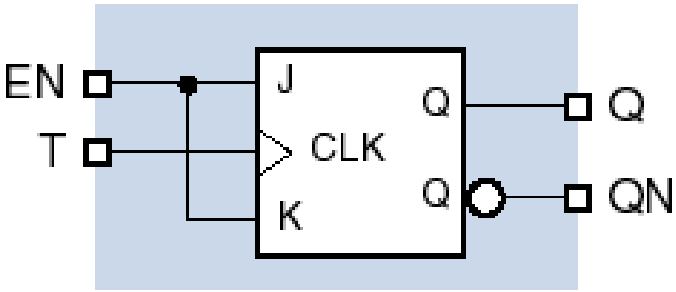
Tlip-flops T (Toggle)

- Importantes para implementação de contadores









Circuitos Sequenciais

Table 7–1
Latch and flip-flop characteristic equations.

Device Type	Characteristic Equation
S-R latch	$Q^* = S + R' \cdot Q$
D latch	$Q^* = D$
Edge-triggered D flip-flop	$Q^* = D$
Master/slave S-R flip-flop	$Q^* = S + R' \cdot Q$
Master/slave J-K flip-flop	$Q^* = J \cdot Q' + K' \cdot Q$
Edge-triggered J-K flip-flop	$Q^* = J \cdot Q' + K' \cdot Q$
T flip-flop	$Q^* = Q'$
T flip-flop with enable	$Q^* = EN \cdot Q' + EN' \cdot Q$