# DAYANANDA SAGAR COLLEGE OF ENGINEERING

(An Autonomous Institute affiliated to Visvesvaraya Technological University (VTU), Belagavi,
Approved by AICTE and UGC, Accredited by NAAC with 'A' grade & ISO 9001 – 2015 Certified Institution)
Shavige Malleshwara Hills, Kumaraswamy Layout, Bengaluru-560 111, India

## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING


**Alternate Assessment Tool (AAT) Report submitted for the subject**

***VLSI Design – 22EC51***

Submitted by


**Nagaraj Hunashal (1DS22EC139)**
**Prajwal D Nadig (1DS2EC155)**
**Ram Prasad H (1DS22EC170)**

Under the Guidance of
Dr. Dinesha P
Professor, ECE


# ***Design of Static Random-Access Memory (SRAM) using Cadence Virtuoso***

| USN | Name | | Simulation & Analysis 05 Marks | Presentation &Report 05 Marks |
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**VISVESVARAYA TECHNOLOGICAL UNIVERSITY**
**JNANASANGAMA, BELAGAVI-590018, KARNATAKA, INDIA**
**2024-25**

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# CERTIFICATE

This is to certify that Alternate Assessment Tool (AAT) entitled **"Design of Static Random-Access Memory (SRAM) using Cadence Virtuoso"** as part of **VLSI Design – 22EC51** is a bonafide work carried out by Nagaraj Hunashal (1DS22EC139), Prajwal D Nadig (1DS22EC155), Ram Prasad H (1DS22EC170) as 10-marks component in partial fulfillment for the 5$^{th}$ semester of Bachelor of Engineering in Electronics and Communication Engineering of the Visvesvaraya Technological University, Belagavi during the year 2024-2025. The AAT report has been approved as it satisfies the academic requirements prescribed for the Bachelor of Engineering degree.

**Signature of Faculty**
**Dr. Dinesha P**

**Signature of HOD**
**Dr. Shobha K R**

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## DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

# DECLARATION

We declare that we abide by the ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice. The work submitted in this report of **VLSI Design – 22EC51**, V Semester BE, ECE has been compiled by referring to the relevant online and offline resources to the best of our understanding and in partial fulfillment of the requirement for the award of the degree of Bachelor of Engineering in Electronics and Communication Engineering, at Dayananda Sagar College of Engineering, an autonomous institution affiliated to VTU, Belagavi during the academic year 2024-2025.

We hereby declare that the same has not been submitted in part or full for other academic purposes.

(1DS22EC139 Nagaraj Hunashal)

(1DS22EC155 Prajwal D Nadig)

(1DS22EC170 Ram Prasad H)

**Place:**

**Date:**

# ABSTRACT

This report presents the design, analysis, and simulation of a Static Random-Access Memory (SRAM) cell using the Cadence Virtuoso software. SRAM is an integral part of digital systems, offering high-speed read and write capabilities. The project aimed to design a 6-transistor (6T) SRAM cell, implement its schematic and verify its performance under different conditions. The simulation results demonstrated efficient read and write operations, low power dissipation, and stable data retention. The designed SRAM cell met industry-standard parameters, showcasing its robustness and applicability in modern electronic systems.

## Introduction

Static Random-Access Memory (SRAM) is widely used in cache memories and registers due to its speed and reliability. Unlike DRAM, SRAM does not require periodic refresh cycles, as it relies on a bistable latch to store data.

## Objective

The objective of this project was to design an efficient 6T SRAM cell using Cadence Virtuoso, focusing on:

- Stability and robustness in data storage.
- Reduced power consumption.
- High-speed read and write operations.

## Methodology

The project followed these steps:

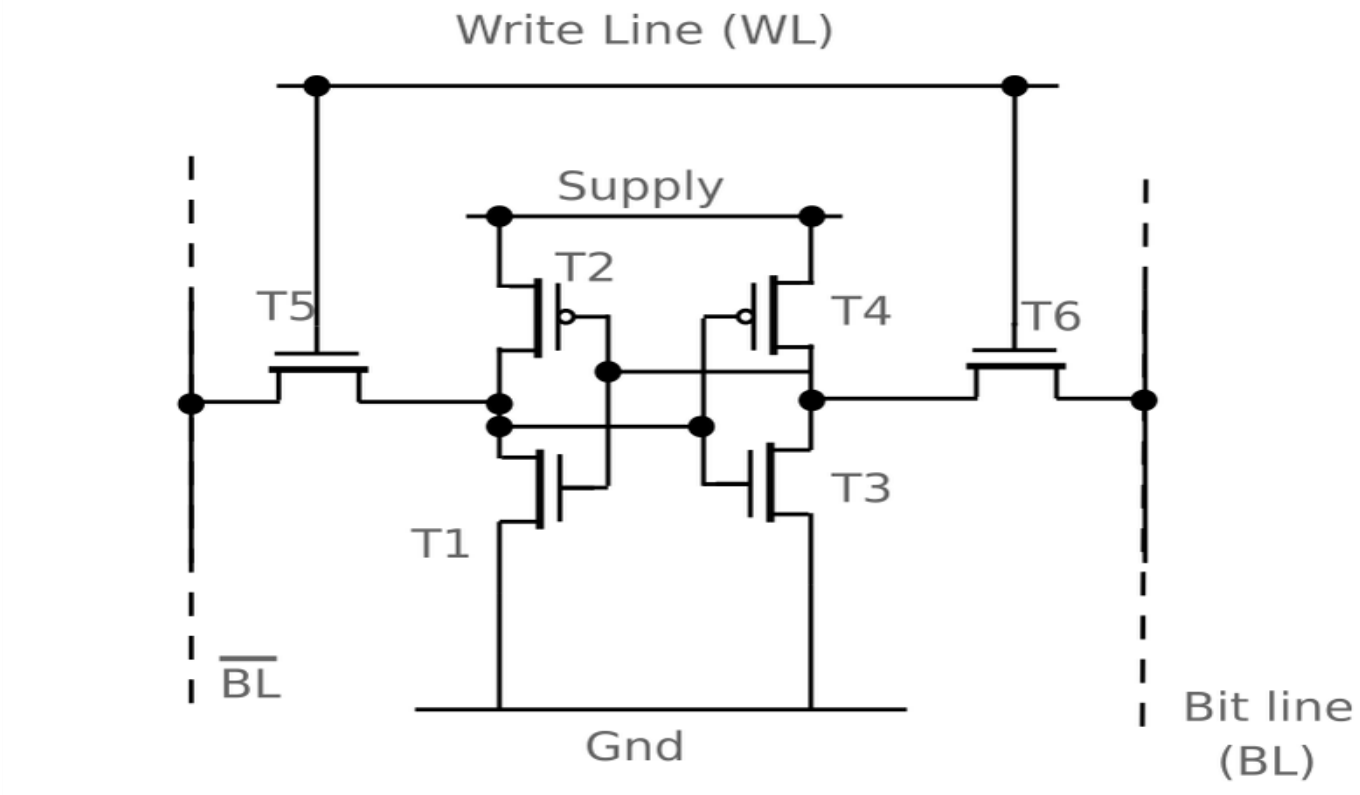
1. Understanding the working of the SRAM cell.
2. Design and simulate the schematic of the SRAM cell.
3. Verify the functionality of the circuit through simulations.

## Schematic design

The SRAM cell was designed using six transistors:

1. Two cross-coupled inverters to store the data.
2. Two access transistors for enabling read and write operations.
3. Appropriate pins were added accordingly.

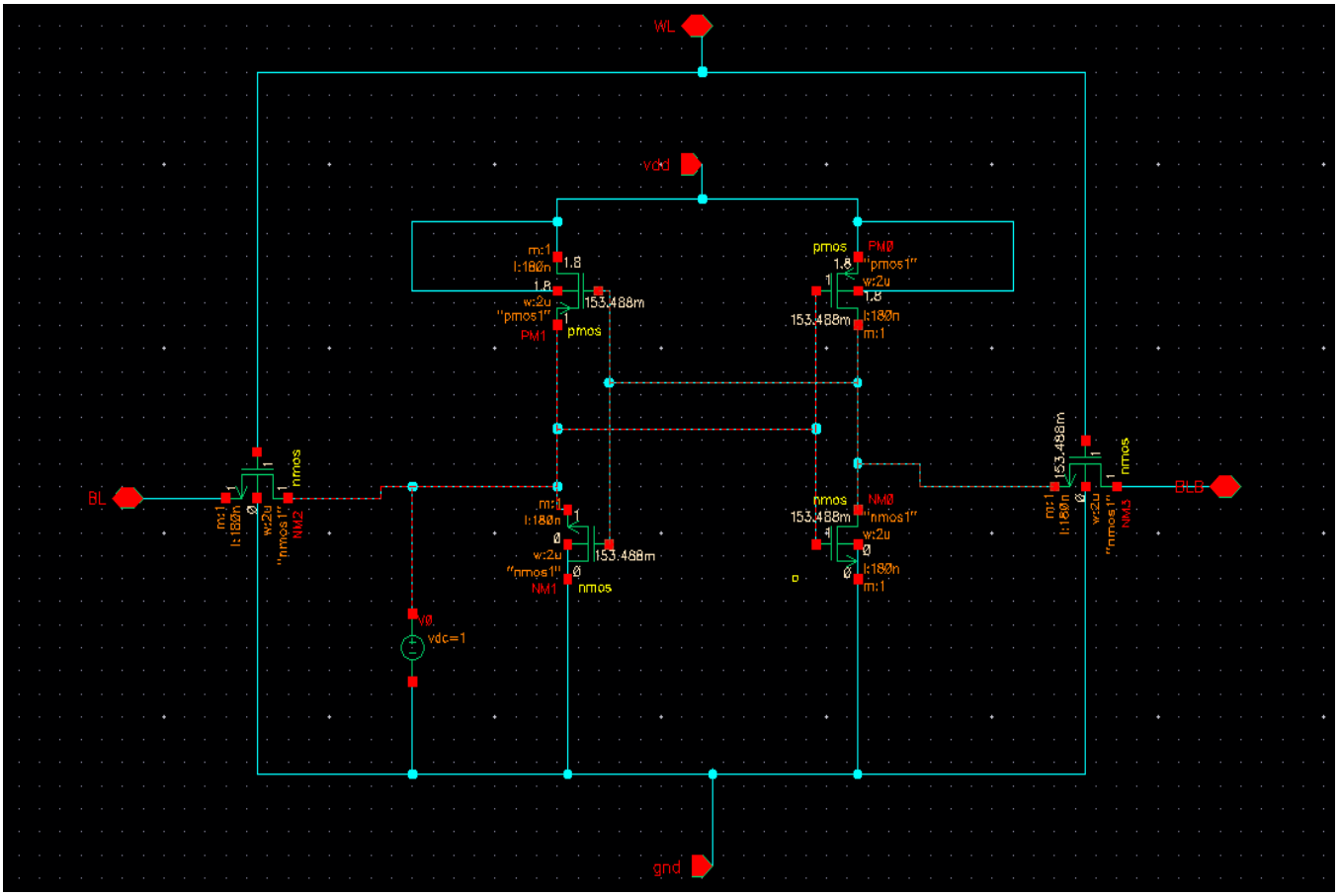
## Circuit Diagram



## Design Details

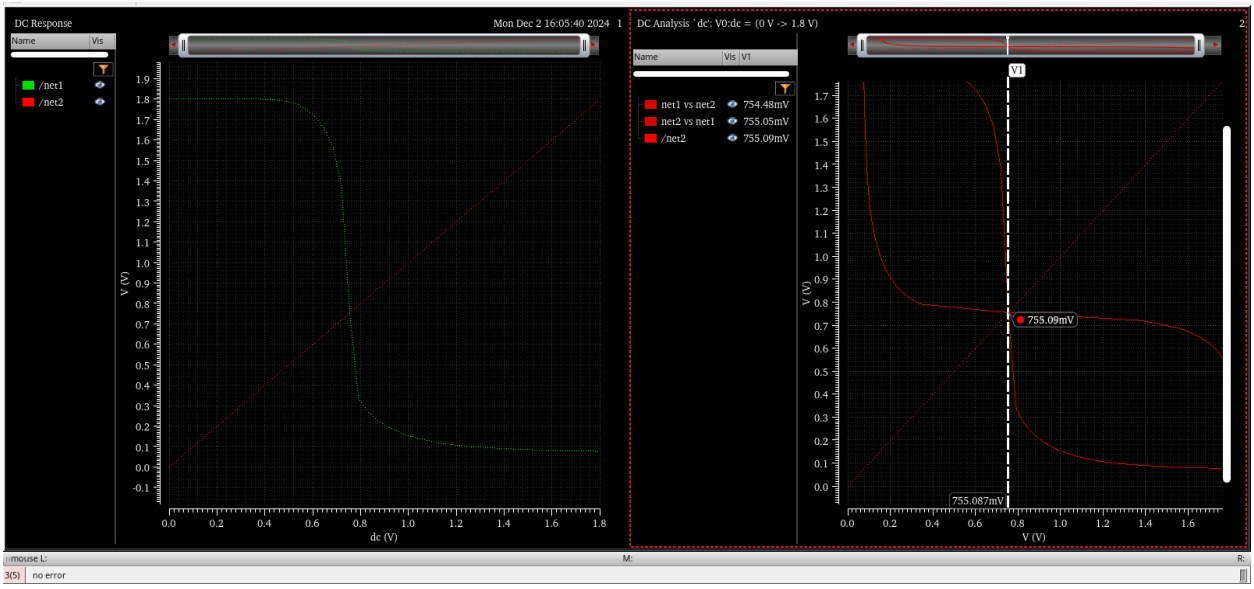
- Technology Node:  180nm
- Transistor Parameters: Channel length, width, and threshold voltages were optimized for power and performance.
- Power Supply: The circuit was designed to operate at a standard supply voltage of 1V].

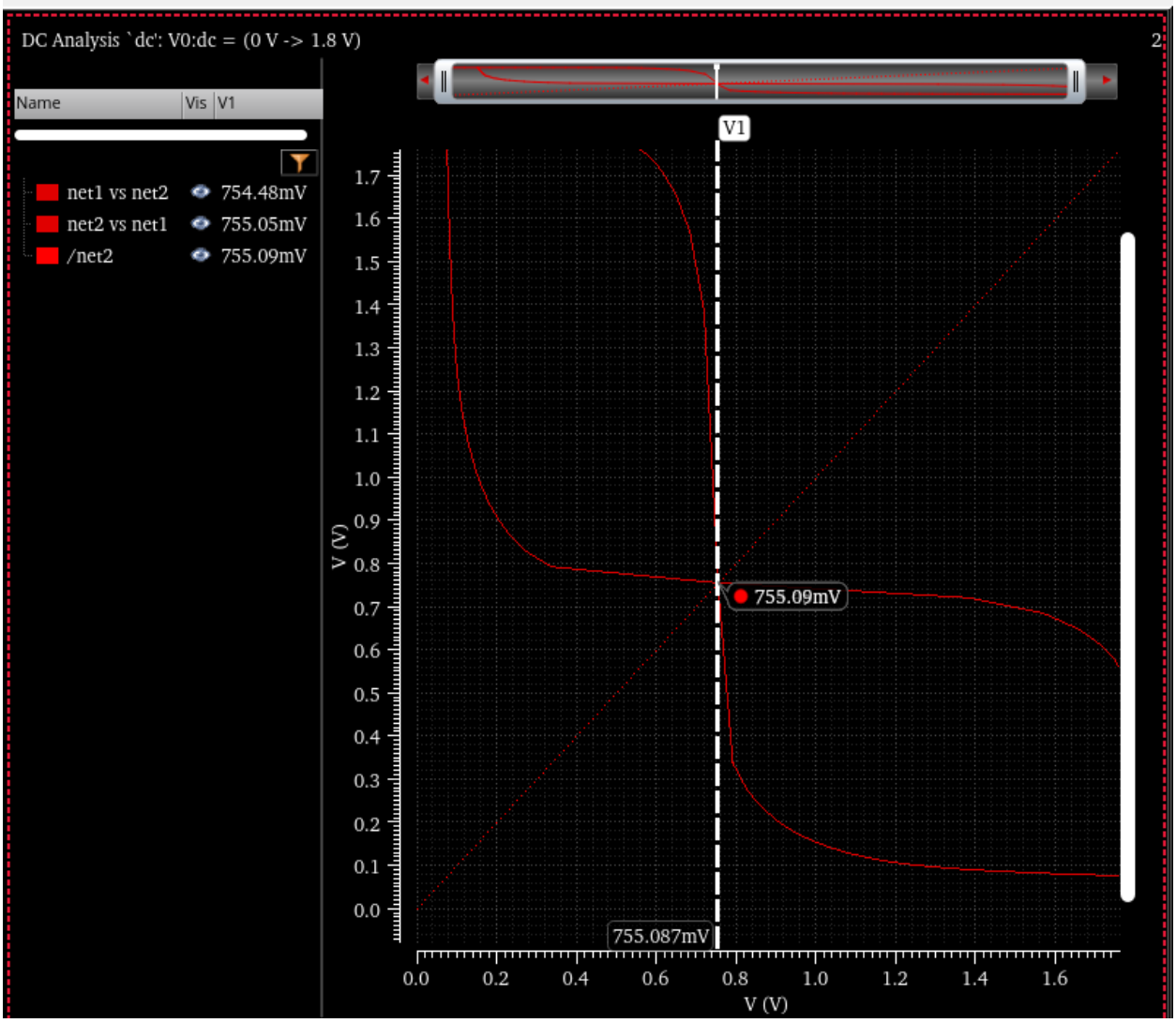
## Test Schematic



## Simulation Results

The designed SRAM cell was tested using dc analysis.




DC Analysis `dc': V0:dc = (0 V -> 1.8 V)
Name
Vis
V1
net1 vs net2
754.48mV
net2 vs net1
755.05mV
/net2
755.09mV
V1
755.09mV
755.087mV
V (V)
V (V)
0.0
0.2
0.4
0.6
0.8
1.0
1.2
1.4
1.6
1.7
1.5
1.3
1.1
0.9
0.7
0.5
0.3
0.1

## Conclusion

The designed SRAM cell exhibited robust performance, achieving high-speed operations with minimal power consumption. The implementation of the 6T architecture ensured stability even under varying environmental conditions. The results validated the suitability of the design for use in modern VLSI systems, particularly in high-speed cache memory applications. Future work can explore further optimization for lower power dissipation and higher density designs.