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## 9.2 Register Definition

Register 0x00 (CHIP\_ID)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
CHIP_ID<7:0>								RW	0x90

This register is used to identify the device

Register 0x01 ~ 0x02 (DXL, DXM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DX<5:0>								R	0x00
NEWDATA_X								R	0x00
DX<13:6>								R	0x00

DX: 14bits acceleration data of x-channel. This data is in two's complement.

NEWDATA\_X: 1, acceleration data of x-channel has been updated since last reading  
0, acceleration data of x-channel has not been updated since last reading

Register 0x03 ~ 0x04 (DYL, DYM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DY<5:0>								R	0x00
NEWDATA_Y								R	0x00
DY<13:6>								R	0x00

DY: 14bits acceleration data of y-channel. This data is in two's complement.

NEWDATA\_Y: 1, acceleration data of y-channel has been updated since last reading  
0, acceleration data of y-channel has not been updated since last reading

Register 0x05 ~ 0x06 (DZL, DZM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DZ<5:0>								R	0x00
NEWDATA_Z								R	0x00
DZ<13:6>								R	0x00

DZ: 14bits acceleration data of z-channel. This data is in two's complement.

NEWDATA\_Z: 1, acceleration data of z-channel has been updated since last reading  
0, acceleration data of z-channel has not been updated since last reading

Register 0x07 ~ 0x08 (STEP\_CNT)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CNT<7:0>								R	0x00
STEP_CNT<15:8>								R	0x00

STEP\_CNT<15:0>: 16 bits of step counter, out of total 24bits data. The MSB data are in 0x0e

Register 0x09 (INT\_ST0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
NO_MOT	STEP_FLAG			ANY_MOT_SIGN	ANY_MOT_FIRST_Z	ANY_MOT_FIRST_Y	ANY_MOT_FIRST_X	R	0x00

NO\_MOT: 1, no\_motion interrupt active  
0, no\_motion interrupt inactive

STEP\_FLAG: 1, STEP detected  
0, STEP not detected

ANY\_MOT\_SIGN: 1, sign of any\_motion triggering signal is negative  
0, sign of any\_motion triggering signal is positive

ANY\_MOT\_FIRST\_Z: 1, any\_motion interrupt is triggered by Z axis  
0, any\_motion interrupt is not triggered by Z axis

ANY\_MOT\_FIRST\_Y: 1, any\_motion interrupt is triggered by Y axis  
0, any\_motion interrupt is not triggered by Y axis

ANY\_MOT\_FIRST\_X: 1, any\_motion interrupt is triggered by X axis  
0, any\_motion interrupt is not triggered by X axis

Register 0x0a (INT\_ST1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
S_TAP_INT	SIG_STEP	D_TAP_INT	T_TAP_INT	STEP_INT	HD_INT	RAISE_INT	SIG_MOT_INT	R	0x00



S\_TAP\_INT: 1, single tap is active  
0, single tap is inactive

SIG\_STEP: 1, significant step is active  
0, significant step is inactive

D\_TAP\_INT: 1, double tap is active  
0, double tap is inactive

STEP\_INT: 1, step valid interrupt is active  
0, step quit interrupt is inactive

T\_TAP\_INT: 1, triple tap is active  
0, triple tap is inactive

HD\_INT: 1, hand down interrupt is active  
0, hand down interrupt is inactive

RAISE\_INT: 1, raise hand interrupt is active  
0, raise hand interrupt is inactive

SIG\_MOT\_INT: 1, significant interrupt is active  
0, significant interrupt is inactive

## Register 0x0b (INT\_ST2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_OR	FIFO_WM_INT	FIFO_FULL_INT	DATA_INT			EARIN_FLAG	Q_TAP_INT	R	0x00

FIFO\_OR: 1, FIFO Over-Run occurred  
0, FIFO Over-Run not occurred

FIFO\_WM\_INT: 1, FIFO watermark interrupt is active  
0, FIFO watermark interrupt is inactive

FIFO\_FULL\_INT: 1, FIFO full interrupt is active  
0, FIFO full interrupt is inactive

DATA\_INT: 1, data ready interrupt active  
0, data ready interrupt inactive

EARIN\_FLAG: 1, ear-in interrupt is active  
0, ear-in interrupt is inactive

Q\_TAP\_INT: 1, quad tap is active  
0, quad tap is inactive

## Register 0x0c (INT\_ST3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
TAP_SIGN								R	0x00

TAP\_SIGN: 1, tap sign is along with positive direction  
0, tap sign is along with negative direction

## Register 0x0d (INT\_ST4)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CNT<23:16>								R	0x00

STEP\_CNT<23:16>: 8bit MSB data of step counter, out of total 24bits data. The LSB data are in 0x07 and 0x08

## Register 0x0e (FIFO\_ST)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_FRAME_COUNTER<7:0>								R	0x00


FIFO\_FRAME\_COUNTER<7:0>: Fill level of FIFO buffer. An empty FIFO corresponds to 0x00. The frame counter can be cleared by reading out all of the frames, or by writing register 0x3e (FIFO\_CFG1) or 0x31.

## Register 0x0f (FSR)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	LPF_HPF			RANGE<3:0>				RW	0x00

RANGE<3:0>: set the full scale of the accelerometer. Setting as following

RANGE<3:0>	Acceleration range	Resolution
0001	2g	244ug/LSB
0010	4g	488g/LSB
0100	8g	977ug/LSB
1000	16g	1.95mg/LSB
1111	32g	3.91mg/LSB
Others	2g	244ug/LSB

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#### Register 0x10 (BW)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
HPF[2]	NLPF<1:0>		BW<4:0>					RW	0xE0

NLPF<1:0>:  
00: no LPF.  
01: NLPF=2.  
10: NLPF=4.  
11: NLPF=8

BW<4:0>: bandwidth setting, as following

#### Register 0x11 (PM)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
MODE_BIT		T_RSTB_SINC_SEL<1:0>		MCLK_SEL<3:0>				RW	0x00

MODE\_BIT: 1, set device into active mode  
0, set device into standby mode

T\_RSTB\_SINC\_SEL<1:0>: Reset clock setting. The preset time is reserved for CIC filter in digital

MCLK\_SEL<3:0>: set the master clock to digital

#### Register 0x12 (STEP\_CONF0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_EN	STEP_SAMPLE_CNT<6:0>							RW	0x14

STEP\_EN: enable step counter, this bit should be set 1 when using step counter

STEP\_SAMPLE\_CNT: sample count setting to renew dynamic threshold. The actual value is STEP\_SAMPLE\_CNT<6:0>\*8, default is 0xC, 96 sample count

#### Register 0x13 (STEP\_CONF1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_CLR	STEP_PRECISION<6:0>							RW	0x7F

STEP\_CLR: clear step count in register 0x0D, 0x08 and 0x07

STEP\_PRECISION<6:0>: algorithm setting

#### Register 0x14 (STEP\_CONF2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_TIME_LOW<7:0>								RW	0x19

STEP\_TIME\_LOW<7:0>: algorithm setting

#### Register 0x15 (STEP\_CONF3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_TIME_UP<7:0>								RW	0x00

STEP\_TIME\_UP<7:0>: algorithm setting

#### Register 0x16 (INT\_EN0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
S_TAP_EN	SIG_STEP_I_EN	D_TAP_EN	T_TAP_EN	STEP_IEN	HD_EN	RAISE_EN	Q_TAP_EN	RW	0x00

S\_TAP\_EN: 1, enable single tap  
0, disable single tap

SIG\_STEP\_IEN: 1, enable significant step interrupt  
0, disable significant step interrupt

D\_TAP\_EN: 1, enable double tap  
0, disable double tap

T\_TAP\_EN: 1, enable triple tap  
0, disable triple tap


STEP\_IEN: 1, enable step valid interrupt  
0, disable step valid interrupt

HD\_EN: 1, enable hand-down interrupt  
0, disable hand-down interrupt

RAISE\_EN: 1, enable raise-hand interrupt  
0, disable raise-hand interrupt

Q\_TAP\_EN: 1, enable quad tap  
0, disable quad tap

#### Register 0x17 (INT\_EN1)

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Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
	INT_FWM_EN	INT_FFULL_INT	INT_DATA_EN					RW	0x00

INT\_FWM\_EN: 1, enable FIFO watermark interrupt  
0, disable FIFO watermark interrupt

INT\_FFULL\_EN: 1, enable FIFO full interrupt  
0, disable FIFO full interrupt

INT\_DATA\_EN: 1, enable data ready interrupt  
0, disable data ready interrupt

#### Register 0x18 (INT\_EN2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
NO_MOT_EN_Z	NO_MOT_EN_Y	NO_MOT_EN_X			ANY_MOT_EN_Z	ANY_MOT_EN_Y	ANY_MOT_EN_X	RW	0x00

NO\_MOT\_EN\_Z: 1, enable no\_motion interrupt on Z axis  
0, disable no\_motion interrupt on Z axis

NO\_MOT\_EN\_Y: 1, enable no\_motion interrupt on Y axis  
0, disable no\_motion interrupt on Y axis

NO\_MOT\_EN\_X: 1, enable no\_motion interrupt on X axis  
0, disable no\_motion interrupt on X axis

ANY\_MOT\_EN\_Z: 1, enable any\_motion interrupt on Z axis  
0, disable any\_motion interrupt on Z axis

ANY\_MOT\_EN\_Y: 1, enable any\_motion interrupt on Y axis  
0, disable any\_motion interrupt on Y axis

ANY\_MOT\_EN\_X: 1, enable any\_motion interrupt on X axis  
0, disable any\_motion interrupt on X axis

#### Register 0x19 (INT\_MAP0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT1_S_TAP	INT1_SIG_STEP	INT1_D_TAP	INT1_T_TAP	INT1_STEP	INT1_HD	INT1_RAISE	INT1_SIG_MOT	RW	0x00

INT1\_S\_TAP: 1, map single tap interrupt to INT1 pin  
0, not map single tap interrupt to INT1 pin

INT1\_SIG\_STEP: 1, map significant step interrupt to INT1 pin  
0, not map significant step interrupt to INT1 pin

INT1\_D\_TAP: 1, map double tap interrupt to INT1 pin  
0, not map double tap interrupt to INT1 pin

INT1\_T\_TAP: 1, map triple tap interrupt to INT1 pin  
0, not map triple tap interrupt to INT1 pin

INT1\_STEP: 1, map step valid interrupt to INT1 pin  
0, not map step valid interrupt to INT1 pin

INT1\_HD: 1, map hand down interrupt to INT1 pin  
0, not map hand down interrupt to INT1 pin

INT1\_RAISE: 1, map raise hand interrupt to INT1 pin  
0, not map raise hand interrupt to INT1 pin

INT1\_SIG\_MOT: 1, map significant interrupt to INT1 pin  
0, not map significant interrupt to INT1 pin

#### Register 0x1a (INT\_MAP1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT1_NO_MOT	INT1_FWM	INT1_FFULL	INT1_DATA			INT1_Q_TAP	INT1_ANY_MOT	RW	0x00

INT1\_NO\_MOT: 1, map no\_motion interrupt to INT1 pin  
0, not map no\_motion interrupt to INT1 pin


INT1\_FWM: 1, map FIFO watermark interrupt to INT1 pin  
0, not map FIFO watermark interrupt to INT1 pin

INT1\_FFULL: 1, map FIFO full interrupt to INT1 pin  
0, not map FIFO full interrupt to INT1 pin

INT1\_DATA: 1, map data ready interrupt to INT1 pin  
0, not map data ready interrupt to INT1 pin

INT1\_Q\_TAP: 1, map quad tap interrupt to INT1 pin  
0, not map quad tap interrupt to INT1 pin

INT1\_ANY\_MOT: 1, map any motion interrupt to INT1 pin

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0, not map any motion interrupt to INT1 pin

Register 0x1b (INT\_MAP2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT2_S_TAP	INT2_SIG_STEP	INT2_D_TAP	INT2_T_TAP	INT2_STEP	INT2_HD	INT2_RAISE	INT2_SIG_MOT	RW	0x00

INT2\_S\_TAP: 1, map single tap interrupt to INT2 pin  
0, not map single tap interrupt to INT2 pin

INT2\_SIG\_STEP: 1, map significant step interrupt to INT2 pin  
0, not map significant step interrupt to INT2 pin

INT2\_D\_TAP: 1, map double tap interrupt to INT2 pin  
0, not map double tap interrupt to INT2 pin

INT2\_T\_TAP: 1, map triple tap interrupt to INT2 pin  
0, not map triple tap interrupt to INT2 pin

INT2\_STEP: 1, map step valid interrupt to INT2 pin  
0, not map step valid interrupt to INT2 pin

INT2\_HD: 1, map hand down interrupt to INT2 pin  
0, not map hand down interrupt to INT2 pin

INT2\_RAISE: 1, map raise hand interrupt to INT2 pin  
0, not map raise hand interrupt to INT2 pin

INT2\_SIG\_MOT: 1, map significant interrupt to INT2 pin  
0, not map significant interrupt to INT2 pin

Register 0x1c (INT\_MAP3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT2_NO_MOT	INT2_FWM	INT2_FFULL	INT2_DATA			INT2_Q_TAP	INT2_ANY_MOT	RW	0x00

INT2\_NO\_MOT: 1, map no\_motion interrupt to INT2 pin  
0, not map no\_motion interrupt to INT2 pin

INT2\_FWM: 1, map FIFO watermark interrupt to INT2 pin  
0, not map FIFO watermark interrupt to INT2 pin

INT2\_FFULL: 1, map FIFO full interrupt to INT2 pin  
0, not map FIFO full interrupt to INT2 pin

INT2\_DATA: 1, map register data ready interrupt to INT2 pin  
0, not map register data ready interrupt to INT2 pin

INT2\_Q\_TAP: 1, map quad tap interrupt to INT2 pin  
0, not map quad tap interrupt to INT2 pin

INT2\_ANY\_MOT: 1, map any motion interrupt to INT2 pin  
0, not map any motion interrupt to INT2 pin

Register 0x1d (STEP\_CFG0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_INTERVAL<7:0>								RW	0x00

STEP\_INTERVAL <7:0>: algorithm setting

Register 0x1e (STEP\_CFG1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
NLPF_STEP<1:0>		TAP_QUIET<5:0>						RW	0x08

NLPF\_STEP<1:0>: Moving Average of Step: 1/2/4/8

TAP\_QUIET\_TH<5:0>: Tap quiet threshold selection, LSB of TAP\_QUIET\_TH<5:0> is 31.25mg in all full scale.

Register 0x1f

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
STEP_START_CNT<2:0>			STEP_COUNT_PEAK<1:0>		STEP_COUNT_P2P<2:0>			RW	0xA9

STEP\_START\_CNT<2:0>: algorithm setting

STEP\_COUNT\_PEAK<2:0>: algorithm setting

STEP\_COUNT\_P2P<2:0>: algorithm setting

Register 0x20 (INTPIN\_CONF)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
DIS_PU_SENB	DIS_IE_AD0	EN_SPI3W	STEP_COUNT_PEAK<2>	INT2_OD	INT2_LVL	INT1_OD	INT1_LVL	RW	0x05



DIS\_PU\_SENB: 1, disable pull-up resistor of PIN\_SENB  
0, enable pull-up resistor of PIN\_SENB

DIS\_IE\_AD0: 1, disable input of AD0  
0, not disable input of AD0

EN\_SPI3W: 1, enable 3W SPI  
0, 4W SPI

STEP\_COUNT\_PEAK<2>: Definition in 0x1F<4:3>

INT2\_OD: 1, open-drain for INT2 pin  
0, push-pull for INT2 pin

INT2\_LVL: 1, logic high as active level for INT2 pin  
0, logic low as active level for INT2 pin

INT1\_OD: 1, open-drain for INT1 pin  
0, push-pull for INT1 pin

INT1\_LVL: 1, logic high as active level for INT1 pin  
0, logic low as active level for INT1 pin

## Register 0x21 (INT\_CFG)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
INT_RD_CLR	SHADOW_DIS	DIS_I2C				LATCH_INT_STEP	LATCH_INT	RW	0x0C

INT\_RD\_CLR: 1, clear all the interrupts in latched-mode, when any read operation to any of registers from 0x09 to 0x0D  
0, clear the related interrupts, only when read the register INT\_ST (0x09 to 0x0D),  
no matter the interrupts in latched-mode, or in non-latched-mode.  
Reading 0x09 will clear the register 0x09 only and the others keep the status

SHADOW\_DIS: 1, disable the shadowing function for the acceleration data  
0, enable the shadowing function for the acceleration data.  
When shadowing is enabled, the MSB of the acceleration data is locked,  
when corresponding LSB of the data is reading.  
This can ensure the integrity of the acceleration data during the reading.  
The MSB will be unlocked when the MSB is read.

DIS\_I2C: 1: disable I2C. Setting this bit to 1 in SPI mode is recommended  
0: enable I2C

LATCH\_INT\_STEP: 1, step related interrupt is in latch mode  
0, step related interrupt is in non-latch mode

LATCH\_INT: 1, interrupt is in latch mode  
0, interrupt is in non-latch mode

## Register 0x22

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
RAISE_WAKE_DIFF_TH<1:0>		RAISE_WAKE_SUM_TH<5:0>						RW	0xD8

RAISE\_WAKE\_DIFF\_TH&lt;1:0&gt;: Threshold = 0 ~ 31.5 (LSB 0.5)

RAISE\_WAKE\_SUM\_TH&lt;5:0&gt;:

0	0.2
1	0.3
2	0.4
3	0.5
4	0.6
5	0.7
6	0.8
7	0.9
8	1.0
9	1.1
10	1.2
default	0.2

## Register 0x23


Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
HD Z TH<2:0>			HD X TH<2:0>			RAISE WAKE DIFF TH<3:2>		RW	0x7C

HD\_Z\_TH&lt;2:0&gt;: hand down z threshold, 0~7

HD\_X\_TH&lt;2:0&gt;: hand down x threshold, 0~7

RAISE\_WAKE\_DIFF\_TH&lt;3:2&gt;: Threshold = 0 ~ 31.5 (LSB 0.5)

## Register 0x24

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Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
RAISE_WAKE_TIMEOUT_TH<7:0>								RW	0x00

RAISE\_WAKE\_TIMEOUT\_TH<7:0>: Raise\_wake\_timeout\_th[11:0] \* ODR period = timeout count

#### Register 0x25

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
RAISE_WAKE_PERIOD<7:0>								RW	0x00

RAISE\_WAKE\_PERIOD<7:0>: Raise\_wake\_period[10:0] \* ODR period = wake count

#### Register 0x26

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
RAISE_MODE	RAISE_WAKE_PERIOD<10:8>			RAISE_WAKE_TIMEOUT_TH<11:8>				RW	0x02

RAISE\_MODE: 0:raise wake function, 1:ear-in function

RAISE\_WAKE\_PERIOD<10:8>: Raise\_wake\_period[10:0] \* ODR period = wake count

RAISE\_WAKE\_TIMEOUT\_TH<11:8>: Raise\_wake\_timeout\_th[11:0] \* ODR period = timeout count

#### Register 0x27 (OS\_CUST\_X)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_X<7:0>								RW	0x00

OS\_CUST\_X<7:0>: offset calibration of X axis for user, the LSB depends on full-scale of the device which is 3.9mg in 2g range, 7.8mg in 4g range, 15.6mg in 8g range, 31.2mg in 16g, and 62.5mg in 32g

#### Register 0x28 (OS\_CUST\_Y)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_Y<7:0>								RW	0x00

OS\_CUST\_Y<7:0>: offset calibration of Y axis for user, the LSB depends on full-scale of the device which is 3.9mg in 2g range, 7.8mg in 4g range, 15.6mg in 8g range, 31.2mg in 16g, and 62.5mg in 32g

#### Register 0x29 (OS\_CUST\_Z)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
OS_CUST_Z<7:0>								RW	0x00

OS\_CUST\_Z<7:0>: offset calibration of Z axis for user, the LSB depends on full-scale of the device which is 3.9mg in 2g range, 7.8mg in 4g range, 15.6mg in 8g range, 31.2mg in 16g, and 62.5mg in 32g

#### Register 0x2a (RAISE\_WAKE\_SUM\_TH RAISE\_WAKE\_DIFF\_TH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
TAP_QUIET	TAP_SHOCK	TAP_DELAY	TAP_EARIN		TAP_DURATION<2:0>			RW	0x05

TAP\_QUIET: 1: Tap quiet time = 30ms 0: Tap quiet time = 20ms

TAP\_SHOCK: 1: Tap shock time = 50ms 0: Tap shock time = 75ms

TAP\_DELAY\_Y: 0: Triple tap interrupt would not wait for quadruple tap result.

1: Triple tap interrupt would wait for quadruple tap result.

If quadruple tap is not toggle, triple tap would toggle after tap duration time finish.

TAP\_EARIN: 1: Tap enable would be related with EARIN\_FLAG (reg 0x0B<1>).

If EARIN\_FLAG is low, tap detection will be disabled.

If EARIN\_FLAG is high, tap detection is enabled by reg 0x16.

0: Tap detection is enabled by reg 0x16.

TAP\_DURATION<2:0>: Tap duration time selection

000: 100ms

001: 150ms

010: 200ms

011: 250ms

100: 300ms

101: 400ms


110: 500ms

111: 700ms

#### Register 0x2b (RAISE\_WAKE\_DIFF\_TH HD\_X\_TH HD\_Z\_TH)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
TAP_IN_SEL<1:0>		TAP_SHOCK_TH<5:0>						RW	0xCD

TAP\_IN\_SEL<1:0>: Tap Detector Input Selection

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0 : X-axis  
1 : Y-axis  
2 : Z-axis  
3 :  $(X^2 + Y^2 + Z^2)^{0.5}$

TAP\_SHOCK\_TH: Tap shock threshold selection, LSB of TAP\_SHOCK\_TH<5:0> is 31.25mg in all full scale.

#### Register 0x2c (MOT\_CONF0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
NO_MOT_DUR<5:0>						ANY_MOT_DUR<1:0>		RW	0x00

NO\_MOT\_DUR<5:0>: no motion interrupt will be triggered when slope < NO\_MOT\_TH for the times which defined by NO\_MOT\_DUR<5:0>  
Duration = (NO\_MOT\_DUR<3:0> + 1) \* 1s, if NO\_MOT\_DUR<5:4> = b00  
Duration = (NO\_MOT\_DUR<3:0> + 4) \* 5s, if NO\_MOT\_DUR<5:4> = b01  
Duration = (NO\_MOT\_DUR<3:0> + 10) \* 10s, if NO\_MOT\_DUR<5:4> = b1x

ANY\_MOT\_DUR<1:0>: any motion interrupt will be triggered when slope > ANY\_MOT\_TH for (ANY\_MOT\_DUR<1:0> + 1) samples

#### Register 0x2d (MOT\_CONF1)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
NO_MOT_TH<7:0>								RW	0x00

NO\_MOT\_TH<7:0>: Threshold of no-motion interrupt. The threshold definition is as following  
TH= NO\_MOT\_TH<7:0> \* 16 \* LSB

#### Register 0x2e (MOT\_CONF2)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
ANY_MOT_TH<7:0>								RW	0x00

ANY\_MOT\_TH<7:0>: Threshold of any motion interrupt. The threshold definition is as following  
ANY\_MOT\_IN\_SEL = 0 : Threshold = ANY\_MOT\_TH<7:0> \* 16LSB  
ANY\_MOT\_IN\_SEL = 1 : Threshold = ANY\_MOT\_TH<7:0> \* 32LSB  
ANT\_MOT\_IN\_SEL is 0x2F<6>.

#### Register 0x2f (MOT\_CONF3)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
RFF_BP_LP F	ANY_MOT _IN_SEL	SIG_MOT_TPROOF<1:0>		SIG_MOT_TSKIP<1:0>			SIG_MOT_ SEL	RW	0x00

RFF\_BP\_LP: 1: Data of register acceleration XYZ (0x01 ~ 0x06) and FIFO (0x3F) would bypass LPF.  
0: Data of register file acceleration XYZ (0x01 ~ 0x06) and FIFO (0x3F) would be filtered by LPF.

ANY\_MOT\_IN\_SEL: 0: Any-motion Input is Slope.  
1: Any-motion Input is Acceleration, it could detect high-g.

SIG\_MOT\_TPROOF<1:0>: 00, T\_PROOF=0.25s  
01, T\_PROOF=0.5s  
10, T\_PROOF=1s  
11, T\_PROOF=2s  
SIG\_MOT\_TSKIP<1:0>: 00, T\_SKIP=1.5s  
01, T\_SKIP=3s  
10, T\_SKIP=6s  
11, T\_SKIP=12s

SIG\_MOT\_SEL: 1, select significant motion interrupt  
0, select any motion interrupt

#### Register 0x30

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
MO_BP_LP F	STEP_BP_L PF	TAP_RST_ N			NO_MOT_ RST_N	SIG_MOT_ RST_N	ANY_MOT_ _RST_N	RW	0x1F

MO\_BP\_LPF: 1: Input of any motion, sig motion and no motion would bypass LPF.  
0: Input of any motion, significant motion and no motion would be filtered by LPF.

STEP\_BP\_LPF: 1: Input of step counter, raise wake, and tap detector would bypass LPF.  
0: Input of step counter, raise wake, and tap detector would be filtered by LPF.


TAP\_RST\_N: 0, Reset tap detector. After reset, user should write 1 back.  
NO\_MOT\_RST\_N: 0, Reset no motion detector. After reset, user should write 1 back.  
SIG\_MOT\_RST\_N: 0, Reset significant motion detector. After reset, user should write 1 back.  
ANY\_MOT\_RST\_N: 0, Reset any motion detector. After reset, user should write 1 back.

#### Register 0x31

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_WTMK_LVL<7:0>									0x00

FIFO\_WTMK\_LVL<7:0>: defines FIFO water mark level. Interrupt will be generated, when the number of entries in the FIFO exceeds FIFO\_WTMK\_LVL<7:0>.



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When the value of this register is changed, the FIFO\_FRAME\_COUNTER in 0x0E is reset to 0.

#### Register 0x32 (ST)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
SELFTEST_BIT					SELFTEST_SIGN	STEP_BP_AXIS<1:0>		RW	0x00

SELFTEST\_BIT: 1, self-test enabled. When self-test enabled, a delay of 3ms is necessary for the value settling.  
0, normal

SELFTEST\_SIGN: 1, set self-test excitation positive  
0, set self-test excitation negative

STEP\_BP\_AXIS<1:0>: 11, bypass Z axis, use only X and Y axes data for step counter algorithm  
10, bypass Y axis, use only X and Z axes data for step counter algorithm  
01, bypass X axis, use only Y and Z axes data for step counter algorithm  
00, use all of 3 axes data for step counter algorithm

#### Register 0x34 (Y\_TH YZ\_TH\_SEL)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
YZ_TH_SEL<2:0>			Y_TH<4:0>					RW	0x9D

Y\_TH: -16 ~ 15 (m/s<sup>2</sup>)

YZ_TH_SEL<2:0>	UNIT (m/s <sup>2</sup> )
0	7.0
1	7.5
2	8.0
3	8.5
4	9.0
5	9.5
6	10.0
7	10.5

#### Register 0x35 (RAISE\_WAKE\_PERIOD)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
Z_TH<3:0>				X_TH<3:0>				RW	0x66

X\_TH[3:0]: 0 ~ 7.5

Z\_TH[3:0]: -8 ~ 7

#### Register 0x36 (SR)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
SOFT_RESET								RW	0x00

SOFT\_RESET: 0xB6, soft reset all of the registers. After soft-reset, user should write 0x00 back

#### Register 0x3e (FIFO\_CFG0)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_MODE<1:0>		RAISE_XYZ_SW<2:0>			FIFO_EN_Z	FIFO_EN_Y	FIFO_EN_X	RW	0x07


FIFO\_MODE<1:0> : FIFO\_MODE<1:0>: FIFO\_MODE defines FIFO mode of the device. Settings as following

FIFO_MODE<1:0>	MODE
11	FIFO
10	STREAM
01	FIFO
00	BYPASS

RAISE\_XYZ\_SW<2:0> is x/y/z axis switcher, default setting is "0: XYZ" and below is the detail configuration. Both raise wake and ear in/out can use this function.

0x3E[5:3]	X	Y	Z
0	X	Y	Z
1	X	Z	Y
2	Y	X	Z
3	Y	Z	X
4	Z	X	Y
5	Z	Y	X
6	X	Y	Z
7	X	Y	Z

0x3E[2:0]: User can select the acceleration data of which axis to be stored in the FIFO. This configuration can be done by setting FIFO\_CH, where '111b' for x-, y-, and z-axis, '001b' for x-axis only, '010b' for y-axis only, '100b' for z-axis only.

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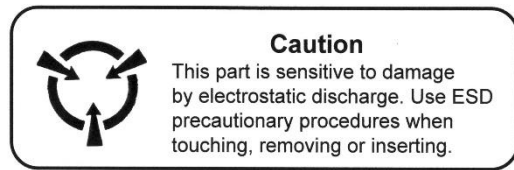
Register 0x3f (FIFO\_DATA)

Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	R/W	Default
FIFO_DATA<7:0>								R	0x00

FIFO\_DATA<7:0>: FIFO read out data. User can read out FIFO data through this register. Data format depends on the setting of FIFO\_CH (0x3e<2:0>). When the FIFO data is the LSB part of acceleration data, and if FIFO is empty, then FIFO\_DATA<0> is 0. Otherwise if FIFO is not empty and the data is effective, FIFO\_DATA<0> is 1 when reading LSB of acceleration.

## ORDERING INFORMATION

Ordering Number	Temperature Range	Package	Packaging
QMA6100P	-40℃~85℃	LGA-12	Tape and Reel: 5k pieces/reel



### CAUTION: ESDS CAT. 1B

For more information on QST's Accelerometer Sensors contact us at 86-21-69517300.

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ISO9001 : 2015

China Patents 201510000399.8, 201510000425.7, 201310426346.3, 201310426677.7, 201310426729.0, 201210585811.3 and 201210553014.7 apply to the technology described.

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